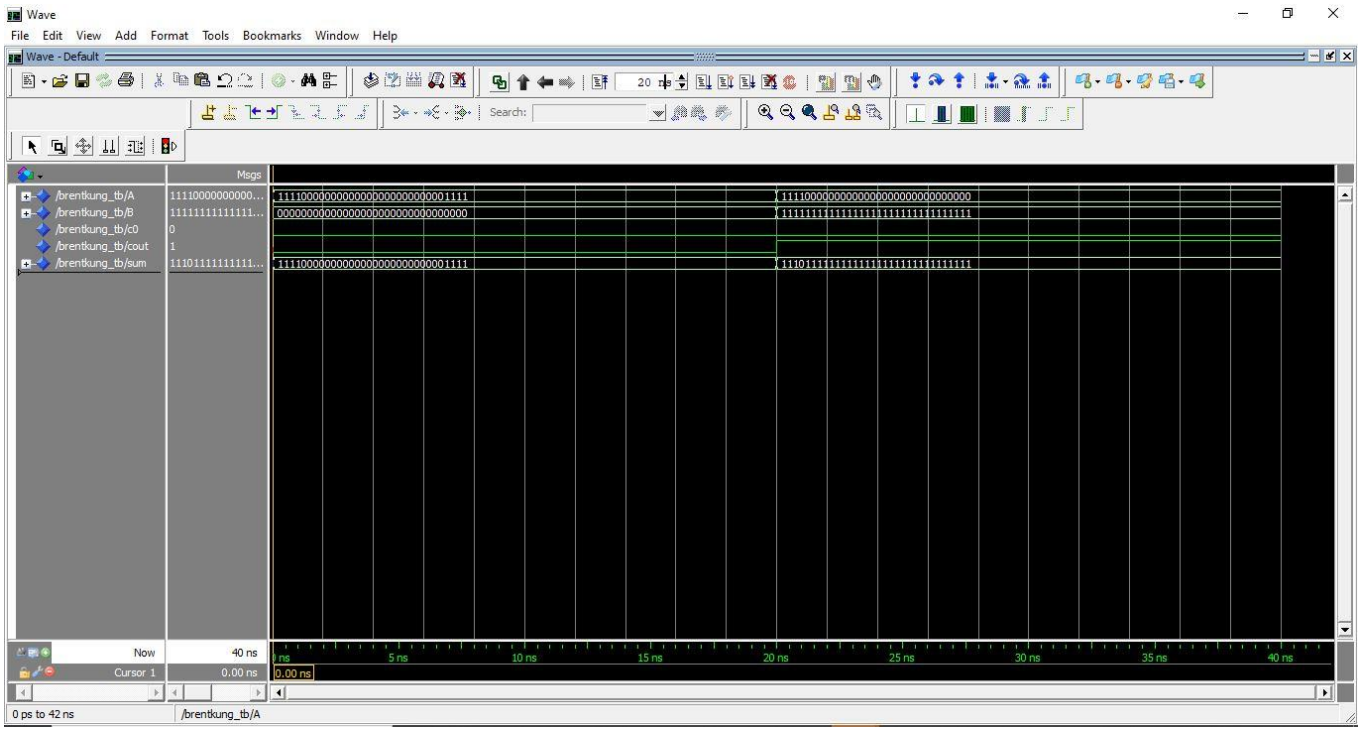
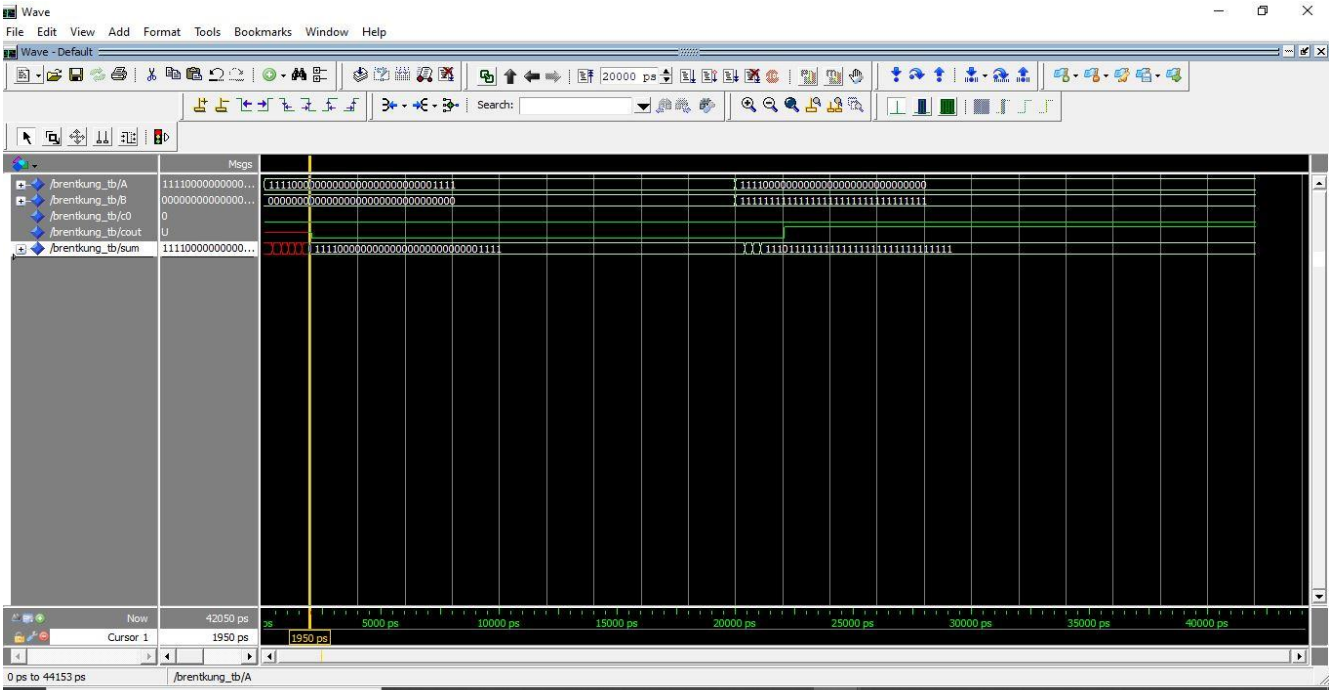
EE 671: VLSI Design Course

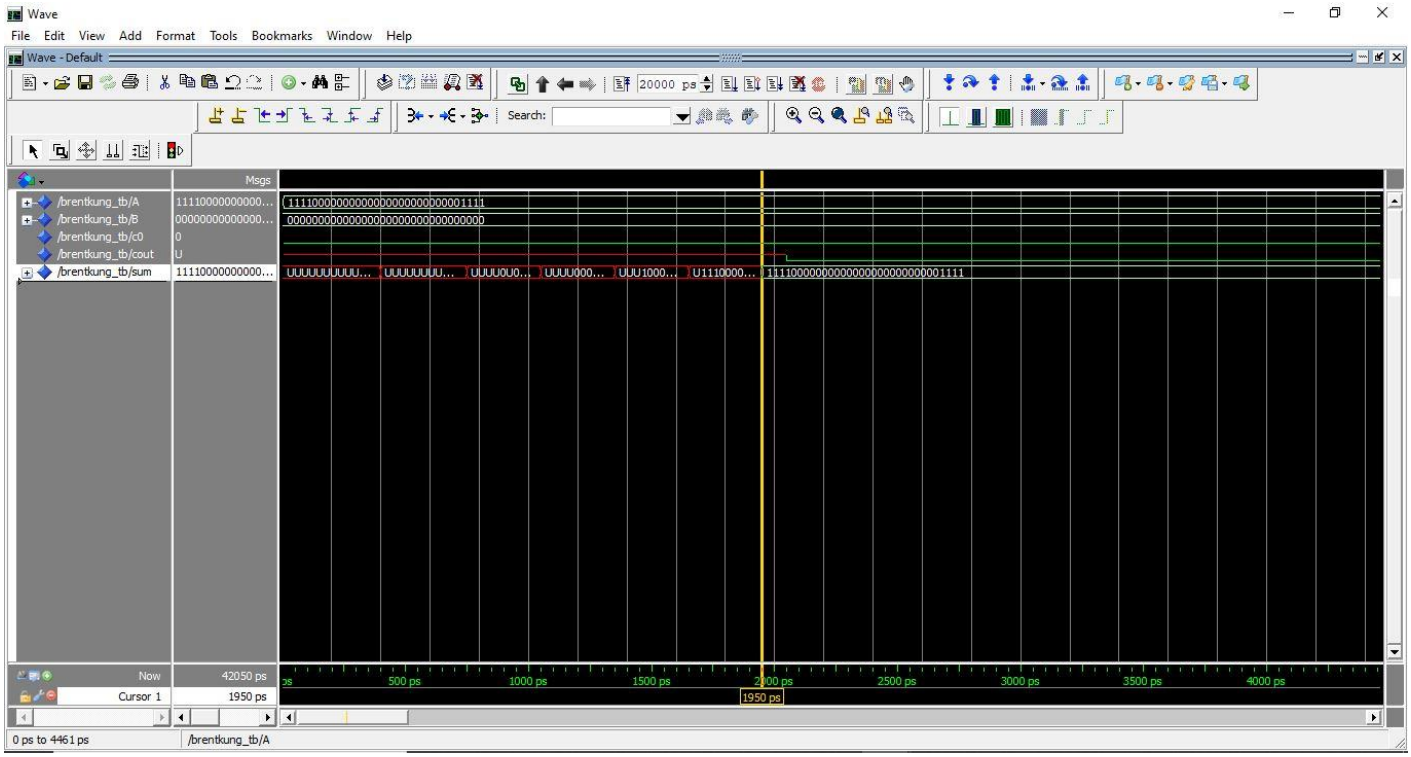
Brent Kung Adder Course Project

1. Without Delays



2. With gate-level Delays

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