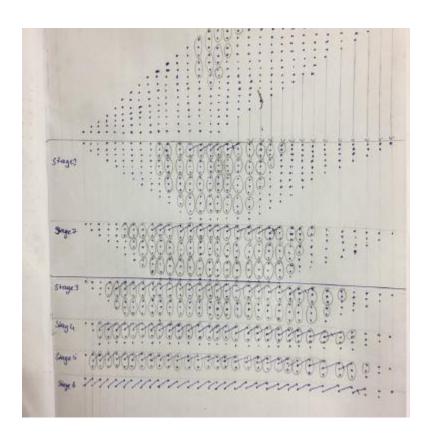
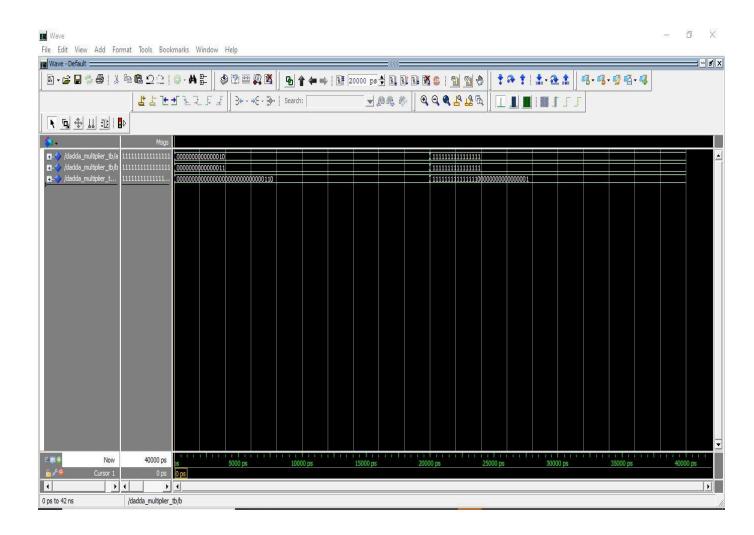
## EE 671: VLSI Design Course Project

## 16x16 Dadda Multiplier

## 1. 16x16 Dadda Multiplier Dot Diagram



 Design a Dadda multiplier for unsigned 16x16 bit multiplication with a Brent Kung adder for the final addition. Write its hardware description in synthesizable VHDL (Without delays) and show its correct working using a test bench with appropriate test vectors.



3. Now back annotate the delays for constituent components and re-simulate the circuit. In how much time can you guarantee that the multiplication will be complete?

