EE 671: VLSI DESIGN
Assignment-3

Posted: Oct. 17, 2019 Due on Oct. 30, 2019

We shall use VHDL for carrying out this assignment.

Q–1 Assume that your library contains components with delays as given below:

Inverter	100 ps
NAND gate	150 ps
NOR gate	150 ps
$\overline{A+B.C}$	200 ps
Tiny XOR	200 ps
Half Adder (carry)	250 ps
Half Adder (sum)	200 ps
Full Adder (carry)	400 ps
Full Adder (sum)	400 ps

a) Design a Dadda multiplier for unsigned 16x16 bit multiplication with a Brent Kung adder for the final addition. Write its hardware description in synthesizable VHDL (without delays) and show its correct working using a test bench with appropriate test vectors.

b) Now back annotate the delays for costituent components and re-simulate the circuit. What is its critical path? In how much time can you guarantee that the multiplication will be complete?