Modeling Analog-Digital-Converter Energy and Area for Compute-In-Memory Accelerator Design

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Abstract—Analog Compute-in-Memory (CiM) accelerators use analog-digital converters (ADCs) to read the analog values that they compute. ADCs can consume significant energy and area, so architecture-level ADC decisions such as ADC resolution or number of ADCs can significantly impact overall CiM accelerator energy and area. Therefore, modeling how architecture-level decisions affect ADC energy and area is critical for performing architecture-level design space exploration of CiM accelerators.

This work presents an open-source architecture-level model to estimate ADC energy and area. To enable fast design space exploration, the model uses only architecture-level attributes while abstracting circuit-level details. Our model enables researchers to quickly and easily model key architecture-level tradeoffs in accelerators that use ADCs.

Index Terms—modeling, compute-in-memory, analog-to-digital converter, design space exploration

I. INTRODUCTION

Analog Compute-In-Memory (CiM) accelerators reduce energy in part by using low-energy and high-throughput analog computation. To read computed analog values, CiM accelerators often use analog-digital converters (ADCs). ADCs can consume significant energy and area, and architecture-level decisions such as ADC resolution or number of ADCs can impact the ADC energy and area by orders-of-magnitude [1]. For this reason, architecture-level ADC decisions can significantly affect full-accelerator energy and area [2]–[4].

ADC energy and area are key limiting factors in some architectures [2], [3], and ADC-focused tradeoffs are key optimization targets in other architectures [4]–[9]. Unfortunately, without an architecture-level model of ADC energy and area, prior work is limited to using particular ADC design points (e.g., 7-bit, 32nm, 10^9 converts/second) and can not interpolate (e.g., 7-bit, 65nm, vary throughput from 10^6 to 10^9 converts per second). The inability to interpolate limits the design points that may be evaluated and precludes exploration of the effects of architectural decisions on ADC energy and area.

To address these challenges, we present an architecturelevel model that estimates ADC energy and area given highlevel architectural parameters of resolution, throughput, and number of ADCs. In doing so, this model lets users (1) see how architectural decisions influence ADCs, (2) use consistent ADC characterizations to fairly compare architectures, and (3) explore CiM accelerator designs using different ADCs.

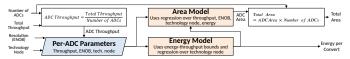


Fig. 1. The energy and area modeling pipeline.

We open-source¹ our model, integrating it into the published CiM modeling tool CiMLoop [10] and using it to model CiM architecture RAELLA [4].

II. THE ENERGY AND AREA MODEL

Fig. 1 shows the modeling pipeline. The model uses four parameters as input: (1) number of ADCs operating in parallel, (2) total throughput (*i.e.*, the aggregate number of values that the ADCs convert per second), (3) technology node, and (4) ADC resolution measured as the effective number of bits (ENOB), which measures effective ADC resolution after considering nonidealities such as noise and nonlinearity [11].

The model uses the total throughput and number of ADCs to calculate per-ADC throughput, then uses per-ADC parameters to calculate per-ADC energy and area. Energy estimates from the energy model are also used as input to the area model.

The energy and area models are generated using statistical analysis of published ADCs. Specifically, energy and area trends [12]–[20] are modeled with piecewise power functions that are fit to the Murmann ADC dataset [1] using regression¹.

Figs. 2 and 3 show the energy and area, respectively, of published ADCs alongside predictions by our model. For ease of visualization, we (1) scale published ADCs to 32nm and set the model to estimate 32nm ADCs, (2) show only lines for 4b, 8b, and 12b ADCs, rounding published ADC ENOB to the nearest of these, and (3) show only ADCs that are near Pareto-optimal.

We note that the area and energy of published ADCs can vary by orders-of-magnitude even for ADCs with the same architecture-level parameters. This is because each ADC is designed with a different microarchitecture and with different design goals. This model is not intended to capture every variable that may influence ADC area and energy. Rather, the model captures ADC area and energy trends and uses them to

¹The model and documentation are available at https://github.com/accelergy-project/accelergy-adc-plug-in.

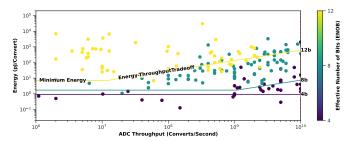


Fig. 2. Published ADC throughput versus energy. Lines show energy bounds identified by the model and dots show published ADCs. ADC energy is limited by two bounds that are a function of throughput, ENOB, and technology node.

estimate a reasonable lower-bound ADC area and energy for a given architecture.

To model a particular ADC, users may tune the tool's estimated area and energy to match that of the ADC of interest. Users may then use the tool to estimate how the area and energy of that ADC would change given a change in throughput, ENOB, or technology node.

A. The Energy Model

To estimate best-case ADC energy, we use Murmann's observation that ADC energy is limited by two throughput-dependent bounds [17]. We observe that ADC energy also depends on ENOB and technology node, so we extend Murmann's idea by using best-case energy bounds that are a function of throughput, ENOB, and technology node. At low throughputs, energy is fixed at the **minimum-energy bound**, shown in the horizontal lines in Fig. 2. At high throughputs, the **energy-throughput-tradeoff bound** leads to increasing energy with throughput. The energy-throughput-tradeoff bound begins to affect high-ENOB ADCs at relatively lower throughputs due to the design complexity of high-throughput, high-ENOB ADCs. We also find that energy increases exponentially with ENOB.

B. The Area Model

Prior works [19], [20] model ADC area using regression based on technology node, throughput, and ENOB. We found that we could improve the correlation coefficient r from 0.66 to 0.75 by using energy in place of ENOB² (note that ENOB still affects energy since energy depends on ENOB).

$$Area(um^2) = 21.1(Tech(nm))^{1.0}(Throughput)^{0.2}(\frac{Energy\ (pJ)}{Convert})^{0.3}$$

After modeling area with Eq. 1, we also optimistically reduce the estimated area to match the lowest-area 10% of ADCs to predict best-case area. The effects of this model can be seen in Fig. 3, which shows published ADC areas alongside predicted area for varying throughputs and ENOBs. The piecewise energy bounds lead to a piecewise relation between throughput and area. We can also see that area increases with throughput and ENOB.

²We hypothesize that energy improves correlation over ENOB alone because low-area layouts also reduce energy through lower wire capacitance.

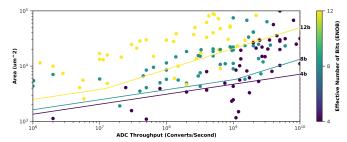


Fig. 3. Published ADC throughput versus area. Lines show predicted area and dots show published ADCs. As throughput increases, area first increases slowly, then quickly. This is because the two energy bounds influence area.

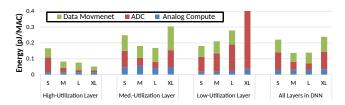


Fig. 4. Energy for varying utilization and analog sum size. Summing more analog values and reading the results with higher-ENOB ADCs (towards XL) consumes less energy with higher-utilization DNN layers.

III. EVALUATION

In this section, use our model to explore how different ADC resolutions, throughputs, and numbers of ADCs affect full-accelerator energy and area. Such explorations are made possible because our model can interpolate between many different design points. Experiments are based on the recent CiM accelerator RAELLA [4].

A. Exploring Architectures while Considering ADCs

If an accelerator performs more computations per ADC convert, it can use fewer ADC converts (less energy), but the additional computations can generate higher-ENOB analog values and require higher-ENOB ADCs (more energy). We explore this trade-off with four parameterizations of RAELLA. Small (S) sums up to 128 analog values and reads the sum with a 6-bit ADC. Medium (M), large (L), and extra-large (XL) sum up to 512, 2048, and 8192 values, reading results with 7-bit, 8-bit, and 9-bit ADCs, respectively.

Fig. 4 shows full-accelerator energy while running layers of varying sizes from the ResNet18 [21] deep neural network (DNN). For the large-tensor layer, summing more analog values reduces ADC energy by performing more computation per ADC convert. For the small-tensor layer, the small tensor size limits the number of values that may be summed, so the architectures with higher-ENOB ADCs consume more energy due to the higher-ENOB ADCs consuming more energy per convert. Over all layers in the DNN, the M and L architectures consume less energy because they balance these two effects.

B. Picking the Number of ADCs for an Architecture

Using more ADCs consumes more area but also reduces per-ADC throughput, potentially reducing ADC energy. In this test, we generate RAELLA CiM arrays that use 1, 2, 4, 8, and 16 ADCs in parallel. For each configuration, we vary

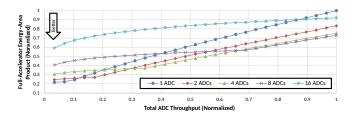


Fig. 5. Accelerator energy-area product (EAP) versus number of ADCs for varying throughputs. The number of ADCs significantly impacts EAP, and the lowest-EAP number of ADCs depends on throughput requirements.

total ADC throughput from 1.3×10^9 to 40×10^9 converts per second and measure the overall accelerator energy-area-product (EAP) while running a chosen ResNet18 layer.

Fig. 5 shows the results. We find that (1) higher total throughput leads to higher EAP as it requires more ADCs or larger, higher-energy ADCs, (2) the choice of number of ADCs can influence overall accelerator EAP by a factor of three, and (3) to minimize EAP, low-throughput accelerators should use fewer ADCs to reduce area and high-throughput accelerators should use more ADCs to reduce energy.

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