Ain Shams University
Faculty of Engineering
CSE Department

Juniors / Fall 2024
CSE 312: EDA
Group Project

Washing Machine Controller

Project Description:

The project aims at practicing the ASIC flow by implementing a washing machine controller, assume realistic design specifications for a washing machine containing the different options and buttons as the power button, alarms etc…

Teamwork:

Every group is recommended to be divided into “Design Team” and “Verification Team”:

• Design Team: Gather the Specifications and make FSM state diagram to use it in writing the Verilog Code of the Washing machine controller.

• Verification Team:

- Define a Verification plan that covers your verification intension, in word format. This should include test stimulus generation methods (random, constrained random or directed) justified when and why you will use every type with which design inputs/signals. List of Assertions/Properties that you will create in your testbench and justify which you pick this set of assertions to assure critical scenarios verified through assertion based verification, finally you should identify your code coverage goal as well as what are type of code coverage you will enable and why, i.e you will enable FSM coverage to assure good coverage for which parts, same for branch coverage for project control/data flow or toggle coverage for appropriate critical signals transitions checks.
- Create Testbench that covers (Test Stimulus using variation of directed, constrained random)
- Define design properties or assertions using PSL

- Enable code coverage and create coverage report for Statement, Branch, Toggle and FSM Coverage.

Delivery Time:

Upload Projects Deliverables on LMS by 19 Nov 2024

Project Deliverables Discussion:

Interactive discussion will be in labs, each group will have around 15 minutes time slot to show deliverables and go through project work.

Tools to Use:

• QuestaSim

Deliverables List:

The group must submit the following for evaluation:

1. PDF documenting the following:
    1. Title, group number, members names and IDs.
    2. Proposed Design Specifications
    3. FSM State Diagram.
    4. Design RTL Code.
    5. Verification Plan.
    6. Testbench Code.
    7. Simulations Waveform Snippets.

2. Compressed file contains (.v files , PDF slides).

Grades:

• 15 marks for each Contributor