CT-303 Digital Communications (LAB 3)

EXP 3: Pseudo Noise Sequence Generator and Differential Phase Shift Keying

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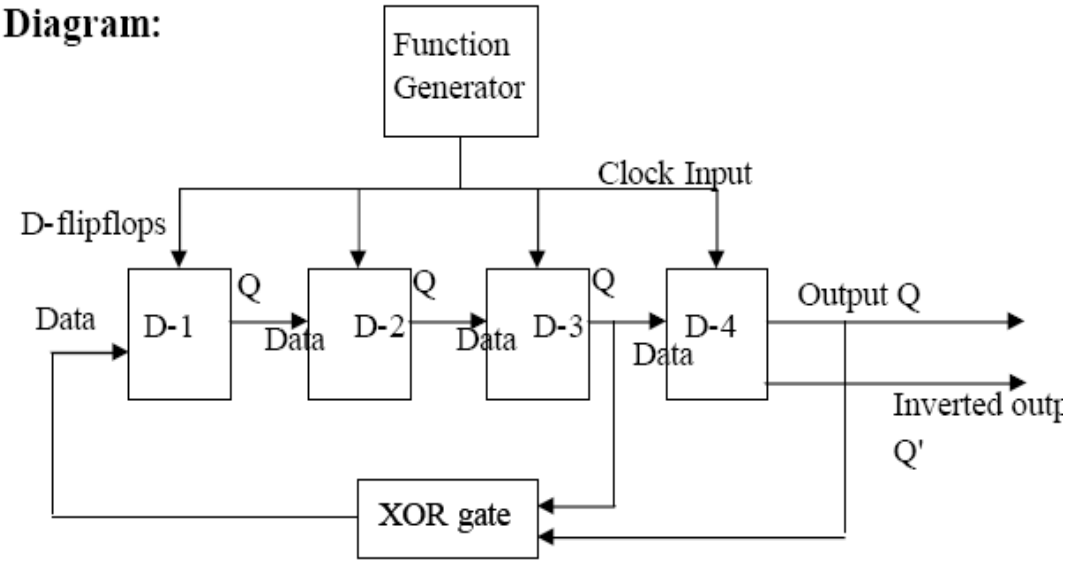
Design a PN Sequence Generator to generate random binary sequences using hardware.

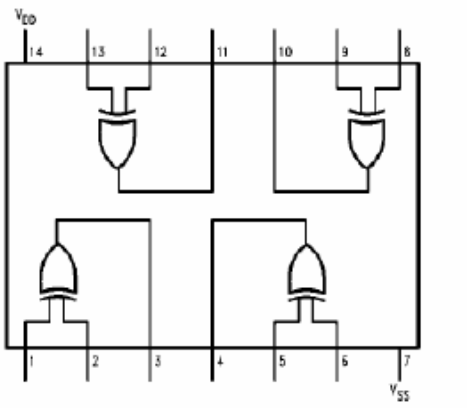
- PN sequence generator is such a device that can be used to generate experimentation data. The sequence generator generates a sequence of bits that appears to be random. Actually, the sequence repeats after some time that can be made large by increasing the no. of states of the sequence generator. Here word pseudo means that the random generated data will be periodic means it will be repeated after sometimes hence it is not completely random but it is pseudo random.

- The basic sequence generator is implemented as a Ring Counter using D-flip-flops and using combinational circuit to give the input to the counter from the current output of the flip- flops.

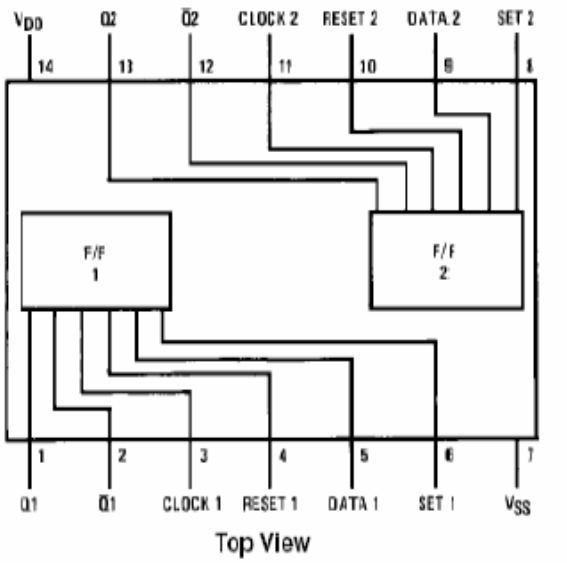
Here for D-flip flop we use IC-CD4013 and For XOR gate we use IC-CD4030.

Circuit Diagram:





IC CD4030 (XOR gate)



IC CD4013 (D flip flop)

Procedure:

1. Connect the circuit as shown above in circuit diagram.

2. For both the ICs take Vdd=5V and Vss=GND

3. First test all the flip flops in both ICs. All the Set and Reset pins should be connected to ground.

4. Connect the circuit for a Ring Counter using 4 flip- flops.

5. Give a clock of 1 KHz frequency and amplitude of 0-5V (by using DC offset) using the function generator.

6. Test the Ring counter first without connecting XOR gate, it should work as a simple 4 bit counter.

7. To generate pseudo-random sequence we need to give initial seed to the flip-flops which should not be equal to 0000

8. To give a sequence of 0001, connect Inverted output of last flip- flop (Q) to one input of XOR gate

9. Initially check the circuit by finding expected theoretical output at each point.

Properties the PN Sequence Generator(m-sequence)

1) Length of the sequence :

The length of the sequence is L = 2^N – 1. where the N represent the Number of flip flops used in the sequence generation.

2) Number of 1's and 0's in the sequence :-

No of 1's in sequence is greater than the No of 0's by one.

3) Clustering in the Sequence :-

PN sequence generator gives evidence of the fact that its sequence are not truly random and that its sequence display cluster.A cluster is a run of identical bits that occurs in sequence. That cluster is given in the table.

Number of the cluster	*Length of cluster*	*Bit value if Q output is used.*
1	N	1
1	N-1	0
1	N-2	1
1	N-2	0
2	N-3	1
2	N-3	0
4	N-4	1
4	N-4	0

4). Auto correlation of a PN sequence :-

The auto correlation function R(T) of a truly random data pulse data d(t) with bit duration Tb is defined as

Rd(T) = E{d(t)*d(t-T)}

and has a form of Triangle from [-Tb Tb] and maximum value of 1.

For a bit stream (1 represented by +1 and 0 represented by -1, which is periodic), the autocorrelation is given by

$$R_x(T) = \frac{1}{N}\sum_{n=0}^{N-1} x_(n)x_(n-T)$$

where N is the length of the sequence (period) and T is the delay. Note that this is periodic.

OUTPUT:

1. Here we connected 4 D-flip flops so that total 2^4 = 16 random sequences are generated.

2. The length of the sequence is L = 2^N – 1 = 15. where the N represent the Number of flip flops which is 4.

3. The seed value should not be 0000 because the seed value should not be 0000 because if we send this seed value the inputs in XOR gate will be both 0 and 0 so the output of XOR gate will be 0 and it will be always zero.

4. No of 1's in sequence is greater than the No of 0's by one.

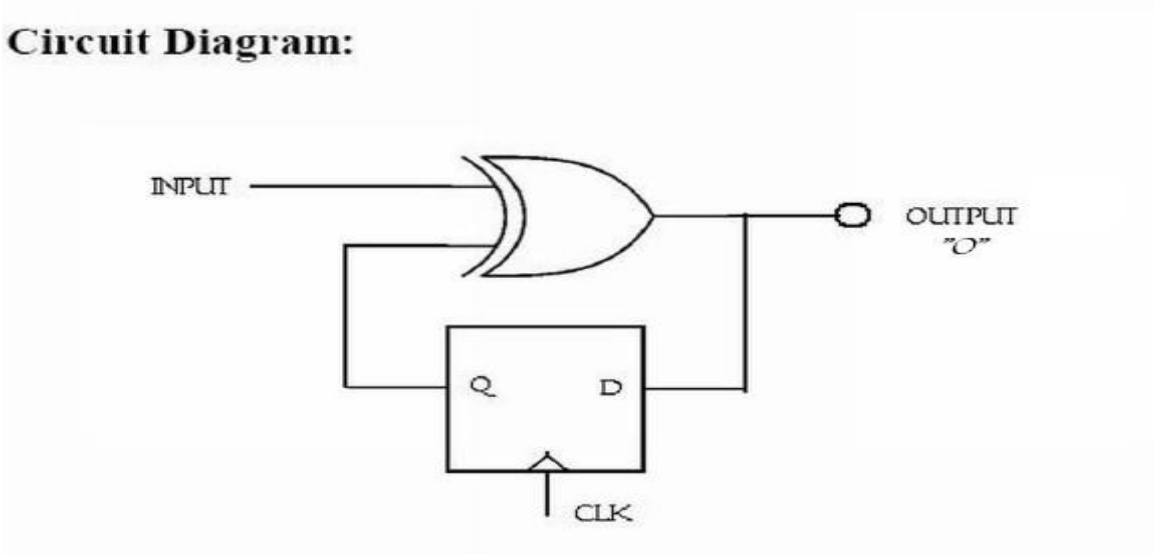
B) Differential Phase Shift Keying

AIM: Design a DPSK Generator to generate binary sequences using hardware.

Theory:

The Differential Phase Shift Keying is a non-coherent version of PSK. It eliminates the need of reference signal at the receiver by combining two basic transmitter operations, namely, a) differential encoding and b) phase-shift keying. The basic form of circuit is shown in figure. The XOR gate acts as coding logic element and D-flip-flop is used as memory element to store previous bit. The receiver would also be built on same norms. It will also have a memory element to store previous input bit for decoding.

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in circuit diagram, for both the ICs take Vdd=5V and Vss=GND.

2. First test all the flip flops in both ICs. All the Set and Reset pins should be connected to ground

3. Apply the PN sequence as one input to XOR gate.

4. Note the output of XOR gate.

In DPSK we compare the old output and latest input, If there is a difference between them then the phase shift keying is taken place otherwise not.