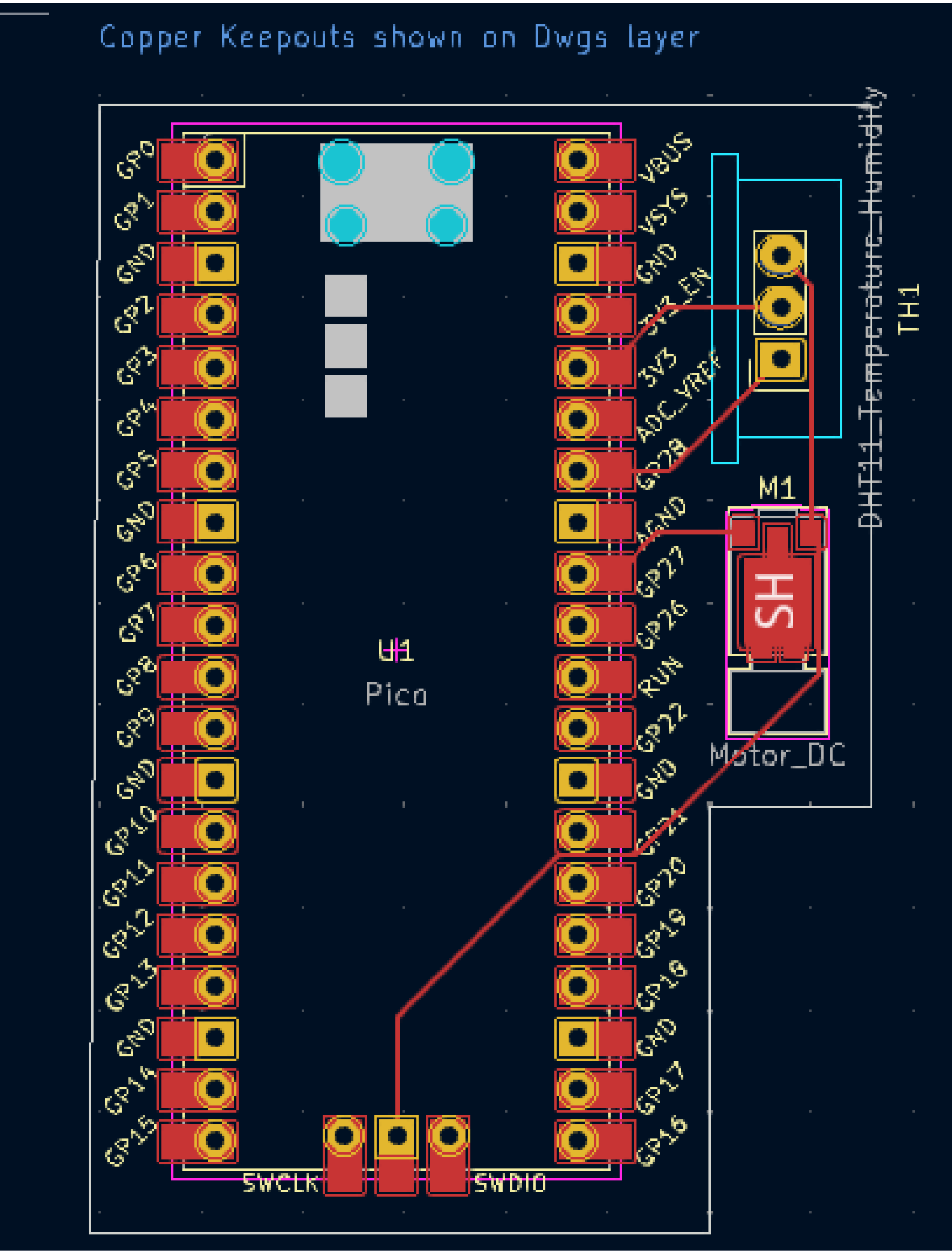
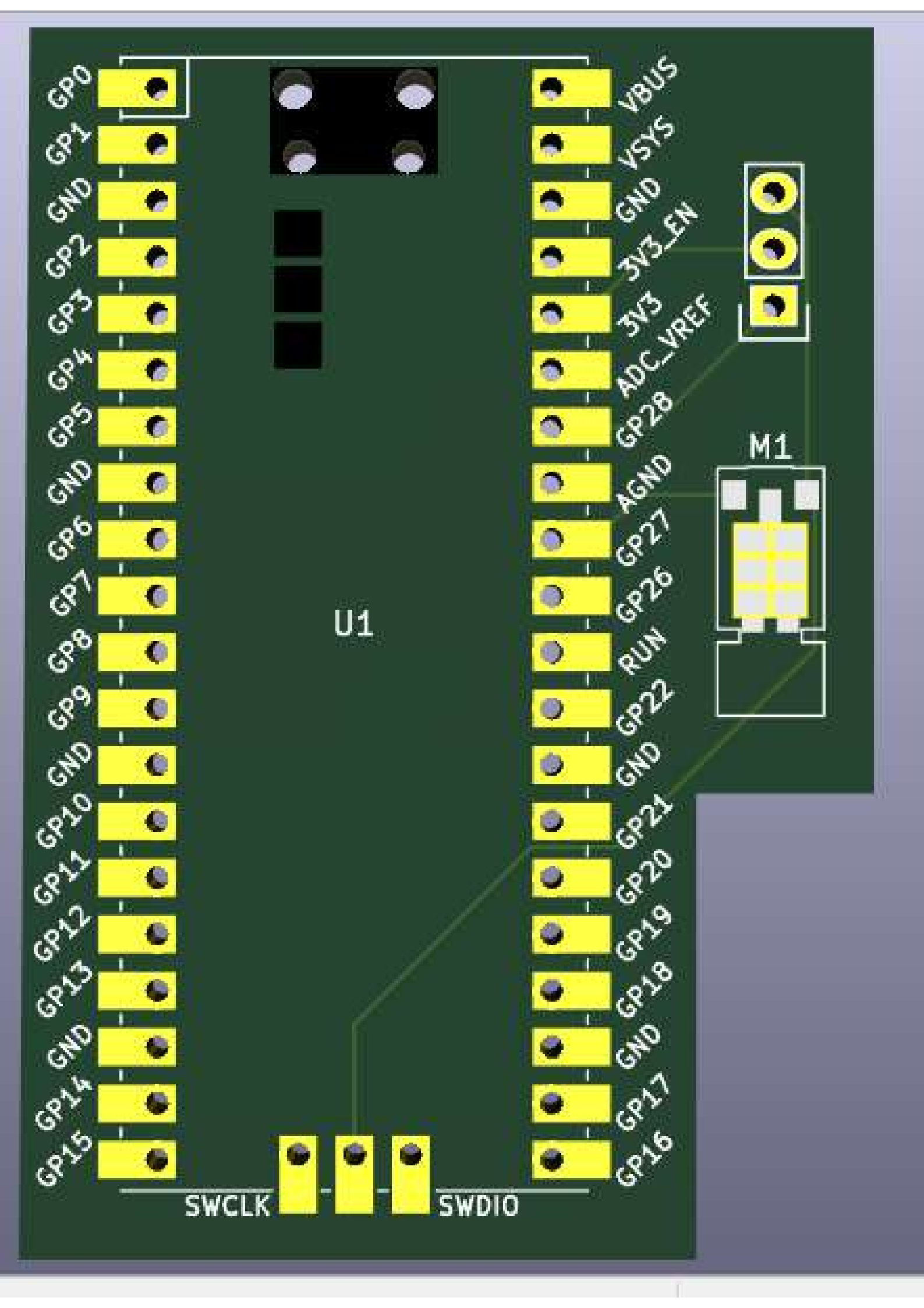
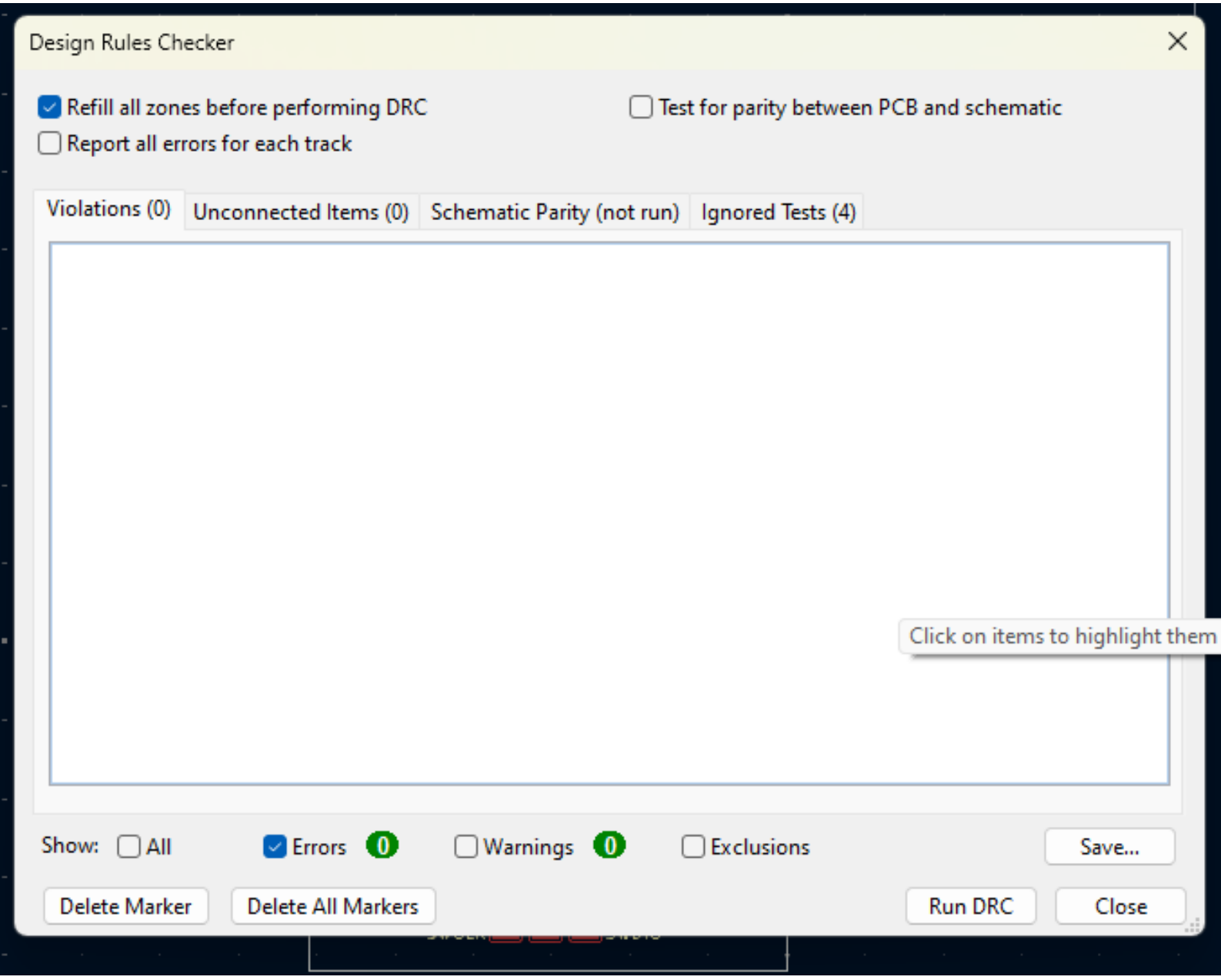

Copper Keepouts shown on Dwgs layer
GP0
GP1
GND
GP2
GP3
GP4
GP5
GND
GP6
GP7
GP8
GP9
GND
GP10
GP11
GP12
GP13
GND
GP14
GP15
VBUS
VSYS
GND
3V3_EN
3V3
ADC_VREF
GP28
AGND
GP27
GP26
RUN
GP22
GND
GP21
GP20
GP19
GP18
GND
GP17
GP16
U1
Pico
SWCLK
SWDIO
M1
SH
Motor_DC
DHT11_Temperature_Humidity
TH1


GP0
GP1
GND
GP2
GP3
GP4
GP5
GND
GP6
GP7
GP8
GP9
GND
GP10
GP11
GP12
GP13
GND
GP14
GP15
VBUS
VSYS
GND
3V3_EN
3V3
ADC_VREF
GP28
AGND
GP27
GP26
RUN
GP22
GND
GP21
GP20
GP19
GP18
GND
GP17
GP16
U1
M1
SWCLK
SWDIO


Design Rules Checker
Refill all zones before performing DRC
Test for parity between PCB and schematic
Report all errors for each track
Violations (0)
Unconnected Items (0)
Schematic Parity (not run)
Ignored Tests (4)
Click on items to highlight them
Show:
All
Errors
0
Warnings
0
Exclusions
Save...
Delete Marker
Delete All Markers
Run DRC
Close