Malcom Chiaji  
SCT212-0063/2021  
Lab3

E1: Identify hazard types and registers involved

a.  
Hazard: Data hazard (RAW)  
Registers: R1 (LD writes, DADD reads)

b.  
Hazard: Write-after-write (WAW) hazard (if in pipeline with multiple writes in-flight)  
Registers: R1 (both MULT and DADD write to R1)

c.  
Hazard: Structural hazard (if no multiple multiply units)  
Registers: None shared, but contention for multiplier

d.  
Hazard: Data hazard (RAW)  
Registers: R1 (DADD writes, SD reads)

e.  
Hazard: Data hazard (RAW)  
Registers: R1 (DADD writes, SD uses R1 as address)

E2: 2-bit Saturating Counter Predictor

a. Explanation:

A 2-bit predictor has 4 states:

* 00: Strongly not taken
* 01: Weakly not taken
* 10: Weakly taken
* 11: Strongly taken

Transitions:

* On taken, state increments (up to 11)
* On not taken, state decrements (down to 00)

Example transitions:

* From 00 → 01 → 10 → 11 on repeated taken
* From 11 → 10 → 01 → 00 on repeated not taken

b. Prediction Outcomes:

Since every other x[i] == 0 starting from first, BNEZ F1, else outcome alternates:  
NT, T, NT, T, NT, T, ...

Assuming counter starts at 00:

| Iteration | Branch Outcome | Counter Before | Prediction | Counter After |
| --- | --- | --- | --- | --- |
| 1 | NT | 00 | NT | 00 |
| 2 | T | 00 | NT | 01 |
| 3 | NT | 01 | NT | 00 |
| 4 | T | 00 | NT | 01 |
| 5 | NT | 01 | NT | 00 |
| 6 | T | 00 | NT | 01 |
| ... | ... | ... | ... | ... |

Result:  
Prediction is mostly wrong because the outcome alternates, and the counter is too slow to adapt due to its hysteresis.