LAB 5 Pre - Lab

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Exercise 1:
Code is not synthesizable as the value of n is not defined, thus the loop does not know how many times it needs to run. Secondly the sum is being read before being written inside the loop which could lead to the synthesizer creating an undefined state.

Exercise 2:
Arbitrary time delays are not supported in FPGA hardware. Clock timing is provided by external oscillators or FPGA clocking resources.
Fixed code:

```
initial clk = 0;
always begin
   #10 clk = ~clk; //in this case every 10 ns the clk toggles
end
```

Exercise 3:
A positive edge triggered D flipflop i.e the hardware reacts only on the rising edge of the clock, where en is the enable bit. When the enable bit is high i.e. **en = 1** and the clock is at the positive edge then the value of **d** is reflected as the output and when **en = 0**, **q** retains its current value.