COMPUTER ARCHITECTURE

Homework # 1

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[Question 1: 2.8]

2.8 [10] <2.2> What is the read latency experienced by a memory controller on a row buffer miss?

1) Precharge tRP = 13 ns
2) Actiavte tRCD = 13 ns
3) CAS CL =13 ns

Total = 13+ 13+ 13= 39 ns

This is because latency is the time from when the request is made till the first bit is transferred. Also, as this is a miss, the bank is charged and then activated, once the correct row is brought in the buffer, CAS is made.

[Question 2: 2.9]

2.9 [10] <2.2> What is the latency experienced by a memory controller on a row buffer hit?

CAS CL = 13 ns

As correct row is in the buffer, only column has to be specified.

[Question 3: 2.10]

2.10 [10] <2.2> If the memory channel supports only one bank and the memory access pattern is dominated by row buffer misses, what is the utilization of the memory channel?

Utilization of memory channel given by only 1 bank and only row buffer mosses is given by:

Utilization: Time in use / Total time

- The memory channel is used during data transfer only & the time it takes to transfer is 4 ns
- Total time for a row buffer miss & transfer is 39 + 4 = 43ns

  hence utilization becomes

  memory utilization = 4/ 43 x 100 = 9. 3 %

[Question 4: 2.11]

2.11 [15] <2.2> Assuming a 100% row buffer miss rate, what is the minimum number of banks that the memory channel should support in order to achieve a 100% memory channel utilization?

Assuming a 100 % row buffer miss, minimum number of banks required for 100% memory channel utilization are:

if 1 bank takes 9.3 % utilization
x banks will take 100 % utilization

1 bank = 9. 3 %
x banks = 100 %

x= 100/9.3 = 10.75 ~ 11 banks

or we can write as follows:
(4* x) / 43 = 100 %

x=(1 *43) / 4 = 10.75 ~ 11 banks

[Question 5 : 2.12]

2.12 [10] <2.2> Assuming a 50% row buffer miss rate, what is the minimum number of banks that the memory channel should support in order to achieve a 100% memory channel utilization?

So here we shall consider both row buffer miss which is 50%, rest 50% would be row buffer hit

Miss		hit (# of banks)	
0.5(4/43)*x	+	0.5(4/17)*x	= 1
(2x/43)	+	(2x/17)	= 1

x = 6.091 ~ 7 banks are required

[Question 6: 2. 13]

2.13 [15] <2.2> Assume that we are executing an application with four threads and the threads exhibit zero spatial locality, that is, a 100% row buffer miss rate. Every 200 ns, each of the four threads simultaneously inserts a read operation into the memory controller queue. What is the average memory latency experienced if the memory channel supports only one bank? What if the memory channel supported four banks?

If there is only 1 bank then latency for 1st read operation should be

1) 1st read operation (latency) = 39ns (miss latency)
2) for 2nd read operation, latency would be (1st operation full time) 39 + 4 = 43 ns wait then its own read time + (39 ns) = 82 ns
3) for 3rd read operation, it should be 43 + 43 + 39 = 125 ns
4) for 4th operation it will be 43 + 43 + 43 + 39 = 168ns

Average memory latency is (39 + 82 + 125 + 168) / 4 = 103.5 ns

What if the memory channel supported 4 banks?

If there are 4 banks and assuming every read operation looks into a different bank, then we can have pipelining which will reduce the average memory latency

1) for first memory read operation, latency would be 39 ns
2) for 2nd, considering pipelining, latency would be 39 + 4 = 43 ns
3) for 3rd, latency is 43 + 4= 47 ns
4) for 4th, latency is1st (39+4 ns) + 2nd (4 ns) + 3rd(4 ns) = 51 ns

average memory latency = 39+43+47+51 / 4 = 180/4 =45 ns

[Question 7: 2.14]

[10] <2.2> From these questions, what have you learned about the benefits and downsides of growing the number of banks?

Benefits:

1. Increasing number of bank decreases memory latency and quite obviously, as we observed in the last question.
2. More banks allow pipelining concept to be implemented
3. Having more banks, allows 100 % memory utilization and the memory channel does not remain idle.

Downsides:

1. Increasing number of banks of course inverses the hardware cost.
2. Fabrication and designing of the DRAM is also a challenge

[Question 8 : 2. 15] optional

2.15 [20] <2.2> Now let's turn our attention to memory power. Download a copy of the Micron power calculator from this link: https://www.micron.com/$/media/ documents/products/power-calculator/ddr3_power_calc.xlsm. This spreadsheet is preconfigured to estimate the power dissipation in a single 2 Gb Â8 DDR3 SDRAM memory chip manufactured by Micron. Click on the "Summary" tab to see the power breakdown in a single DRAM chip under default usage conditions (reads occupy the channel for 45% of all cycles, writes occupy the channel for 25% of all cycles, and the row buffer hit rate is 50%). This chip consumes 535 mW, and the breakdown shows that about half of that power is expended in Activate operations, about 38% in CAS operations, and 12% in background power. Next, click on the "System Config" tab. Modify the read/write traffic and the row buffer hit rate and observe how that changes the power profile. For example, what is the decrease in power when channel utilization is 35% (25% reads and 10% writes), or when row buffer hit rate is increased to 80%?

< micron Power Calculator for DDR3 SDRAM >

Default usage conditions in the excel under system Config tab

were RD % - 30 %

WR – 30 %

and power consumption on Summary Tab was

Total DPR3 SDRAM power 349. 7 mW

If channel utilization is altered, and changed to

25 % - read
10 % - write

in System Config tab

Observation : Total DDR3 SDRAM power decreases to 215.9 mw

If row buffer hit rate is increased from 50 % (default) to 80 %

we observe total power remains same 215.9 mw

* Hence, channel utilization is proportional to power consumption whereas hit rate does not affect power

Last Question 2.16 continued ahead

[Question 9 : 2.16] optional

2.16 [20] <2.2> In the default configuration, a rank consists of eight Â8 2 Gb DRAM chips. A rank can also comprise16Â4 chips or 4Â16 chips. You can also vary the capacity of each DRAM chip—1 Gb, 2 Gb, and 4 Gb. These selections can be made in the "DDR3 Config" tab of the Micron power calculator. Tabulate the total power consumed for each rank organization. What is the most power-efficient approach to constructing a rank of a given capacity?

With Default configuration, of 2GB x 8;
power consumption is 210 mW

Power consumption varies as follows with different ranks

	DRAM	
1.	1 GB x 8	207.2 mW
2.	2 GB x 8	210.0 mW
3.	4 GB x 8	196.5 mW

	DRAM	
1.	1 GB x 16	349.7 mW
2.	2 GB x 16	352.0 mW
3.	4 GB x 16	302.1 mW

As per the above values we observe a capacity size of 4 GB is best with either 8 or 16 DRAM chips per rank, as then we get minimum power consumption.