Digital Electronic Circuits

CA #5

Layout Design

Required Part:

You are already familiar with the very abstract form of layout representation of relative placement and interconnections between transistors using stick diagrams. In this assignment, you are about to design the layout of a 3-bit add-and-shift multiplier in a more-detailed paradigm using L-edit environment.

The suggested representation of the add-and-shift multiplication design is shown in *Figure1* and *Figure 2*.

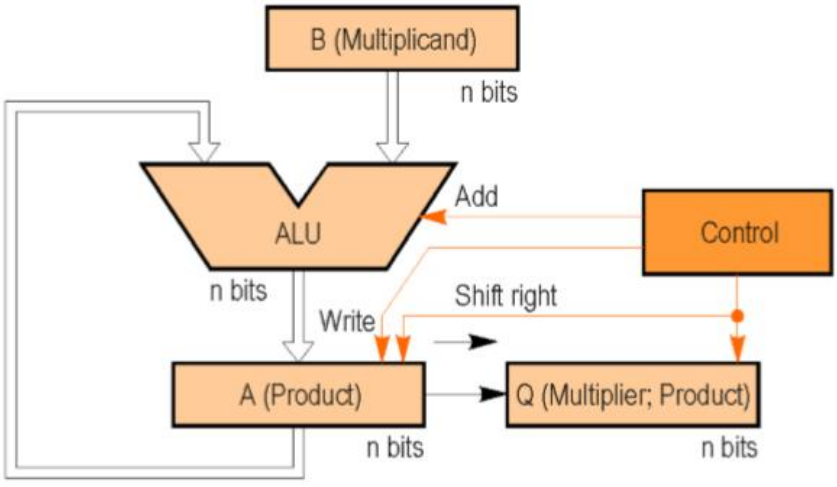

Figure 1. Add-and-shift multiplication circuit

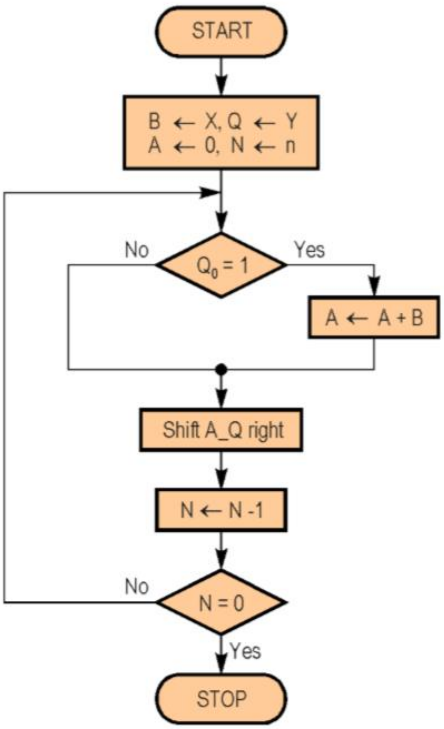

Figure 2. Add-and-shift multiplication algorithm

Bonus Part:

Here is an extra part if you wish higher marks.

You should sketch a 6-bit ripple carry adder (RCA). Afterwards, it must be connected to the first part in order to make a multiplier-accumulator unit (MAC).

Objectives:

1. Implement these designs using *L-edit*.
   Use MHP_NS8.TDB as layout template and MHP_NS8.EXT to extract your netlist.
2. Extract the layout into a *.sp* file and simulate it in *H-spice* using 180nm_bulk.pm.
3. Present a complete report including clear plots, algorithms, schematics and etc.

Attentions:

- It is recommended to design and verify each gate individually to make sure they are working accurately.
- Most of your mark is based on your report.
- The lesser your area, the higher your mark.

Good luck
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