Enhancing the lifetime of Non-Volatile Memory by hybrid cache-replacement-policy

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Problem Statement

- Due to **limited write endurance** and **high write energy** in NVM, Effective write mechanism is required to utilize the full efficiency of Non-Volatile Memory.
- The proposed technique will **improve the lifetime** of the cache sub systems by combining **Wear-leveling** and **Write Minimization techniques**.

Existing Solution

EqualWrites

- Using Wear-Leveling Technique, EqualWrites reduces the Intra-Set variations by redirecting writes of the hot blocks (Maximum writes) to the cold blocks (Minimum writes).

LER Replacement Algorithm

- The idea is to place the incoming block in a line that incurs the minimum error rate in WRITE operation. This is done by comparing the contents of the incoming block with lines in a cache set.

Drawbacks of Existing Solution

- Existing Solution does not utilize the full capacity and efficiency of the Non-Volatile Memory.
- The major disadvantage of Non-Volatile Memory is their high error rate during write operation, which is not considered.
- EqualWrites distribute the number of writes on the block level and it does not handle repeated writes on the same cell inside the cache block, which may lead to Security threat.

Proposed Methodology

- The high error rate during write operation and unequal writes can be controlled by designing a **hybrid cache-replacement-policy** which in turn improves the lifetime of the Cache Subsystems.
- During new data write into memory cell, bit flipping (either **0 to 1** or **1 to 0 transition**) can happen.
- The error rate during **0 to 1 transition** is 100 times higher than **1 to 0 transition**, because of voltage fluctuation.

Proposed Methodology

- Before writing a new data into the cache block, a quick bit-by-bit inspection is done to compute,
  - Hamming distance between Existing data and Incoming data
  - number of 0 to 1 transition
- If the hamming distance is more than half of the size of the block, data will be stored in inverted format, which will ensures at-most half number of cells will be involved in write operation.
- The line within the set which has least number of **0 to 1 transition and minimum writes within the set** will be chosen.

Proposed Methodology

- Within the cache block, a repeated write operations of data on the selective cells may shorten the lifetime of the cache block, which is considered as serious Security threat.
- This can be overcome by rotating the bit location within the cache line without fixing the static location.

Work done

Tools

- GEM5 Simulator
- Evaluation using PARSEC benchmark suite
- **Operating System :** Ubuntu 14.04
- **Language :** C++, Python

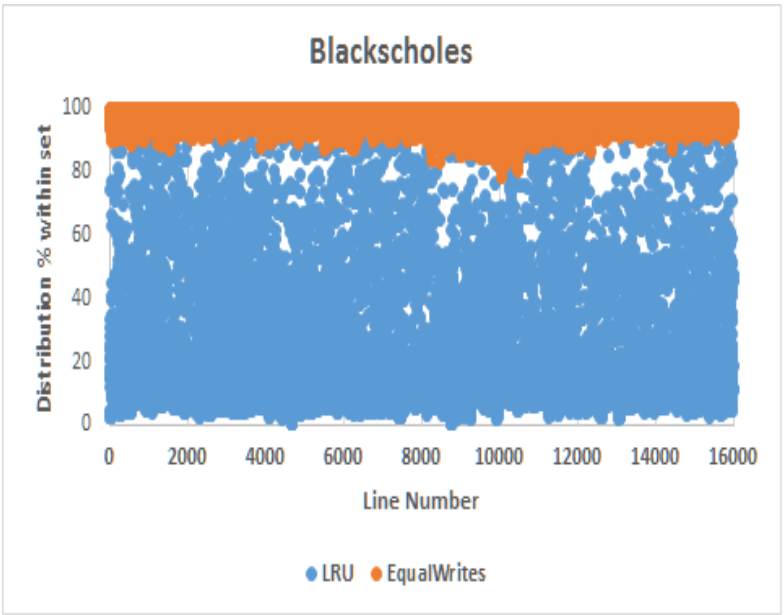
Experimental Setup

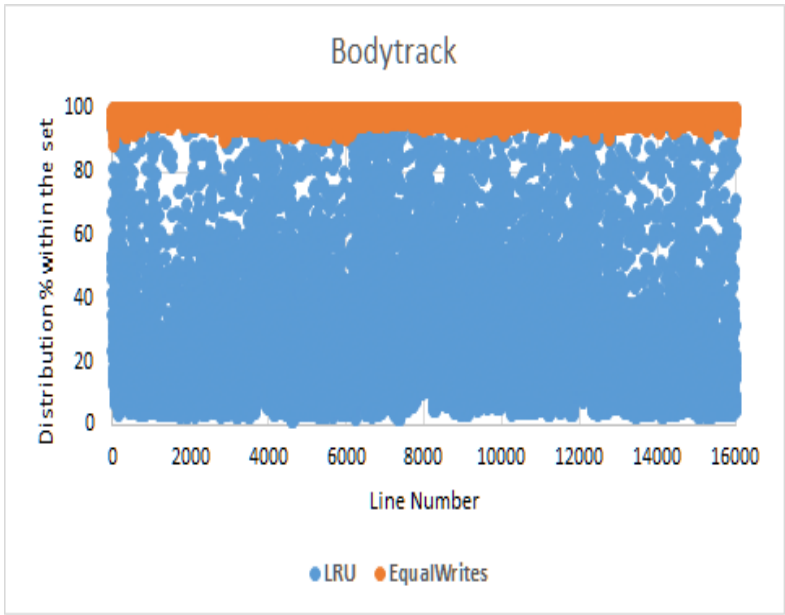
- Installation of GEM5 Simulator
- Integration of GEM5 with PARSEC benchmark suite

Results

EqualWrites

- Implemented **EqualWrites** Technique, compared the Intra-set variations with **LRU** Replacement policy

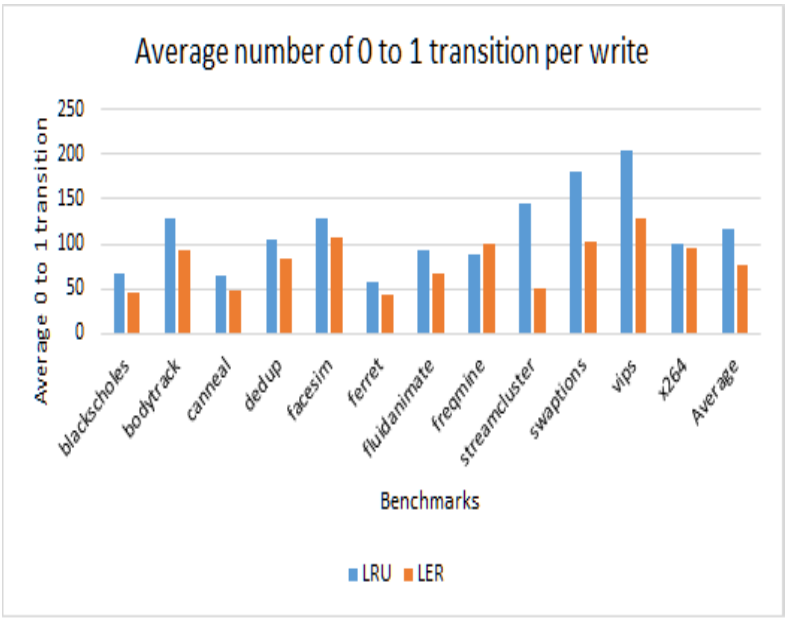


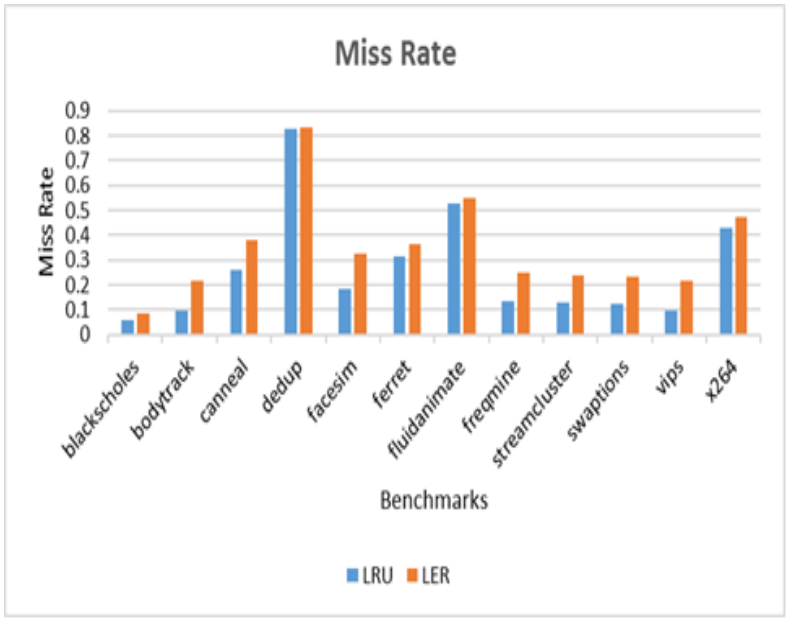


Results

LER Replacement Policy

- Implemented **LER** Replacement Technique, compared the Error-rate with **LRU** Replacement policy





References

[1] Mittal, Sparsh, and Jeffrey S. Vetter. "Equalwrites: Reducing intra-set write variations for enhancing lifetime of non-volatile caches." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.1 (2016): 103-114.

[2] Monazzah, Amir Mahdi Hosseini, Hamed Farbeh, and Seyed Ghassem Miremadi. "LER: Least-error-rate replacement algorithm for emerging STT-RAM caches." IEEE Transactions on Device and Materials Reliability 16.2 (2016): 220-226.

[3] Cho, Sangyeun, and Hyunjin Lee. "Flip-N-Write: A simple deterministic technique to improve PRAM write performance, energy and endurance." Microarchitecture, 2009. MICRO-42. 42nd Annual IEEE/ACM International Symposium on. IEEE, 2009.

Thank You