A Low Power Phase-Change Random Access Memory using a Data-Comparison Write Scheme

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***Abstract*—A low power PRAM using a data-comparison write (DCW) scheme is proposed. The PRAM consumes large write power because large write currents are required during long time. At first, the DCW scheme reads a stored data during write operation. And then, it writes an input data only when the input and stored data are different. Therefore, it can reduce the write power consumption to a half. The 1K-bit PRAM test chip with 128×8bits is implemented with a 0.8μm CMOS technology with a 0.5μm GST cell.**

I. INTRODUCTION

Phase-change random access memory (PRAM) is an attractive nonvolatile memory. PRAM has many advantages such as random access, non-volatility, good scalability, fast read time, moderately fast write time, good endurance for repetitive writing, and compatibility with CMOS process [1]. PRAM is much faster than Flash memory because PRAM can write any byte data but Flash memory writes data in block unit with complicated time consuming process [2]. PRAM is smaller than SRAM, and it does not consume standby power like as DRAM and SRAM. Therefore, PRAM is very attractive for low power mobile applications.

Fig. 1 shows the basic structure of the implemented PRAM unit-cell. The PRAM cell is composed of a standard NMOS access transistor and a storage element of chalcogenide alloy (GST: $Ge_2Sb_2Te_5$). The GST is connected to a bit line (BL). When the PRAM cell is selected, the word line (WL) turns on the NMOS access transistor. The GST has two resistances according to the stored data as shown in Fig. 2. At SET state, the GST has low resistance with data '0'. At RESET state, the GST has high resistance with data '1'. PRAM utilizes the reversible phase-change phenomena between crystalline state (SET) and amorphous state (RESET) by electrical resistive joule heating. To make SET state, the GST is heated by SET current during SET time, as shown in Fig. 3. On the contrary, to make RESET state, the GST is heated by RESET current during RESET time.

The PRAM write power is significantly large because the SET and RESET currents are large and the SET and RESET times are considerably long. It can limit the PRAM applications for mobile devices. In this paper, a low power PRAM using a data-comparison write (DCW) scheme is proposed to reduce the write power.

This paper is organized as follows. Section 2 introduces the concept and circuit implementation of the data-comparison write scheme. Section 3 shows the chip implementation and simulation results. Finally, Section 4 concludes this paper.

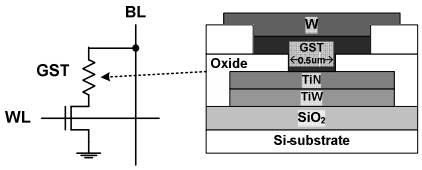

Figure 1. Basic structure of PRAM unit-cell

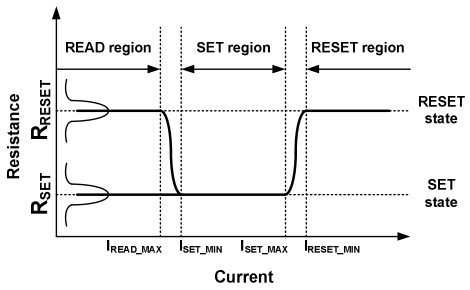

Figure 2. Typical GST R-I curve

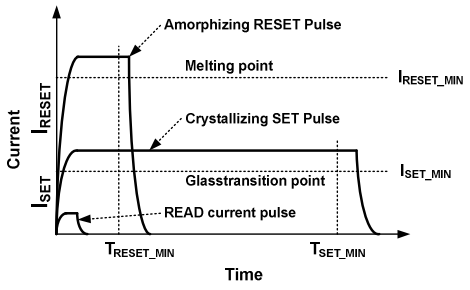

Figure 3. Current pulses during the read, set, reset operations

II. DATA-COMPARISON WRITE SCHEME

A. Concept of the DCW Scheme

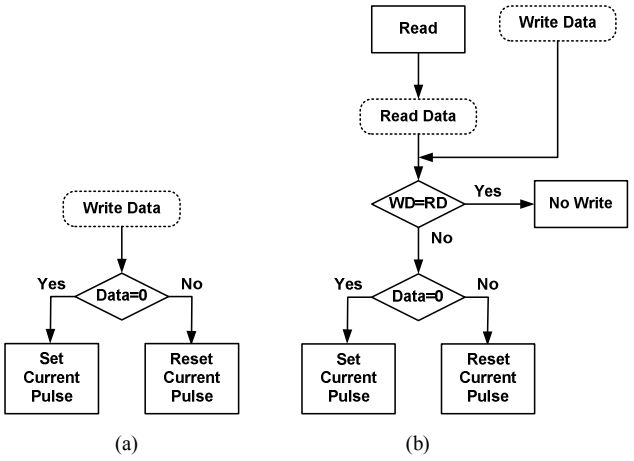

Figure 4. Flowchart of (a) Conventional write scheme (b) Proposed data-comparison write scheme

TABLE I. POWER COMPARISON OF TWO WRITE SCHEMES

Cell Data Transition	Conventional Scheme		Proposed Scheme	
	Power	*Probability*	*Power*	*Probability*
0 → 0	P_{SET}	1/4	0	1/4
0 → 1	P_{RESET}	1/4	P_{RESET}	1/4
1 → 0	P_{SET}	1/4	P_{SET}	1/4
1 → 1	P_{RESET}	1/4	0	1/4
Average Power	**$(P_{SET} + P_{RESET})/2$**		**$(P_{SET} + P_{RESET})/4$**	

Fig. 4(a) shows the flowchart of the conventional write scheme. The conventional PRAM directly writes data on the selected PRAM cell independent of the previously stored data. If input data is '0', the SET operation consumes the SET power (P_{SET}). If input data is '1', the RESET operation consumes the RESET power (P_{RESET}). There are four cases for cell data transition as shown in Table 1. (0→0, 0→1, 1→0, 1→1) When the probabilities of four cases are 1/4, the average power of the conventional write scheme is (P_{SET} + P_{RESET})/2.

Fig. 4(b) shows the flowchart of the proposed data comparison write (DCW) scheme. The DCW scheme performs the read operation before the write operation to know the previously stored data in the selected PRAM cell. If the input data and the previously stored data are the same, no write operation performs. If not, the write operation is the same as the conventional write scheme. When the probabilities of four cell data transitions are 1/4, the DCW scheme does not consume the write power for two cases (0→0, 1→1). Therefore, the average power of the DCW scheme is (P_{SET} + P_{RESET})/4 which is a half of that of the conventional write scheme.

B. Circuit Implementation of the DCW-PRAM

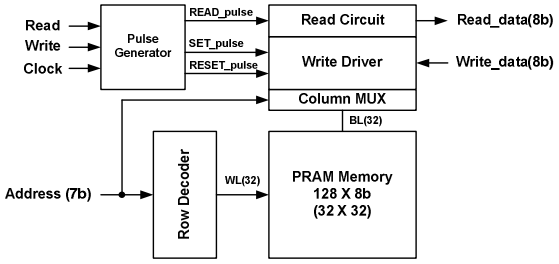

Figure 5. Simplified block diagram of the DCW-PRAM

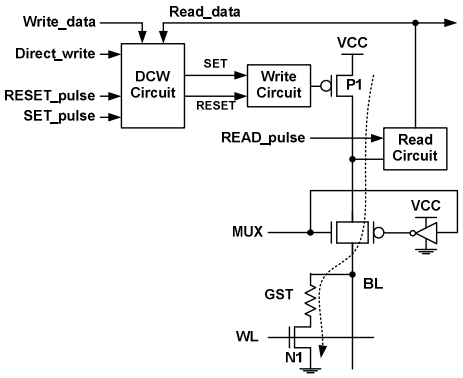

Figure 6. Simplified DCW circuit

Fig. 5 shows the simplified block diagram of the data comparison write PRAM (DCW-PRAM). Input address selects 8 cells with a selected word line and 8 selected bit lines. The pulse generator makes 3 timing pulse signals (READ_pulse, SET_pulse, RESET_pulse) with 3 external signals (Read, Write, Clock). The read circuit and write driver perform the read and write operations with 3 timing pulse signals and the write data.

Fig. 6 shows the simplified DCW circuit to write data. A PRAM cell is selected by an enabled word line (WL). A bit line (BL) is connected to the read and write circuits by a MUX. The read circuit senses the stored data from the GST resistance according to the stored data. The write circuit supplies SET and RESET current pulses to changes the GST resistance.

The PRAM uses two power supply voltages V_{CC} and V_{DD}. High voltage V_{CC} is required to supply large SET and RESET currents into the GST cell. The MUX signals also use V_{CC} to pass the write currents with high voltage. Low voltage V_{DD} is used for most of circuits except for the write current related circuits.

Fig. 7 and 8 show waveforms of the conventional and proposed write operations, respectively. In the conventional write scheme, if the write data is '0', a long SET current pulse is supplied into the selected PRAM cell. If the write data is '1', a short SET current pulse is supplied. The conventional write scheme consumes the write power independent of the cell data transition. In the DCW scheme,

the selected cell data is sensed in the read circuit by the read pulse. The DCW circuit in Fig. 5 generates the SET or RESET signal for the write circuit only when the write data and read data are different, as shown in Fig. 8. Although the DCW scheme needs an additional read operation during the write operation, the read time and power are quite smaller than the write time and power. The write power of the DCW scheme is almost a half of the conventional write scheme.

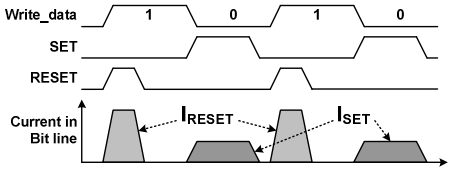

Figure 7. Waveforms of the conventional write operation

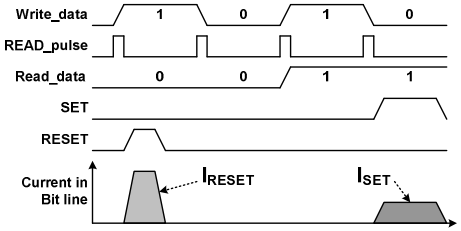

Figure 8. Waveforms of the proposed write operation

Fig. 9 shows the read circuit of the DCW-PRAM. During the read operation, the P2 transistor supplies the small read current into the selected bit line. To prevent unintentional write, the bit line is clamped by the N3 transistor with Vclamp. The voltage of the bit line is sufficiently lower than the threshold voltage of GST cell. When the GST has high resistance, the voltage of the sense amplifier input (Vread) rises to V_{DD}. When the GST has low resistance, Vread falls to ground.

Fig. 10 shows the DCW circuit of the DCW-PRAM. The DCW circuit is very simple. It compares the read data and write data. When the cell data is changed or the direct_write signal is '1', the DCW circuit generates the SET or RESET signal. The driect_write signal is required for the GST cell initialization after the fabrication. If the write data is '0', the SET signal is generated by the SET_pulse. If the write data is '1', the RESET signal is generated by the RESET_pulse.

Fig. 11 shows the digital controlled write circuit of the DCW-PRAM. It can supply exact two SET and RESET currents by various size driver transistors. The driver transistor size is digitally controlled by setting SET_current and RESET_current values. The width of the transistors varies from 1 to $2^{(i-1)}$. The total transistor widths for the SET and RESET currents are easily selected by the combination of *i*-transistors. A level shifter for each driver transistor is required. The SET and RESET currents are easily adjusted by the digitally controlled current setting signals for process, temperature, and voltage variations.

Although the write circuit can be implemented by a simple current mirror as shown in Fig. 12, the current driver transistor size is much larger than that of the digital controlled write circuit. The voltage between gate and source (V_{GS}) of the current driver transistor in the digital controlled write circuit is V_{CC}, but V_{GS} of that in the current mirror write circuit is closed to V_{TH} of PMOS transistor, which is much lower than V_{CC}. Much smaller transistor is enough for the same SET and RESET currents in the digital controlled write circuit.

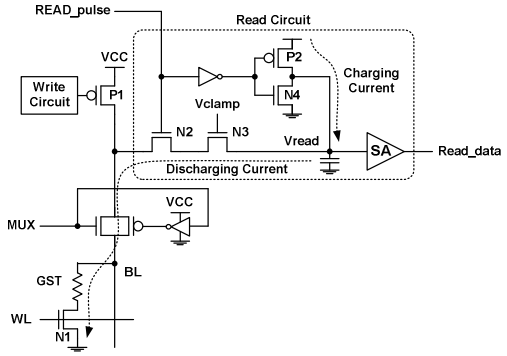

Figure 9. Read circuit of the DCW-PRAM

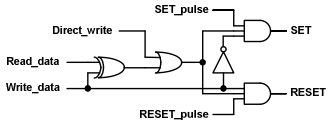

Figure 10. DCW circuit of the DCW-PRAM

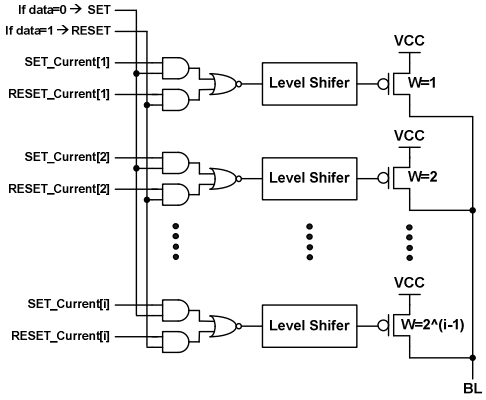

Figure 11. Digitally controlled write circuit of the DCW-PRAM

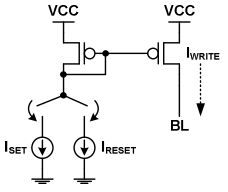

Figure 12. Current mirror write circuit of the DCW-PRAM

III. CHIP IMPLEMENTATION

The 1K-bit PRAM test chip with 128×8bits is implemented with a 0.8µm CMOS technology with a 0.5µm GST cell. Fig. 13 shows the chip layout. The core area of the test chip is 2.11mm^2. The features of the test chip are tabulated at Table 2. The PRAM chip uses two power supply voltages V_{DD}=5V for logic circuits and V_{CC}=14V for SET and RESET currents.

Fig. 14 shows the simulated waveforms. After the 10ns read pulse, if the write data is different from the read data, 4.5mA SET current or 16mA RESET current is supplied into the GST cell during 1µs or 50ns. The current pulse values are from the electrical characteristics of the GST cell in Fig. 15. To improve the stability of the write operation, slightly larger SET and RESET current pulse values are selected than the measured electrical characteristics.

The read time is 10ns and the read energy is only 74pJ/bit, whereas the write time is about 1µs and the SET and RESET energies are 64nJ/bit and 12nJ/bit respectively. The additional read operation of the DCW scheme has only 1% time and 0.2% energy overheads, but it can reduce the write power to a half.

IV. CONCLUSION

In this paper, a low power PRAM is proposed to reduce the large write power by using the data-comparison write (DCW) scheme. It performs the read operation before the write procedure, and executes the writes operation only if the input and the stored data are different. Therefore, it can reduce the write power consumption to a half when all probabilities for cell data transitions are the same. The 1K-bit PRAM test chip with 128×8bits is implemented with a 0.8µm CMOS technology with a 0.5µm GST cell. The DCW scheme can reduce the write power to a half with negligibly small time overhead.

V. ACKNOWLEDGEMENT

This work was supported by the Regional Research Center Program of the Ministry of Education and Human Resources Development in Korea. Authors thank IDEC for CAD tool support.

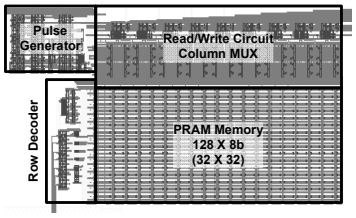

Figure 13. Layout of the DCW-PRAM chip

TABLE II. FEATURES OF THE DCW-PRAM CHIP

Technology	0.8µm CMOS process with 0.5µm GST cell and 2 metals
Organization	128 × 8 bits
Supply Voltage	V_{DD} = 5V
	V_{CC} = 14V
Read Time	10 ns
Write Time	SET = 1000 ns @ 4.5mA
	RESET = 50 ns @ 16mA
Chip Core Area	2.11 mm^2 (2.03mm × 1.04mm)
Energy / bit	READ = 74pJ
	SET = 64nJ
	RESET = 12nJ

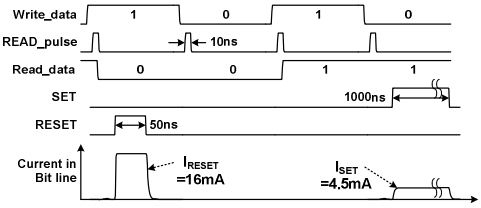

Figure 14. Simulated waveforms of the DCW-PRAM

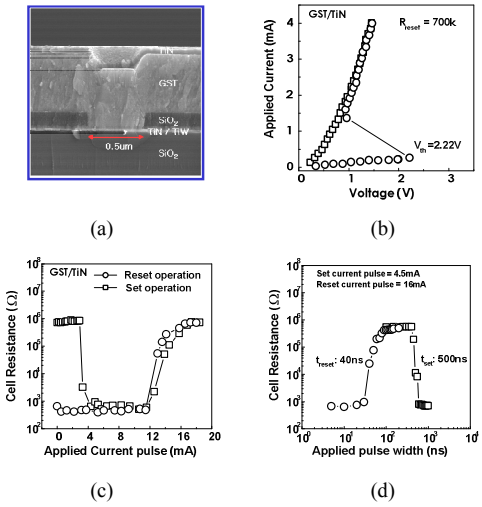

Figure 15. Electrical characteristics of the GST cell

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