Lecture 16 – Sequential circuits 2

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Chapter 5

Latches

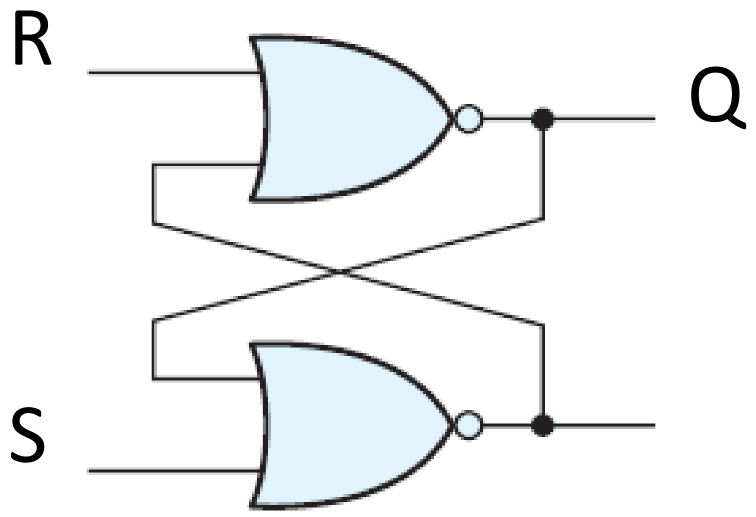
- A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states

- Such a storage element is called a latch

- The major differences among various types of storage elements are in the number of inputs they possess and in the manner in which the inputs affect the binary state

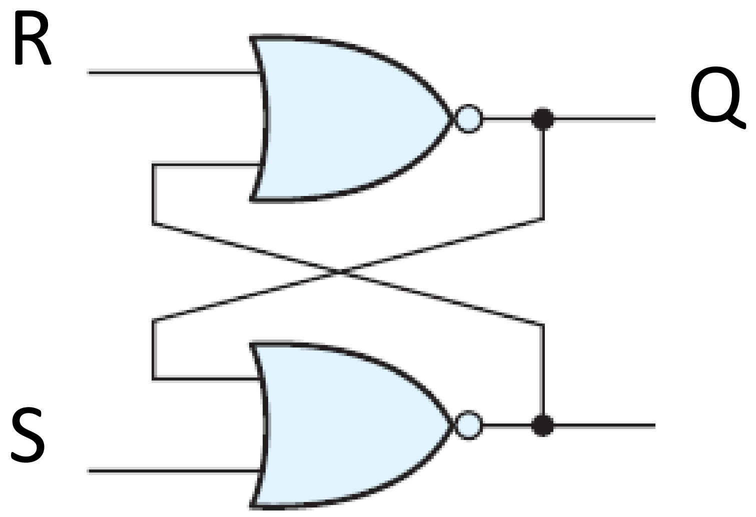
SR Latch

- The *SR* latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled *S* and *R*
- Let’s analyze…



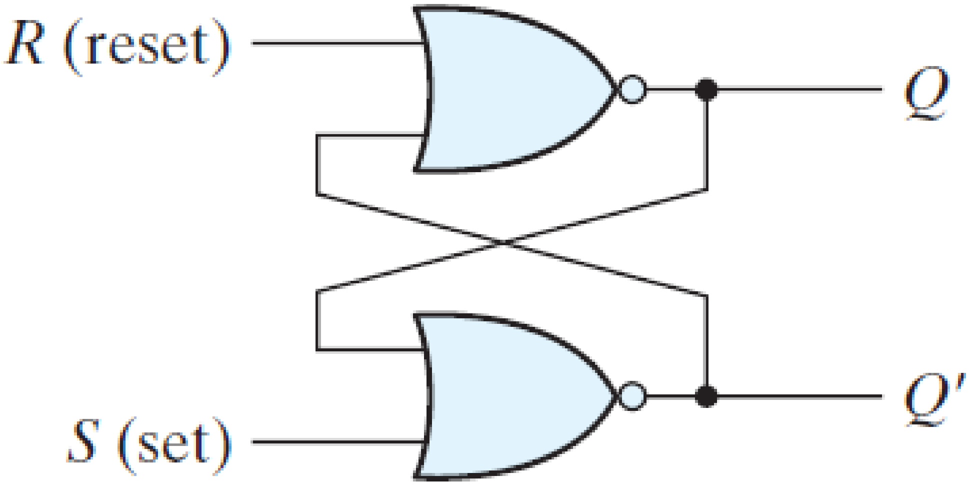
SR Latch

- We realize that the outputs *Q* and *Q′* are normally the complement of each other
- The latch has two stable states
- When output *Q* = 1 and *Q′* = 0, the latch is said to be in the *set state*
- When *Q* = 0 and *Q′* = 1, it is in the *reset state*



SR Latch

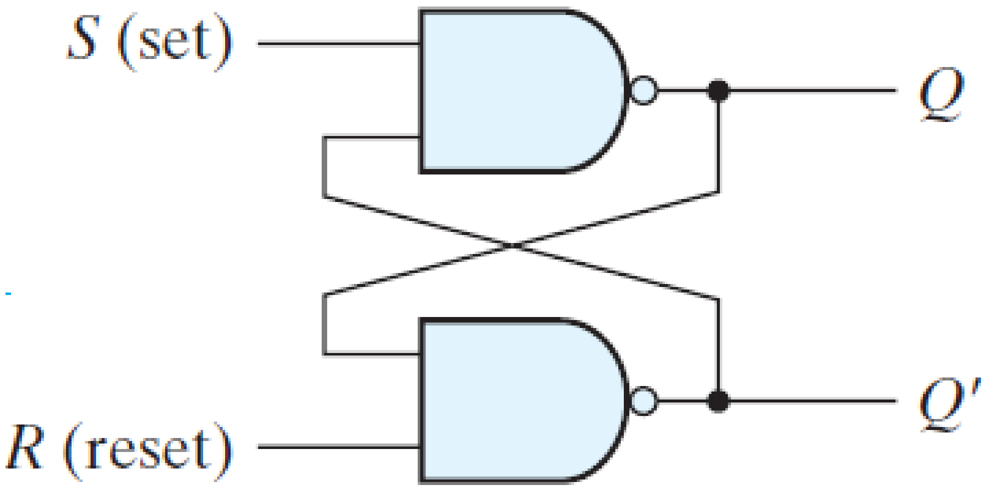
- Setting and resetting can be done through the two inputs (SR)
- After setting or resetting, applying 00 at the input retains the previous state
- However, when both inputs are equal to 1 at the same time, a condition in which both outputs are equal to 0 (rather than be mutually complementary) occurs
- If both inputs are then switched to 0 simultaneously, the device will enter an unpredictable or undefined state or a metastable state



S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

SR Latch – NAND implementation

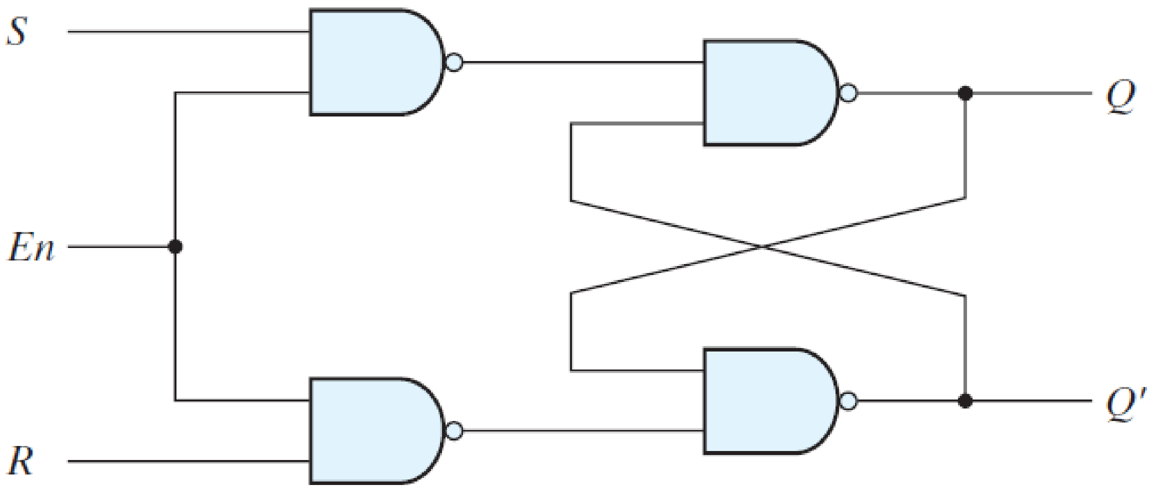
- The *SR* latch with two cross-coupled NAND gates behaves in a similar way to NOR implementation
- It operates with both inputs normally at 1, unless the state of the latch has to be changed
- The application of 0 to the *S* input causes output *Q* to go to 1, putting the latch in the set state
- When the *S* input goes back to 1, the circuit remains in the set state
- The condition that is forbidden for the NAND latch is both inputs being equal to 0 at the same time, an input combination that should be avoided



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

Latch with enable

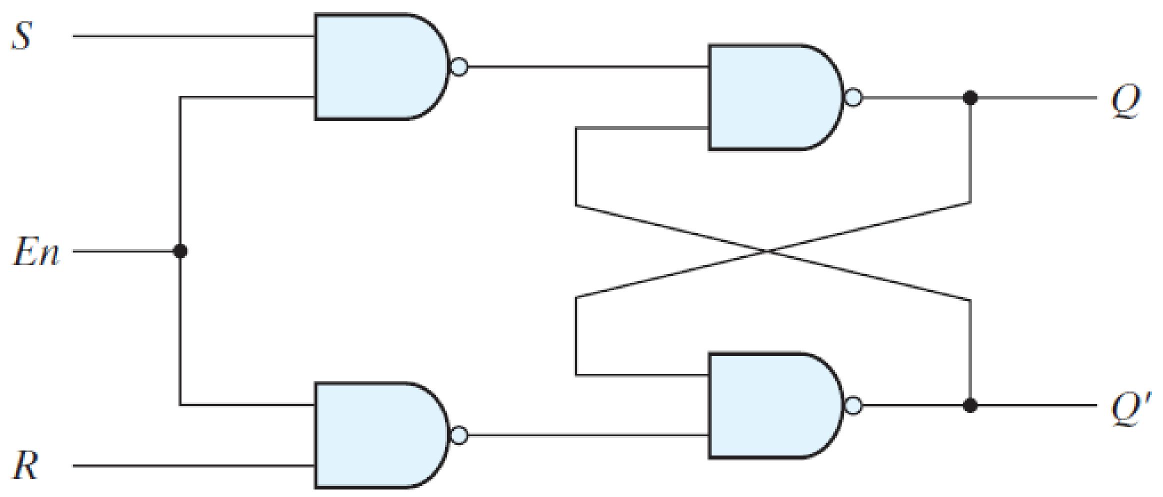
- The operation of the basic *SR* latch can be modified by providing an additional input signal that determines (controls) *when* the state of the latch can be changed by determining whether *S* and *R* (or *S* and *R*) can affect the circuit
- It consists of the basic *SR* latch and two additional NAND gates
- The control input *En* acts as an *enable* signal for the other two inputs
- The outputs of the NAND gates stay at the logic-1 level as long as the enable signal remains at 0
- This is the quiescent condition for the *SR* latch



En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

Latch with enable

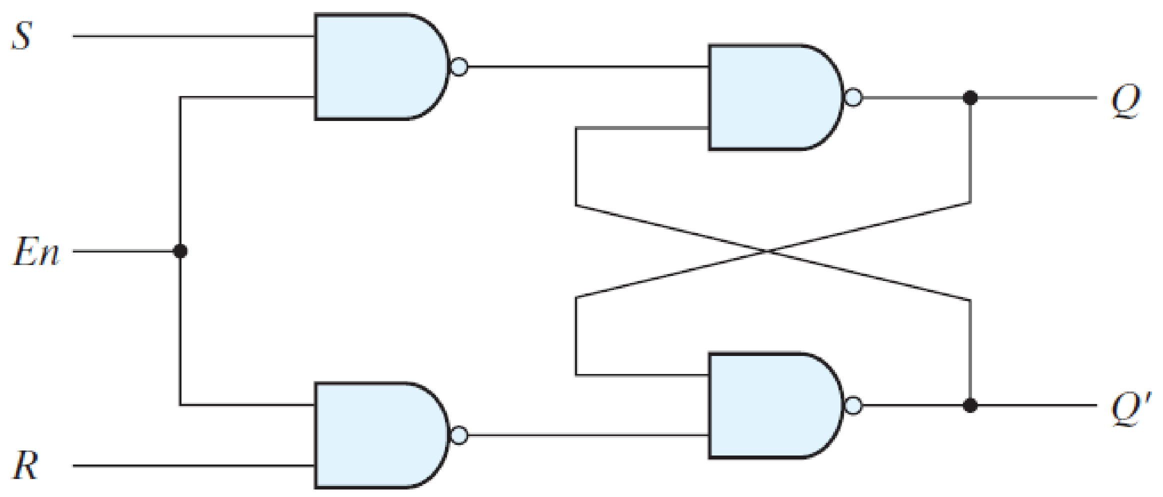
- When the enable input goes to 1, information from the *S* or *R* input is allowed to affect the latch
- The set state is reached with *S* = 1, *R* = 0, and *En* = 1 (active-high enabled) and reset is reached with *S* = 0, *R* = 1, and *En* = 1
- In either case, when *En* returns to 0, the circuit remains in its previous stable state
- Further, when *En* = 1 and both the *S* and *R* inputs are equal to 0, the state of the circuit does not change



En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

Latch with enable

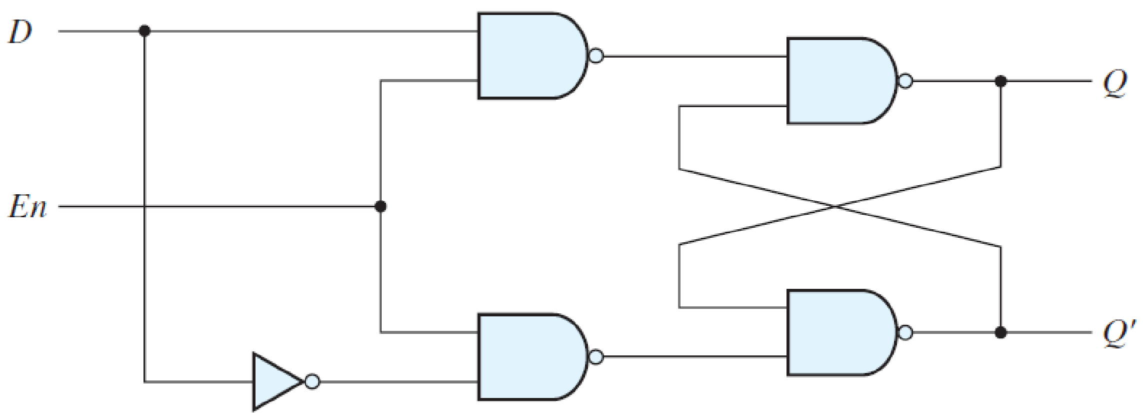
- An indeterminate condition occurs when all three inputs are equal to 1
- This condition places 0's on both inputs of the basic *SR* latch, which puts it in the undefined state
- When the enable input goes back to 0, one cannot conclusively determine the next state, because it depends on whether the *S* or *R* input goes to 0 first
- This indeterminate condition makes this circuit difficult to manage, and it is seldom used in practice
- Nevertheless, the *SR* latch is an important circuit because flip-flops are constructed from it



En	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

D Latch

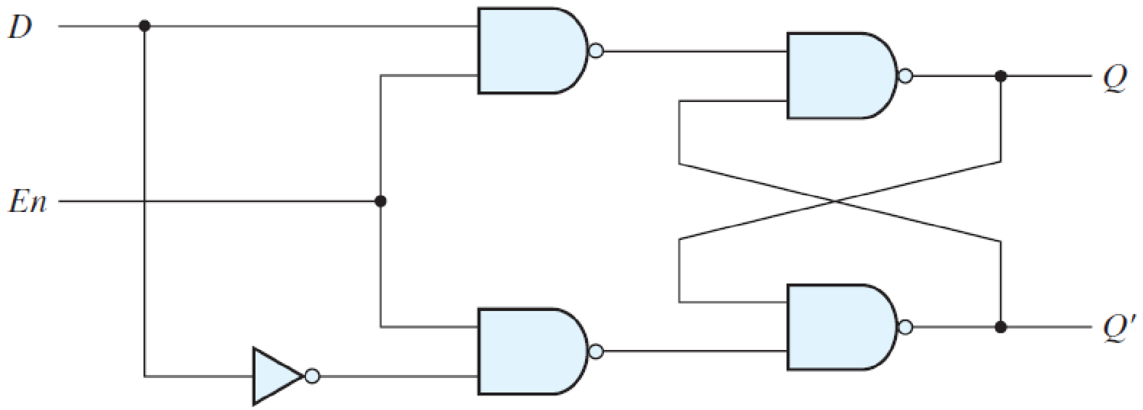
- One way to eliminate the undesirable condition of the indeterminate state in the *SR* latch is to ensure that inputs *S* and *R* are never equal to 1 at the same time
- This is done in the *D* latch
- The *D* input goes directly to the *S* input, and its complement is applied to the *R* input
- As long as the enable input is at 0, the cross-coupled *SR* latch has both inputs at the 1 level and the circuit cannot change state regardless of the value of *D*
- The *D* input is sampled when *En* = 1. If *D* = 1, the *Q* output goes to 1, placing the circuit in the set state
- If *D* = 0, output *Q* goes to 0, placing the circuit in the reset state



En	*D*	Next state of *Q*
0	X	No change
1	0	*Q* = 0; reset state
1	1	*Q* = 1; set state

D Latch

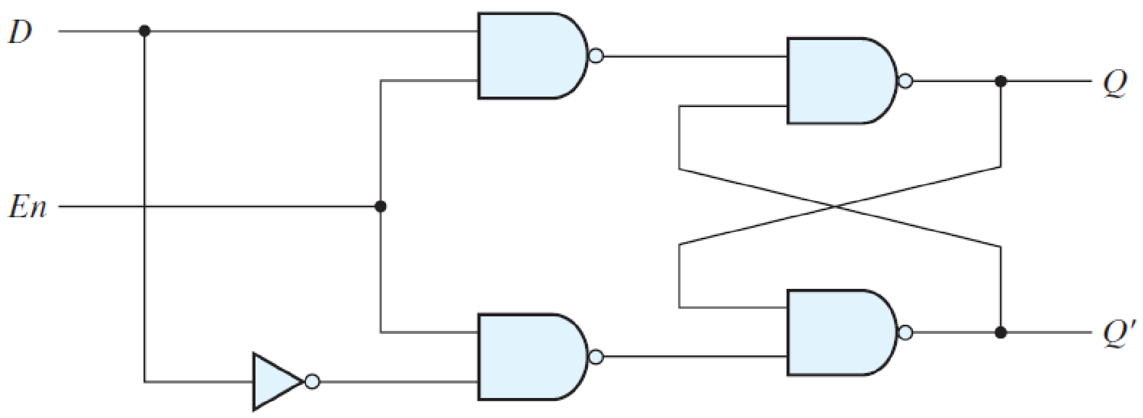
- The *D* latch receives that designation from its ability to hold *data* in its internal storage
- It is suited for use as a temporary storage for binary information between a unit and its environment
- The binary information present at the data input of the *D* latch is transferred to the *Q* output when the enable input is asserted
- The output follows changes in the data input as long as the enable input is asserted
- This situation provides a path from input *D* to the output, and for this reason, the circuit is often called a *transparent* latch



En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

D Latch

- When the enable input signal is de-asserted, the binary information that was present at the data input at the time the transition occurred is retained (i.e., stored) at the *Q* output until the enable input is asserted again
- Note that an inverter could be placed at the enable input
- Then, depending on the physical circuit, the external enabling signal will be a value of 0 (active low) or 1 (active high)



En	D	Next state of Q
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state