PATRIoT lab

Lecture 17 – Sequential circuits 3

Dr. Aftab M. Hussain,

Assistant Professor, PATRIoT Lab, CVEST

Chapter 5

Problem with latches

- A sequential circuit has a feedback path from the outputs of the flip-flops to the input of the combinational circuit
- Consequently, the inputs of the latches are derived in part from the outputs of the same and other latches
- The state transitions of the latches start as soon as the enable/data pulse changes to the logic-1 level
- The new state of a latch appears at the output while the pulse is still active
- This output is connected to the inputs of the latches through the combinational circuit
- If the inputs applied to the latches change again while the enable pulse is still at the logic-1 level, the latches will respond to new values and a new output state may occur
- The result is an unpredictable situation, since the state of the latches may keep changing for as long as the enable pulse stays at the active level
- Because of this unreliable operation, the output of a latch cannot be applied directly or through combinational logic to the input of the same or another latch when all the latches are triggered by a enable signal
- <Cue: Hero's entry…>

Flip flops

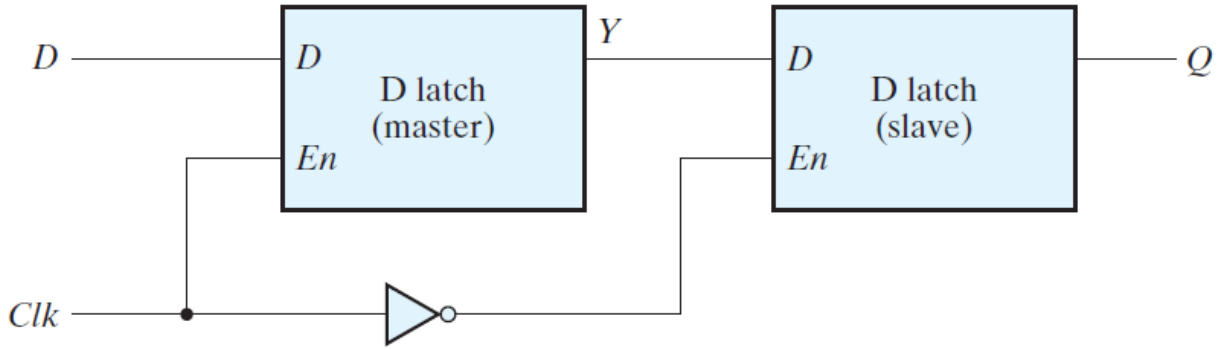
- Enter: the Flip flop!

Flip flops

- Flip-flops are constructed in such a way as to make them operate properly when they are part of a sequential circuit that employs a common clock
- The problem with the latch is that it responds to a change in the *level* of a clock pulse
- A positive level response in the enable input allows changes in the output when the *D* input changes while the clock pulse stays at logic 1
- The key to the proper operation of a flip-flop is to trigger it only during a signal *transition*
- A clock pulse goes through two transitions: from 0 to 1 and the return from 1 to 0
- The positive transition (0->1) is defined as the positive edge and the negative transition (1->0) as the negative edge

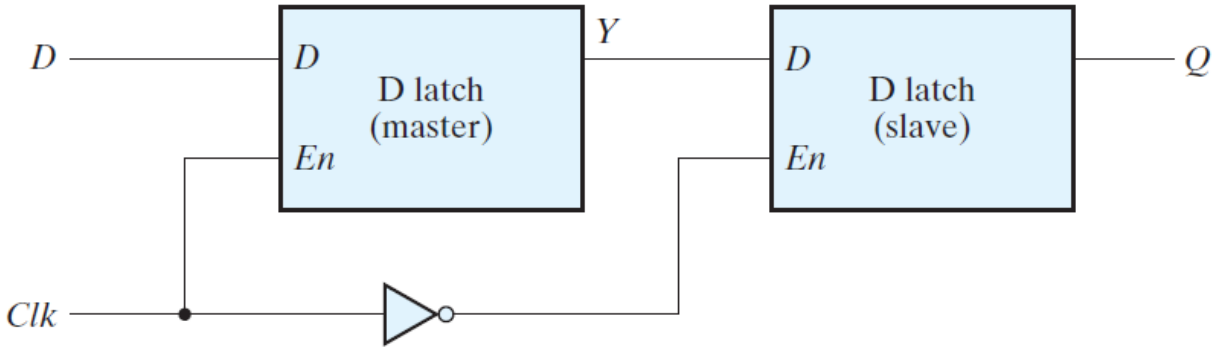
Flip flops

- We can implement flip flops using two latches
- The first latch is called the master and the second the slave
- The circuit samples the *D* input and changes its output *Q* only at the negative edge of the synchronizing or controlling clock (designated as *Clk*)
- When the *Clk = 0*, the slave latch is enabled, and its output *Q* is equal to the master output *Y*
- When the input pulse changes, the data from the external *D* input are transferred to the master

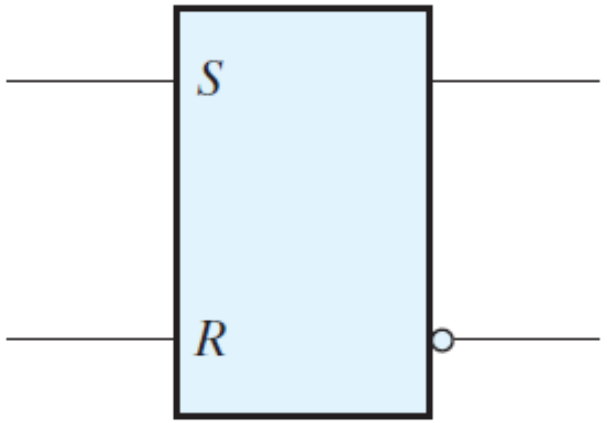


Flip flops

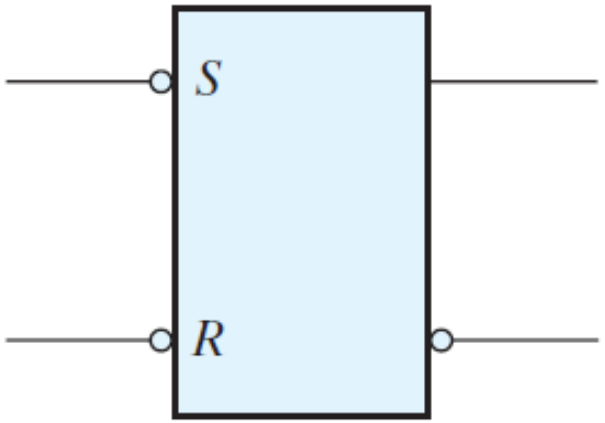
- The slave, however, is disabled as long as the clock remains at the 1 level, because its *enable* input is equal to 0
- Any change in the input changes the master output at *Y*, but cannot affect the slave output
- When the clock pulse returns to 0, the master is disabled and is isolated from the *D* input
- At the same time, the slave is enabled and the value of *Y* is transferred to the output of the flip-flop at *Q*
- Thus, *a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0 (-ve edge)*



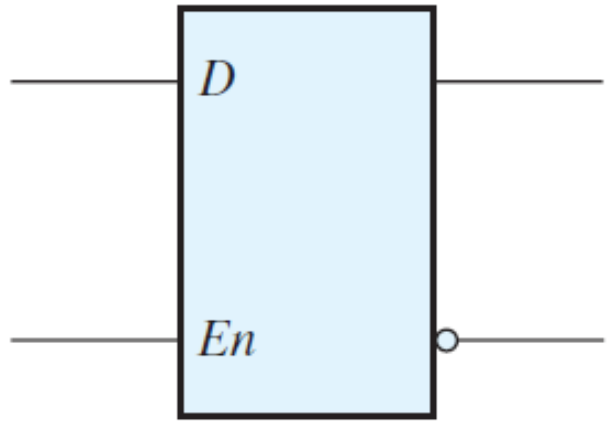
Graphical symbols



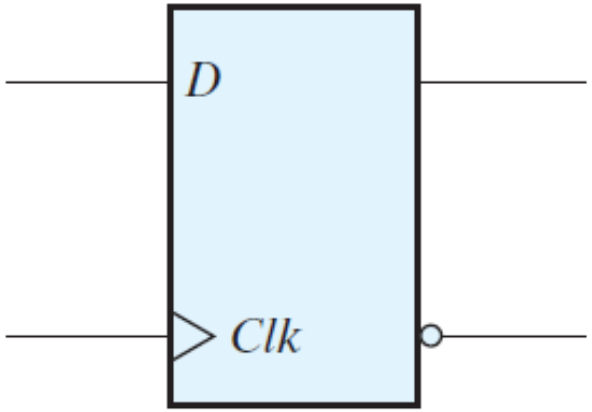
SR



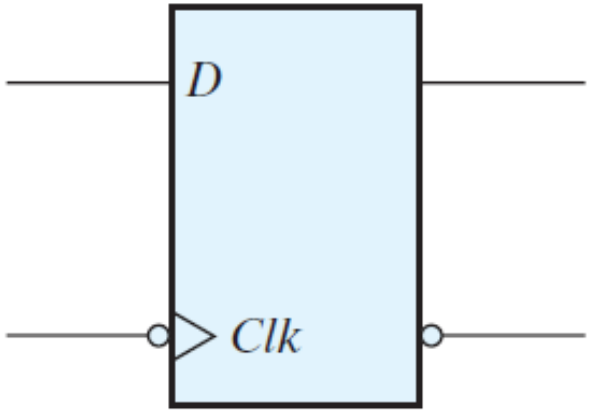
$\overline{S}\overline{R}$



D



(a) Positive-edge



(a) Negative-edge

JK Flip Flop

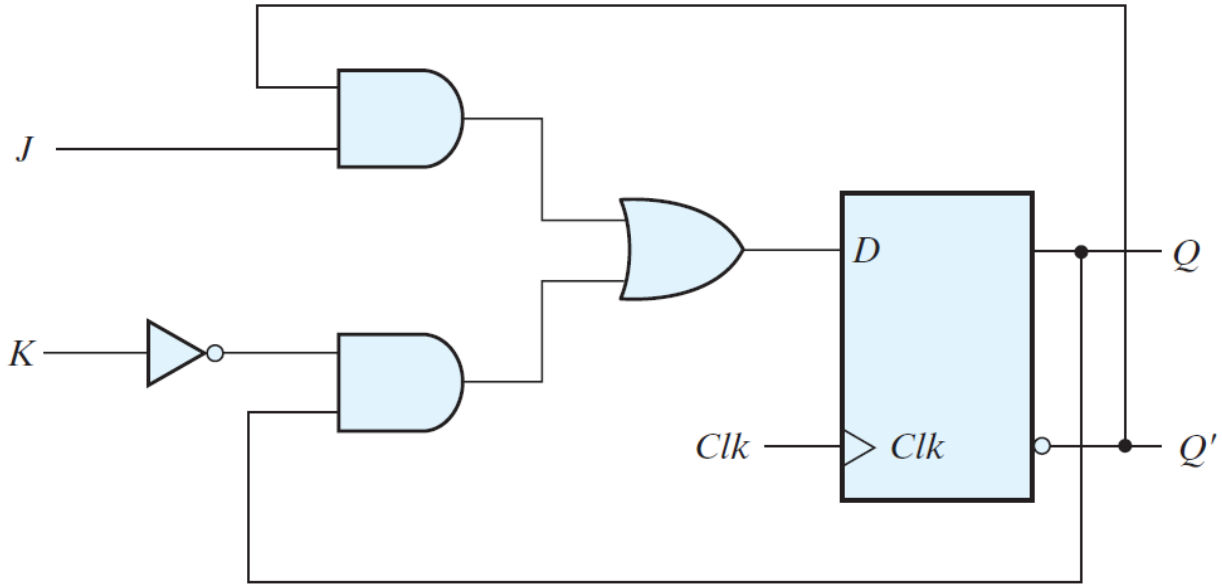
- There are four operations we are looking to perform in a flip-flop: Set it to 1, reset it to 0, retain or complement its output
- With only a single input, the *D* flip-flop can set or reset the output, depending on the value of the *D* input immediately before the clock transition
- Synchronized by a clock signal, the *JK* flip-flop has two inputs and performs all four operations
- The *J* input sets the flip-flop to 1, the *K* input resets it to 0, and when both inputs are enabled, the output is complemented
- This can be obtained if the *D* input is:

$$D = JQ' + KQ$$

JK Flip Flop

$$D = JQ' + K'Q$$

- When $J = 1$ and $K = 0$, $D = Q' + Q = 1$, so the next clock edge sets the output to 1
- When $J = 0$ and $K = 1$, $D = 0$, so the next clock edge resets the output to 0
- When both $J = K = 1$ and $D = Q'$, the next clock edge complements the output
- When both $J = K = 0$ and $D = Q$, the clock edge leaves the output unchanged
- Because of their versatility, JK flip-flops are called *universal flip-flops*



(a) Circuit diagram

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement