논리회로 #3 201302392. 나재성

1. 1) Specification

- Compares number of 1's and 0's of inputs
- Determine where there are more 1's or 0's
- Input : A, B, C
- Output : D=1 if there are more 1's.
  - =0 if there are more 0's.

2) Formulation.

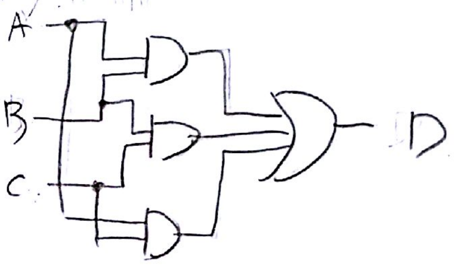
	A	B	C	D
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

A \ BC			B	
	0	1	1 (3)	2
A	4	1 (5)	1 (7)	1 (6)
		C		

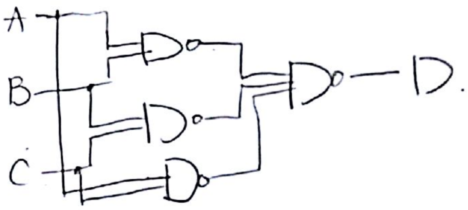
D = AC + AB + BC.

3) Optimization.

D = AC + AB + BC

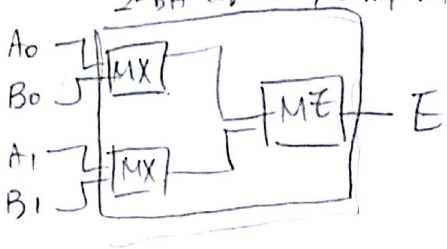


4) Technology mapping

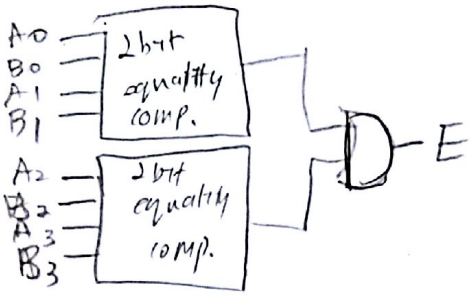


Scanned by CamScanner

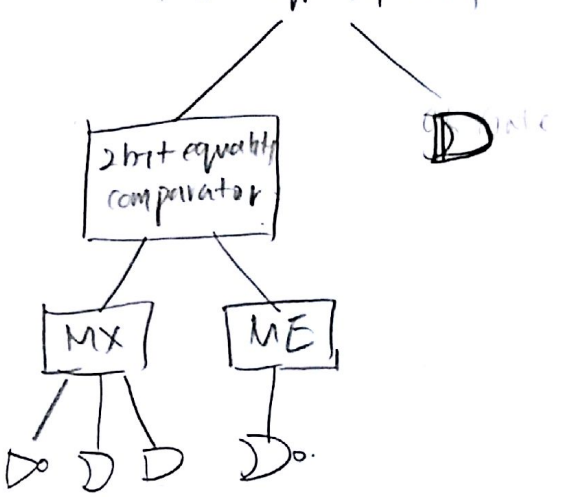
2. a)


2-bit equality comparator
A0
B0
A1
B1
MX
MX
ME
E

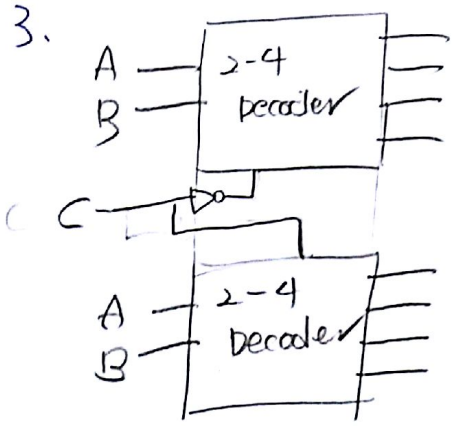
b)


A0
B0
A1
B1
2bit equality comp.
A2
B2
A3
B3
2bit equality comp.
E

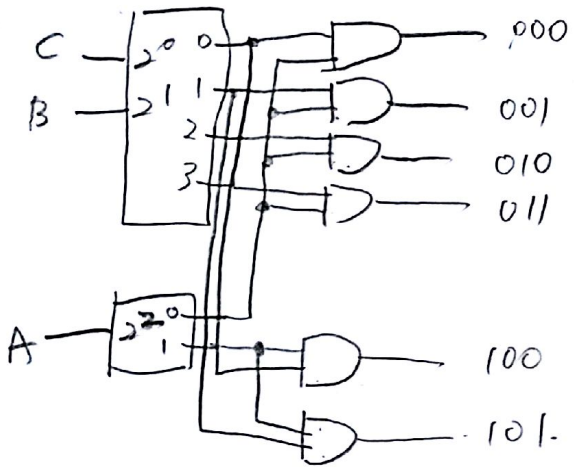
c)


4 bit equality comparator.
2bit equality comparator
MX
ME

3.


A
B
2-4 decoder
C
A
B
2-4 decoder

4.


C
B
A
000
001
010
011
100
101

a) $n_1 = 8$

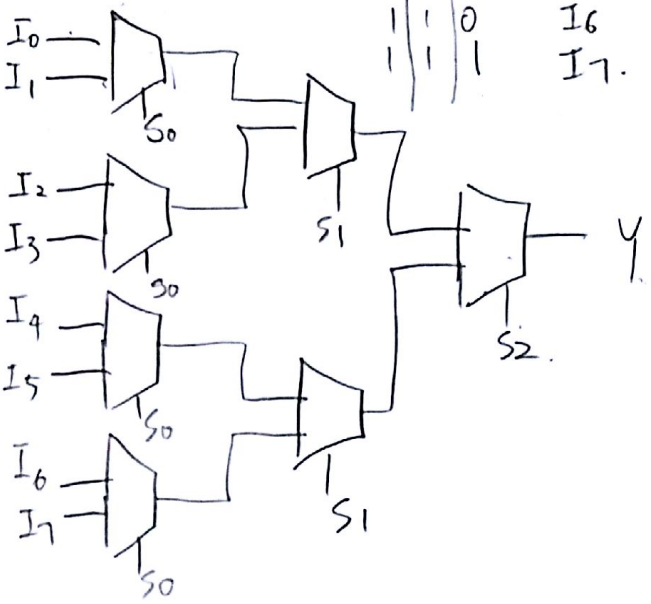
$n_2 = 2$

$8/2 = 4$.

$4/2 = 2$.

$2/2 = 1$.

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

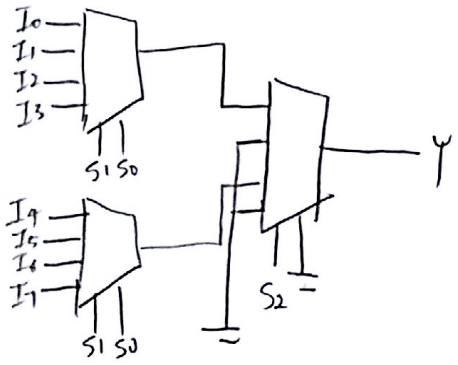


b) $n_1 = 8$

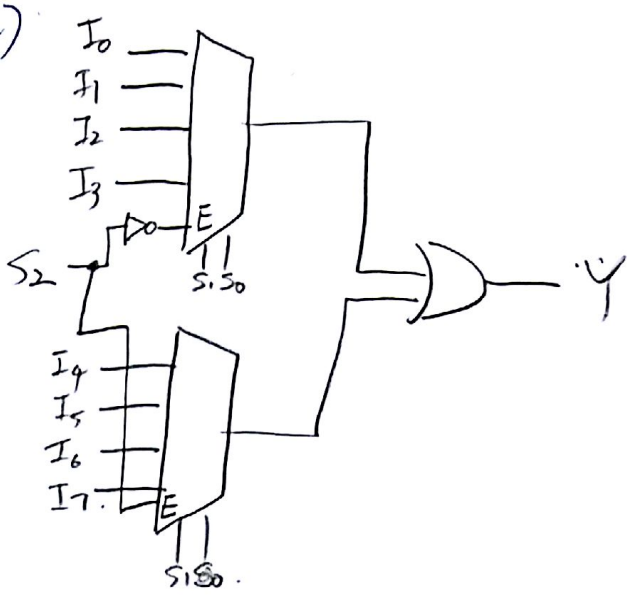
$n_2 = 4$

$8/4 = 2$

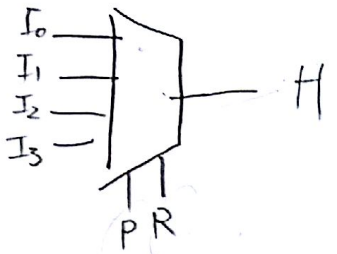
$2/4 = 0.5$



c)



(.a)



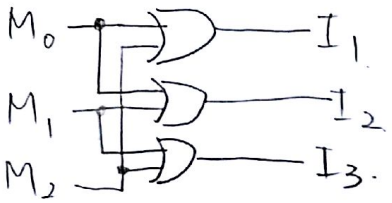
P	R	H
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3.

	M_0	M_1	M_2
I_0	0	0	0
I_1	1	0	0
I_2	0	1	0
I_3	0	0	1

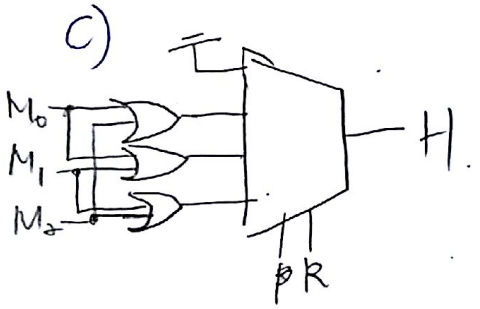
b) $I_1 = M_0 + M_2$

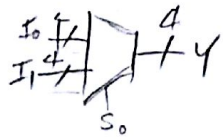
$I_2 = M_0 + M_1$

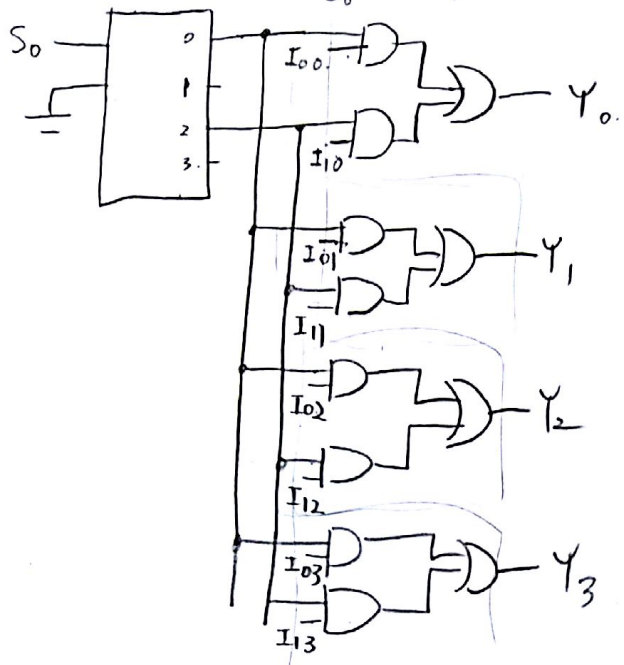
$I_3 = M_1 + M_2$



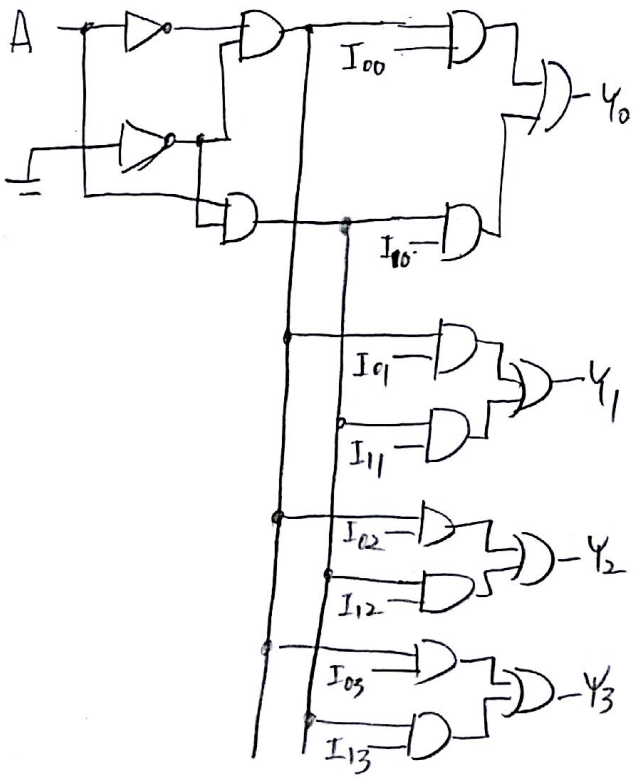
c)







b)



8. a)

	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

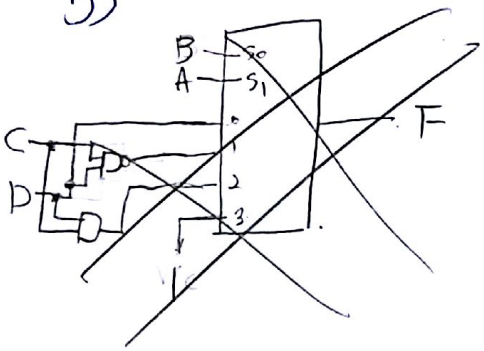
$F = D$

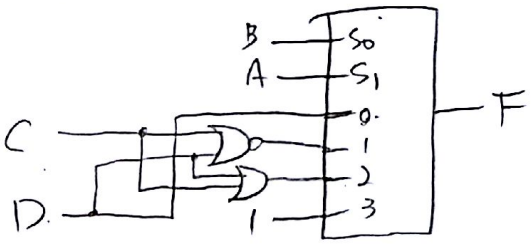
$F = \overline{C+D}$

$F = (C \oplus D)$

$F = 1$

b)



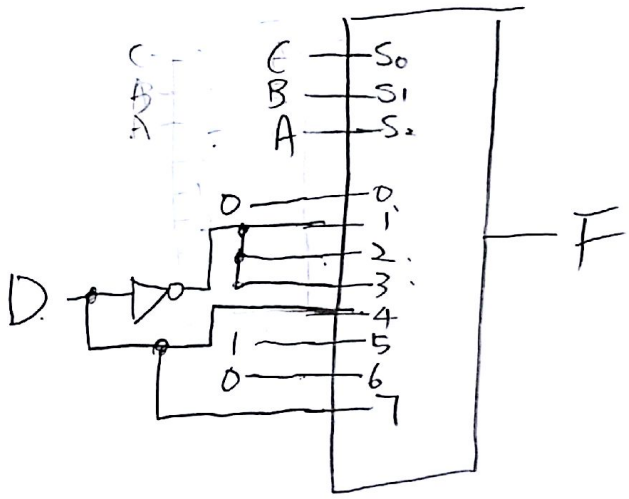


9

AB \ CD	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	0	0	1	0
10	0	1	1	1

S_2 S_1 S_0 = 1 1 1

	S_2	S_1	S_0	F
0	0	0	0	0
1	0	0	1	$\overline{D}$
2	0	1	0	D
3	0	1	1	$\overline{D}$
4	1	0	0	D
5	1	0	1	1
6	1	1	0	0
7	1	1	1	D



a) 4×16 decoder.

b)