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PES University, Bangalore
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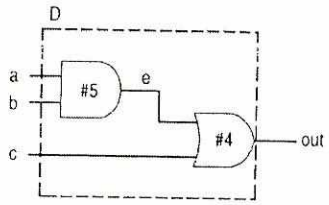
UE15EC353

END SEMESTER ASSESSMENT (ESA) B.TECH. VI SEMESTER- May, 2018
UE15EC353-DIGITAL SYSTEM DESIGN USING HDL

Time: 3 hrs. Max. Marks: 100

1.	a)	Explain the four levels of abstraction at which the internals of a Verilog Module can be defined.	4
	b)	Write the structural model in Verilog for negative-edge triggered 4-bit binary asynchronous up counter using D flip flop module and a not gate.	10
	c)	Explain two types of Variable vector part select operators in Verilog HDL with example declarations and usage. With this feature, show using a loop, selection of an 8-bit vector at a time from a vector of 256 bits.	6
2.	a)	What will be the output of the following primitive gates in Verilog, if the two inputs (i1,i2) take values (0,x), (1,x), (0,z), (z,1) ? (i) nand (ii) nor and (iii) xnor .	6
	b)	Using primitive buffers available, write a Verilog code to synthesize a 4 to 1 multiplexer.	4

	c)	Write a Verilog design module to synthesize the circuit shown in fig.Q2(c). Draw the waveforms for a,b,c,e and out when the following stimulus is applied to the design module.
		module stimulus;
		reg A, B, C;
		wire OUT;
		D d1(OUT, A, B, C); //design module instantiation
		initial
		begin
		A= 1'b0; B= 1'b0; C= 1'b0;
		#10 A= 1'b1; B= 1'b1; C= 1'b1;
		#10 A= 1'b1; B= 1'b0; C= 1'b0;
		#20 $finish;
		end
		endmodule
		 
		
		Fig. Q2(c)
			5

	d)	Write a Verilog code to synthesize 8 to 3 line priority encoder using continuous assignment statement.	5
3.	a)	What is the value to which the following expressions in Verilog are evaluated? Given reg [0:5]b; integer t; integer p, q, r ; p = 0; q = -13; (i) 15 % -4 (ii) 43 < 8'hxFF (iii) 'b10x1 + 'b01111 (iv) if b = -4'd12; what is the value in binary? (v) if t = -2 + (-4) what is the value in binary? (vi) r = p + (q >>> 4)	6
	b)	Write a Verilog model at data flow level of abstraction to synthesize D flip-flop shown in fig. Q3(b).	5

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		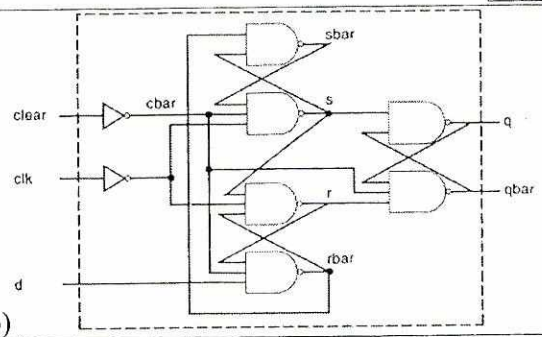 Fig.Q3(b)	
	c)	Explain with example the difference between static and automatic tasks. Write a Verilog code to calculate factorial of a number using function.	9

4.	a)	From the code given below write the values of each register along with simulation time unit at which each statement is executed.
		module analysis(); reg x,y,a,b,p,m;
		initial begin
		x = 1'b0;
		#5 y = 1'b1;
		fork
		#20 a = x;
		#15 b = y;
		join
		#40 x = 1'b1;
		fork
		#10 p = x;
		begin
		#10 a = y;
		#30 b = x;
		end
		#5 m = y;
		join
		#5 $finish;
		end endmodule
			5

	b)	Using generate statement write a Verilog module to synthesize 4-bit comparator using 1-bit comparator module. The comparison has to be carried out from msb to lsb.	10
	c)	What are the three types of delay models used in Verilog that helps for timing simulation of the hardware? Give example of **specify** block for a D flip flop for which the Clock to q delay and d to q delay values are not hardcoded.	5
5	a)	Write the number of variables and functions that can be realized in different modes of the combinatorial functional block of XC3000 CLB? With the help of neat diagram show the realization of Adder/Subtractor with accumulator using XC3000 CLB.	10
	b)	Define an UDP for negative-edge triggered D flip-flop with active high clear input.	6

	c)	What the following codes snippets synthesize to? (no need of circuit diagram)
		(i) always @ (clk or d)
		if (clk)
		q <= d;
		(ii) always @ (ctrl or a or b)
		if(ctrl)
		out = a;
		else out = b;
		(iii) always @ (positive clk)
		if(rst)
		q <= 1'b0;
		else q <= d;
			4