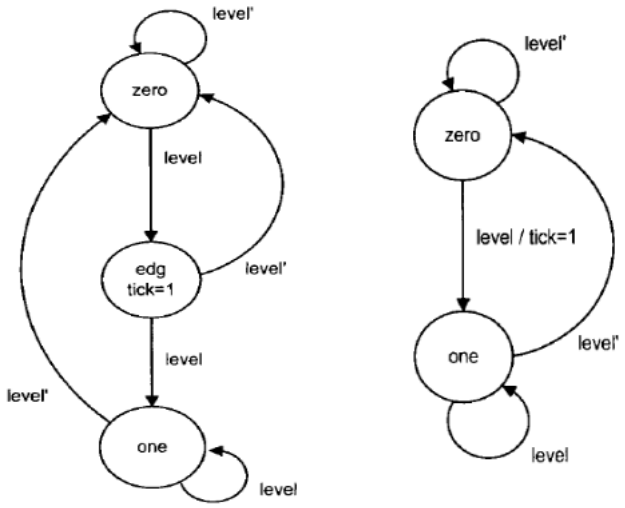
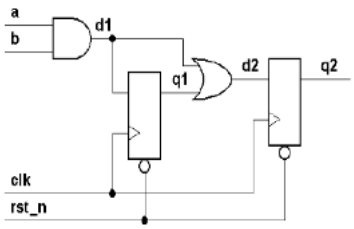
UNIT - 1

Q1) Write a Verilog code for both the types of Moore and Mealy machines (8M)



Q2) Write HDL code for the given circuit in 2 segment style (10M)



Q3) List out the differences between Asynchronous Reset and Synchronous Reset (7M)

UNIT -2

Q1) With a neat labelled diagram explain about Eye Diagram (9M)

Q2) What are the methods to avoid metastability and with a neat diagram explain about metastability test circuitry (8M)

Q3)

Let's take a practical example of performance increase due to the increase in pipeline stages.

Numbers of pipeline stages were increased from 10 in Pentium III to 20 in Pentium IV resulting in a 20% reduction in instructions per cycle (IPC). Assuming a constant 2% timing overhead as a fraction of the total non-pipelined delay, performance increase is calculated as

(8M)

UNIT – 3

Q1) Explain all the three stages of Equivalence Checking (9M)

Q2) Explain the following: (10M)

1) Different Stages of Linting
2) Global Routing and Special Routing
3) Area capacitance and Fringing capacitance with diagrams
4) Different PVT Conditions with diagrams
5) Electrical and Logical Effort

Q3) Explain the following: (6M)

1) What are the basic standard cells present in a Standard cell library
2) Power Planning
3) What are the constraints for Synthesis

UNIT – 4

Q1) Explain the following (9M)

1) Why is Multi Cycle Path propagation necessary
2) MPC Formulation with feedback (with neat diagram)
3) Two Flip Flop Synchroniser with neat diagram

Q2)

- **Case – 1 : $f_A > f_B$** with no idle cycles in both write and read.
- **Transmitter frequency** f_A = 80MHz.
- **Receiver Frequency** f_B = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.

Case – 3 : $f_A > f_B$ with idle cycles in both write and read.

- Writing frequency = f_A = 80MHz.
- Reading Frequency = f_B = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- No. of idle cycles between two successive writes is = 1.
- No. of idle cycles between two successive reads is = 3.

(10M)

Q3) Find the minimum delay (6M)