5th Semester Course Information

UE22EC342AB1 – DIGITAL SYSTEM DESIGN (4-0-0-4-4)

RR: Dr. K Sudeendra Kumar
EC: NA **56 (Teaching) +10 (A/H/P) Hours**

Unit No.	Slot No.	Unit Title	No. of lecture hours/slots	A/H/P slots/hr	DD in-charge
1	1-15	RTL Coding using Verilog HDL	11/15	1/1	Dr. KSK
2	16-35	Clocks and Resets	15/20	2/1.5	Dr. KSK
3	36-55	ASIC Design flow	15/20	4//3	Dr. KSK
4	56-75	STA and Synchronizer Design	15/20	3/2.5	Dr. KSK

Class No.	Chapter Title / Referenvce Literature	Topics to be covered	% of Portions covered	
			Reference chapter	Cumulative
UNIT 1: RTL CODING USING VERILOG HDL				
1	Text 1: Section 1.1- 1.7, pages 01-14	Review of Verilog HDL	1	1
2	Text 1: Section 3.1-3.8, pages 39-65	RT Level Combinational Circuit	2	3
3	Text 1: Section 4.1-4.5,pages83-110	Regular Sequential Circuit	2	5
4	Text 1: Section 5.3 -5.3, pages 125-133	Verilog RTL Coding styles for FSM	2	7
5	Text 1: Section 5.3 -5.3, pages 125-133	FSM -Moore and Mealy	2	9
6	Text 1: Section 4.5.3, pages 110-110	Circular FIFO, Concept of FSM + D	2	11
7	Text 1: Section 5.3.2, pages 130-130	FSMD Example: Debouncing circuit	2	13
8	Slides, Tool manual and Lecture notes provided by Instructor (Cadence EDA tool manual)	Code Coverage	2	14
9	Slides, Tool manual and Lecture notes provided by Instructor (Sunburst Paper)	Verilog: Comparisons and Recap	2	16

Class No.	Chapter Title / Reference Literature	Topics to be covered	% of Portions covered	
			Reference chapter	Cumulative
11	Text 2: Section 9.1-9.2, pages 394-400	Skew and jitter analysis	1	19
12	Text 2: Section 9.1-9.2, pages 394-400	Skew and jitter analysis	2	21
13	Text 2: Section 9.5.1-9.5.3, pages 394-400	Eye Diagram Analysis	2	23
14	Text 2: Section 9.5.1-9.5.3, pages 394-400	Eye Diagram Analysis	1	24
15	Text 2: Section 9.4-9.4, pages 401-409	Encoding Techniques and its applications	1	25
UNIT 2: CLOCKS AND RESETS				
16	Text 2: Section 9.3-9.4, pages 401-409	Timing issues in Flip-flop	2	27
17	Text 2: Section 9.3-9.4, pages 401-409	Maximum Operating frequency of Sequential circuits	1	28
18	Text 3: Section 2.1 – 2.4, pages 11-26	Clock Generation Techniques	1	29
19	Text 2: Section 9.6 - 9.6.7 18.6, pages 428-447	Closed loop timing and PLL	1	30
20	Text 2: Section 9.6 - 9.6.7 18.6, pages 428-447	PLL Operation.	1	31
21	Text 2: Section 9.6 - 9.6.7 18.6, pages 428-447	DLL operation	1	32
22	Text 2: Section 9.6 - 9.6.7 18.6, pages 428-447	Difference between PLL and DLL	1	33
23	Text 2: Section 9.6 - 9.6.7 18.6, pages 428-447	Metastability and Resets -1	1	34
24	Text 2: Section 9.6 - 9.6.7 18.6, pages 428-447	Metastability and Resets -2	1	35
25	Text 3: Section 1.2 -1.8 pages 1 -10	Metastability and Resets -3	1	36
26	Text 3: Section 1.2 -1.8 pages 1 -10	Metastability and Resets -4	1	37
27	Text 3: Section 6.1 - 6.8, pages 129 -145	Introduction to Pipelining	1	38
28	Text 3: Section 6.1 - 6.8, pages 129 -145	Pipelining -2	1	39
29	Text 3: Section 6.1 - 6.8, pages 129 -145	Pipelining -3 (Processor)	1	40
30	Text 3: Section 6.1 - 6.8, pages 146-150 (including Verilog code)	Pipelined Adder	1	41
31	Text 3: Section 6.1 - 6.8, pages 146-150 (including Verilog code)	Pipelined Adder	1	42
32	Text 3: Section 6.1 - 6.8, pages 129 -145	Timing Analysis of Pipelined Circuits	1	43

Class No.	Chapter Title / Reference Literature	Topics to be covered	% of Portions covered	
			Reference chapter	Cumulative
33	Text 3: Section 6.1 - 6.8, pages 148 -152	Pipelined Multiplier	1	44
34	Text 3: Section 6.1 - 6.8, pages 148 -152	Fan-out of 4	1	45
35	Text 3: Section 6.1 - 6.8, pages 148 -152	Standard Cell library design	2	47
36	Text 3: Section 6.1 - 6.8, pages 148 -152	Standard Cell library design	1	48
UNIT 3: ASIC DESIGN FLOW				
37	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Introduction to ASIC Design flow: Full custom design and Semi-custom design	1	51
38	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Introduction to ASIC Design flow: Full custom design and Semi-custom design	1	52
39	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Synthesis	1	53
40	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Gate level simulation	1	56
41	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Synthesis for constraints and Gate level simulation	1	57
42	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Equivalence Checking -1	1	58
43	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Equivalence Checking -2	1	59
44	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Equivalence Checking -3	1	60
45	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Equivalence Checking -4	1	61
46	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Semi-custom Layout -1 (Introduction)	1	62
47	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Semi-custom Layout -2 (Floor planning)	1	63
48	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Semi-custom Layout -3 (Placement)	1	64

Class No.	Chapter Title / Reference Literature	Topics to be covered	% of Portions covered	
			Reference chapter	Cumulative
49	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Semi-custom Layout -4 (Placement)	1	65
50	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Semi-custom Layout -5 (Routing)	1	66
51	Slides, Tool manual and Lecture notes provided by Instructor (Cadence EDA tool manual)	Semi-custom Layout -5 (Routing)	2	67
52	Slides, Tool manual and Lecture notes provided by Instructor (Cadence EDA tool manual)	Importance of Parasitic extraction	2	69
53	Slides, Tool manual and Lecture notes provided by Instructor (Cadence EDA tool manual)	Power Analysis -1	2	71
54	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Power Analysis - 2	2	73
55	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Power Analysis - 3	2	75
UNIT 4: STATIC TIMING ANALYSIS AND SYNCHRONIZER DESIGN				
56	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Static Timing Analysis	1	76
57	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Importance and Limitations of STA	1	77
58	Text 1: Page No. 15 to 39	Timing Arcs, Un-ateness, Max and Min timing paths, Timing Models: Combinational cells	1	78
59	Text 1: Page No. 43 to 99	Timing Models: Sequential cells	1	79
60	Text 1: Page No. 43 to 99	Setup and Hold measurements	1	80
61	Text 1: Page No. 43 to 99	Setup and Hold measurements	1	81
62	Text 1: Page No. 43 to 99	Characterization and Operating conditions	1	82
63	Text 1: Page No. 101 to 123	RLC for Interconnect, Wire-load Models	1	83

Class No.	Chapter Title / Reference Literature	Topics to be covered	% of Portions covered	
			Reference chapter	Cumulative
64	Text 1: Page No. 101 to 123	Representation of Extracted Parasitics, coupling capacitances and reducing parasitics for critical nets	1	84
65	Text 1: Page No. 147 to 176	Overview of Crosstalk	1	85
66	Text 1: Page No. 147 to 176	Crosstalk Glitch Analysis	1	86
67	Text 1: Page No. 147 to 176	Crosstalk Glitch Analysis cont'd	1	87
68	Text 2: Section 10.1 to 10.2, 463-473	Introduction to Synchronization fundamentals -2	1	88
69	Text 2: Section 10.3.1 to 10.3.1, 475-480	Delay line Synchronizer design and Two Flip-flop sync	1	89
70	Text 2: Section 10.3.2 to 10.3.3, 463-473	FIFO Synchronizer	1	90
71	Text 2: Section 10.3.2 to 10.3.3, 463-473	Plesiochronous Synchronizers	1	91
72	Slides and Lecture notes provided by Instructor (Sunburst Reference Paper)	Multicycle Path (MCP) for Clock Domain Crossing	1	93
73	Text 2: Section 10.3.3 to 10.3.4, 483-485	Dual Clock Asynchronous FIFO	1	95
74	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Reset Domain Crossing -1	1	98
75	Slides, Tool manual and Lecture notes provided by Instructor (Ref: - Cadence EDA Tool manual)	Reset Domain Crossing-2	1	100

A/H/P Slot. No	Title of the experiment
1	Simulation: Full adder, Sign adder and two segment coding of D-FF and Counter using Cadence NcSim. Demonstration of FIFO, Mealy and Moore FSM. Simulation of Debouncing Circuit and Code Coverage
2	Demonstration of Synthesis with and without constraints
3	Demonstration of Gate level simulation and functional coverage
4	Demonstration of linting
5	Demonstration of Equivalence Checking
6	Simulation of CDC solution
7	Experiment on Power Analysis
8	Experiment on Timing Analysis
9	Demonstration of Semi-custom Layout
10	Demonstration of Pipelining

Book Type	Author & Title	Edition	Publisher	Year
Text book 1	Pong P Chu, "*FPGA Prototyping by Verilog Examples: Xilinx Sparta-3 Version",*	First	Wiley Blackwell	2008
Text book 2	William J Dally, John W Poulton, "*Digital Systems Engineering*", Cambridge University Press	First	Cambridge University Press	2010 reprint
Text book 3	MohitArora, "*The Art of Hardware Architecture: Design Methods and Techniques for Digital Circuits.*	First	Springer	2012

A note onA/H/P:

- A/H/P mainly focus on simulation of important digital design blocks like clock management, synchronizers, etc.
- Hardware implementation will focus on HDL Simulation tools(both proprietary and Open source).
- Tool licenses and access will be given to students to their residence.

Assignments:

Questions on Digital System design, Timing Analysis, Clock, Reset, Pipelining and Clock Domain Crossing and ASIC Design flow.

Skills imparted by the course (NEP component):

Design,Problem solving skills and simulation skillswhich are applied to digital designs and building blocks for SoC design.

Assessment (100 Marks):

ESA (pen-paper mode) – 100 marks; **Weightage:** ISA (50) + ESA (50); **Grading:** As per university policy

Assessment		Marks	Method adopted for Assessment
ISA	**CBT**	30	CBT for each unit (best 4 out of 5 are taken to calculate final marks)
	Project	10	Project demonstration
	Conduction of Hands-on Experiment	10	Batch of 5 students will be created (13 batches in each section). In last 15 min of AHP Slot, students will be demonstrating the experiment. Batch is randomly picked for assessment.
	ISA Total	50	

Mapping of PSOs and COs

	PSO1	PSO2	PSO3	PSO4	PSO5	PSO6	PSO7	PSO8	PSO9	PSO10
CO1	2	2								1
CO2		2								2
CO3	3	3								2
CO4	2	2								
CO5		3								

Mapping of POs and COs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2			2								2
CO2	2			3								2
CO3	2			3								2
CO4				2								1
CO5				3								1

Digital Deliverables Status

Part 1: Introduction, Objectives, Outcomes, Outline, Syllabus & References – Available

Part 2: Digital Deliverables

	Attributes								
Unit	**AV**	**Live**	**Slides**	**Notes**	**Assignments**	**Qn.**	**QA**	**MCQ**	**References**

#	Summary	Videos				Bank			
1	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done
2	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done
3	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done
4	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done	To be done