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PES University, Bengaluru (Established under Karnataka Act No. 16 of 2013)

UE14EE316

END SEMESTER ASSESSMENT B.Tech 5th Semester

UE14EE316 - Digital System Design Using VHDL

Time: 3 Hrs		Hrs Answer All Questions Max Marks: 100	Marks: 100	
2.	a)	With an example briefly explain the differences between std_logic_vector and bit_vector types in VHDL.	5M	
	b)	Write the structural VHDL program to instantiate the 2-input NOR gate component twice in a design with the following specifications using generics. (i) rise_time = 5ns, fall_time = 2ns (ii) rise_time = 10ns, fall_time = 4ns	5M	
	c)	Write the Structural VHDL Program for the following: (i) Half-Adder using EX-OR and AND gate as components.	10M	
		(ii) 2:4 Decoder using basic gates as components.		
2.	a)	With an example briefly explain signal assignment and variable assignment statements in VHDL.	5M	
	b)	Write a behavioral description of D Flip-Flop which changes state on the rising edge of clock input and also consider the propagation delay of Flip-Flop is 10ns.	5M	
	c)	Write a behavioral description in VHDL for the following; (i) 4:2 priority Encoder using if-else condition statements. (ii) To count number of ones in a given 8-bit data using 'FOR' loop statement.	10M	
3.	a)	Write a VHDL snippet to add two bit_vectors of data using a procedure.	5M	
	b)	With a neat block diagram, explain the operation of serial adder with accumulator.	5M	
	c)	For the given state graph of binary multiplier control, write the behavioral model for 4 X 4 unsigned binary multiplier.	10 M	

