Question Paper

SEP 2024 - UE22EC352A - ISA 1 (set- 1)

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1.a : Marks (4.0)

Translate the following C code to RISC-V. Assume that the variables i and j are assigned to registers x28, and x29, respectively. Assume that the base address of the arrays A and B are in registers x10 and x11, respectively. Assume that the elements of the arrays A and B are 4-byte words:

B[8] = A[i] + A[j];

Expected Answer

```
SLLI  x28, x28,2
ADD  x10, x10, x28
SLLI  x29, x29,2                    2M
ADD  x11, x10, x29
LW   X1, 0(x10)
LW   X2, 0(x11)                     2M
ADD  X3, X1, X2
SW  X3,32(X11)
```

1.b : Marks (4.0)

Write a assembly program to search an element in an array using leaf procedure to check.
Assume the element to be searched is in register X10, base address of array is in X1.

Expected Answer

```
    .data
ary: .word 11,22,33,44,55,66,77,88,99
res1: .string "SEY"
res2: .string "ON"
.text
    la x4,ary
    la x5,res1
    la x6,res2
    li x12,0
    li x5,9
    li x10,88
  back: lw x11,0(x4)
    jal  x1,check
     addi x1,x1,4
    addi x5,x5,-1
    bne  x5,x0,back
   nop

    check: beq x11,x10,found
               lw x12,0(x6)
               jalr  x0,0(x1)
               found:lw x12,0(x5)
               jalr  x0,0(x1)
```

To push x6 and x5 and pop before JALR

1.c : Marks (4.0)

Write control signals issued and their status in each stage in the 5- stage pipeline RISC V processor for the following instruction.

LW X10, 32(X1)

Expected Answer

Execution Stage

ALUOp=00 ALU Control=0010

ALUSrc=1

Memory stage

Branch=0

MemRead=1

MemWrite=0

Write Back stage

MemtoReg=1

RegWrite=1

1.d : Marks (4.0)

write conditions for detecting hazards, and the control signals to resolve in following 2 cases

i) **ADD X10, X1, X2**
ADD X11, X3, X4
ADD X12 , X5, X10

ii) **LW X10, 32(X1)**
XOR X11, X10, X12

Expected Answer

i) MEM Hazard:
if (MEM/WB.RegWrite and (MEM/WB.RegisterRd ? 0)
and not(EX/MEM.RegWrite and (EX/MEM.RegisterRd ? 0) and (EX/MEM.RegisterRd =ID/EX.RegisterRs2))
and (MEM/WB.RegisterRd = ID/EX.RegisterRs2)) **ForwardB = 01**

ii) Load Hazard:
if (ID/EX.MemRead
and ((ID/EX.RegisterRd = IF/ID.RegisterRs1) or
(ID/EX.RegisterRd = IF/ID.RegisterRs2)))
stall the pipeline

5 : Marks (2.0)

Consider the following code:

```
lb x6, 0(x7)
sb x6, 8(x7)
```

Assume that the register x7 contains the address 0×10000000 and the data at the address is 0×ABC0FFEE. What value is stored in 0×10000008 on a big-endian machine?

Expected Answer

6 : Marks (2.0)

After executing following code ,what will be the contents of x1 and where does the execution jumps to?

```
0x 0:   lui   x10, 0x18000
0 x4:   jalr  x1, x10, 0x7f8
```

Expected Answer

7 : Marks (2.0)

Assume that individual stages of the data path have the following latencies:

IF	ID	EX	MEM	WB
200 ps	**90 ps**	**100 ps**	**250 ps**	**120 ps**

What is the clock cycle time in a non-pipelined processor?
And what is the latency of a LW instruction in a pipelined architecture?

Expected Answer

i) 200+90+100+250+120=760ps
ii)Each stage of pipeline =250
250*5=1250 ps

8 : Marks (2.0)

Following are the latencies of logic elements of a processor?s data path .

I-Mem / D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Sign extend	Control
250 ps	150 ps	25 ps	200 ps	150 ps	5 ps	30 ps	20 ps	50 ps	50 ps

?Register read? is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. ?Register setup? is the amount of time a register?s data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

Expected Answer

9 : Marks (1.0)

If X5= -1024 (decimal) then what will be the value in X5 after executing following instruction?

SRAI X5, X5, 4

Expected Answer

10 : Marks (1.0)

If x1=0 x7FA00001 & x2=0x8A000001 ,the following instruction results in

BLT x2, x1, loop

Expected Answer

11 : Marks (1.0)

Let x5=0 xAAAAAAAA & x6=0xFFFF00FF, the following instruction results in

XOR x5, x5, x6

Expected Answer

12 : Marks (1.0)

sltiu X10, X1, 1 If X10 =1 then X1=?

Expected Answer

13 : Marks (1.0)

X10 should be loaded with a 32 bit data 0XABC0FFEE. We use following code.

LUI X10, -------

ADDI X10 ,X10, 0XFEE

What is the immediate data (2nd operand) of LUI instruction?

Expected Answer

14 : Marks (1.0)

An **addi** instruction is encoded as **0 X a2400113**.
What is the result in destination register after its execution?

Expected Answer

0 X a2400113.= 101000100100-00000-000-00010-0010011
addi X2,X0,0Xa24

15 : Marks (1.0)

What is the maximum distance a jump instruction can reach to in RISC-V in number of bytes?

Expected Answer

16 : Marks (1.0)

.data
label: .half 0x8899,0xaabb
on RIPES simulator assembled as

Expected Answer

17 : Marks (1.0)

What is the minimum number of cycles needed to completely execute **n** instructions on a CPU with a **k** stage pipeline?

Expected Answer

18 : Marks (1.0)

Consider the following instruction mix:

R-type	I-type (non-lw)	Load	Store	Bra
24%	28%	25%	10%	11

What fraction of all instructions use the sign extend?

Expected Answer

19 : Marks (1.0)

Which instruction uses all stages of 5 stage RISC V pipeline?

Expected Answer

20 : Marks (1.0)

What are the inputs to ALU control in RISC-V data path?

Expected Answer

21 : Marks (1.0)

All control signals are generated in ------ stage of datapath

Expected Answer

22 : Marks (1.0)

Which type of instructions require to use **RegWrite** control signal ?

Expected Answer

23 : Marks (1.0)

C extension of RISC-V offers ---------

Expected Answer

24 : Marks (1.0)

Whenever stall in the pipeline is introduced , all control signals are made-------

Expected Answer