Question Paper

SEP 2024 - UE22EC342AB1 - ISA 1 (set- 1)

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1.a : Marks (4.0)

Differentiate between Asynchronous reset and synchronous reset

Expected Answer

Asynchronous reset	Synchronous reset
Reset signal is not a part of the data path, that is, not a part of logic for D input of the FF	Reset signal is part of the data path, that is, the D input of the FF
Effect of reset can happen anytime asynchronously	Effect of reset will happen only on the active edge of a clock
Doesn't depend upon the presence of an active clock signal	Depends upon the presence of the clock signal for the reset to happen
Asynchronous event is an overload, compared to synchronous reset in the cycle based simulators	Works well when using cycle based simulators
Not recommended for internally generated resets, due to glitches	For internally generated resets, synchronous approach is the best mechanism
Reset input from external sources can be prone to glitches, the final reset signal needs to be synchronized before applying it to all storage elements	Not prone to glitches from internal or external sources
Asynchronous reset input still needs the double FF synchronization to avoid race condition during de-assertion	The additional synchronization circuitry is not required as it is a part of the default synchronous logic requirement
Needs to meet only the minimum reset pulse width required for the FF	Reset pulse width has to be long enough to be sampled on an active clock edge

1.b : Marks (4.0)

Write a Verilog HDL code for Barrel Shifter.

Expected Answer

```
module barrel_shifter_case
    (
      input wire [7:0] a,
      input wire [2:0] amt,
      output reg [7:0] y
     );

    // body
    always @*
        case(amt)
            3'o0: y = a;
            3'o1: y = {a[0], a[7:1]};
            3'o2: y = {a[1:0], a[7:2]};
            3'o3: y = {a[2:0], a[7:3]};
            3'o4: y = {a[3:0], a[7:4]};
            3'o5: y = {a[4:0], a[7:5]};
            3'o6: y = {a[5:0], a[7:6]};
            default: y = {a[6:0], a[7]};
        endcase

endmodule
```

1.c : Marks (4.0)

Explain the importance of Fan out of 4 (FO4)

Expected Answer

?Digital circuit delays vary with feature size, process corner, operating voltage, and junction temperature. Delays are steadily decreasing with advances in process technology, so comparing results reported in nanoseconds between process generations is difficult. The delay of a fanout-of-4 inverter (FO4) to normalize process and operating condition variations and quantifies how well this normalization works.

?Reporting the FO4 delay of a process along with any circuit performance results

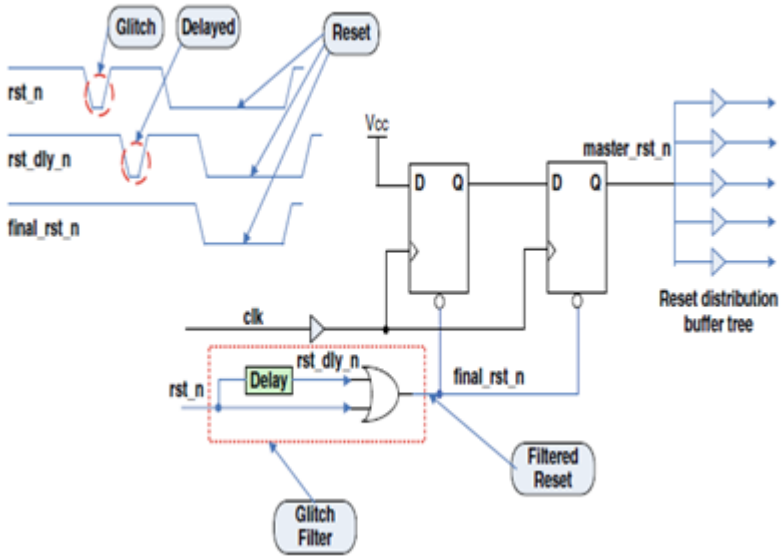
1.d : Marks (4.0)

With neat circuit diagram explain the following: -

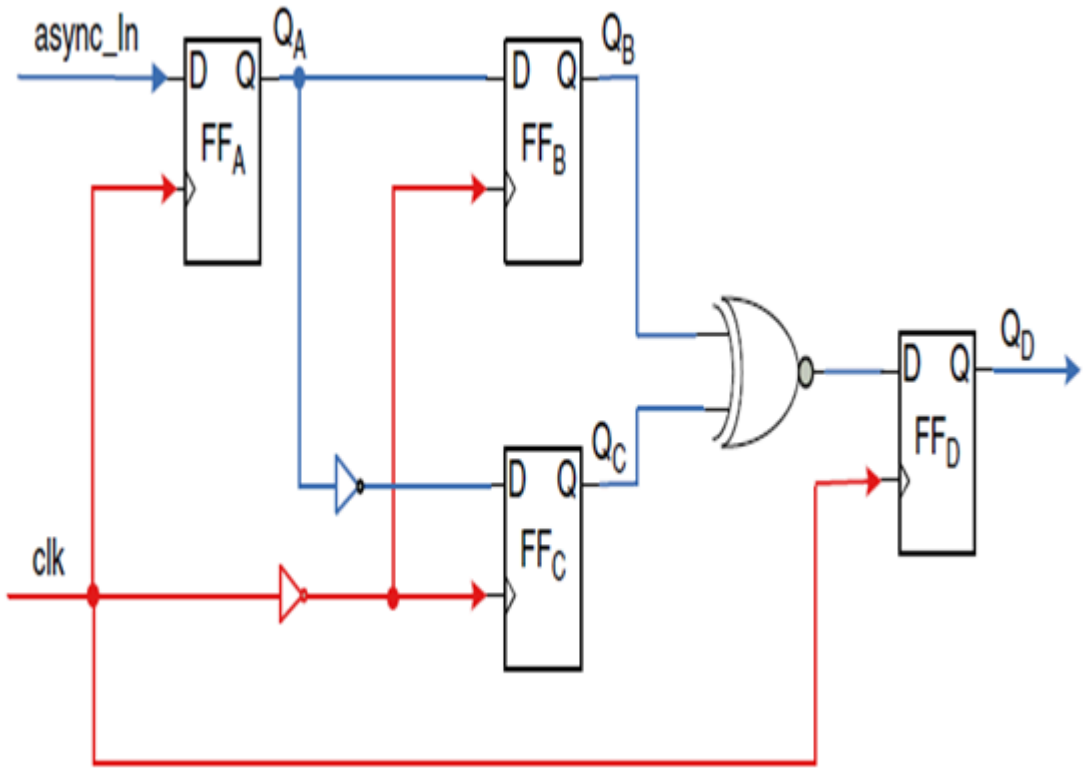
1. filtering glitches in Reset
2. Metastability test circuit

Expected Answer

Reset Glitch Filtering: -



Metastability test circuit:



5 : Marks (2.0)

Clock gating may lead to the partial reset of the circuits in the following design

Expected Answer

Synchronous reset based designs

6 : Marks (2.0)

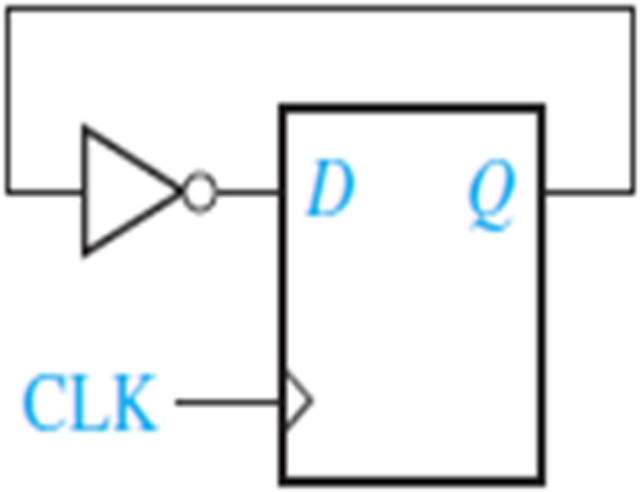
The technqiues to minimize the clock skews are

Expected Answer

- Adding Delay in Data Path
- Clock Reversing.
- Alternate Phase Clocking.
- Balancing Trace Length

7 : Marks (2.0)

Calculate the maximum operating frequency for the following circuit: - THold = 3 ns, Tsetup = 2 ns, TClock-to-Q (Tcq) delay = 1ns, Tinverter (Tinv) = 3ns.



Expected Answer

166.6 MHz

8 : Marks (2.0)

When the values in the item expressions are mutually exclusive (i.e., a value appears in only one item expression), the statement is know as (in Verilog HDL):

Expected Answer

Parallel case statement

9 : Marks (1.0)

Intial block in Verilog HDL is

Expected Answer

a non-synthesizable construct and exectues only once during simulation

10 : Marks (1.0)

"Always" block in Verilog HDL is

Expected Answer

Synthesizable construct and executes every time when there is a change in the sensitivity list.

11 : Marks (1.0)

A coverage measures how well the design code has been excerized by testbench is known as

Expected Answer

Code Coverage

12 : Marks (1.0)

$display statement will be executed in

Expected Answer

Active region of the stratified event queue

13 : Marks (1.0)

$strobe is preferred in the place of $display during simulation because

Expected Answer

$strobe executes in postponed region and get the final value of the signals.

14 : Marks (1.0)

The sources of jitter are

Expected Answer

Power supply variation, Process and Temperature variation

15 : Marks (1.0)

Skew is a

Expected Answer

Spatial Variation on clock

16 : Marks (1.0)

Eye diagram is useful in measuring

Expected Answer

Jitter and strobing point

17 : Marks (1.0)

A pulse strectcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock is required for

Expected Answer

synchronous reset

18 : Marks (1.0)

A time between when reset is de-asserted and the time that the clock signal goes high again is known as

Expected Answer

Recovery Time

19 : Marks (1.0)

T-flipflop can be used as divide by clock/2 circuit by

Expected Answer

Connecting "T" to Clock

20 : Marks (1.0)

Ripple Counters should not be used as clock dividers because

Expected Answer

Cumulative effect with more than two flipflops connnected leads to addition of skew and phase shifts in derived clock

21 : Marks (1.0)

A technique to split the critical timing path with memory element betwen the clock cycles is called

Expected Answer

Pipelining

22 : Marks (1.0)

Short path problem arises when

Expected Answer

the data propagation delay between two adjacent flip-flops is less than the clock skew.

23 : Marks (1.0)

Reset synchronizers are necessary to address the

Expected Answer

Asynchronous Reset Removal Problem

24 : Marks (1.0)

MTBF is calculated as

Expected Answer

is the reciprocal of the failure rate in the special case when the failure rate is constant.