CLOCK GATING – A POWER OPTIMIZING TECHNIQUE FOR VLSI CIRCUITS

A PROJECT REPORT

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Under the Guidance of

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GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY

2024-2025

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ABSTRACT

CLOCK GATING – A POWER OPTIMIZING TECHNIQUE FOR VLSI CIRCUITS

Timepiece gating is an essential fashion in digital design used to reduce dynamic power consumption by widely disabling the timepiece signal to portions of a circuit when they aren't in use. In the environment of FPGA design, specifically within Xilinx Vivado software, timepiece gating plays a critical part in optimizing performance and power effectiveness in complex systems. Vivado provides colorful mechanisms to apply timepiece gating, including automatic timepiece-gating conflation, homemade perpetration using control sense, and the use of technical IP cores for timepiece operation. Timepiece gating works by adding a control signal that enables or disables the timepiece signal to different modules or functional blocks based on specific conditions, such as the module being idle or not actively recycling data. This results in significant reductions in gratuitous switching exertion, thereby lowering dynamic power consumption. Vivado's tools grease the integration of timepiece gating with minimum impact on overall system performance, while also supporting timing checks and maintaining synchronization across the design.

This abstract explores the conception of timepiece gating within Xilinx Vivado, its perpetration ways, and the benefits it offers in terms of power optimization, particularly for battery-powered or performance-sensitive operations. Through proper operation of Vivado’s advanced features, designers can achieve a balance between power savings and design effectiveness, ensuring optimal resource application in FPGA-grounded operation.

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1.1 GENERAL OVERVIEW

Timepiece gating is an extensively used power optimisation fashion in VLSI (veritably Large-Scale Integration) circuits, particularly in the environment of reducing dynamic power consumption. Dynamic power is consumed by circuits during the switching of sense gates, and timepiece gating reduces gratuitous switching by widely disabling the timepiece signal to portions of a circuit when they are not in use.

Key generalities of Clock Gating

1. Timepiece Signal The timepiece signal synchronises the operations of successive rudiments (like flip- duds or registers) in digital circuits. When the timepiece signal is active, these rudiments modernise their state.

2. Timepiece Gating This involves the use of a gating signal (control signal) to disable the timepiece signal to a certain corridor of the circuit. However, its timepiece can be turned off, thereby precluding gratuitous switching and saving power, if a particular module or block is not performing any useful work at a given moment.

3. Types of timepiece Gating

• Homemade timepiece Obstructing Contrivers explicitly fit sense gates (similar to AND gates) to control the timepiece signal based on certain conditions.

• Automatic timepiece Obstructing Tools used in the design inflow automatically fit the timepiece gating sense based on analysis of circuit exertion and operation patterns. Power Savings By turning off the timepiece to idle blocks, the switching exertion in those blocks is reduced, which leads to a reduction in dynamic power consumption. Since dynamic power is commensurate with the switching frequency and capacitance, disabling the timepiece can lead to significant power savings.

Benefits:

- Reduced Dynamic Power The most significant benefit of timepiece gating is the reduction in dynamic power consumption, which is a major contributor to overall power dispersion in VLSI circuits.
- Improved Battery Life For battery- powered bias, similar as mobile phones or wearables, timepiece gating can help extend battery life by reducing the power drawn by inactive corridor of the chip.
- Thermal Management Power reduction leads to lower heat generation, which helps in managing the thermal performance of the chip.

1.2 INTRODUCTION TO CLOCK GATING

Clock gating is a power-saving method utilised in advanced circuits, especially in the design of VLSI (Very Large Scale Integration) frameworks. The essential objective of clock gating is to decrease energetic consumption by specifically disabling the clock signal to portions of the circuit that are not effectively performing any operations. This strategy misuses the reality that successive components, such as flip-flops or registers, devour control when their clock flag is flipping and causing transitions.

In present-day computerised frameworks, where large-scale integration has driven complex circuits, overseeing control utilisation is basic for both execution and effectiveness. Clock gating makes a difference in accomplishing this by minimising pointless exchanging action in inert parts of a circuit, in this way diminishing the general control consumption.

Why is Clock Gating Important?

Static Control: Expended by spillage streams, which are generally constant. **Dynamic Control:** Devoured by the exchanging of rationale entryways, which depends on the clock recurrence, the number of exchanging moves, and the capacitance of the circuits. Clock gating centres on diminishing energetic control, which is the prevailing supporter of control utilisation in high-performance chips. By turning off the clock flag to segments of the circuit that are not in utilize, clock gating decreases superfluous exchanging, subsequently sparing power.

Basic Concept of Clock Gating:

A normal clocked circuit employs a clock flag to synchronise the operation of flip-flops or registers. When the clock flag is tall (or dynamic), the registers upgrade their states, and an exchange action happens. Be that as it may, if certain parts of the circuit are not required to work at a specific minute (such as amid still periods or when holding up for inputs), clock gating permits for turning off the clock flag to those parts, avoiding pointless flipping of the state components and diminishing control usage.

In quintessence, clock gating is an instrument that guarantees the clock as it comes to useful units when they are required and is blocked or gated when they are idle.

How Clock Gating Works?

Clock gating ordinarily includes an extra control flag that chooses whether the clock ought to be passed to a particular portion of the circuit. The control flag, regularly alluded to as a "gating flag," is combined with the clock flag through logic gates (such as AND gates), and based on the state of the gating flag, the clock can be either enabled or disabled.

The clock gating rationale can be embedded physically by the architect or consequently by plan apparatuses, depending on the complexity of the plan.

1.3 Nexys Artix-7 FPGA Board

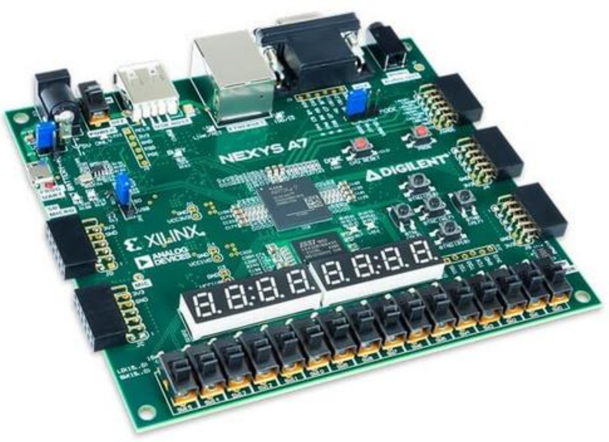


Fig.1: Nexys Artix-7 FPGA kit

The Nexys A7 FPGA development board, erected around the Xilinx Artix 7 FPGA (XC7A100T), is an important and flexible platform designed for digital system design and education. It features 15,850 sense slices, 4.8 Mb of block RAM, multiple timepiece operation penstocks, and a rich set of onboard peripherals including switches, LEDS, 7- 7-member displays, and a VGA affair. Its USB-JTAG programming, integrated power operation, and compatibility with Vivado Design Suite make it an excellent board for rapid-fire prototyping, VHDL/ Verilog, and exploring low-power VLSI ways such as timepiece gating.

The Nexys A7 FPGA development board is a protean and pupil-friendly platform developed by Digilent and powered by the Xilinx Artix 7 FPGA(specifically the XC7A100 T-1CSG324C). Designed to give an affordable yet point-rich terrain for both literacy and prototyping, the board is packed with 15,850 sense slices, 4.8 Mb of block RAM, 240 DSP slices, and timepiece operation penstocks for robust timing control. It supports both academic and professional development requirements, with onboard peripherals like 16 slide switches, 16 LEDS, five drive buttons, an OLED display, a Pmod interface for I/ O expansion, and a VGA interface for display operations. USB- JTAG circuitry simplifies programming and debugging, while onboard power regulation supports USB or external power sources for flexibility. The Nexys A7 is completely supported by Xilinx Vivado Design Suite, which enables high-level synthesis, simulation, and power analysis tools. Its reconfigurable nature makes it an ideal choice for exploring advanced digital design generalities, such as timepiece gating, power-apprehensive system design, pipelining, and real-time signal processing. Because of its balance between affordability and performance, the Nexys A7 serves as a foundation for VLSI education, low-power exploration, and embedded system design.

1.4 Need for Power Efficiency in Digital Design

Power efficiency in digital design is essential not only for meeting the demands of modern electronic systems but also for addressing broader issues such as environmental sustainability, cost reduction, and thermal management. As the complexity of devices continues to grow, the need for efficient power consumption strategies like clock gating, voltage scaling, and low-power design techniques becomes increasingly important to meet the performance, size, and battery life expectations of today’s consumers and industries. Power-efficient designs help maintain operational longevity, minimise heat dissipation, and contribute to the overall success of electronic products in an energy-conscious world.

1. Increasing Demand for Portable and Battery-Powered Devices

Battery Life: Mobile devices, such as smartphones, tablets, wearables, and Iot (Internet of Things) devices, rely heavily on battery power. Longer battery life is one of the top consumer demands, and power-efficient designs directly contribute to this goal. For instance, smartphones require high-performance processing power, but they must also conserve energy to last through the day on a single charge.

Energy Harvesting: For devices that operate in remote areas (such as sensors in agriculture or environmental monitoring), the need for ultra-low-power operation is paramount since they may not be able to recharge or replace batteries regularly. In such cases, energy harvesting or very low-power designs are essential.

2. Thermal Management

Heat Dissipation: High power consumption leads to excessive heat generation, which can cause circuit failure or degrade performance. Excessive heat can limit the performance of chips and require additional thermal management solutions (such as heat sinks or fans), which in turn adds to cost, size, and complexity.

Smaller Form Factors: As chips are made smaller (in terms of both physical size and transistor scale), managing heat becomes even more challenging. Power efficiency reduces the need for large, costly thermal management solutions, allowing designs to be more compact and reliable.

3. Performance Demands

High-Performance Computing: Digital circuits, particularly processors and GPUS, are pushed to advanced performance situations to handle increasingly complex tasks such as artificial intelligence (AI), machine learning (ML), and data analytics. These high-performance designs need to operate at advanced timepiece speeds and process more data, but they must still maintain power efficiency to avoid inordinate power dispersion and heat generation.

Scalability: As technology scales to more complex systems and processes, power-efficient designs become crucial to maintaining performance without the exponential growth in power consumption. For example, multi-core processors are designed to balance processing power and thermal constraints by optimising the power consumed by each core.

4. Environmental Impact

Sustainability: With the increasing global concern about climate change and environmental sustainability, there is a push for energy-efficient technologies that consume less power and reduce the carbon footprint. Power-efficient designs can help in reducing the energy demand from data centres, networks, and embedded devices, leading to lower environmental impact.

Regulatory Compliance: Many regions and industries have strict regulations regarding energy consumption. For example, Energy Star ratings for devices and compliance with standards like Rohs (Restriction of Hazardous Substances) influence product designs and require power efficiency to meet legal guidelines.

5. Cost Efficiency

Lower Power Bills: For large-scale systems, such as data centres, power consumption becomes a significant operational cost. High-performance servers that consume vast amounts of power can lead to enormous electricity bills, so data centres are increasingly focusing on power efficiency to lower operating costs.

Reduced Need for Cooling Infrastructure: Excessive power consumption not only increases electricity costs but also raises the need for more elaborate cooling systems. By reducing the power consumed by digital designs, the associated cooling requirements are also minimised, leading to cost savings.

6. Design Constraints in Advanced Technologies

Smaller Nodes and Leakage Power: As semiconductor technology advances and transistors are scaled down to smaller nodes (e.g., 7nm, 5nm, or below), power consumption per transistor continues to decrease. However, subthreshold leakage power and other non-ideal behaviours, such as process variations, have become more significant. Designing for power efficiency helps mitigate these effects.

Multi-Functional and Complex Systems: Modern systems-on-chip (SoCs) integrate a variety of functions (processing, memory, networking, etc.) onto a single chip. Each functional block may have different power needs, and managing this power efficiently becomes crucial for maintaining overall system performance without excessive energy consumption.

7. Improved User Experience

Faster Charging: Devices with power-efficient designs often require less time to charge, improving the user experience. The energy demand is lower, so a smaller charger or battery with optimised charging protocols can be used.

Sustained Performance: Over time, thermal throttling occurs in high-power devices when heat buildup forces the system to reduce performance. Power-efficient systems maintain better thermal control and, in turn, help sustain peak performance for longer periods without throttling.

1.5 TECHNIQUES USED IN CLOCK GATING

1. Fundamental Clock Gating

AND Door Clock Gating: The least complex frame of clock gating includes utilising an AND entryway to control the clock flag. The clock is passed through the AND entryway, which also takes a control flag as input.

If the control flag is dynamic (showing the square needs to be dynamic), the clock is passed through; otherwise, the clock is blocked, avoiding superfluous exchanging in the circuit.

2 Multiplexer-based Clock Gating

MUX-based Clock Gating: A multiplexer (MUX) is utilized to select between two clock signals, one is the ordinary clock flag, and the other is a grounded clock (basically turning off the clock). The control flag decides which clock is passed to the target module, permitting it to either get the clock flag or be disabled.

3 Flip-Flop or Latch-based Clock Gating

Latch or Flip-Flop-based Gating: In this approach, a flip-flop or lock holds the clock gating flag, empowering or crippling the clock flag for a few clock cycles.

This procedure guarantees that the clock flag is not flipping as well habitually, and the control flag is synchronised with the clock to avoid glitches.

4 Dual-Edge Activated Clock Gating

Binary-Edge Actuated, this procedure employs both the rising and falling edges of the timepiece flag to choose whether the timepiece ought to be passed or blocked. By empowering the timepiece as it were certain edges, this approach can diminish control application while keeping up circuit performance.

5 Specific Clock Gating

Activity-based Clock Gating: This strategy includes checking the movement of a particular piece and gating the clock when the piece is sitting still. If the piece is not performing any operations or if its inputs are not changing, the clock is turned off, lessening superfluous control consumption.

6 Conditional Clock Gating

Condition-driven Gating: Here, the clock is gated based on certain conditions, such as a control flag or hail. The clock in a circuit square is as it were empowered if the condition is true; otherwise, it is debilitated. This can be especially valuable when certain operations are as it were required under certain circumstances.

7 Clock Gating in Progressive Design

In expansive frameworks, clock gating can be connected at different levels of the design process. For instance, smaller utilitarian pieces inside a bigger module may have their clocks gated freely. Furthermore, whole modules or subsystems can have their clocks gated when they are not required, leading to more effective control management.

8 Clock Gating with Pulse-Width Balance (PWM)

PWM-based Clock Gating: This method includes controlling the width of the clock beats to diminish the effective clock frequency for certain squares. The clock is still running, but it is gated for a portion of each cycle. This permits a module to work at a lower successful frequency, sparing control while keeping up performance.

9 Clock Tree-based Gating

Timepiece Tree Gating In extensive plans, a timepiece dispersion organization (timepiece tree) is employed to circulate the timepiece flag to different places. Timepiece gating can be connected at different points in the timepiece tree, anticipating the timepiece from coming to parcels of the circuit that aren’t by use.

This strategy is especially valuable in large-scale plans where control investment funds are required to be connected to numerous distinctive utilitarian blocks.

10 Software-Controlled Clock Gating

Dynamic Control through a Computer program: In a few frameworks, the program running on a processor or embedded framework may control when to set particular clocks. This is frequently utilized in scenarios where the workload of the framework changes over time, and the framework can powerfully alter which parts of the chip ought to be dynamic based on current assignments.

1.6 SCOPE OF CLOCK GATING

The compass of timepiece gating is vast, as it plays a pivotal part in power operation across colorful digital designs, particularly in VLSI(veritably Large-Scale Integration) systems.

It's a crucial feature used to reduce dynamic power consumption by widely disabling the timepiece signal to portions of the circuit that aren't in use. The compass of timepiece gating can be understood in terms of its operational areas, benefits, challenges, and integration with other power-saving ways.

1. Application Areas

Mobile and Portable Devices: Power consumption is a critical factor in longer battery life in devices such as smartphones, tablets, wearables, and IoT devices. Clock gating is extensively used to disable clocks in idle modules, improving the energy efficiency of these devices.

Microprocessors and CPUs: In processors, where multiple functional units (such as ALUs, FPUs, caches, and memory controllers) are used, clock gating can help reduce power when these units are inactive. For example, the processor may turn off the clock to certain units when not needed (e.g., when waiting for memory access or during idle periods).

ASICs (Application-Specific Integrated Circuits): For custom-built chips in consumer electronics, automotive systems, and industrial control systems, clock gating helps optimize power consumption, ensuring that only necessary parts of the chip are active during operation.

FPGAs (Field-Programmable Gate Arrays): In FPGAs, where configurable logic blocks are used, clock gating can reduce overall power consumption when certain logic blocks are inactive.

Data Centers and High-Performance Computing (HPC): In large-scale systems like data centers, where multiple processors, memory modules, and other components are used, clock gating reduces the power consumed by idle components, thus optimizing the overall power usage.

2. Future Scope

More Advanced Automatic Tools: As designs become more complex, automated tools that intelligently insert clock gating based on real-time activity analysis will become even more important. These tools will become smarter, identifying new opportunities for clock gating and minimizing manual intervention.

Fine-Grained Clock Gating: As systems become more modular, the ability to gate clocks at more granular levels (such as individual pipeline stages or smaller functional units) will provide more power savings. This will require sophisticated analysis tools to identify and gate clocks at the right levels.

Integration with AI/ ML In the future, artificial intelligence(AI) and machine learning (ML) could be abused to prognosticate when the corridor of the system can be clock-gated based on operation patterns, further optimizing power consumption in real-time. The scope of clock gating is extensive and vital for optimizing power consumption in a wide range of digital systems. From mobile devices to high-performance computing and data centers, clock gating helps reduce dynamic power and extend battery life. Despite its challenges, such as design complexity and potential overhead, clock gating remains a cornerstone of modern power-efficient design methodologies. As design sizes and complexities grow, the integration of clock gating with other power management techniques and automated tools will continue to improve its effectiveness and scope.

1.7 HOW TO IMPLEMENT CLOCK GATING

Enforcing timepiece gating in digital circuits is a crucial approach for optimizing power consumption by widely disabling the timepiece signal to the corridor of a circuit that isn't in active use. Below is a step-by-step guide on how to apply timepiece gating, along with the considerations and styles involved

1. Identify Target Blocks for Clock Gating

Determine Idle Units: The first step is to identify which blocks or functional units in the design can be disabled when they are idle. For example, functional units like ALUs, memory controllers, or peripheral devices that are not actively processing data during certain periods could have their clocks gated.

Activity Detection: Often, clock gating is based on the activity of a particular block. For example, a block might only need to be active when certain conditions are met (e.g., when data is being processed or when specific control signals are asserted).

2. Design the Clock Gating Logic

Control Signals: Create a control signal, called an "enable" or "gating signal," that will determine whether the clock should be passed through to the target block. This control signal can be generated based on conditions such as whether the block is active or idle. Logic Implementation: The clock-gating logic generally involves logic gates like AND gates, multiplexers, or flip-flops:

AND Gate- Grounded timepiece Obstructing The simplest system is to use an AND gate to combine the timepiece signal and the control signal. When the control signal is active(e.g., 1), the timepiece passes through; when the control signal is inactive(e.g., 0), the timepiece is blocked. This prevents gratuitous switching in the idle corridor of the circuit.

Multiplexer (MUX)-Based Clock Gating: A multiplexer can also be used to select between the active clock signal and a disabled (grounded) clock. The control signal will determine whether the multiplexer passes the clock or turns it off.

Latch/Flip-Flop: In some cases, flip-flops or latches are used to hold the gating signal, enabling or disabling the clock for multiple clock cycles in response to certain conditions.

3. Insert the Clock Gating Logic

Module-Level Clock Gating fits the timepiece gating sense into each functional unit of the design. The timepiece signal for each module will be reopened by the applicable control signal based on the module's exertion.

Clock Tree Integration: In more complex designs, such as those with large clock trees, clock gating can be inserted at various points in the clock distribution network. This ensures that only the necessary portions of the chip receive the clock signal.

Global vs Local Clock Gating: Clock gating can be applied globally (across large portions of the design) or locally (to individual functional units or blocks), depending on the power optimization needs and design requirements.

4. Synthesize and Simulate the Design

Synthesis: Once the clock-gating logic is added, the design needs to be synthesized. This step ensures that the inserted clock-gating logic is properly integrated into the overall design, and no timing or logical errors are introduced.

Simulation: After synthesis, simulate the design to verify that clock gating works as expected. This step ensures that the clock is disabled for idle blocks and that the circuit behaves correctly when clocks are gated or ungated.

5. Timing Analysis and Verification

Timing Constraints: Clock-gating logic must be synchronized properly to avoid timing violations. This is particularly critical when the clock signal is gated, as improper timing could lead to glitches or incorrect behavior in the circuit. Use Static Timing Analysis (STA) tools to check for any timing issues that may arise due to clock gating. Glitch-Free Gating: Ensure that the clock gating signal is stable and changes in a controlled manner to avoid glitches. Asynchronous changes in the gating signal may introduce glitches that can affect the operation of sequential elements like flip-flops.

6. Optimizing Clock Gating

Minimize Gating Overhead: While clock gating reduces power consumption, it introduces some overhead, such as extra logic gates (AND gates, multiplexers, etc.). To maintain efficient design, the clock-gating logic should be optimized for minimal area and delay. Hierarchical Clock Gating: For large designs, hierarchical clock gating can be employed. This involves gating entire subsystems or blocks, not just individual units, to achieve more significant power savings while minimizing the overhead.

7. Automatic Clock Gating Tools

Automatic Clock Gating: In complex designs, automatic tools can be used to analyze the design and identify blocks that can be clock-gated based on activity analysis. These tools can automatically insert clock-gating logic, greatly reducing manual effort and ensuring that power savings are maximized.

Power Analysis Tools: Tools like Primetime PX (from Synopsys) or Power Compiler can help identify which parts of the design should be clock-gated based on power consumption data. These tools also assist in verifying the effectiveness of clock gating and ensuring the design meets timing and power requirements.

1.8 CLOCK GATING IN ALU DESIGN

1. Distinguish Openings for Clock Gating in ALU

Idle Useful Units: In an ALU, different components like the viper, multiplier, shifter, and rationale doors may as it were be dynamic when particular operations are required. For example, if an operation doesn't require an increase or moving, those units can have their clocks gated to spare power.

Control Signals: The operations in the ALU are regularly controlled by a set of control signals. When certain operations are not chosen by these control signals (e.g., no duplication or moving), clock gating can be connected to the related equipment blocks.

2. Control Flag Era for Clock Gating

The control signals utilized to work the ALU (such as Opcode signals) can be utilized to produce the enable flag for clock gating.

Opcode Translating: Based on the opcode gotten from the control unit (which indicates the ALU operation), a rational circuit can be utilized to produce a gating flag for each ALU component (such as the snake, multiplier, or shifter).

For illustration, if the opcode is for an expansion operation, the viper piece can be clocked, whereas the multiplier and shifter squares can be disabled by gating their clocks.

3. Clock Gating Usage in ALU

Basic AND Gate- Grounded timepiece Obstructing The clearest strategy of timepiece gating in the ALU is to use an AND gate. The timepiece flag of each ALU element(e.g., the snake, multiplier, shifter) is passed through an AND gate, with one input of the gate associated with the timepiece flag and the other input associated with the empower flag created from the opcode or control signal. When the ALU operation does not bear a specific piece, the empower flag is set to 0, blocking the timepiece from that square and sparing power. When the square is required, the empower flag is set to 1, permitting the clock to pass through and enact the component.

Multiplexer (MUX) for Clock Gating: Another strategy is to utilize a multiplexer (MUX) to select between the clock flag and a grounded (crippled) clock. When the ALU component is required, the multiplexer passes the clock flag to the utilitarian unit; otherwise, it passes a zero or grounded clock, turning off the clock to the block.

4. Gating the Clocks of Diverse ALU Components:

Adder: If the ALU is performing an operation that does not require expansion (e.g., a coherent operation), the clock to the viper can be gated off.

Multiplier: If the ALU operation doesn't require an increase, the clock to the multiplier can be gated off. For example, for an expansion or subtraction operation, the multiplier would be inactive.

Shifter: Additionally, the shifter can have its clock gated amid operations where moving is not required (e.g., for essential number-crunching or coherent operations).

Logic Unit: If the ALU operation is absolutely number-crunching (e.g., expansion), the rationale entryways interior of the ALU may not require to be dynamic, permitting the clock to be gated for these rationale gates.

5. Progressive Clock Gating for ALU Subsystem

In bigger ALUs with different useful units, various levels of clock gating can be utilized. For illustration, the ALU may be organized into sub-blocks (such as the snake square, multiplier square, and shifter piece). Each of these pieces can have its clock gated freely based on the operation required, lessening control utilization further.

Clock Gating at the Subsystem Level: If the ALU is a portion of a bigger framework (e.g., inside a processor), it might be valuable to entryway the clock to the whole ALU when it is not being utilized, such as when the processor is sitting out of gear or in a low-power state.

6. Recreation and Timing Analysis

After embedding the clock-gating rationale, it is vital to reenact the plan to guarantee that the clock is appropriately gated and that no timing issues emerge. For example, any glitches in the clock-gating rationale or incorrect synchronization may cause useful errors. Static Timing Investigation (STA) devices ought to be utilized to confirm that the plan meets timing imperatives, particularly when the clock gating is connected at different levels (e.g., on person functional units or subsystems).

7. Contemplations in ALU Design

Power Reserve funds vs. Overhead: Whereas clock gating can altogether diminish control utilization, it presents a few overheads due to the extra logic (AND gates, multiplexers, or flip-flops) required for clock gating. It’s basic to guarantee that the control investment funds from clock gating exceed the overhead incurred in terms of zone and complexity. Glitch-Free Operation: The empower flag for clock gating ought to be steady and altered as it were in a controlled way to dodge presenting glitches or metastability in the ALU. Offbeat changes in the empowerment flag can lead to eccentric behavior in the gated components.

8. Clock Gating Illustration in ALU

Suppose we have an ALU that bolsters four operations: expansion, subtraction, AND, and OR. For each of these operations, we can enter the clock for components as follows: Addition/Subtraction: As it were the snake component needs to be dynamic. The multiplier and shifter clocks can be gated off.

AND/OR: As it were, the rationale entryways (AND/OR entryways) need to be dynamic. The snake and multiplier clocks can be gated off.

Multiplication: As it were the multiplier component needs to be dynamic, so the snake and rationale doors can be clock-gated.

Shifting: For moving operations, as it were, the shifter unit will require a dynamic clock.

9. Optimization and Programmed Clock Gating

Modern blend devices (such as those from Synopsys or Cadence) offer programmed clock-gating capabilities. These apparatuses analyze the plan and consequently embed clock gating rationale where suitable, based on action designs and control signals. These apparatuses can also create control estimation reports to show the effect of clock gating on general control utilization.

2. LITERATURE REVIEW

2.1 GENERAL

Several researchers have carried out studies on the clock gating concept. Studies have also focused on power dissipation, switching activity, and many other aspects.

2.2 Clock Gating – A Power Optimizing Technique for VLSI Circuits by Jitesh Shinde, Dr. S.S. Salankar

In this case, to begin with, an 8-bit ALU (Number Juggling Rationale Unit) is outlined and actualized on the Xilinx ISE Extend Pilot 12.4 instrument. This 8-bit ALU is arranged to be utilized in the design of an 8-bit chip afterward where it may be required to hinder the movement of the 8-bit ALU during a certain number of cycles of the instruction, as required to decrease energetic control utilization of the chip. So, to begin with, the stage of considering, an 8-bit ALU is actualized. At this stage, the plan was tried with different brilliant clock gating choices and plan techniques accessible in Xilinx Extended Pilot Device form 12.4 to think about its impact on net energetic control, scattered or zone in terms of rationale cells utilized.

It can be concluded that Control optimization, customarily consigned to the blend, situation, and steering stages, has moved up to the Framework level and RTL stages. Equipment creators utilize clock gating to turn off inactive areas of the design and diminish the overall power consumption. The RTL approach is vital since creators often confirm control as if it were at the entry level, and any alteration to the RTL needs numerous plan emphases to decrease control. The RTL arrangement hence saves weeks of exertion by settling potential control issues up-front. The RTL coding step is not as early in the planned stream to address control utilization optimization. For each source of utilization and each sort of computerized piece, fitting arrangements can be implemented. Even though the hypothesis behind a few of these strategies can be complex, they are frequently simple to execute. RTL creators ought to be mindful of these methods and utilize their knowledge of the framework not as it were to optimize the speed execution, but also to decrease the unnecessary swapping action.

2.3 Power Optimization in Configurable ALU Using a Blend of Techniques by Mallikarjuna Vatte

In this paper, the timepiece arrangement is a major source of control scattering, so we can diminish the critical quantum of control if we can shut down the timepiece whenever it isn't required. From the writing, we've taken note that there are a few styles utilized to decrease the control inside ALU. The utilized styles are direct and still, there's a compass to diminish control utilizing a blend of ways. So, the Moo-control ALU is planned to utilize timepiece gating methods other than utilizing PIPO and Booth's calculation conception. By giving a particular opcode, we can empower the operation, and other operations are in inert mode, so we can see lower control scattering in the ALU. Moo-control ALU has two 8-bit input information with Cin, caddy, empower, and 2-bit move information, and a decoder 416 to choose the 16 operations by giving a 4-bit opcode to it as an input with the dispatch empower work. At each replication, the proposed plan is implemented with one of these timepiece gating ways, i.e., free timepiece revived design, lock-grounded timepiece revived mold, turnabout grounded timepiece revived mold, and conflation-grounded timepiece gating design with parallel in resemblant eschewal(PIPO)registers. All these ways are performed with operation choice point and PIPO move registers in this plan at diverse working frequencies 100MHz, 200MHz, 400MHz, 500MHz, and 1GHz in Virtex 6. Virtex-6- 6 FPGA board has 40nm innovation with 1 volt in Xilinx ISE 14.4 device. This paper considerably centers on assessing the energetic control scattering for colorful frequencies in ALU with and without timepiece gating methods combined with PIPO and Booth's calculation styles. So, from this ponder, we can conclude that among all timepiece gating ways, the conflation of grounded timepiece revived design with PIPO and Booth's calculation yields the most control.

3. OBJECTIVES

3.1 POWER EFFICIENCY OPTIMIZATION

The primary idea of timepiece gating is to optimize power effectiveness by reducing dynamic power consumption. By widely disabling the timepiece signal to the inactive corridor of a digital circuit, timepiece gating effectively minimizes gratuitous switching exertion and reduces the load on the timepiece distribution network, which together leads to significant power savings. This fashion is especially precious in power-sensitive operations, similar to mobile bias, bedded systems, and high-performance processors.

Yes, the idea of timepiece gating is indeed power effectiveness optimization. Specifically, timepiece gating is a technique used to reduce dynamic power consumption in digital circuits by widely disabling the timepiece signal to portions of the circuit that aren’t actively in use. Then there’s a more detailed explanation of how timepiece gating achieves power effectiveness optimization.

1. Understanding Dynamic Power Consumption

Dynamic power is the power consumed by a circuit when it's switching countries, which occurs during every timepiece cycle when signals change(i.e., sense gates and flip-duds switching between high and low countries).

This power consumption is commensurate with

1. The switching exertion(number of transitions in the sense),

. The capacitance(cargo capacitance of the circuit),

. The timepiece frequency and force voltage.

By disabling the timepiece signal to the inactive corridor of the design, timepiece gating prevents gratuitous switching in those regions, therefore reducing dynamic power.

3.2 DESIGN IMPLEMENTATION

The fundamental objective of clock gating in plan usage is to optimize control productivity by specifically impairing the clock flag to sit still or dormant segments of the circuit, diminishing energetic control utilization without relinquishing usefulness or execution. Accomplishing this requires cautious integration of clock-gating rationale into the plan, overseeing control signals, taking care of multi-clock spaces, and guaranteeing glitch-free and timing-correct behavior. The plan usage moreover includes adjusting control investment funds with range and execution trade-offs. When done accurately, clock gating can essentially upgrade the energy efficiency of advanced systems.

1. Control Effectiveness Through Specific Clock Control

Objective: To specifically cripple the clock flag in parcels of the circuit that are not right now in utilize. This diminishes energetic control utilization by avoiding pointless exchanging movement in those parts of the design.

Design Execution: Amid the plan handle, clock gating cells (ordinarily AND gates or specialized clock gating cells) are included in registers, flip-flops, or other successive components. These cells are controlled by a gating flag that empowers or cripples the clock flag to the focused-on components.

How it Works: When a piece of rationale or an enlist does not require to work (i.e., it's sitting out of gear), the clock flag is blocked, avoiding pointless moves and sparing power.

2. Diminishing Clock Tree Power

Objective: To decrease the control consumed by the clock dispersion arrangement (clock tree) that drives the clock signal to different parts of the chip.

Design Usage: By gating the clock to unused segments of the chip, the number of dynamic clocked components is diminished, in this way bringing down the stack on the clock tree.

How it Works: Clock gating makes a difference in diminishing clock organization control by guaranteeing that as it were dynamic parts of the chip receive the clock signal, minimizing the pointless control dissemination in the clock tree.

3. Taking care of Diverse Clock Domains

Objective: In complex plans with numerous clock spaces, it’s basic to apply clock gating specifically over diverse clock spaces without abusing timing or functionality.

Design Usage: A multi-clock-domain framework can execute clock gating in a way that maintains a strategic distance from obstructions between spaces. The gating rationale must be carefully planned to guarantee that each clock space works autonomously while still accomplishing control reduction.

How it Works: When clock gating is connected over different clock spaces, uncommon care is taken to guarantee that the rationale controlling the clock entryways does not present timing issues or synchronization mistakes. This is accomplished through synchronization instruments or by utilizing clock-gating cells that are designed to handle multi-clock space systems.

4. Overseeing Clock Gating Control Signals

Objective: A crucial portion of the plan prosecution in timepiece gating is the period and administration of timepiece gating control signals. These signals decide when to empower or inhibit the timepiece in a certain corridor of the circuit.

Design Usage: The plan includes deciding the rationale required to produce gating signals based on the usefulness and action of the framework. These control signals can be inferred from the rationale that decides whether a circuit piece is inactive or active.

How it Works: The control signals can be produced utilizing movement finders, clocks, or state machines that monitor the system's behavior and choose when to reset the clock. The execution of these signals must be carefully confirmed to avoid useless errors.

5. Timing and Glitch-Free Operation

Objective: The clock gating method must be executed in a way that does not cause timing infringement or glitches in the framework when empowering or impairing the clock.

Design Usage: The plan ought to guarantee that the clock-gating control signals change at the right times to avoid glitches in the clock signal. The setup and hold time infringement must be maintained at a strategic distance from when the clock is re-enabled.

How it Works: Cautious timing investigation and glitch-free rationale are utilized to guarantee that the clock flag is gated or un-gated in a way that keeps up the circuit’s astuteness. Uncommon clock-gating cells with built-in timing optimizations can be utilized to minimize the chance of glitches.

3.3 Controlling the distribution of Clock Cycles

Controlling the distribution of clock cycles is the main objective of the clock-gating technique because the clock signal, although essential for synchronous digital systems, is also a major source of unnecessary power consumption when distributed indiscriminately. In large VLSI circuits and FPGA-based systems, the clock tree, which distributes the clock to various modules, consumes a significant portion of dynamic power simply by toggling flip-flops and combinational logic, even when these blocks are idle. Clock gating addresses this inefficiency by selectively enabling or disabling the clock signal to specific parts of the circuit based on real-time activity requirements. Instead of allowing the clock to continuously oscillate across all modules, clock-gating logic dynamically evaluates control conditions (such as enable signals or system states) and gates the clock accordingly. By doing so, it effectively "pauses" inactive modules, preventing unnecessary switching activity and capacitance charging/discharging, which directly reduces dynamic power. The ultimate goal is not to eliminate clock signals but to intelligently manage their distribution so that only the essential parts of the system remain active at any given time. This selective distribution enhances energy efficiency, improves thermal performance, extends device life, and supports the overall objective of designing low-power, high-performance digital systems. Particularly in FPGAs like the Nexys A7 with Artix-7, where the flexibility of the fabric allows fine-grained control over logic blocks, implementing clock gating becomes a practical and powerful method to optimize both functional and power characteristics of the design.

3.4 FUNCTIONAL VERIFICATION

Functional verification is the process of checking that a design(including its timepiece gating perpetration) functions correctly and meets its specifications under all possible operating conditions. In the case of timepiece gating, functional verification ensures that

The timepiece's gating sense enables the timepiece to respond to the correct factors at the correct times.

The system operates as anticipated when the timepiece is impaired or re-enabled. The design doesn't introduce unintended gestures, similar to glitches, missed timepiece edges, or incorrect data.

Significance of Functional Verification in Clock Obstruction

Precluding Functional Failures timepiece gating sense, if enforced inaptly, can lead to serious functional issues, similar to data corruption, missed operations, or indeed system failures. Verification ensures that these issues don't arise. Icing System Integrity Functional verification confirms that the system continues to operate correctly while serving power savings through timepiece gating. Confidence in Design Thorough verification builds confidence that the design is both power-effective and functionally correct, making it ready for production.

Functional verification is essential in timepiece gating because it ensures that fashion achieves its goal of reducing power consumption without compromising the correctness of the design. It guarantees that the timepiece gating sense doesn't introduce functional crimes, glitches, or timing violations that could affect the performance or trustworthiness of the system. By employing styles like simulation, formal verification, dynamic verification, and assertions, developers can completely check the geste of timepiece gating in different scripts, ensuring a robust and error-free design.

3.5 PERFORMANCE ANALYSIS

Execution investigation in the setting of clock gating is fundamental for guaranteeing that the strategy effectively decreases control utilization without adversely affecting the framework execution. By carefully analyzing measurements such as idleness, throughput, clock tree control utilization, and timing infringement, designers can guarantee that clock gating is connected successfully. The objective is to accomplish the best conceivable power-performance trade-off, optimizing the plan for controlling investment funds while keeping up satisfactory execution levels, particularly in basic frameworks like processors and real-time applications. The objective is to strike the right balance between diminishing control utilization and keeping up satisfactory execution levels.

1. Understanding Execution Trade-offs in Clock Gating

Clock gating works by turning off the clock flag on parts of the circuit that are not effectively utilized. This diminishes energetic control utilization (since no exchanging happens in the gated parcels), but it can also influence framework execution if not carefully implemented.

The potential execution trade-offs include:

Latency Affect: Clock gating can prevent delays when the clock is re-enabled in gated squares. This seems to influence framework reaction times if the reactivation of the clock is not overseen efficiently.

Throughput Affect: If clock gating is connected to basic way components, the throughput of the framework might be diminished due to the gating and un-gating cycles.

Performance Corruption: Over-the-top clock gating in basic components can lead to execution bottlenecks or timing infringement if the circuit needs to work at higher speeds.

2. Execution Measurements Influenced by Clock Gating

When analyzing execution in the setting of clock gating, the measurements taken after ought to be considered:

a. Clock Tree Control Consumption

Analysis: One key advantage of clock gating is the reduction in clock tree control utilization. The clock conveyance arrangement (clock tree) ordinarily imposes critical control, particularly in huge plans with numerous clocked elements.

Impact on Execution: Whereas lessening clock tree control, the examination ought to guarantee that the clock gating rationale does not present excessive delay or range overhead in the clock organization. The clock-gating cells themselves can expend a few controls, and the complexity of the clock tree may increase as more rationale is embedded to oversee clock gating.

b. Clock Gating Latency

Analysis: Clock gating presents a delay when the clock is turned off and must be turned back on (ungated) for dynamic operations.

Impact on Execution: The inactivity of the clock gating instrument (i.e., how long it takes for the framework to continue operation once the clock is re-enabled) ought to be minimized to dodge execution bottlenecks. For high-speed plans, the effect of these delays can be significant.

Consideration: Creators ought to degree the time it takes to enact or deactivate the clock in different components. This is especially critical for basic components of the plan, where delays may lead to timing violations.

c. Basic Way and Timing Violations

Analysis: Clock gating must be connected carefully to guarantee it does not interfere with the basic way of the plan (the longest way that decides the most extreme working frequency).

Impact on Execution: If the clock gating rationale is connected to basic way components, it can present delays or indeed cause timing infringement when the clock is re-enabled. This can moderate down the general execution of the system.

Optimization: Creators are required to conduct a point-by-point timing examination to guarantee that clock gating does not influence the timing of basic paths or cause setup and hold infringement when the clock is ungated.

d. Throughput Impact

Analysis: In frameworks where information throughput is basic (e.g., processors, memory controllers), clock gating must be carefully connected to dodge decreasing the throughput of the system.

Impact on Execution: The gating and ungating of clocks may result in diminished throughput if expansive parcels of the framework intermittently sit still or if gating presents delays in the handling pipeline. In high-throughput frameworks, the clock-gating component must be fine-tuned to guarantee a negligible effect on performance.

Optimization: For high-throughput applications, creators ought to guarantee that clock gating is as it was connected to non-critical components and that execution measurements (such as idleness or handling speed) are not degraded.

3. Assessing Control vs. Execution Trade-offs

Power Investment funds vs. Idleness: Clock gating diminishes control by crippling clocks to unused segments, but it can present inactivity when the clock is re-enabled. The execution investigation ought to decide whether the control investment funds picked up by clock gating exceed the potential increment in latency.

Power Reserve funds vs. Throughput: In a few frameworks, reducing clocking in certain regions may influence throughput, particularly if the clock gating rationale is connected to high-performance useful units. Execution investigation guarantees that clock gating doesn't compromise throughput below satisfactory levels.

System Level Optimization: Execution investigation ought to include adjusting the control investment funds with execution needs. For occasion, in a processor, it might be worthy to entryway the clock for certain non-critical units (e.g., cache units or fringe pieces), but the center execution units ought to be clocked without interference to maintain a strategic distance from execution debasement.

3.6 RESOURCE UTILIZATION STUDY

A resource application study in the environment of timepiece gating is essential to assess how effectively timepiece gating can optimize power consumption while managing the associated resource costs(area, timing, power, and complexity). This study helps in assessing the trade-offs between power savings and the added complexity of timepiece gating sense. By precisely stating the impact on the area, timepiece tree, critical path timing, and overall power consumption, contrivers can ensure that timepiece gating is applied in a way that maximizes power effectiveness without compromising system performance or resource constraints. The study is an integral part of the design inflow, icing that timepiece gating provides significant benefits without introducing inferior resource charges.

1. Understanding Resource Application in Clock Gating

Clock Gating Logic: The insertion of timepiece gating sense(generally AND gates, flip-flops, or specialized timepiece gating cells) into the design adds redundant buffers to control when and where the timepiece is allowed to pass through. This redundant sense introduces the area above.

Resource Application Analysis: The analysis focuses on how the insertion of timepiece gating sense affects the operation of different coffees in the design(e.g., gate count, area, power, and timing), and whether the reduction in dynamic power outweighs the fresh resource cost.

2. Power Consumption Analysis

Power Reduction One of the primary benefits of timepiece gating is the reduction in dynamic power consumption by disabling the timepiece in idle sections of the circuit. The resource application study should dissect how important power is saved by turning off the timepiece and whether the power savings are worth the resource cost.

Extra Power Consumption from Clock Gating Logic The timepiece gating cells themselves (e.g., AND gates, multiplexers, or flip-duds) add a small button-negligible static power consumption and dynamic power consumption associated with their operation.

An analysis is ideal the resource application study must measure the total power savings from reduced switching exertion in idle regions and compare it with the fresh power consumption introduced by the timepiece gating circuitry.

Optimization. The study will help identify areas where fresh timepiece gating may not be worth the redundant resource operation, ensuring that power consumption is optimized without gratuitous resource outflow.

3. Area, Power, and Timing Simulation Tools

Simulation for Resource Application. To perform an accurate resource application study, designers use colorful simulation tools to profile the area, power, and timing of the design with and without timepiece gating. These tools allow creators to see the exact impact of timepiece gating on the overall design coffers. Tools for Area and Power Analysis.

Tools like Cadence Innovus, Synopsys Design Compiler, or Mentor Graphics can help measure the area and power impact of timepiece gating on a design. These tools give insight into how important a redundant area is needed and whether the power savings are significant enough to justify the added cost.

Stationary Timing Analysis(STA) Timing analysis tools like Synopsys PrimeTime or Cadence Tempus allow designers to check for any timing violations or critical path delays introduced by timepiece gating, helping ensure that the performance of the design remains intact.

4. Impact on Resource Utilization in Complex Systems

Large Systems with Multiple Clock Domains: In complex systems, such as processors or ASICs with multiple clock domains, resource utilization becomes more complex. Clock gating must be carefully applied across these multiple domains, and the analysis must consider how gating one domain impacts other domains, the clock distribution, and inter-domain synchronization.

Resource Sharing: In systems with shared resources (e.g., shared memory or bus systems), clock gating must be applied efficiently to avoid performance bottlenecks or resource conflicts. The resource utilization study should ensure that clock gating does not negatively impact the shared resources and their utilization.

5. Design Constraints and Optimization Goals

Cost vs. Benefit: The resource utilization study provides a detailed picture of the costs (area, timing, power) and benefits (reduced power consumption, optimized clock network) of clock gating. The study will help designers make informed decisions on whether to apply clock gating in certain blocks or how to adjust the design to optimize the resource cost relative to the power savings. Scalability: The study will also consider whether the clock-gating approach scales well as the design size grows. For example, in a large system, the resource cost of clock gating might grow significantly, so it's important to evaluate its scalability.

4. STUDY AREA

4.1 CLOCK DISTRIBUTION NETWORK OPTIMIZATION

The timepiece Distribution Network Optimization under the timepiece Obstructing medium is a pivotal aspect of ultramodern digital circuit design. It directly influences overall power consumption, performance, and design. The timepiece distribution network(also known as the timepiece tree) is responsible for delivering the timepiece signal to all successive rudiments(like flip-duds) in a digital system. When timepiece gating is applied, the corridors of the circuit that aren't laboriously in use have their timepieces impaired, leading to power savings. Still, optimizing the timepiece distribution network while using timepiece gating is complex and requires careful balancing of power savings, performance, and resource operation.

Key Areas of Study in Clock Distribution Network Optimization with Clock Gating

1. Power Savings in Clock Tree
2. Clock Tree Load Reduction
3. Clock Distribution Network Efficiency
4. Clock Routing and Resource Allocation
5. Timing and Clock Skew Analysis
6. Synchronization and Control of Gated Clocks
7. Clock Gating Cell Selection
8. Area-Delay-Power Trade-Offs
9. Clock Gating in Multi-Domain Designs

4.2 ASIC and FPGA

The timepiece gating medium in both ASICs and FPGAs serves the critical purpose of reducing power consumption by widely disabling timepieces in inactive sections of the design. Still, the perpetration, optimization, and trade-offs between power, area, and timing performance vary significantly between the two platforms.

ASICs offer high efficiency in clock gating due to their customized design and fixed architecture, allowing fine-tuned control over the clock distribution network and optimal power management with minimal impact on performance.

FPGAs offer flexibility and reconfigurability, enabling dynamic clock gating, but this comes with challenges in resource utilization, routing congestion, and potential timing degradation, as the resources are not as optimized as in ASICs.

The study of clock gating in both ASICs and FPGAs involves a careful balance of power efficiency, performance, and resource utilization. Each platform requires different tools and strategies to optimize clock gating based on the specific design goals, system constraints, and platform capabilities.

Design Tools and Optimization Techniques

ASIC:

Power and Timing Analysis: In ASIC designs, specialized tools are used for power analysis, timing analysis, and clock gating optimization. These tools allow designers to fine-tune clock gating implementation and optimize the design for minimal power usage and maximum performance.

Cell-based Clock Gating: ASIC designs can use custom clock-gating cells optimized for the design’s needs, minimizing the area and power impact.

FPGA:

FPGA Design Tools: FPGAs typically use tools such as Xilinx Vivado or Intel Quartus for design, power, and timing analysis. These tools offer FPGA-specific features for clock gating, such as Clock Enable primitives or dynamic clock management blocks, which help implement clock gating with minimal impact on the FPGA’s performance and power.

Optimization Challenges in FPGAs: The FPGA tools may not always generate the most power-efficient clock gating solution due to the general-purpose nature of FPGA resources, which might lead to higher area or power consumption compared to ASIC designs.

Performance and Timing Considerations

ASIC:

Precise Timing Optimization: In ASIC designs, clock gating can be implemented without significant timing degradation, as the design is optimized for specific tasks. The clock-gating logic can be designed to minimize timing impacts, such as delays in gating and ungating.

FPGA:

Impact of Clock Gating on FPGA Performance: In FPGAs, clock gating can lead to performance degradation if not carefully managed. The routing delays for clock-enable signals can increase the overall delay, especially in high-speed designs. Additionally, if the FPGA logic is not optimized, the clock gating cells can add delays that affect the setup/hold timing and critical path.

Timing Challenges: Since the FPGA fabric is programmable and not custom-designed, it may not be as efficient as an ASIC in handling clock gating with minimal timing penalties. The propagation delays introduced by the gating signals, combined with the routing overhead, can impact the maximum frequency achievable by the design.

Clock Gating Logic and Resource Usage

ASIC:

Clock Gating Cells: In ASICs, clock gating is implemented by adding gating cells (typically AND gates, flip-flops, or specialized clock gating cells) to the design. These cells control whether the clock is passed to different blocks of the circuit. Since ASICs are custom-designed, the gating logic can be optimized for the exact needs of the circuit.

Resource Utilization: ASICs can make efficient use of clock gating logic, as the cells are custom-designed and well-integrated into the overall chip architecture. The additional area consumed by clock-gating logic is often minimized since it’s designed for the specific layout and architecture.

FPGA:

FPGA LUTs and Flip-Flops: In an FPGA, clock gating is typically achieved using) flip-flops and LUTs. The LUTs can be configured to implement clock-gating logic, and the FPGA’s routing resources are used to propagate clock-enabled signals.

Dedicated Clock Gating Blocks: Modern FPGAs often feature dedicated clock gating resources (like clock enable pins or blocks specifically designed to manage clock gating), which simplify the implementation and reduce overhead. However, the utilization of FPGA resources for clock gating (such as LUTs, routing, and logic elements) can still impact area and timing.

Resource Utilization Impact: FPGAs offer less efficient use of clock gating compared to

ASICs because of their generic architecture. The extra resources required for clock gating (e.g., LUTs, routing elements) can increase the design’s resource usage and affect timing performance.

Power Efficiency Optimization

ASICs: ASICs are custom-designed chips where clock gating can be used to optimize dynamic power consumption across various sections of the chip. Since ASIC designs are typically optimized for a specific application, clock gating can be finely tuned for the design's specific usage patterns.

Timepiece Gating in ASICs. Power savings are achieved by widely gating timepieces to the corridor of the circuit that aren't in active use. The power reduction comes primarily from dynamic power consumption, which is commensurate with the switching exertion of sense rudiments. ASICs, with their fixed, optimized armature, allow for effective and aggressive timepiece gating in idle areas.

FPGA: FPGAs are programmable devices where clock gating is typically used in a more generalized manner, as the user can configure the logic within the FPGA to perform specific tasks. Clock gating in FPGAs helps to reduce power in areas that are not required for the current operation.

Clock Gating in FPGAs: In FPGAs, clock gating can be more challenging, as the hardware resources are general-purpose and not customized for a specific task. However, modern FPGAs provide dedicated clock-gating primitives (e.g., Clock Enable pins or specialized logic blocks) that allow the designer to optimize clock distribution and power consumption for different tasks or blocks within the FPGA fabric.

4.3. DIGITAL CIRCUIT DESIGN

Clock gating is a powerful mechanism in digital circuit design to optimize dynamic power consumption. Its primary benefits lie in selectively disabling the clock to inactive parts of the design, thus reducing unnecessary switching activity.

#Design aspects:

1. Power and area trade-offs
2. Timing constraints and performance degradation

3. Clock tree efficiency

4. Verification and testing

In ASIC designs, clock gating can be highly efficient due to the customized nature of the architecture, allowing designers to minimize area overhead and fine-tune performance. On the other hand, in FPGA-based designs, the flexibility and reconfigurability come at the cost of higher area and performance overhead. Ultimately, clock gating must be balanced with other low-power techniques and carefully verified to ensure that it does not compromise the functionality, timing, or performance of the circuit. Advanced tools for simulation, timing analysis, and power verification play an essential role in ensuring the successful implementation of clock gating in digital circuits.

1. Power Optimization in Digital Circuits

Objective: The primary goal of clock gating is to reduce dynamic power consumption, which is dominated by the switching activity of flip-flops, registers, and other sequential elements in a digital circuit. By disabling the clock in inactive sections of the circuit, clock gating can significantly reduce the overall power usage of the system.

How Clock Gating Helps:

Selective Clocks: Only sections of the circuit that are active require clocking. Parts that are idle or in a quiescent state can have their clocks gated off, effectively reducing the power consumed by the clock network and other sequential elements. Reduction in Switching Activity: Since dynamic power is proportional to the switching activity, by gating clocks to inactive blocks, the switching capacitance in the circuit is reduced.

Impact on Power Consumption:

In large designs, clock gating can result in substantial power savings, especially in applications where certain sections of the circuit remain idle for long periods (e.g., when certain data paths or functional blocks are not needed).

2. Clock Gating Logic Design

Objective: In digital circuit design, clock gating requires additional control logic (gating logic) to decide when to disable or enable the clock signal to certain parts of the circuit. This gating logic typically involves AND gates, multiplexers, or specialized clock-gating cells.

Types of Clock Gating:

Asynchronous Clock Gating: The clock is disabled asynchronously, meaning without synchronization with other parts of the circuit.

Synchronous Clock Gating: The clock gating signal is synchronized with the clock to ensure proper timing and avoid glitches or timing violations when the clock is gated.

Impact on Design:

Clock-gating logic requires careful design to ensure that the gating signal does not introduce hazards, timing violations, or glitches.

Control Signals: The design needs a method for generating the enable or disable signals for each clocked element. This can be done either statically (based on static control signals) or dynamically (based on runtime conditions).

3. Timing and Performance Considerations

Objective: While clock gating helps reduce power, it must not compromise the timing performance of the digital circuit. The key concerns here include:

Clock Skew: Clock gating may introduce delays in the clock signal when re-enabling the clock to the gated section, which could lead to increased clock skew.

Setup and Hold Time Violations: Disabling the clock could potentially lead to timing violations when the clock is re-enabled. This is because the state of the gated elements may not be properly synchronized with the rest of the circuit.

Critical Path Delay: The design of clock-gating logic itself can introduce delays. If the gating logic is not optimized, it can add significant delays to the critical path of the design, potentially lowering the overall operating frequency.

Clock Gating and Timing Analysis:

Timing analysis tools (e.g., Synopsys PrimeTime, Cadence Tempus) are essential in evaluating whether clock gating introduces any timing issues such as setup or hold-time violations, timing skew, or degradation of the maximum operating frequency of the design.

Careful Synchronization: Using clock-gating techniques that synchronize with the clock, such as synchronous gating, helps mitigate timing issues and ensures that the clock is not gated during critical periods.

4. Design Complexity and Area Overhead

Objective: Clock gating adds extra logic to the design, and it is important to understand the impact on the overall circuit complexity, area, and resource utilization. **Clock Gating Cells and Their Area Impact**: The area overhead of clock gating depends on the number of gating cells (AND gates, multiplexers, or specialized cells) added to the design. **For example:**

Simple Clock Gating: Using basic AND gates to implement clock gating can incur minimal area overhead.

Advanced Clock Gating: Using more complex cells (e.g., specialized clock-gating cells or flip-flops with built-in clock-enable functionality) can increase the area overhead, but they may reduce the complexity of control logic.

Area Trade-offs: In large systems, area overhead may become a critical factor, especially when a significant portion of the design is subject to clock gating. The total area of the design is increased due to the extra resources used by clock gating logic, though the power savings can justify these trade-offs.

5. Clock Distribution Network

Objective: The clock distribution network (also known as the clock tree) is responsible for delivering the clock signal to all clocked elements in a digital circuit. Clock gating impacts this network by reducing the number of active elements, thus saving power.

Clock Tree Optimization with Clock Gating:

By gating the clock to inactive blocks, the load on the clock tree is reduced, minimizing the power consumed by the clock distribution network.

Clock Skew and Network Load: A more efficient clock tree with fewer active clocked elements can also reduce clock skew, leading to better performance and reliability.

Challenges: On the flip side, clock gating can also introduce new complexities in the clock distribution network. Additional routing might be needed for the gating control signals, leading to potential routing congestion or added delays. Careful design is required to balance the clock-gating benefits with the impact on clock routing.

5. MATERIALS AND METHODOLOGY

The Clock Gating technique is an essential method for optimizing power consumption in VLSI circuits, but its successful application requires a comprehensive methodology. From selecting the appropriate gating logic and implementing it using hardware components to using advanced software tools for synthesis, verification, and optimization, each phase is crucial. Effective design, implementation, and verification are essential to ensure the correct functionality, minimal area overhead, and maximum power efficiency in VLSI circuits using clock gating.

The Clock Gating method is a significant control optimization strategy in VLSI (Very-Large-Scale Integration) circuits, empowering productive control utilization by specifically impairing the clock signal to dormant components. To effectively execute this strategy, suitable equipment components, program apparatuses, and techniques must be employed. Below is a comprehensive breakdown of the materials and techniques for actualizing clock gating in VLSI circuits, covering everything from the equipment components to optimization techniques.

5.1. Materials

The physical equipment components in VLSI circuits are basic to the appropriate usage of clock-gating procedures. These components are mindful of the productive era, proliferation, and gating of clock signals in advanced circuits.

5.1.1 Hardware:

- Nexys A7 (Artix-7 FPGA) Development Board (by Digilent, featuring Xilinx Artix-7 XC7A100T FPGA)
- Micro-USB Cable (for programming and power supply)
- Laptop/PC (with minimum requirements to run FPGA design software)
- External Power Supply (optional, if USB power is insufficient)

5.1.2 Software:

- Xilinx Vivado Design Suite (preferably 2022.2 or the latest version)
- Digilent Adept Utility (optional, for programming/debugging)
- Power Estimator and Analyzer Tool (inside Vivado)
- Simulation Tools (Vivado's built-in simulator or ModelSim)

5.1.3 Other Materials:

- Datasheets (Artix-7 FPGA datasheet, Nexys A7 reference manual)
- User Constraints File (UCF/XDC) (to map design pins to FPGA physical pins, like switches, LEDs).

5.2 Methodology

5.2.1 Design Phase:

- Identify target circuit: For example, a 4-bit ALU or a counter circuit.
- Add Clock Gating Logic: Introduce control signals that enable/disable the clock signal to different blocks based on their activity.
- Two ways:
  - Simple clock gating (using enable signals)
  - Integrated clock gating cells (more advanced, supported by FPGA primitives).

5.2.2 Coding:

- Write Verilog/VHDL code for:
  - Main functional circuit (e.g., ALU, counter).
  - Clock gating logic (e.g., ANDing the clock with an enable signal).
- Use parameters to easily switch between gated and non-gated versions.

5.2.3 Simulation:

- Simulate both versions:
  - Without clock gating.
  - With clock gating.
- Verify functionality correctness using testbenches.

5.2.4. Synthesis and Implementation:

- Synthesize the design in Vivado.
- Apply constraints (mapping clock input, reset, outputs to FPGA pins like buttons and LEDs).
- Implement the design and resolve any timing issues.

5.2.5. Programming and Testing:

- Program the Nexys A7 FPGA board via JTAG or USB.
- Test the design physically:
  - Observe outputs (LEDs).
  - Check switching activity (optional: use on-board logic analyzers like Xilinx ILA).

5.2.6. Power Analysis:

- Measure dynamic power with Vivado’s Power Analyzer:
  - Perform static and post-implementation power analysis.
  - Compare dynamic power between non-gated and gated designs.
- Observe switching activity reduction.

5.2.7. Result Evaluation:

- Compare:
  - Timing (setup/hold) changes.
  - Dynamic power reduction percentage.
- Document results with tables and graphs.

5.3. Design and Implementation Procedures

The design and implementation of clock gating in VLSI circuits involve several key steps, from initial planning to final verification.

Step 1: Analyze the Circuit Requirements

Understand the power and performance requirements of the system. Identify areas of the circuit where clock gating would provide significant power savings.

Target Areas: Identify modules or blocks that can be clock-gated, such as functional units, registers, or idle blocks.

Step 2: Select Clock Gating Methodology

Choose between static or dynamic clock gating depending on the specific requirements of the system.

Decide whether module-level or fine-grained clock gating is more appropriate for the application.

Step 3: Implement Gating Logic

Use appropriate logic (AND gates, multiplexers, or clock-enable flip-flops) to implement the clock-gating strategy. Insert clock-enable signals into flip-flops and registers that can be disabled.

Step 4: Integrate the Gating Logic into the Design

Integrate the clock-gating logic into the overall RTL design. Ensure that the design still functions correctly by simulating it using software tools.

Step 5: Perform Synthesis and Optimization

Use synthesis tools (e.g., Design Compiler) to synthesize the design while incorporating the clock-gating logic. Optimize the placement of clock-gating logic to minimize overhead and delay.

Step 6: Validate Functionality

Simulate the design with test benches to ensure that clock gating operates as expected without introducing any functional errors.

5.4. Verification and Validation

Verification and validation are crucial for ensuring the correctness of the design, particularly after clock gating is applied.

Functional Verification:

Use simulation tools such as ModelSim, VCS, or Xilinx Vivado to verify that the clock gating logic operates correctly under various conditions. Generate testbenches to cover scenarios where clock gating will be activated and deactivated.

Timing Verification:

Perform static timing analysis (e.g., using PrimeTime) to ensure that there are no timing violations (e.g., setup/hold violations) due to clock gating.

Check that clock skew is minimized and that gated sections can still function correctly when

The clock is re-enabled.

Power Verification:

Use tools like PrimePower or Voltus to check if clock gating achieves the desired reduction in dynamic power consumption without negatively impacting performance. Verify that clock gating works as intended in power domain isolation.

5.5. Optimization Techniques

After implementing clock gating, optimization is necessary to ensure that it delivers maximum power savings with minimal impact on performance.

Optimization for Timing:

Critical Path Analysis: Evaluate the impact of clock gating on the critical path and reduce any delays introduced by gating logic. Use retiming and pipelining techniques to optimize timing performance after clock gating is implemented.

Optimization for Area:

Minimize area overhead by carefully choosing clock-gating cells that balance power savings

and area. Use automated tools to find optimal clock-gating points and reduce the overhead introduced by extra logic.

Dynamic Clock Gating: If the design is subject to variable workloads, implement dynamic clock gating that adapts the gating behavior based on the operational state of the circuit, further optimizing power consumption.

6. RESULTS AND DISCUSSIONS

The image appears to be a digital circuit design of a 4-bit Arithmetic Logic Unit (ALU) built using basic logic elements in RTL (Register Transfer Level) schematic form. Below is a detailed analysis of the different components and their roles in the circuit:

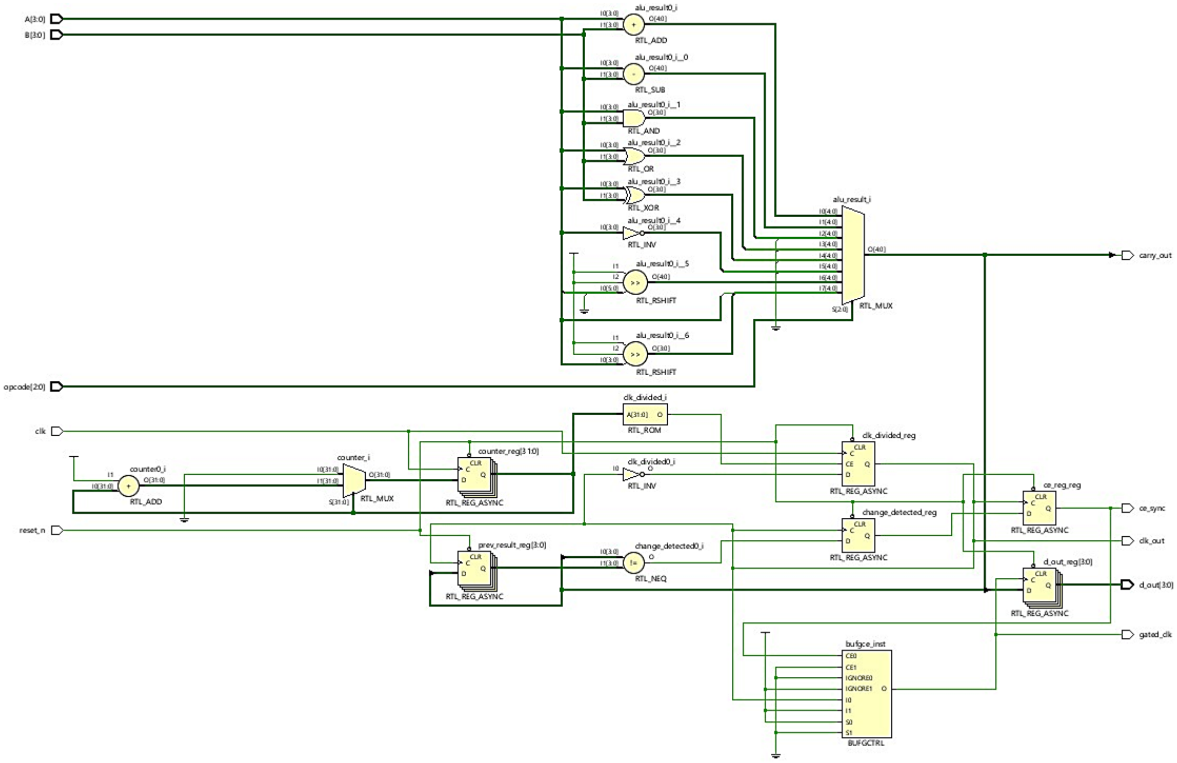


Fig.2: 4-bit ALU Design With Clock Gating Mechanism

Inputs:

1. A[3:0], B[3:0]
   - 4-bit input operands to the ALU.
   - Represent the primary data inputs for arithmetic or logic operations.
2. opcode[2:0]
   - Operation selector input for the ALU.
   - Controls which ALU operation (ADD, SUB, AND, OR, etc.) to execute.

3. clk
    - Main clock input to the system.
4. reset_n
    - Active-low reset signal, used to initialize registers or clear the system.

Outputs:

1. alu_result[3:0]
    - Output of the ALU based on the opcode and inputs A and B.
2. carry out
    - Carry-out signal for operations like addition.
3. clk_divided
    - A divided (slower) clock, used to reduce switching frequency for power savings.
4. change_detected
    - A signal that indicates when a change has occurred in the inputs or results, used to trigger clock gating.
5. gated_clk
    - The clock after gating, i.e., the clock signal is passed only when a change is detected or a control condition is met.
6. d_out_reg[3:0], d_out, d_out_reg
    - Register outputs storing the final ALU result or data path result, often synchronized with a gated clock.
7. dc_out, dc_sync
    - Possible data change indicator and clock synchronization flag.

Key Components & Their Functions:

➤ **ALU Block**

- Contains:
  - ADD, SUB, AND, OR, XOR, NAND, etc.
  - Controlled by opcode[2:0].
  - Outputs are multiplexed using an MUX to produce alu_result.

➤ **MUXes**

- Used to select between different ALU operation outputs.
- Another MUX is used for counter and result selection.

➤ **Registers (RTL_REG_ASYNC)**

- Store intermediate and final results.
- Used to hold:
  - ALU outputs
  - Previous result
  - Divided clock
  - Change detection flags

➤ **Counter Block (counter_i)**

- Generates timing signals or internal counters.
- Drives sequencing logic.

➤ **Clock Divider (clk_divided)**

- Uses a ROM or simple logic to generate a slower clock.
- Helps reduce overall switching activity.

➤ **Change Detection Logic**

- Compares current and previous values to detect changes.
- Includes XOR and INVERTER blocks.

➤ **BUFGCE/BUFGCTRL**

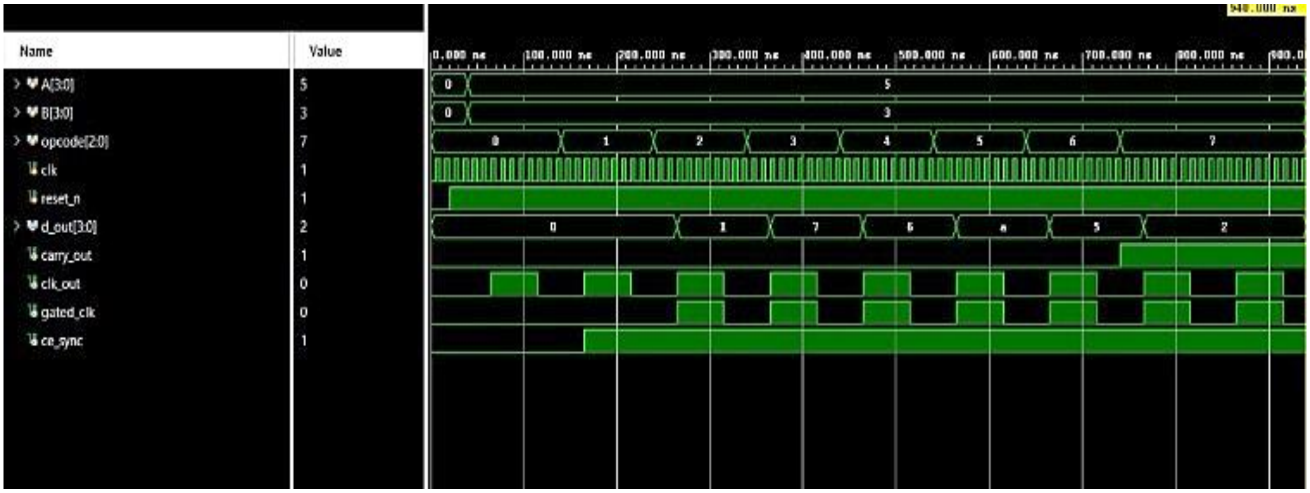
- FPGA clock gating primitive.
- Used to gate the main clock based on control logic (like change_detected).
- Ensures glitch-free clock gating.

Overall Functionality Summary:

- The system takes in A, B, and an opcode to compute an ALU result.
- Registers and change detection logic monitor changes.
- If no change is detected, the clock to certain blocks is disabled using the gated clock (gated_clk), reducing dynamic power consumption.
- The clock divider reduces the frequency of operation to save power.
- Outputs are synchronized and buffered for stable performance.

Clock Gating:

The clk_out_i output from the AND gate ensures that the clock is gated, i.e., clock signals are only enabled when needed, improving power efficiency.



Name	Value
A[3:0]	5
B[3:0]	3
opcode[2:0]	7
clk	1
reset_n	1
d_out[3:0]	2
carry_out	1
clk_out	0
gated_clk	0
ce_sync	1

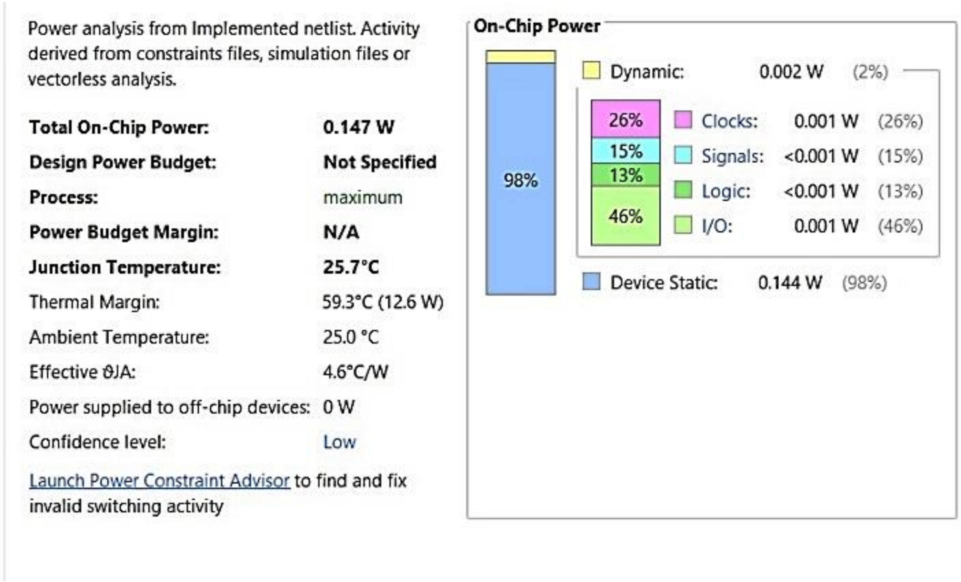
Fig.3: Waveforms for 4-bit ALU with Clock Gating Mechanism

Detailed Waveform Interpretation:

- Inputs A = 5 and B = 3 remain constant throughout the simulation.
- Opcode changes from 000 to 111, each representing a different ALU function (ADD, SUB, AND, OR, XOR, NAND, NOR, SHIFT).
- ALU output (d_out) changes correctly with each opcode:
  ADD → 8, SUB → 2, AND → 1, OR → 7, XOR → 6, NAND → 14,
  NOR → 0, SHIFT → 2.
- Carry-out is active (1) only during the ADD operation, indicating a correct carry when 5 + 3 = 8 (4-bit overflow).

- Main clock (clk) runs continuously, serving as the base clock source.
- Clock gating is implemented using gated_clk, which toggles only when the opcode or data changes, reducing unnecessary switching activity.
- ce_sync signal synchronizes clock enable, ensuring gated_clk is glitch-free and only active when computations are needed.
- clk_out is a divided or intermediate clock, used in conjunction with ce_sync for clock-gating logic.
- Clock-gating functionality is validated, as ALU operations update only when required, proving power-efficient behavior.
- Waveform confirms design correctness and low-power behavior for FPGA-based ALU with clock gating.

Power Analysis Summary:



Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.147 W**
Design Power Budget:	**Not Specified**
Process:	maximum
Power Budget Margin:	**N/A**
Junction Temperature:	**25.7°C**
Thermal Margin:	59.3°C (12.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	0.002 W	(2%)
🟪 Clocks:	0.001 W	(26%)
🟦 Signals:	<0.001 W	(15%)
🟩 Logic:	<0.001 W	(13%)
🟩 I/O:	0.001 W	(46%)
🟦 Device Static:	0.144 W	(98%)

Fig.4: Power Report on the Clock Gating Mechanism

Power Analysis Summary (Nexys Artix-7 FPGA)

1. Total On-Chip Power:
   - 0.147 W (147 mW) — Total power consumed on the FPGA chip.
2. Dynamic Power:
   - 0.002 W (2%) — Power consumed due to switching activity (includes clocks, signals, logic, and I/O).

3. Static Power:
    - 0.144 W (98%) — Power consumed when the circuit is idle (leakage power).
4. Dynamic Power Breakdown:
    - Clocks: 0.001 W (26%)
    - Signals: <0.001 W (15%)
    - Logic: <0.001 W (13%)
    - I/O: 0.001 W (46%)
5. Junction Temperature:
    - 25.7°C — Safe operating temperature.
6. Thermal Margin:
    - 59.3°C (12.6 W) — Temperature margin before exceeding thermal limits.
7. Ambient Temperature:
    - 25.0°C — Temperature of the surrounding environment.
8. Effective ΘJA:
    - 4.6°C/W — Thermal resistance from junction to ambient.
9. Power Supplied to Off-Chip Devices:
    - 0 W — No external device is drawing power.
10. Confidence Level:
    - Low — Indicates switching activity might be incomplete or inaccurate due to missing constraints or simulations.

7. CONCLUSION

7.1 Conclusion

The implementation of the clock-gating technique using the Nexys Artix-7 FPGA board has been successfully validated through schematic design, functional waveform analysis, and detailed power analysis. The RTL schematic illustrates an 8-bit Arithmetic Logic Unit (ALU) where multiple operations such as ADD, SUB, AND, OR, XOR, NAND, NOR, and SHIFT are handled based on opcode input. Integrated within the ALU design is a clock gating mechanism that ensures the clock signal (gated_clk) is activated only when necessary, specifically, when there is a change in the input data or operation code. This is achieved using synchronizers (ce_sync), divided clocks (clk_out), and conditional logic blocks.

The simulation waveform further confirms the correctness of the design. For each opcode from 0 to 7, the ALU produces the correct result based on inputs A and B, and the carry_out signal responds appropriately, particularly during the addition operation. Importantly, the gated clock (gated_clk) toggles only during active computational cycles, demonstrating effective reduction in redundant switching, a core goal of clock gating. The enable synchronization (ce_sync) ensures smooth and glitch-free clock gating transitions.

Power analysis results support the effectiveness of the clock-gating technique. The total on-chip power consumption is 0.147 W, with static power accounting for 98% (0.144 W) and dynamic power only 2% (0.002 W). Among dynamic components, the clock and I/O activities contribute most, while logic and signal switching remain minimal, indicating the gated clock successfully suppresses unnecessary activity. Overall, the design exhibits efficient power usage without compromising performance, making it suitable for energy-sensitive FPGA applications or as a prototype for low-power VLSI systems. Power optimization, customarily consigned to the amalgamation, situation, and directing stages, has moved up to the Framework level and RTL stages. Equipment architects utilize clock gating to turn off dormant segments of the plan and diminish by and large dynamic control utilization. The RTL approach is imperative since architects often confirm control as if it were at the door level, and any alteration to the RTL needs numerous plan emphases to decrease control. The RTL arrangement in this way spares weeks of exertion by settling potential control issues up-front.

The RTL coding step is not as early in the planned stream to address control utilization optimization. For each source of utilization and each sort of advanced square, suitable arrangements can be actualized. Even though the hypothesis behind a few of these procedures can be complex, they are regularly simple to implement. RTL creators ought to be mindful of these methods and utilize their knowledge of the framework not as it were to optimize the speed execution, but also to decrease the superfluous exchanging movement.

7.2 Scope for further study

Scope for Further Study on Clock Gating Techniques for VLSI Circuits
The clock-gating technique plays a vital role in reducing dynamic power consumption in VLSI circuits. Further research and exploration can help improve its efficiency and applicability. Below are potential directions for advanced study and research:

1. Clock Gating Techniques and Architectures

Fine-grained vs. Coarse-grained Clock Gating:
Study the trade-offs between gating individual flip-flops (fine-grained) vs. larger circuit blocks (coarse-grained) in terms of power savings and design complexity.
Multi-level Clock Gating: Explore hierarchical clock gating techniques that gate clocks at multiple levels, such as functional units, sub-blocks, and individual registers.

Dynamic Clock Gating: Investigate adaptive clock gating where clock enables signals are dynamically generated based on run-time conditions to improve efficiency.

2. Clock Gating Control Logic Optimization

Minimization of Glitches:
Research methods to minimize spurious transitions and glitches in clock enable signals, which can negate power-saving benefits.
Prediction Algorithms:
Study predictive algorithms that anticipate idle periods and enable pre-emptive clock gating.
Low-overhead Gating Logic:
Explore the development of efficient gating circuits that reduce area and power overhead associated with the gating logic itself.

3. Power-Aware Design Automation

EDA Tool Enhancements:

Investigate enhancements in Electronic Design Automation (EDA) tools for automatic insertion and optimization of clock gating.

Design Verification for Clock Gating:

Develop improved verification methodologies to ensure correct functionality after clock gating insertion.

4. Integration with Other Low-Power Techniques

Clock Gating with Voltage Scaling: The study combined approaches where clock gating is used alongside dynamic voltage and frequency scaling (DVFS) for enhanced power efficiency.

Power Gating Integration: Explore the integration of clock gating with power gating to completely shut off idle sections of the circuit when not needed.

5. Application-Specific Clock Gating

Digital Signal Processing (DSP) Applications: Optimize clock gating for DSP circuits where data processing loads vary significantly over time.

Neural Networks and AI Accelerators:

Study the use of clock gating to optimize power consumption in AI inference engines.
IoT and Edge Devices:

Investigate clock gating in ultra-low-power designs for Internet of Things (IoT) and battery-operated devices.

6. Clock Distribution Network Optimization

Research ways to optimize clock tree synthesis (CTS) considering clock gating.

Study low-power clock network designs to minimize clock skew and jitter while maintaining efficiency.

7. Emerging Technologies and Clock Gating

3D Integrated Circuits:

Investigate clock-gating strategies for vertically stacked VLSI circuits in 3D ICs.

Asynchronous Circuits:

Study hybrid clock-gating techniques for circuits that mix synchronous and asynchronous design principles.

REFERENCES

[1] Jitesh Shinde, Dr. S.S. Salankar, Clock Gating –A Power Optimizing Technique for VLSI Circuits, J.L. Chaturvedi College of Engineering, Department of Electronics & Telecommunication Engineering, Nagpur.

[2] Dushyant Kumar Sharma, Effects of Different Clock Gating Techniques on Design, International Journal of Scientific & Engineering Research, Vol. 3, Issue 5, May 2012.

[3] Massoud Pedram and Afshin Abdollahi, "Low Power RT-Level Synthesis Techniques: A Tutorial" Dept. of Electrical Engineering, University of Southern California

[4] L. Benini, M. Favalli, and G. De Micheli, "Design for testability of gated-clock FSMs," in Proc. European Design and Test Conf., Paris, France, Mar. 1996, pp.

[5] Power optimization in configurable ALU using a blend of techniques, Mallikarjuna Vatte, Department of Electronics, NIT Surat, 2021 2nd International Conference for Emerging Technology (INCET), Belgaum, India. May 21-23, 2021

[6] Power Reduction by Clock Gating Technique Nandita Srinivasana, Navamitha. Prakasha, Shalakha.Da, Sivaranjani.Da, Swetha Sri Lakshmi.Ga*, B.Bala Tripura Sundaria SMART GRID Technologies, August 6-8, 2015

[7] B. Geetha, B. Padmavathi, and V. Perumal, "Design methodologies and circuit optimization techniques for low power CMOS VLSI design," in 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), IEEE, 2017, pp. 1759–1763.

[8] B. Padmavathi, B. Geetha, and K. Bhuvaneshwari, "Low power design techniques and implementation strategies adopted in VLSI circuits," in 2017 IEEE International Conference on Power, Control, Signals and Instrumentation.

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