Comparator / Sample and Hold

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October 16, 2024

Abstract

This report is a part of a project of Analog-to-Digital Converter, engineered with Paco DAVID, Toufik CHABI and Andy CLEMENT.

1 Generalities

For all the project, we need to set some parameters due to the utilisation of the product.

To use the product, we need to be in a dry room at around 25 °C or 77°F. The frequency of the clock is 115,2 MHz.

2 Comparator

In this part, we would like to compare 2 analog values. In electronic, to compare 2 analog values, we use a comparator.

The role of the comparator is to compare 2 analog values, in this case, V_{in} (output voltage of the Sample and Hold) and V_{R2R} (output voltage of the resistor networks). See below for more details about Sample and Hold. The model used is LM311N. Check reference to find the datasheet.

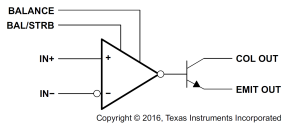

Figure 1: Simplified Schematic LM311N

LM311N is operational amplifier. It works in reverse to a conventional op amp.

This op amp is followed by a bipolar junction transistor (BJT). We use a BJT NPN. It's a transistor made of silicon. Two cases possible : If $V_{\text{BE}} < 0.6V$, there is not current in emitter and collector and the transistor is blocked. If $V_{\text{BE}} > 0.6V$, there is current in emitter and collector (multiplied by the gain of op amp). In this case, the voltage of the collector is V_{CE}.

In our system, IN_+ represents the output voltage of Sample and Hold (SH) and IN_- is the output voltage of the R2R system.

If $V_{\text{SH}} > V_{R2R}$ op amp out is $-V_{\text{CC}}$. So, we have $-V_{\text{CC}} < V_{\text{BE}}\,(0.6V)$ and the transistor is blocked. $V_{\text{COMP}} = 5\text{V}$ and we have a logic 1. That's the same process for $V_{\text{SH}} < V_{R2R}$: If $V_{\text{R2R}} > V_{SH}$ op amp out is V_{CC}. So, we have $V_{\text{CC}} > V_{\text{BE}}\,(0.6V)$ and the current flow through emitter, current flow through collector (multiplied by gain of the transistor). $V_{\text{COMP}} = 0\text{V}$ and we have a logic 0.

In either case, V_{COMP} will be the input of the logical system.

At a temperature T_{A}= 25°C or 77°F, the voltage between the emitter and the collector must not exceed 0,8V otherwise, the logical system can have some errors. To fix this problem, the current between collector and emitter must be 8 mA. We connect a resistor between collector and $V_{\text{CC}} = 5V$ and his value is 575Ω. According to the E12 Series of standard resistor values, we use R=680Ω.

3 Sample and Hold

3.1 Concept of Sample and Hold

In our project, we need to compare a constant value with a bit value (fixed with R2R part). To get and obtain a permanent value, we use a Sample and Hold. To keep this permanent value during a short fixed time, we use a capacity.

3.2 Timetable of Sample and Hold

In the first part, we have compared two values : V_{SH} and V_{R2R}. To compare these two values, we need 9 rising edges. To get the voltage, at one time, we need 1 rising edge. During this rising edge, we must load the capacity at 99,6 percent of the maximum voltage. During the 9 rising edges, we must maintain the voltage of the capacity.

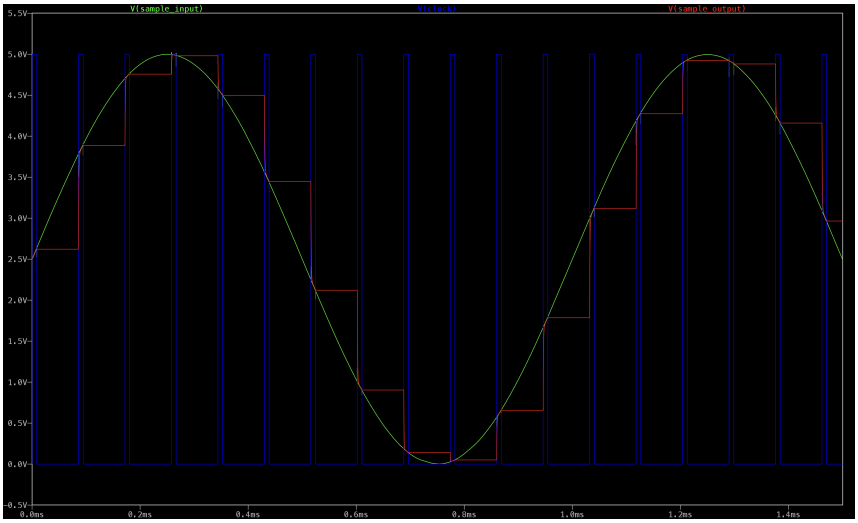

Figure 2: Timetable of Sample and Hold

Keys :
- Green signal : Sinusoidal voltage. Can be a microphone signal.
- Blue signal : Square signal. Each rising edge of the signal is used to operate the Sample. When the signal is equal to 0V, you have 9 other rising edges of the clock.
- Red Signal : Sampled Voltage. That's the same voltage during 1 period of the blue signal. At each rising edge, red signal recopies the voltage value of the green signal.

3.3 Diagram of Sample and Hold

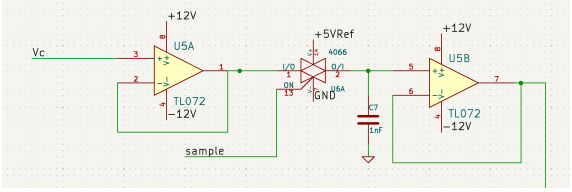

Figure 3: Diagram of Sample and Hold. KiCad Diagram

Keys :
- V_{C} corresponds to the green signal : sinusoidal voltage.
- Sample is the blue signal : square signal.

The output of the last TL072 is one of the input of the comparator, viewed earlier.

3.4 Rules of TL072

TL072 is an aop op. His rule is to maintain the same voltage in output as the input $V_{\mathrm{E}} < V_{\mathrm{BE}}$ $(0.6V)$. Moreover, the input resistance of the circuit is infinite and the output resistance is 0

: no current flows into the component and $I_+ = I_- = 0$. That's our goal.

We use this component because we want to maintain the same voltage in the capacitor as the voltage simulator.

For more information about TL072, let's check the reference at the end of the document.

3.5 Rules of CD4066

The CD4066 CMOS is a quad bilateral witch intended for the transmission or multiplexing of analog or digital signals. The CD4066 device consists of four bilateral switches, each with independent controls. In our case, we need only one bilateral switch.

When CONTROL input is activated (5V analog), CD4066 is equivalent to a wire. Current can flows into the capacity. When CONTROL input is inactivated (0V analog), CD4066 is equivalent to a switch. Current can't flows into the capacity.

The component contains an on-state resistance (R_{ON}). Thanks to the reference, with $V_{\mathrm{DD}} = 5V$ and T_{A}= 25°C or 77°F, the typical value is 470Ω and the critical value is 1050Ω.

For more information about CD4066, let's check the reference at the end of the document.

When the switch is open, the output voltage is the voltage held on the input capacitor. Then, when the switch is closed, the output voltage follows the input voltage thanks to the capacitor. The capacitor cannot reach a specific value immediately. That's why we need to achieve the correct value.

3.6 Determination of capacity value

The precision of the value in R2R is 0.4 percent. We must conserve this precision for the rest of components.

When we have a specific rising edge, we must load the capacity at 99,6 percent of the maximum voltage. For the load of the capacity (same approach for the discharge), we use the formula : $Q(t) = Q_{\max}\left(1 - e^{-\frac{t}{\tau}}\right)$

We find $t = 5,521\tau$. To simply the following calculation, we round up the total to the nearest unit : $t = 6\tau$. Reminder : $f_{\mathrm{clock}} = 115,2kHz$. We can write : $T_{\mathrm{clock}} = \frac{1}{f_{\mathrm{clock}}} \approx 8,6\mu s$ and $T_{\mathrm{clock}} = 6\tau = 6RC$ Then, $C = \frac{8,6\mu s}{6*1050} \approx 1,37nF$.

Thus, we decide to use a capacity of $1nF$ to keep the precision of 0.4 percent. Thanks to Spice, we can see the red signal follows the green signal after half of period.

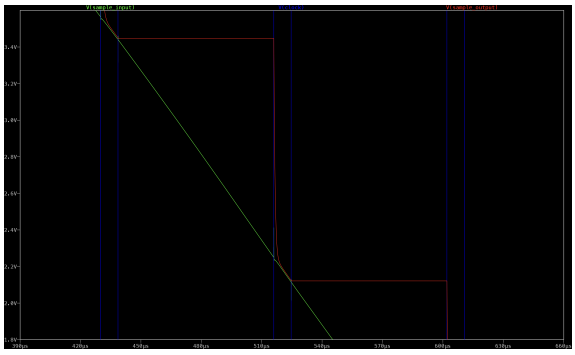

Figure 4: Focus of sinusoidal signal

3.7 Credits

Thank you for all the knowledge and supports for this project :
- Francois JACOB
- Frederic JUAN

3.8 Datasheets

LM311 datasheet : https://www.ti.com/lit/ds/symlink/lm311.pdf
CD4066B datasheet : https://www.ti.com/lit/ds/symlink/cd4066b.pdf
TL072 datasheet : https://www.ti.com/lit/ds/symlink/tl072.pdf