

Literature Review #1: A review of magnetic random-access memory technologies and their feasibility for energy-efficient, datacenter-focused applications.

As of 2025, datacenters consume 1.5% of global electricity, a figure projected to double or triple by 2030, driven by interest in generative AI. This exponential growth stems from the computational demands of large language models and generative AI systems, intensified by competitive pressures among technology companies to achieve AI supremacy. And, while datacenters are built all over the world as long as there is cheap land and good connectivity, this is an especially pressing issue in the United States, where these trends, federal policies prioritizing domestic semiconductor manufacturing and AI competitiveness have incentivized rapid datacenter expansion, often prioritizing speed-to-market over green solutions, placing strain on aging utilities infrastructure and entrenching the cheapest available energy production sources. Given these entrenched economic and policy drivers, addressing datacenter energy consumption requires fundamental advances in hardware efficiency rather than relying solely on grid modernization or building optimization.

Heat dissipation represents the primary constraint on datacenter efficiency and performance scaling. While thermal management poses minor inconveniences for consumer devices, it becomes a critical bottleneck at datacenter scale, where processors operate at maximum load continuously. To put the magnitude of the problem into perspective, datacenters of even a modest size can be 90,000 times computationally powerful than the latest smartphone, so every ounce of lost efficiency matters. Given the ecological concerns shared by many scientists, if more datacenters are to be built, then they must be made cleaner. This thermal wall

coincides with the slowing of Moore's Law scaling, creating what researchers term the 'Beyond-CMOS imperative'—the urgent need for alternative device technologies that can deliver performance improvements without proportional increases in power consumption (Beyond CMOS).

A historically viable alternative to charge-based devices is held by spintronic devices. Spintronic devices, which leverage electron spin as an additional degree of freedom in electronic circuits, have long been a focus on innovation, particularly in data storage technologies such as hard drives. The discovery of giant magnetoresistance in 1988, for which the Nobel Prize would be awarded, would be hugely impactful for bringing large storage sizes to commercial market, kick starting the field of spintronics and bringing gigabyte, and later terabyte sized hard drives to the common person. Furthermore, the discovery of spin-transfer torque, spin-orbit torque, and giant tunneling magnetoresistance would form the basis of magnetic random-access memory (MRAM) technologies, which have been integrated in cache memories for over a decade (Dieny et al.). In the pressing demands for high-speed, high-density, and high-efficiency set forth by datacenters, physicists look towards the integration of MRAM as a solution.

There are multiple application spaces which MRAM has the potential to shine in. The first is on-chip applications, where small, extremely fast MRAM devices would be implemented. This is an extremely important application, as improvements in embedded memory directly improve computing efficiency in two ways. The first is as a replacement for flash memory, responsible primarily for reading and writing operations related to program execution. Second, if one looks into the CPU of their computer, they would also find a few kinds of on-chip caches, designed to be the very fastest memory the computer uses. These are designated L1 to L3, with L1 being the fastest and L3 being the slowest. Unlike other embedded or primary memories, the

CPU cache must remain in use at all times, and pulling data from these can be expensive from a power usage standpoint. L1, at the smallest size, is also the most power-efficient, as L2 and L3 at their larger sizes consume anywhere from 2-5x more power, respectively (Lam).

Indeed, MRAM is already showing viability as a replacement for flash, in the form of spin-transfer torque (STT)-MRAM (Nyugen et al.). STT-MRAM devices are built on magnetic tunnel junctions (MTJs), composed of two magnetic layers separated by a thin gap. One layer works to store the information as a one or a zero, while the other acts as a reference for which the state can be read. In terms of performance, STT-MRAM is three times smaller than conventional flash memory, and is at best able to switch in the few-nanosecond regime (Yang et al.) (Hellenbrand et al.). Recent improvements to switching efficiency and signal-to-noise-ratio have enabled fabs to replace conventional embedded flash memory and static random-access memory with STT-MRAM in high-end electronics. Recent reviews suggest viability in cache applications as well, as new generations of the technology push read-write speeds even lower. Currently, only slow L3 cache is viable at the commercial level due in part to speed demands, but largely due to material endurance.

At the cache level, researchers instead expect spin-orbit torque (SOT)-MRAM to dominate due to the potential to circumvent the aforementioned speed and endurance issues with STT-MRAM (Nyugen et al.). Instead of a MTJ, SOT-MRAM utilizes an in-plane charge current, which injects a spin-polarized current into the ferromagnetic layer via the spin-Hall and/or Rashba-Edelstein effect (Manchon et al.). The construction of SOT-MRAM devices demands the separation of a read and write lane, which effectively reduces device wear by halving the amount of total operations done. Currently, the barrier to commercial implementation lies in material optimization. (something about SHE materials, topological materials)

While cache and flash memory devices pose an important area for improvement, it is actually slower, large scale memory which is responsible for the largest power consumption in terms of read/write operations, albeit they are less frequent. For this purpose, voltage controlled magnetic anisotropy (VCMA)-MRAM is an extremely promising emerging technology. This technique is fundamentally differentiated from the current controlled SOT-MRAM and STT-MRAM. By eliminating this factor, Ohmic energy dissipation, often the predominant inefficiency, may be significantly reduced. VCMA-MRAM devices are therefore highly energy efficient, and have been demonstrated to operate with switching energy of 40 fJ at sub nanosecond speeds (Khalili Amiri et al.).

While memory serves as a critical component to modern day computing, there is an inherent disadvantage in specialized use-cases, such as the training of AI models, in that the physical separation of memory and compute units reduces performance and power-efficiency. Moreover, features such as “non-volatility, stochasticity, and oscillations in MRAM, provide new feasibility for novel computing to solve combinatorial optimization problems, which are notoriously difficult for conventional computers” (Nguyen et al.). Given the emphasis on AI-focused datacenters in the last decade, it is highly desirable, then, to approach the issue of power usage and cooling using these technologies (Shehabi et al.). This unique architectural suitability towards AI workloads positions MRAM technology as a cornerstone to reducing power inefficiency and furthering technological progress.

The commercial success of STT-MRAM in flash memory and solid-state drive applications represents only the beginning of spintronics' transformative potential for datacenter efficiency. As fabrication techniques mature and materials science advances accelerate, next-generation MRAM technologies are poised to revolutionize computing architectures from cache

memory to novel processing paradigms. Recent breakthroughs in achieving room-temperature perpendicular magnetic anisotropy, critical to dense memory architectures, demonstrates that the fundamental materials challenges are yielding to sustained research efforts.

More importantly, the convergence of spintronic devices with AI workloads creates unprecedented opportunities for hardware-software co-optimization. Unlike conventional memory technologies that merely store and retrieve data, spintronic systems offer inherent support for probabilistic computing and combinatorial optimization, precisely the computational primitives driving datacenter growth. As the datacenter industry faces unsustainable energy consumption as a barrier to continued AI advancement, spintronic technologies provide a pathway to transcend traditional performance-power tradeoffs. The question is certainly not whether MRAM technology will transform computing, but how rapidly they can be deployed to alleviate the energy demands of modern computing architecture.

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