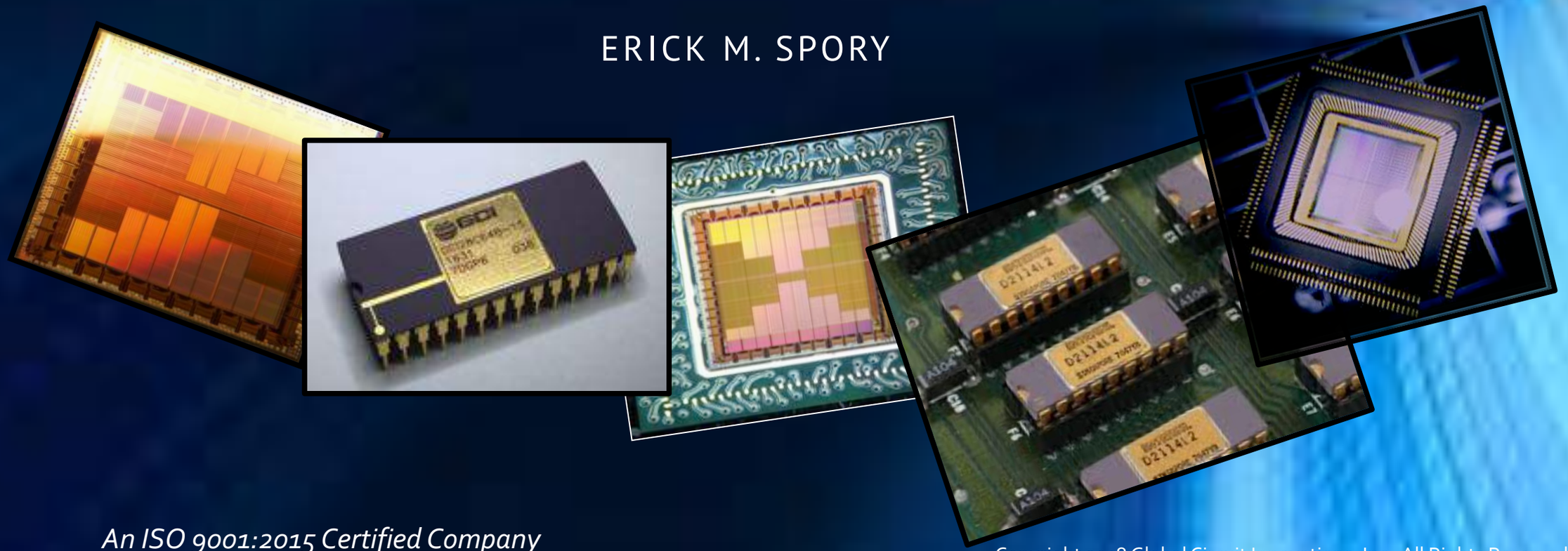
Successful FPGA Obsolescence Form, Fit, and Function Solution Using a MCM and *DER*™ to Implement Original Logic Design

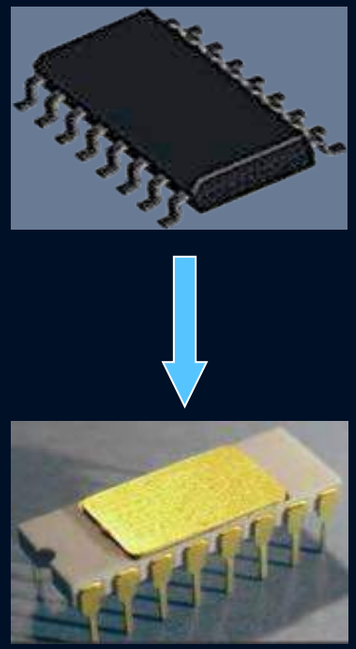
Phoenix, AZ - March 8, 2018

ERICK M. SPORY



An ISO 9001:2015 Certified Company

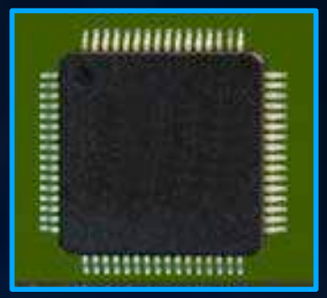
Global Circuit Innovations, Inc.



- **Custom IC Manufacturer Specializing in Custom Packaging and Assembly Options**
- **Patented Die Extraction and Re-Packaging (*DER*™) Technology. Originally Developed to Increase High-Temperature Reliability IC's for the Oil and Gas Industry**
- **This Technology now also used for Military/Commercial Obsolescence Solutions**

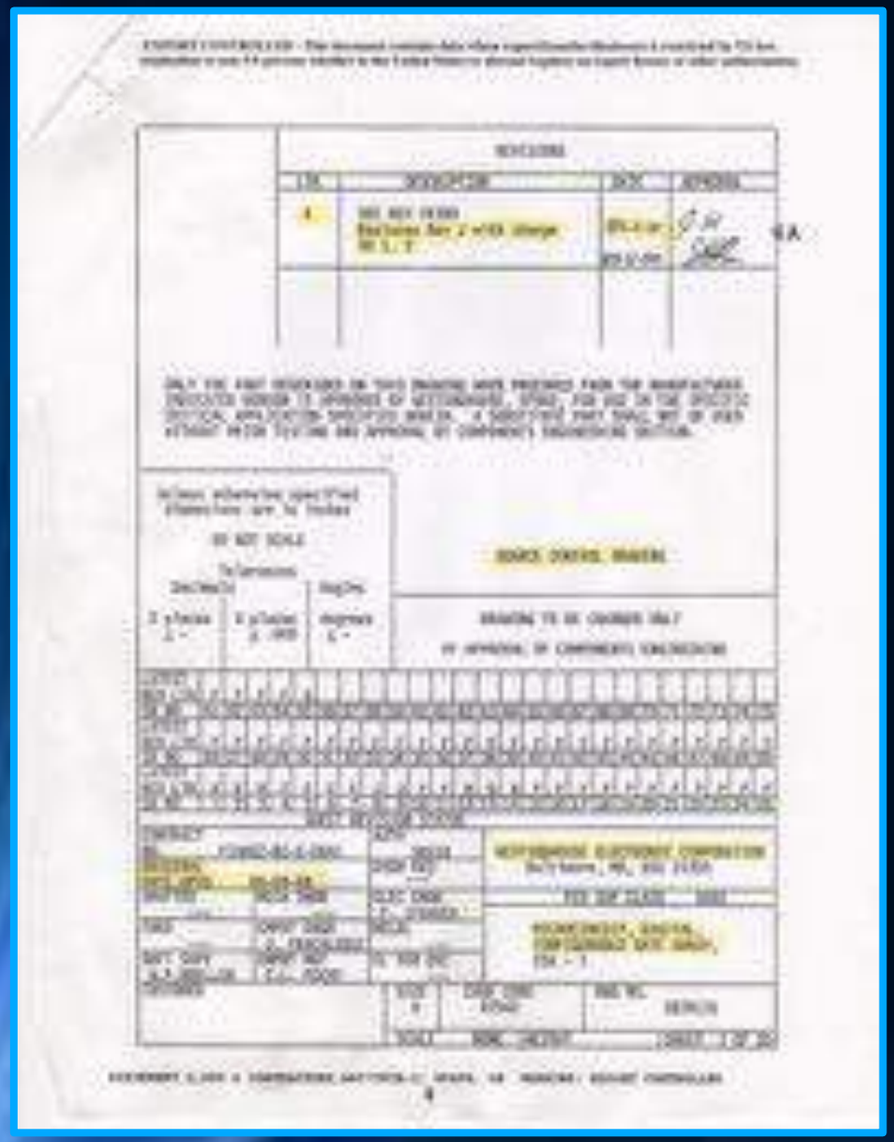
Air Force Rapid Innovation Funding

- RIF 1 (Rapid Innovation Fund) Awarded 2017 - $2.75M Contract to Produce 20+ IC Component Obsolescence Solutions across DoD using GCI's *DER*™ process. FA8615- 17-C-6053 was awarded through the USAF/AFMC/AFLCMC AF LIFE CYCLE Program
- RIF 2 Awarded 2018 - $2.75M Contract to Develop 5 to 10 FPGA Specific Obsolescence Solutions using GCI's *DER*™ process - AFLCMC17-9.e.-P-747
- Target Return on Investment for each RIF is 5:1
  - ~$12M Savings per RIF by Avoiding System Redesigns – Est. ROI to date is ~15:1



RIF1 – Candidate 1 – Identified as a 1800 Gate Bipolar Digital Gate Array Equivalent within a 64 Pin Ceramic Quad Lead Flat-Pack (CQFP) Configuration Emulating 7 Individual Components
Reference: Source Control Drawing (SCD) 587R131

Air Force Rapid Innovation Funding

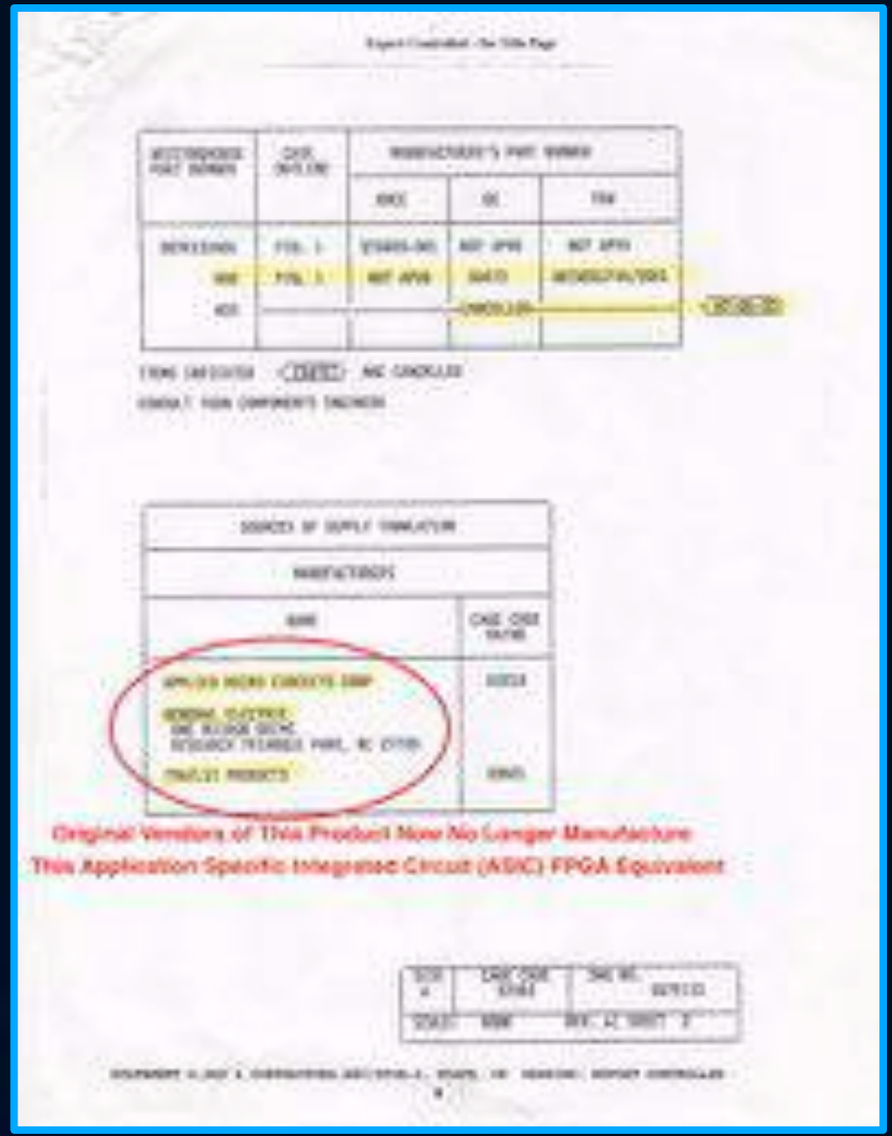


RIF1: Candidate 1
1800 Gate Bipolar FPGA, 64 Pin CQFP Configuration

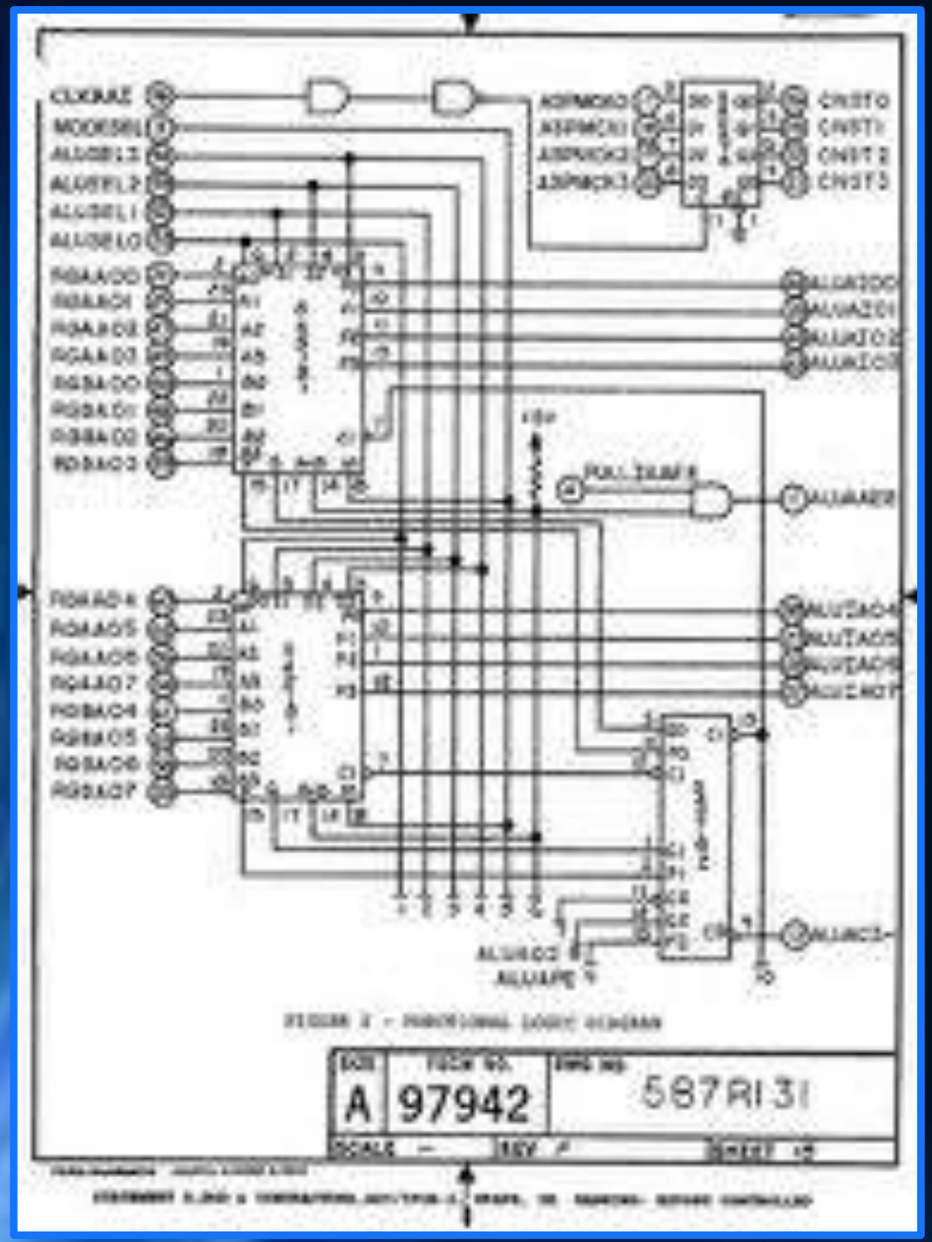
Emulating 7 Individual Components

Reference: Source Control Drawing (SCD) 587R131

Estimated ROI:
10:1 by Avoiding F-16 Radar System ReDesign
or, > $1.8M in Cost Savings

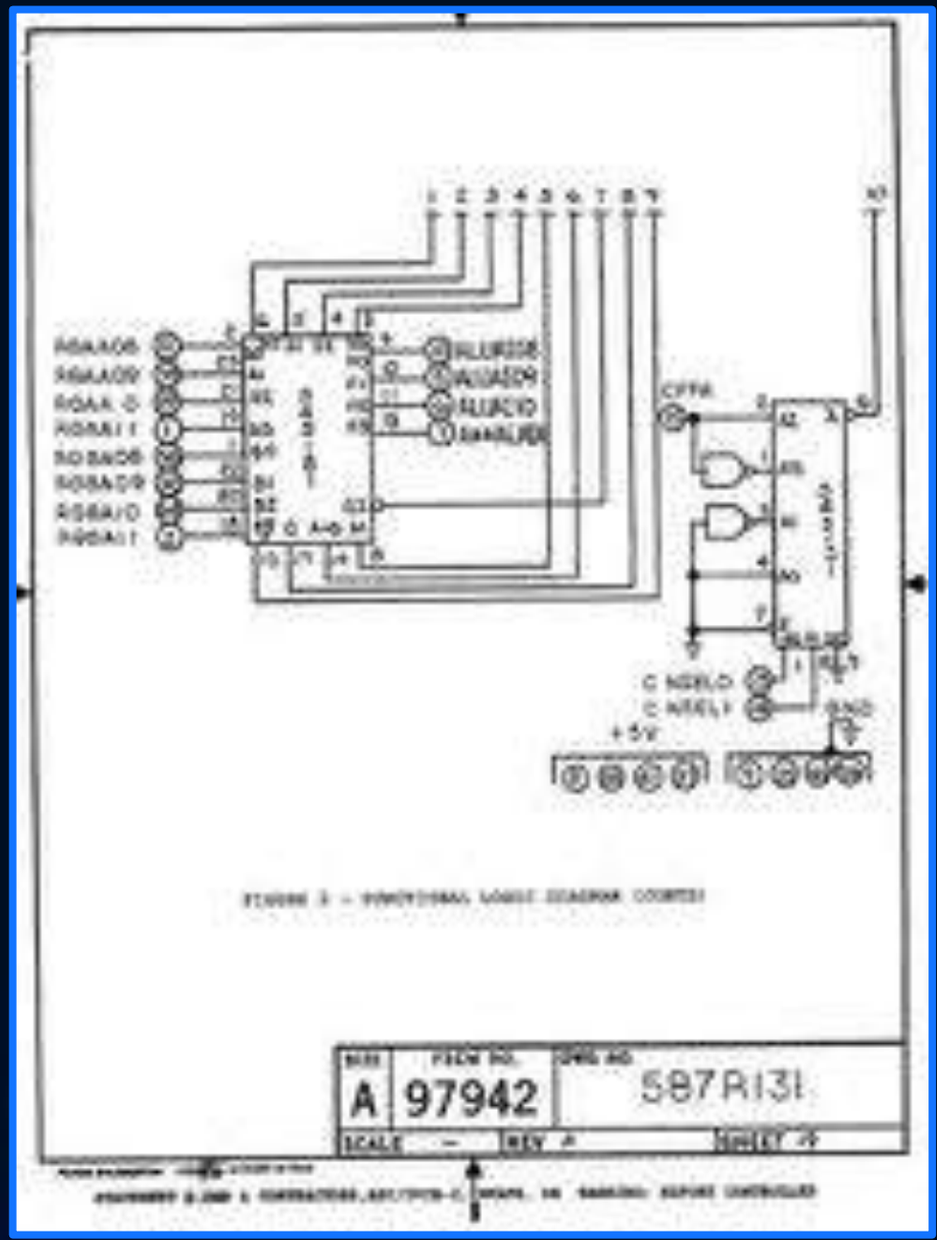


Schematic Equivalent Directly From Original SCD

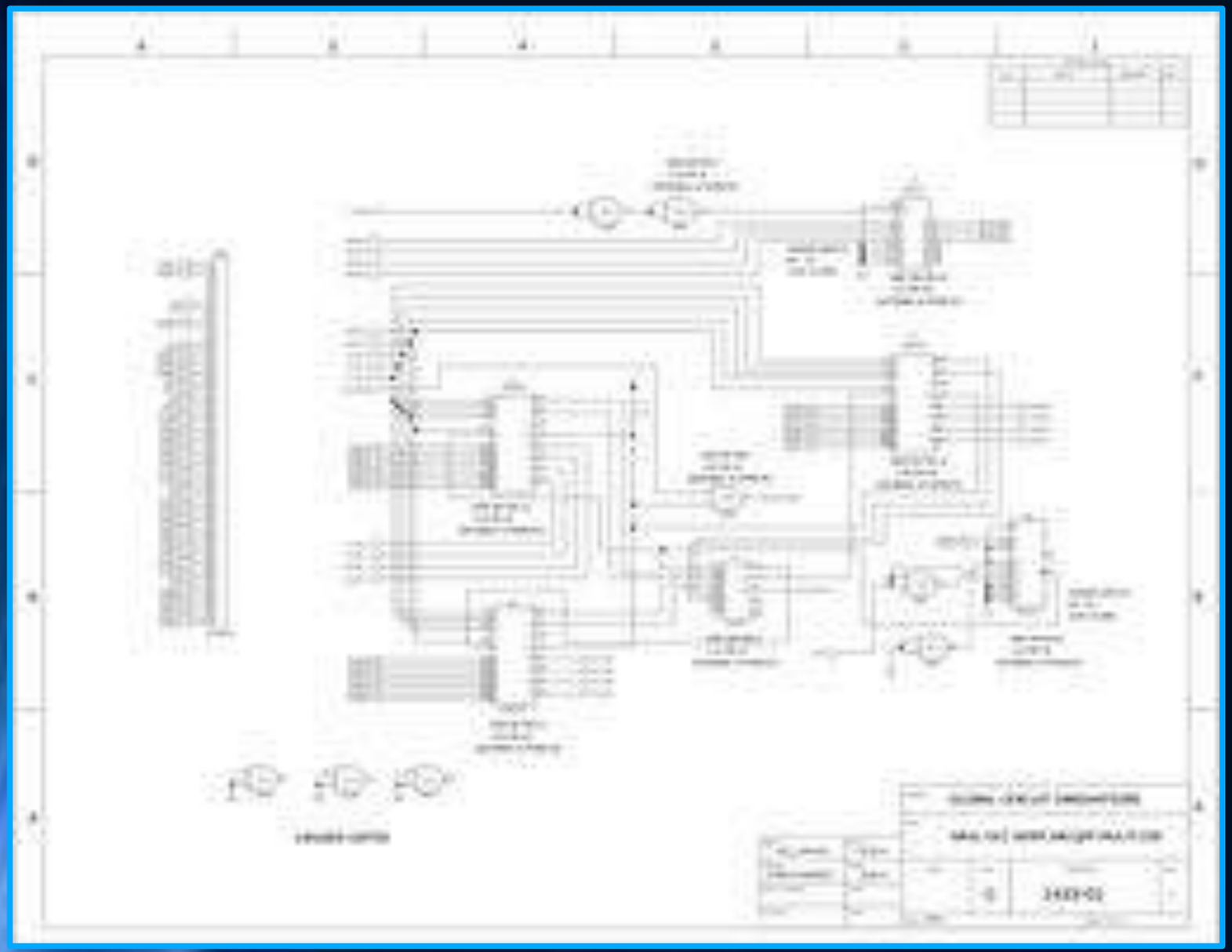


Schematic From Original Source Control Drawing (SCD) for NSN Part#587R131

Supplied by Air Force Depot Hill AFB (Ogden, Utah)



Schematic Reconfigured for MCM Layout



List of all Integrated Circuits for 1800 Digital Gate Array Bipolar Project

3x-54S181 (U1, U2, & U7)

4-Bit Arithmetic Logic Unit (ALU)

1x-54S374 (U3)

Octal D-Type Edge-Triggered Flip-Flop

1x-54S182 (U4)

Carry Lookahead Generator

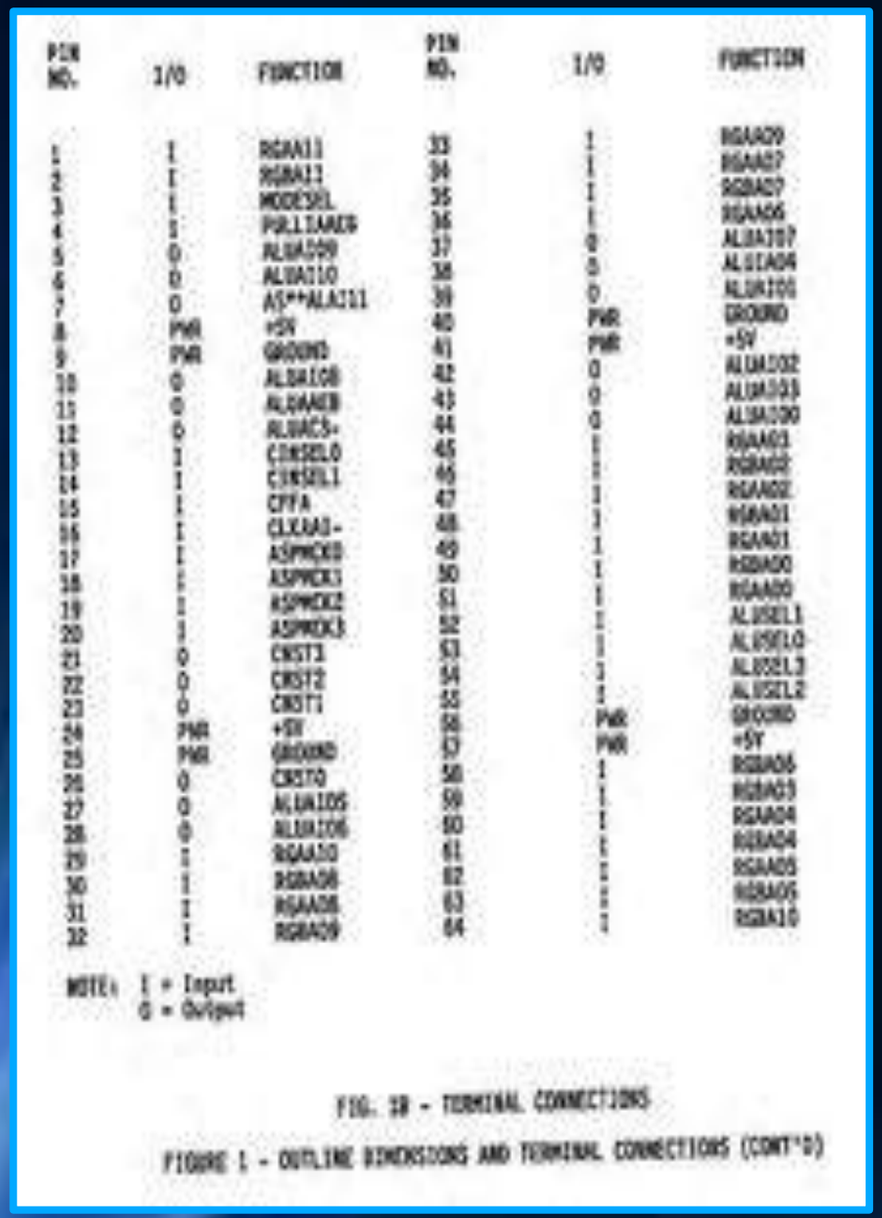
1x-54S08 (U5)

Quad 2-Input AND

1x-54S00 (U6)

Quad 2-Input NAND

Package Signal Requirements and Test Vectors



PIN NO.	I/O	FUNCTION	PIN NO.	I/O	FUNCTION
1	I	RGAA11	33	I	RGAA09
2	I	RGBA13	34	I	RGAA07
3	I	MODESEL	35	I	RGBA07
4	I	PULLAAL0	36	I	RGAA06
5	O	ALUA09	37	O	ALUA107
6	O	ALUA10	38	O	ALUA104
7	O	A5**ALA11	39	O	ALUA101
8	PWR	+5V	40	PWR	GROUND
9	PWR	GROUND	41	PWR	+5V
10	O	ALBA10B	42	O	ALUA102
11	O	ALUAAEB	43	O	ALUA103
12	O	ALUAC5-	44	O	ALUA100
13	I	CINSEL0	45	I	RGAA03
14	I	CINSEL1	46	I	RGBA02
15	I	CFFA	47	I	RGAA02
16	I	CLKAA3-	48	I	RGBA01
17	I	ASPMCK0	49	I	RGAA01
18	I	ASPMCK1	50	I	RGBA00
19	I	ASPMCK2	51	I	RGAA00
20	I	ASPMCK3	52	I	ALUSEL1
21	O	CRST3	53	I	ALUSEL0
22	O	CRST2	54	I	ALUSEL3
23	O	CRST1	55	I	ALUSEL2
24	PWR	+5V	56	PWR	GROUND
25	PWR	GROUND	57	PWR	+5V
26	O	CRST0	58	I	RGBA06
27	O	ALUA105	59	I	RGBA03
28	O	ALUA106	60	I	RGAA04
29	I	RGAA10	61	I	RGBA04
30	I	RGBA08	62	I	RGAA05
31	I	RGAA08	63	I	RGBA05
32	I	RGBA09	64	I	RGBA10

NOTE: I = Input
O = Output

FIG. 1B - TERMINAL CONNECTIONS

FIGURE 1 - OUTLINE DIMENSIONS AND TERMINAL CONNECTIONS (CONT'D)

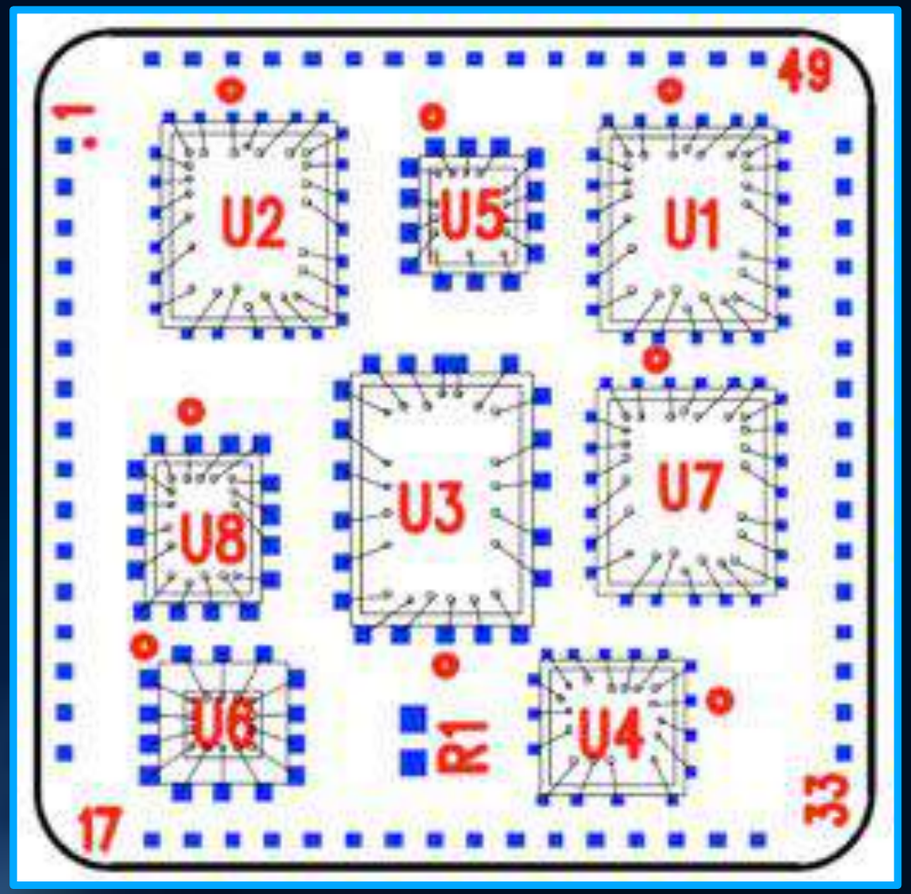
Signal Names
vs.
Pin Numbers
for all 64 Pins
(Left)

Portion of 664
Line Vector Set
Used for Design
Verification,
Simulation, and
Final Test
(Right)

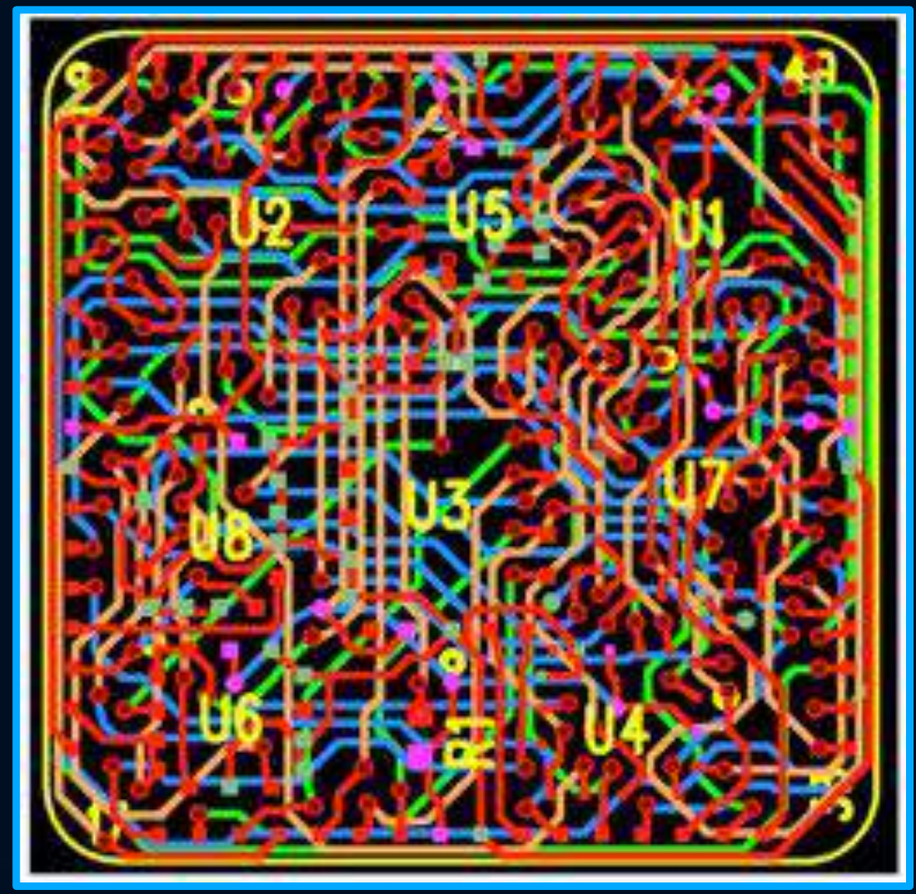
FIGURE 3 - FUNCTIONAL TEST VECTORS (SIMULATION)

IC Layout and Required Routing – 4 Layer Board

A.



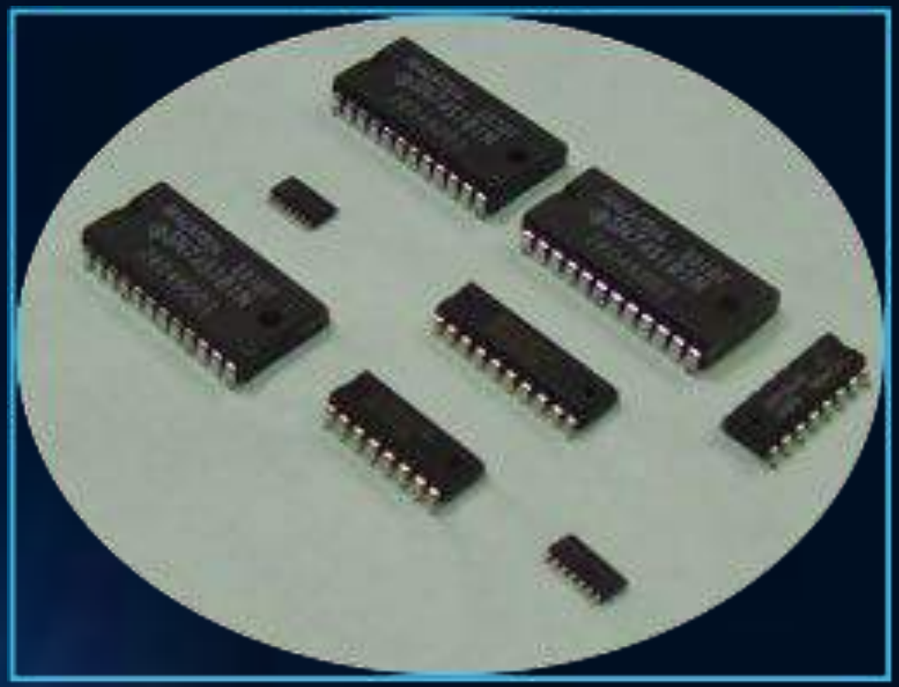
B.

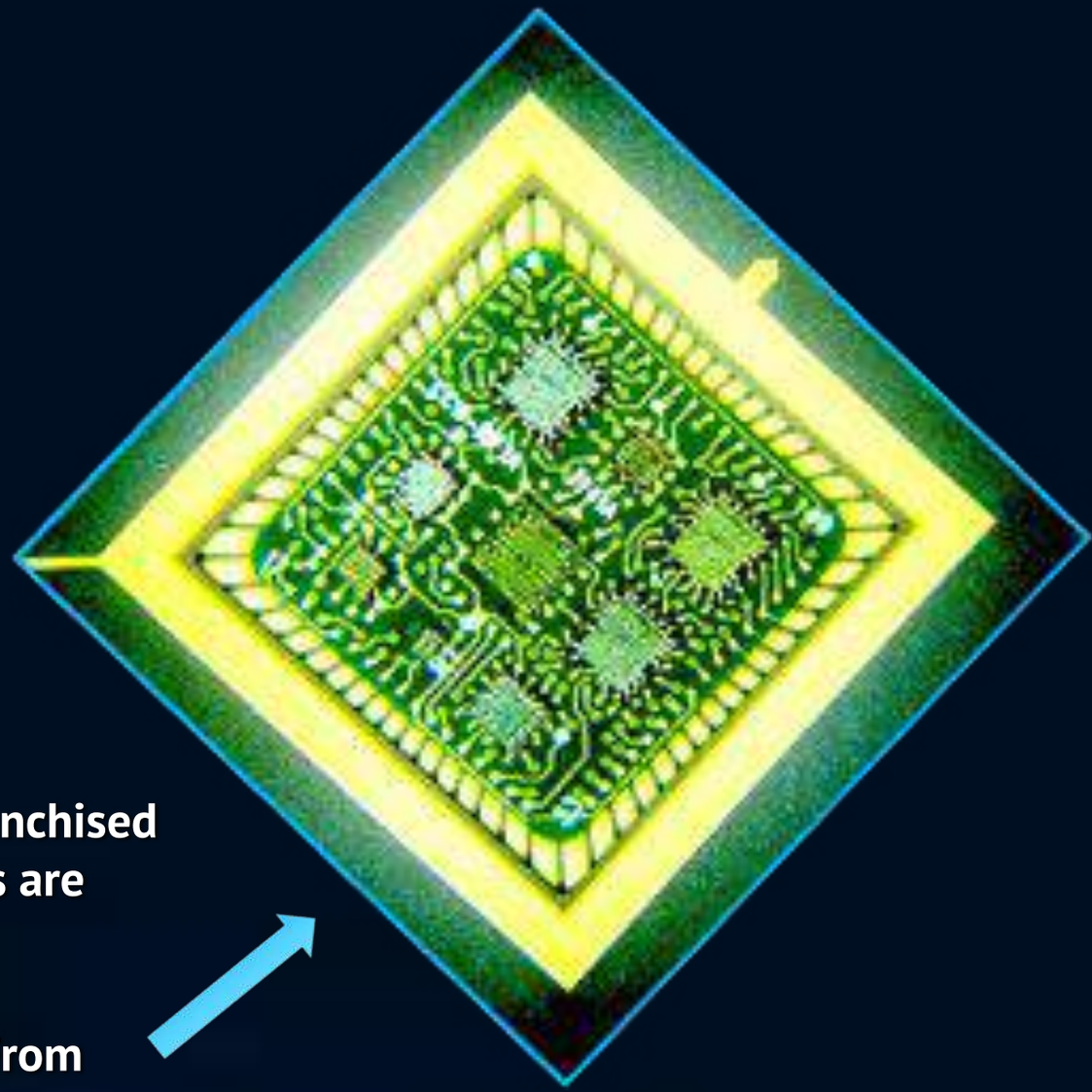


A. Internal Cavity Interposer is Designed for Manufacturability, Bondability/Placement of All Required Die Referenced in Original and New Schematics

B. Signal Routing Requires 4 Layers to Accomplish Proper Connectivity and Peripheral Signal Location for Perimeter Bonding To Package Substrate

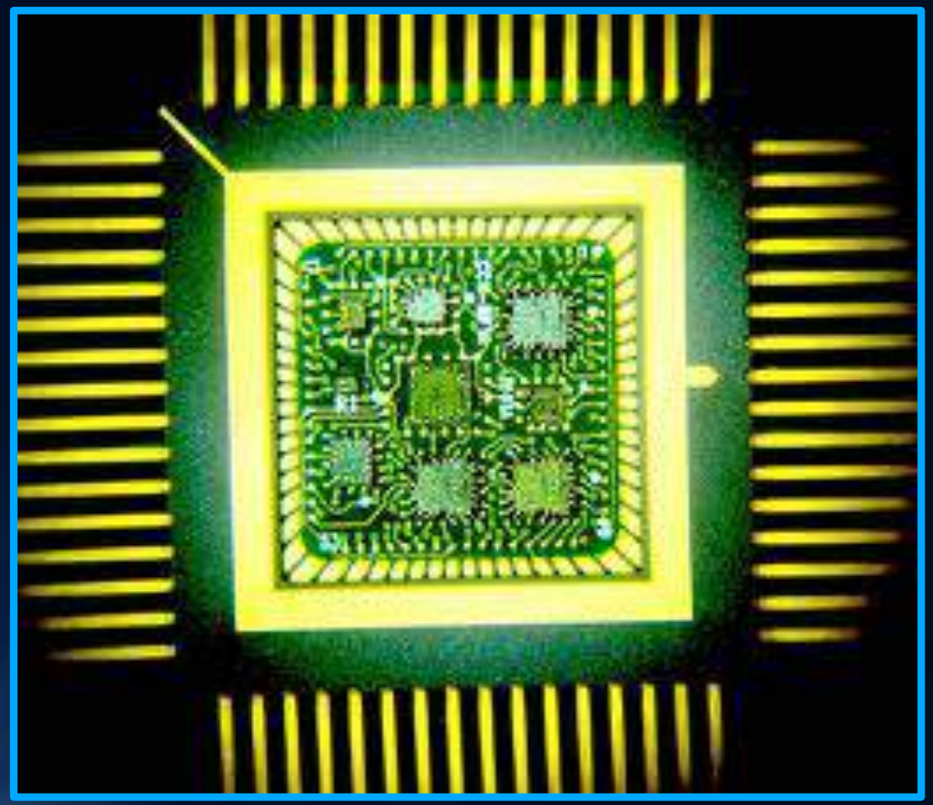
Final MCM Manufactured From Extracted Die

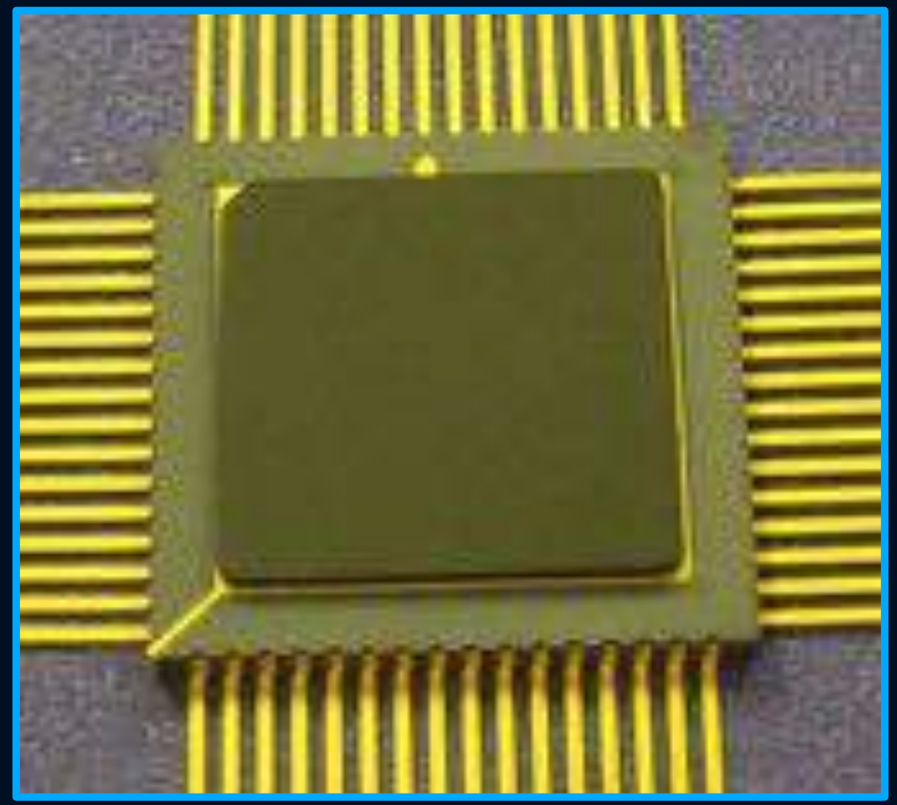




- Plastic Components (above) Represent Actual Franchised Donor IC's used in Final MCM (Plastic Components are Positioned Identically to Bare Die seen to Right)
- Final Multi-Chip Module (MCM) is Manufactured From Extracted Die using GCI's *DER*™ Process.

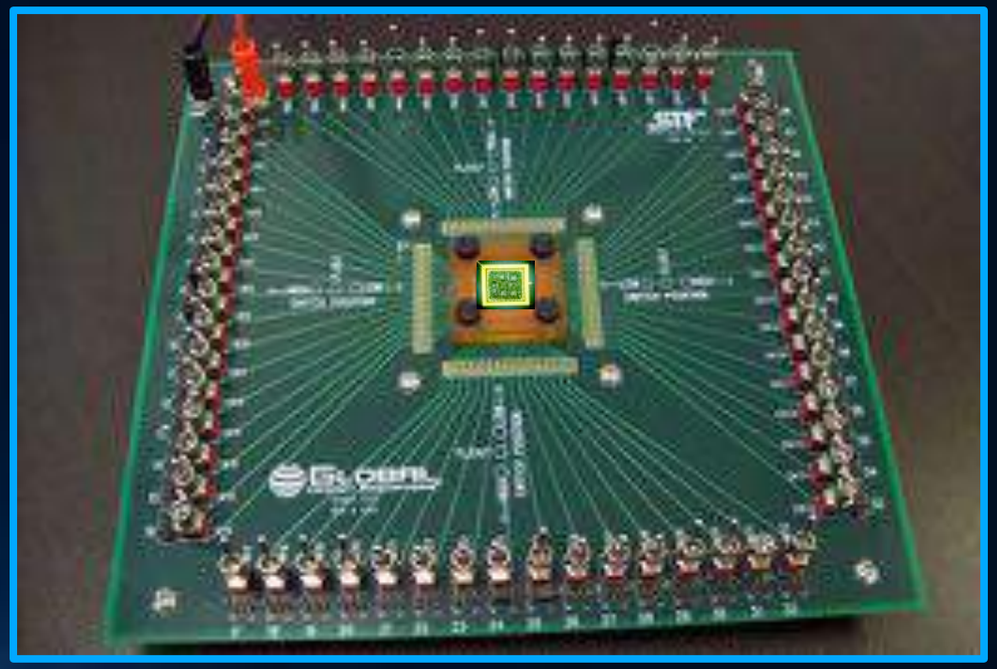
Final Digital MCM Gate Array in Required 64 Pin CQFP

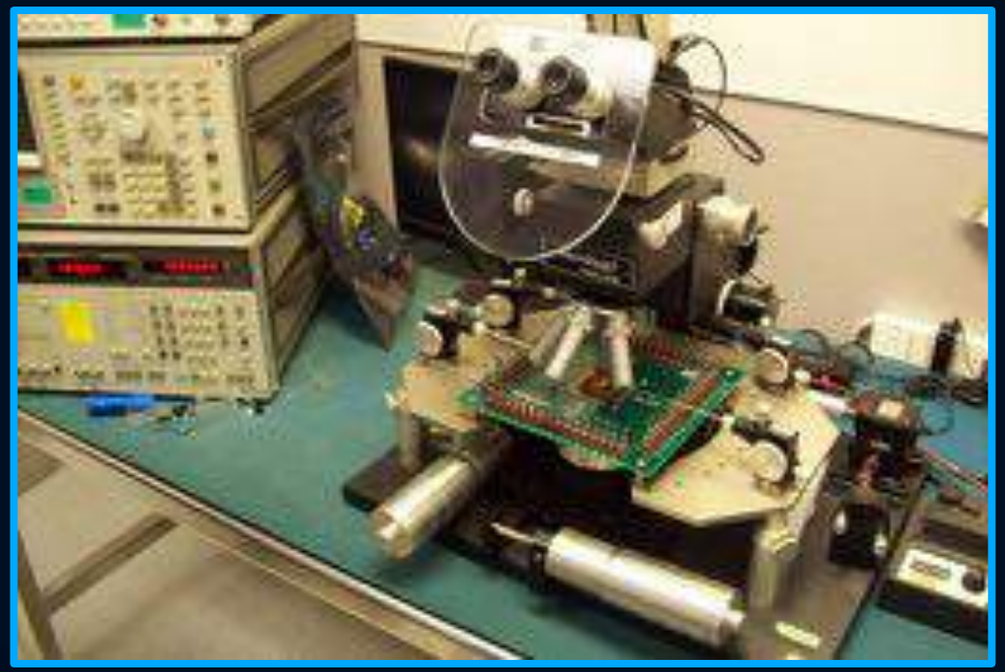




- Final Internal MCM Product Now Emulates Original 64-Pin CQFP Monolithic ASIC
- Device is Ready for Test

In-House Testing and Troubleshooting of MCM

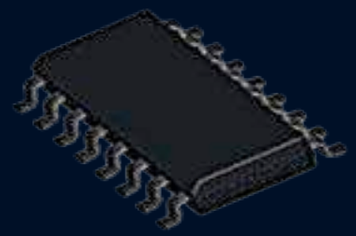




- Test Board and Socket (left) for Manual Input of the Test Vectors Was Designed and Manufactured for Trouble Shooting the Multi-Chip Module
- Test Board was Sized to Fit on the Probe Station (right) for Internal Cavity Probing. No Design Errors Encountered. Only Issues Found Related to Non-Optimized Bonding Process Given Die Proximity

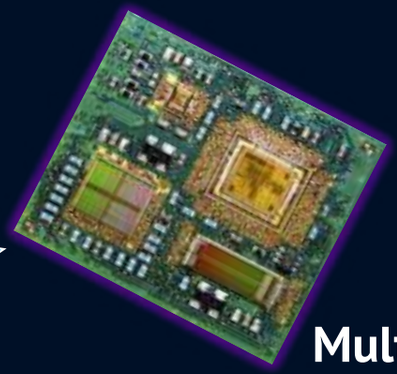
DER™ : Die Extraction And Re-Assembly

If one Package Footprint is Obsolete, but the Die can still be Located in Another Package Footprint, or the Die is in an Undesirable Package, the Die can be Extracted and Re-assembled into the Desired Footprint (*DER*™)

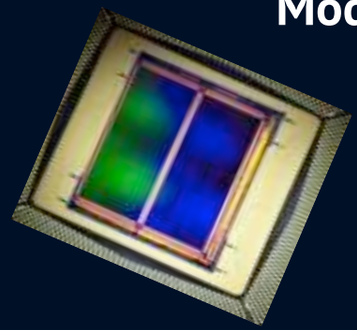


Donor IC Device

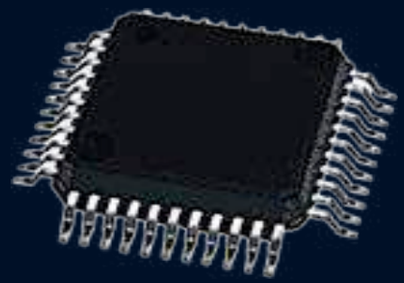
Extracted Die



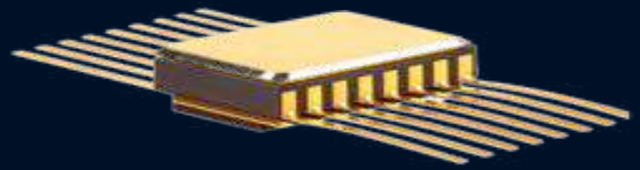
Multi-Chip Module



Ceramic CQFP

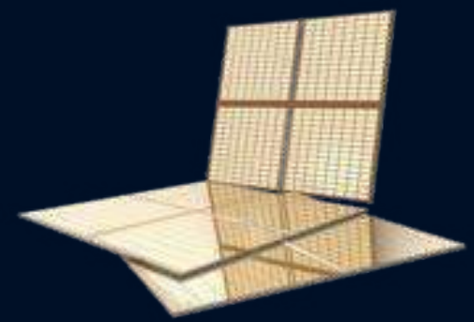


Plastic PQFP



Ceramic Flatpack

Or the *DER*™ Process Can be Used to Inventory Functional Die

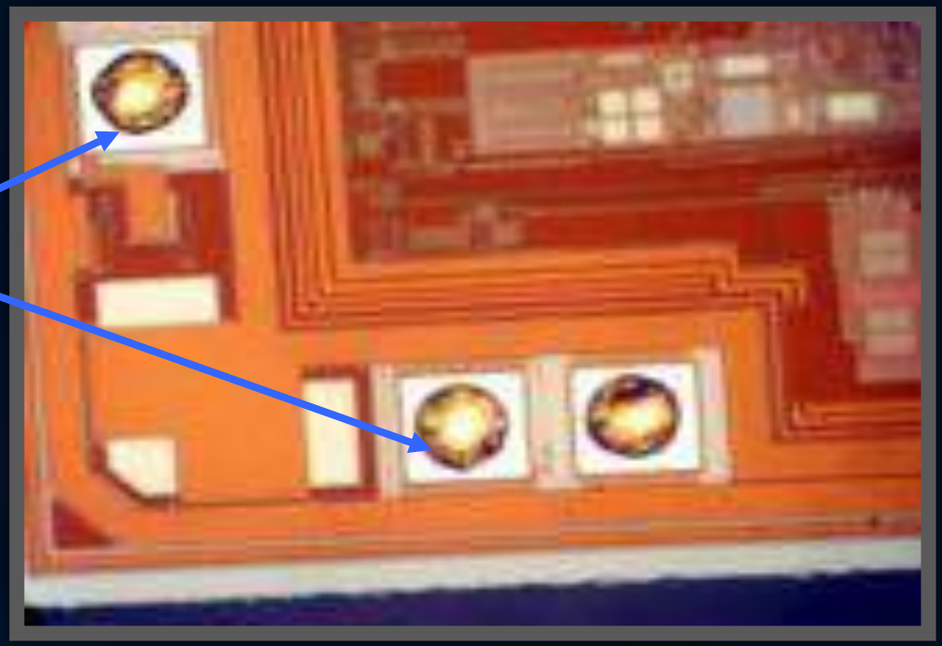


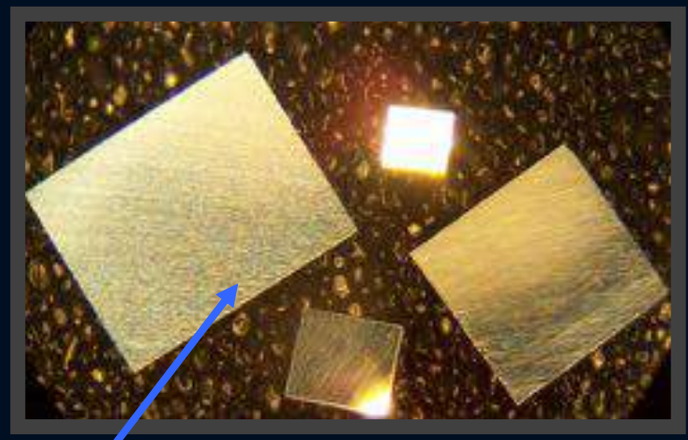
GCI's *DER*™ Technology Up Close

- GCI's Extraction Technology Provides Extremely Clean Front-Side and Back-Side Surfaces
- *DER*™ Relies on Chemical and Mechanical Processes Which Are No More Aggressive Than Those Used During Wafer Fabrication

No Inadvertent Etching of Bond Pads

Die Surface Free of Contaminants

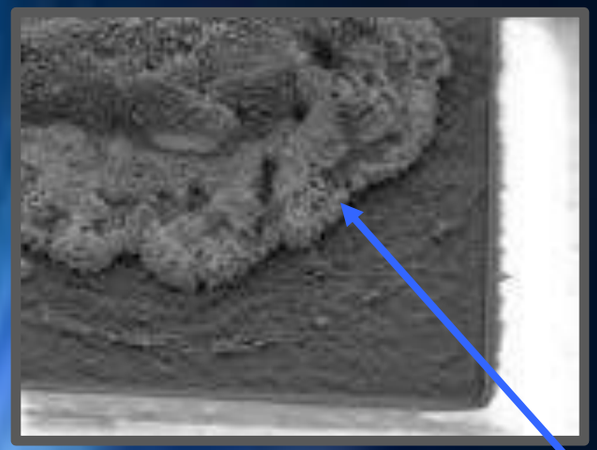




Die Back-Side Surface Free of Contaminants and Returned to Original Mirror Finish

GCI's ***DEER™*** Process Improvements

- Pad Re-Conditioning Using Gold Ball Removal Followed by ***ENEPIG*** (*Electroless Nickel, Electroless Palladium, Immersion Gold*) Plating
  - Potential Original Poor Ball Bond Quality/Reliability is Removed
  - Subsequent Bonding is Non-Compound with Highly Consistent and Reliable Bond Pull Strength
  - New Bond Pad Surface ***Eliminates*** Possibility of Kirkendall Voiding with Gold Bond Wire at Operating Temperatures Above 150° C



General Appearance of Kirkendall or Horsting Voiding at Bond Pad Location

Specifically, at Gold Ball to Aluminum Bond Pad Interface, the following Intermetallic Compounds can be formed:

Au_5Al_2, Au_4Al, Au_2Al, $AuAl_2$

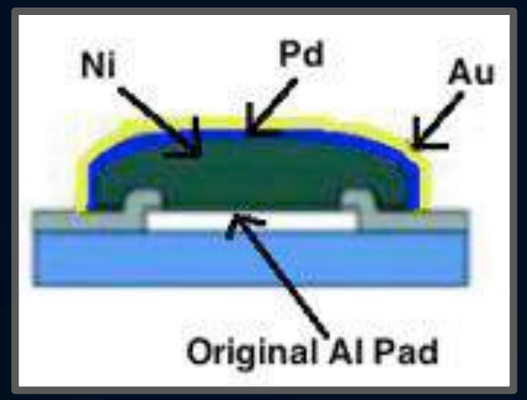
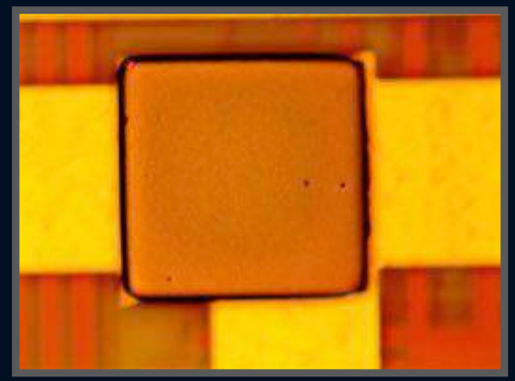
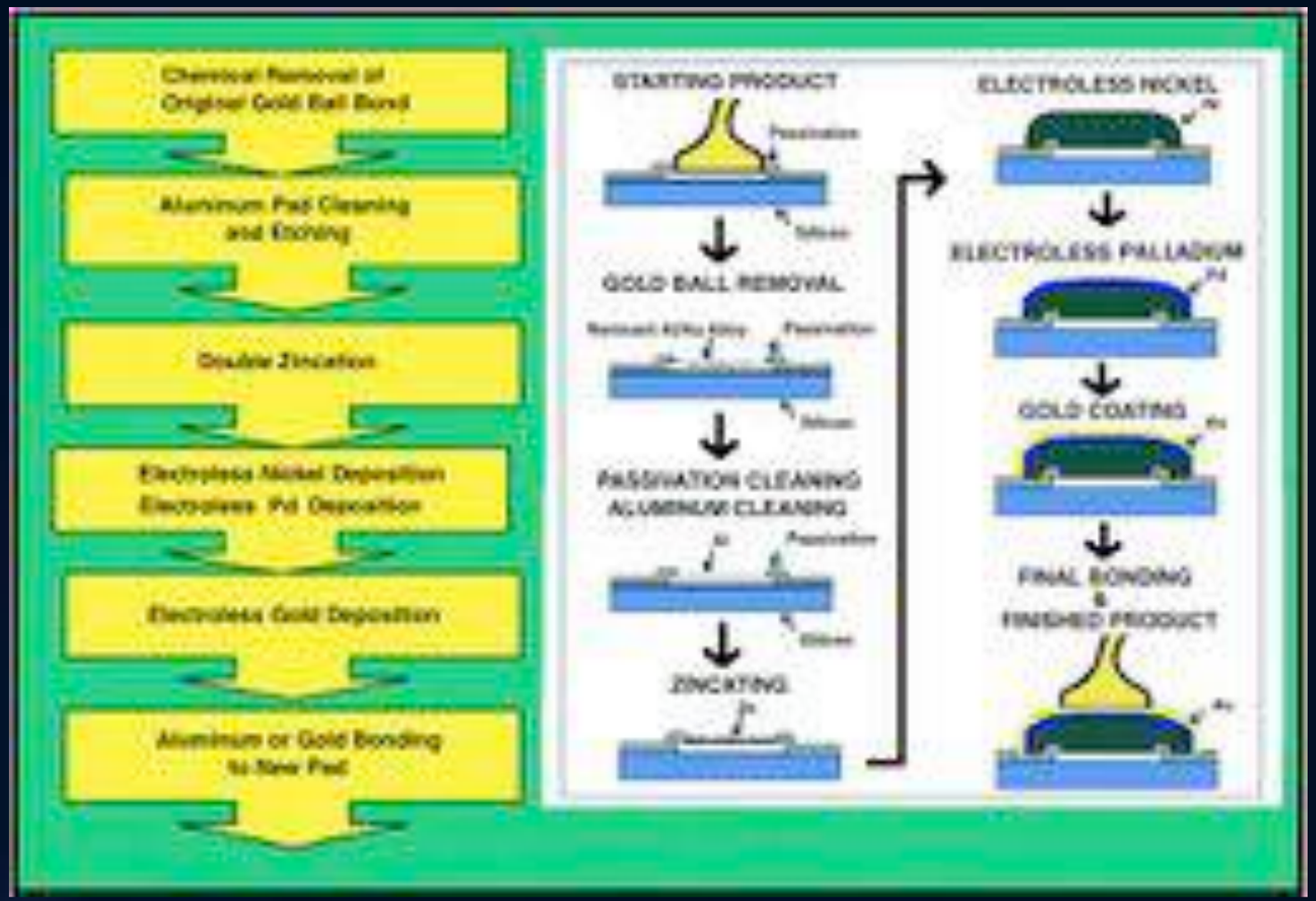


Illustration of *ENEPIG* Pad Plating



Optical Photo of Actual *ENEPIG* Plated Die Pad

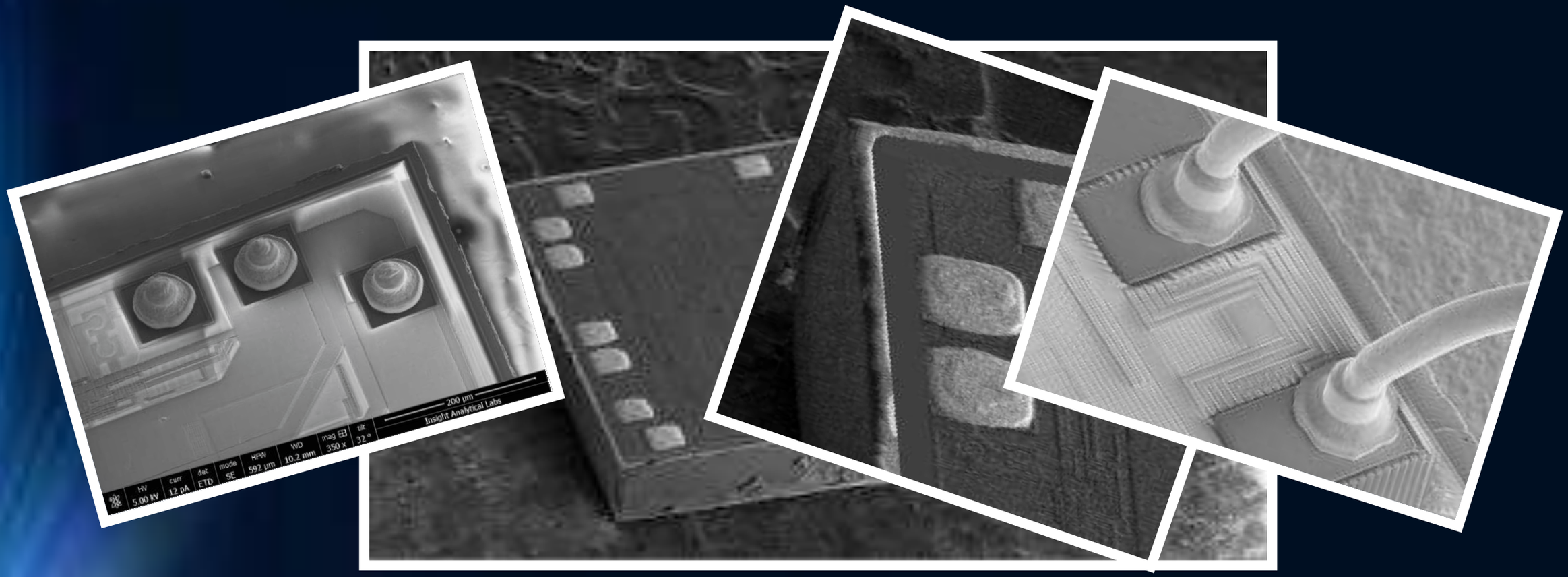
Pad Re-Plating (*DEER*™) – High-Temp Applications



Process Flow for Pad Re-Conditioning Following Extraction

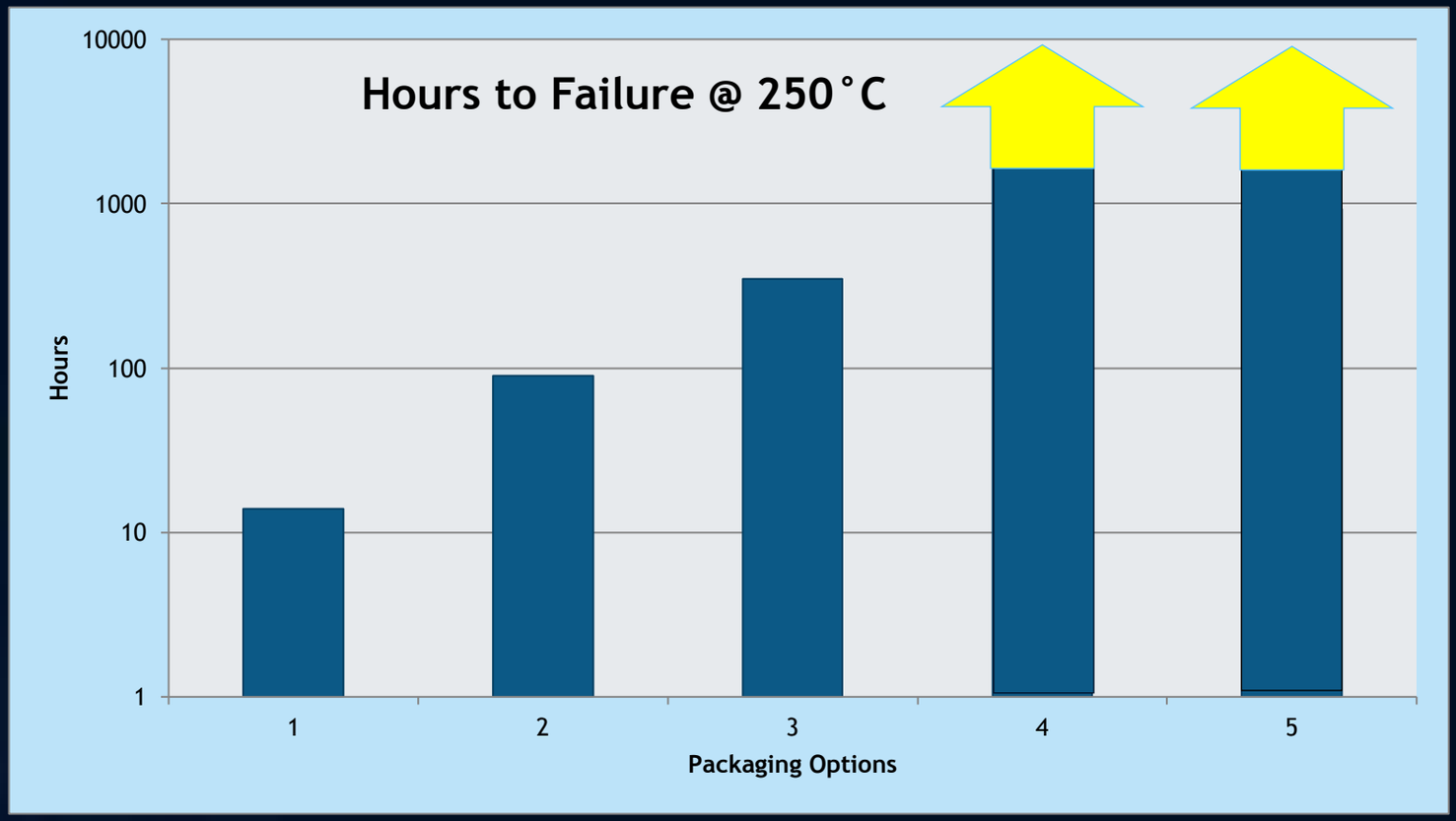
Targeted Thicknesses: 4 µm Ni, 0.25 µm Pd, 0.04 µm Au

DEER™ Gold Ball Removal, Pad Re-Plating with Electroless Ni/Pd/Au Process (***ENEPIG***)



Aluminum Pad Reconditioning for an Extracted Die (Target Total Plate Up is 4 – 5 µm)

Ni/Pd/Au Pad ***DEER***™ Re-Plating Performance at 250°C



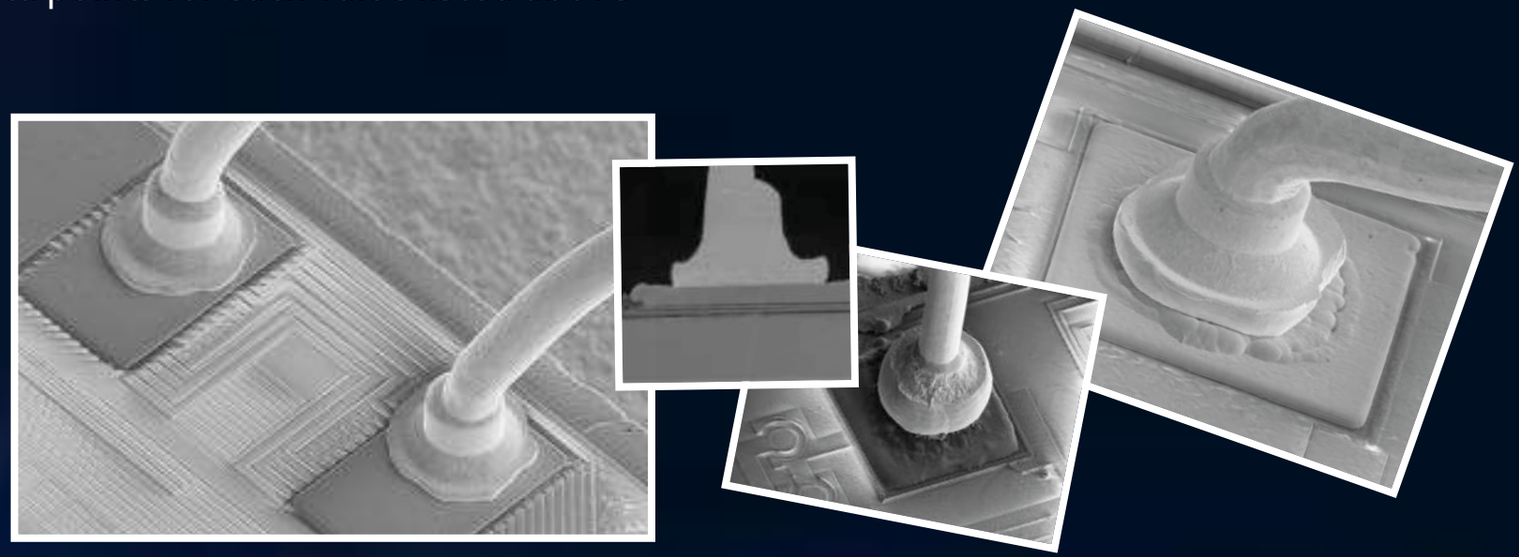
Packaging Option Key:

1 – Standard Plastic (25h)
2 – Extraction, Standard Ceramic Assembly (*DER*™) (95h)
3 – Extraction, Hi-Temp Ceramic Assembly (*DER*™) (600h)
4 – Extraction, Ni/Pd/Au Process, Standard Ceramic Assembly (*DEER*™) (+2500h)
5 – Extraction, Ni/Pd/Au Process, Hi-Temp Ceramic Assembly (*DEER*™) (+6000h)

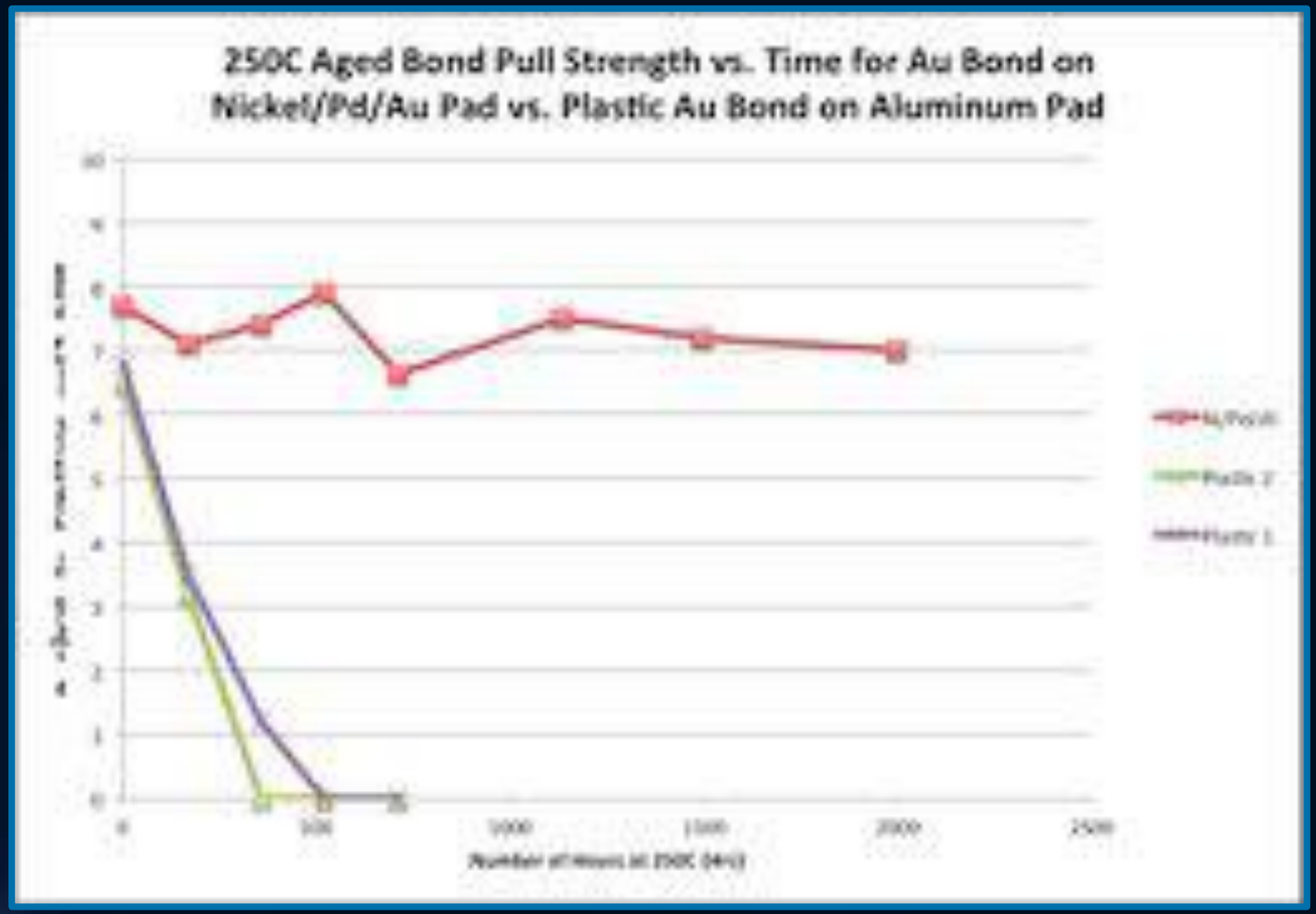
Ni/Pd/Au Pad ***DEER***™ Performance at 250° C

	Avg. Bond Pull Strength	Std. Dev.	Mean-3 SD	Plastic Mean Control
Device as Received:	7.154g	1.03g	4.06g	
Device After Pad Re-Conditioning:				
T= 0 Hr	13.302g	1.52g	8.74g	6.8g
T= 168 Hr (250°C)	12.650g	1.26g	8.89g	3.2g
T= 1000 Hr (250°C)	11.540g	0.90g	8.50g	1.0g
T= 2000 Hr (250°C)	10.913g	0.76g	8.65g	0.0g

Data reflects 16 data points for each value listed above



GCI's Ni/Pd/Au Pad ***DEER***™ Re-Plating Performance at 250° C



Bond Pull Strength vs. Time at 250° C for ***ENEPIG*** Pad Plating

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