LRU, CCA, & IC Microcircuit Obsolescence Solutions without System Redesign

SESSION: PARTS MANAGEMENT, DATA, REFRESH
DECEMBER 5, 2018

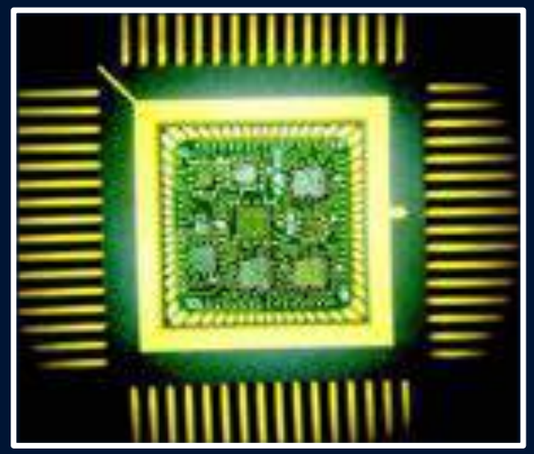
ERICK M. SPORY
GLOBAL CIRCUIT INNOVATIONS, INC.
COLORADO SPRINGS, CO USA
ERICK.SPORY@GCI-GLOBAL.COM
+1 (719) 649-0947

An ISO 9001:2015 Certified Company

AGENDA

- Introduction to Global Circuit Innovations
- Authorized Reverse Engineering Solutions for Integrated Circuits (ICs) & Next Higher Assemblies (NHAs) such as Circuit Card Assemblies (CCAs), and Line Replacement Units (LRUs) to Address Electronics Obsolescence
- GCI's Goal: Form, Fit, and Function (FFF) Replacement Design and Manufacturing to Meet or Exceed Source Control Drawings (SCDs) for Commercial Authorized Replacements (at LRU, CCA, and IC Level)
- GCI's Tools: Bill of Materials (BOM) Scrubbing, Printed Circuit Board (PCB) Design/Layout and Re-Engineering, IC Design and Manufacturing (*DER*™ and *DEER*™ Processing)
- Questions and Answers

Global Circuit Innovations, Inc.



- Solutions-Based, Custom IC Manufacturer Specializing in Packaging/Assembly Options
- Authorized Re-Manufacturer of Integrated Circuits (ICs) and Circuit Card Assemblies (CCAs)
- Patented Die Extraction and Re-Packaging (*DER*™ *& DEER*™) Technologies were Originally Developed to Increase High-Temperature Reliability of IC's for the Oil and Gas Industry
- *DER*™ and *DEER*™ now Leveraged for Military/Commercial Obsolescence Solutions

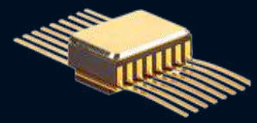
GCI Methods for CCA/IC Obsolescence Solutions

- Commercial Solutions using Engineering and Manufacturing of CCAs and Multi-Chip Modules (MCMs) with Source Control Drawings (SCDs)
- Authorized Reverse Engineering Solutions for Integrated Circuits (ICs), Circuit Card Assemblies (CCAs), and Line Replacement Units (LRUs)
- Successful Chip-Scale CCA Case Studies of a Gate Array IC Equivalent, a FPGA Based CCA, and a Power Amplifier Solution Involving Several Dozen Individual IC and Passive Components
- This Engineering Approach can be Readily Applied to a Wide Variety of other Obsolete CCAs to Generate Functional, Highly-Reliable, Drop-In Replacement Solutions (FFF)

LRU/CCA/IC Obsolescence Flow Chart

Line Replacement Unit (LRU)

Circuit Card Assembly (CCA)



Microcircuit (IC)

Is Your Obsolescence Requirement Known to be a LRU, CCA, or Microcircuit (IC)?

?

Is the LRU Obsolete Because Contractor Will Not Support it, or Due to an Obsolete CCA(s)?

CCA

Is the CCA Obsolete Because Contractor Will Not Support it, or Due to a Component?

IC

Obtain Source Control Drawing for Specifications and Resolve with DER™ or DEER™

Consult with GCI for an Answer

No Support

No Support

Is the Original LRU Source Control Drawing (SCD) Available?

Yes

Is the Original Source Control Drawing (SCD) Available?

After Resolving with Custom Engineered Solutions, does Prototype Evaluation Pass?

No

No

Yes

No

Yes

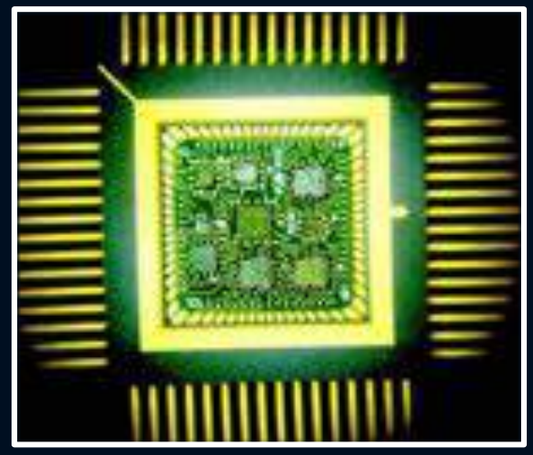
New Design From Contractor (Refresh)

Authorized Reverse Engineering and Manufacturing

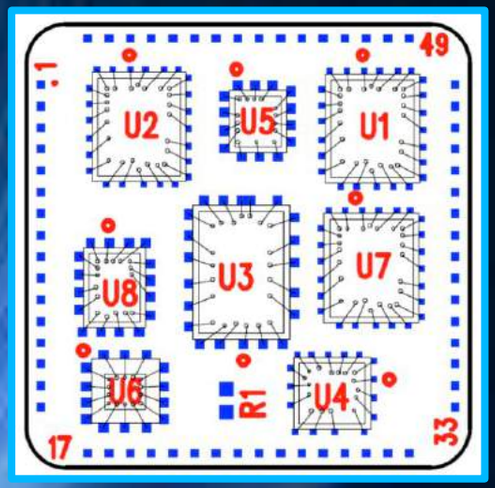
Qualification, Production, & Purchase

Re-Engineered Part
1800-Gate Bipolar Gate Array

F-16

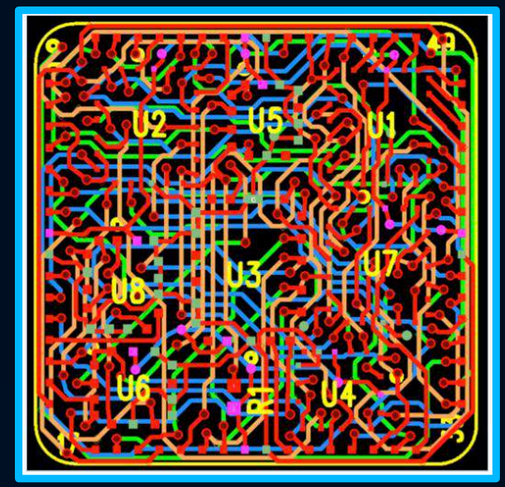


1800 Gate
Bipolar FPGA
Equivalent



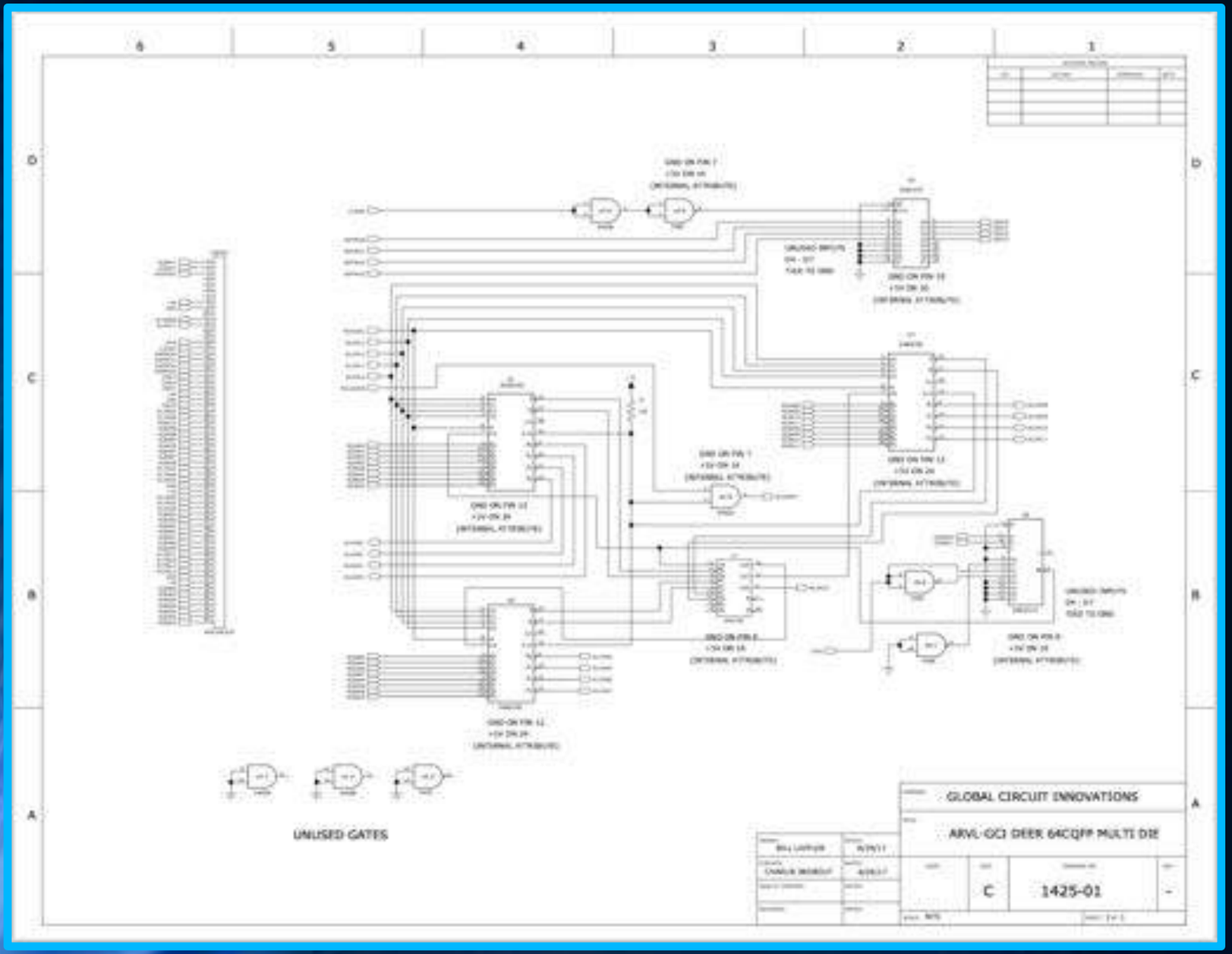
IC Layout

- Used in USAF F-16 Radar
- Multi Chip Module (MCM) product
  Emulates Obsolete 64-Pin CQFP
  Monolithic Bipolar Gate Array
- 4-Layer Internal Cavity Board
- Avoided a $3M System Re-Design
- Similar to Small Circuit Card Assembly



Inter-Cavity
Interposer Layout

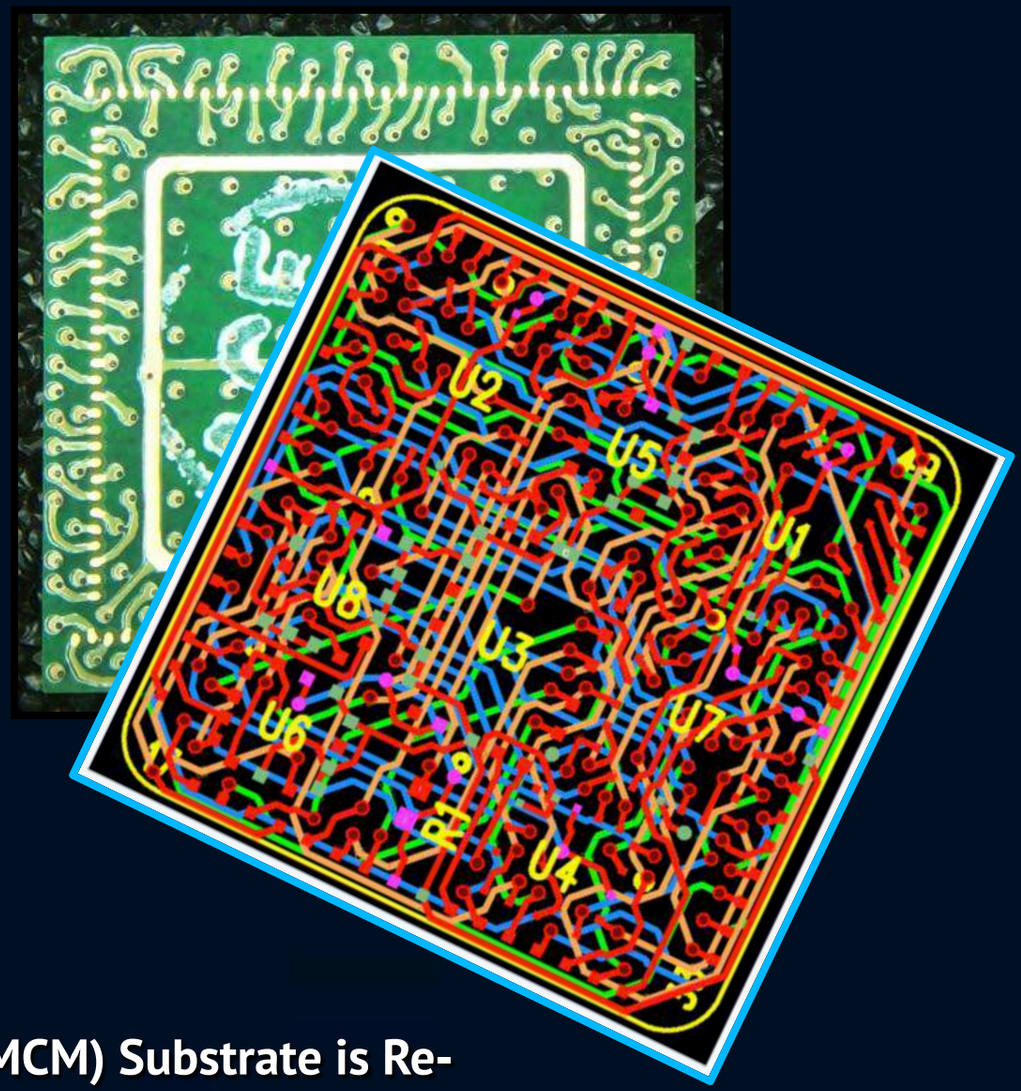
MCM Schematic Reconfigured From SCD Layout



List of all Integrated Circuits for 1800 Digital Gate Array Bipolar Project:

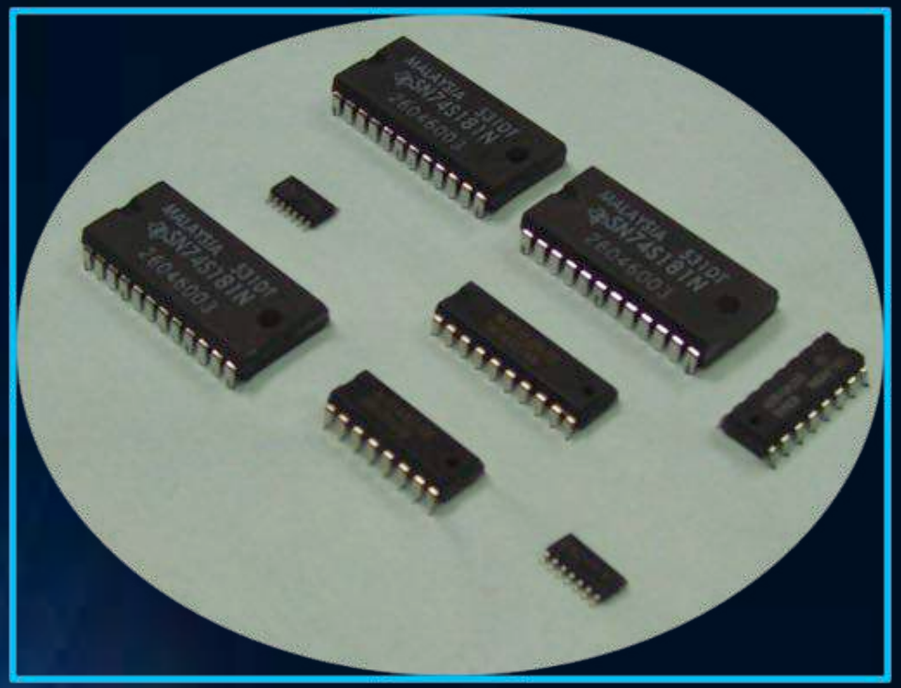
3x-54S181 (U1, U2, & U7)
4-Bit Arithmetic Logic Unit (ALU)
1x-54S374 (U3)
Octal D-Type Edge-Triggered Flip-Flop
1x-54S182 (U4)
Carry Lookahead Generator
1x-54S08 (U5)
Quad 2-Input AND
1x-54S00 (U6)
Quad 2-Input NAND
1x-54S151 (U8)
8-to-1 Multiplexer (MUX)

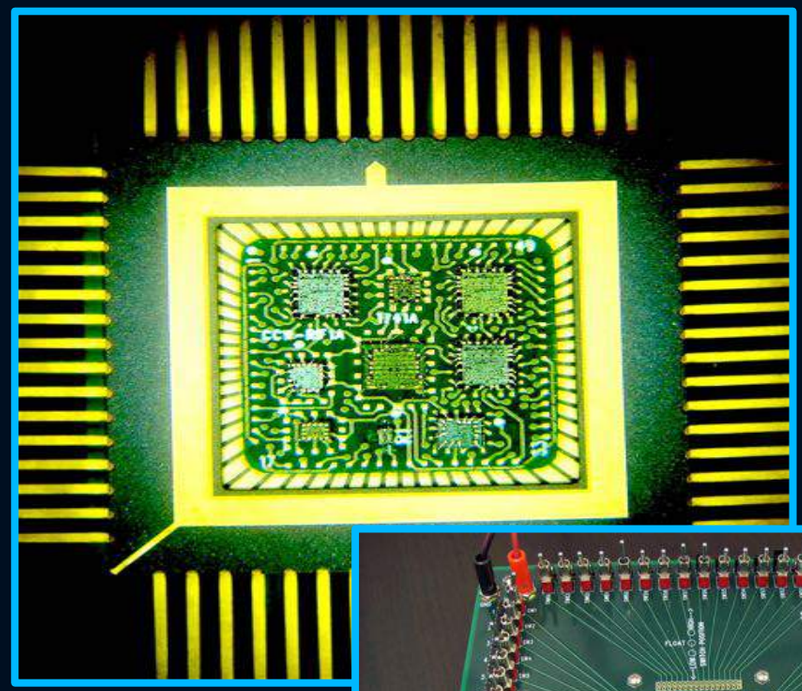
New CCA or Integrated Circuit MCM Design Flow

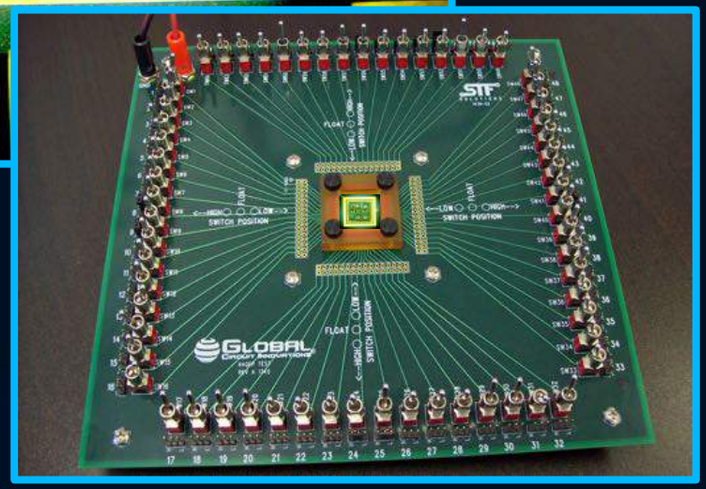


- **Circuit Card Assembly (CCA) or Multi-Chip Module (MCM) Substrate is Re-Designed From Original Source Control Drawing (SCD) Requirements**

MCM Re-Manufactured with Franchised Extracted Donor Die



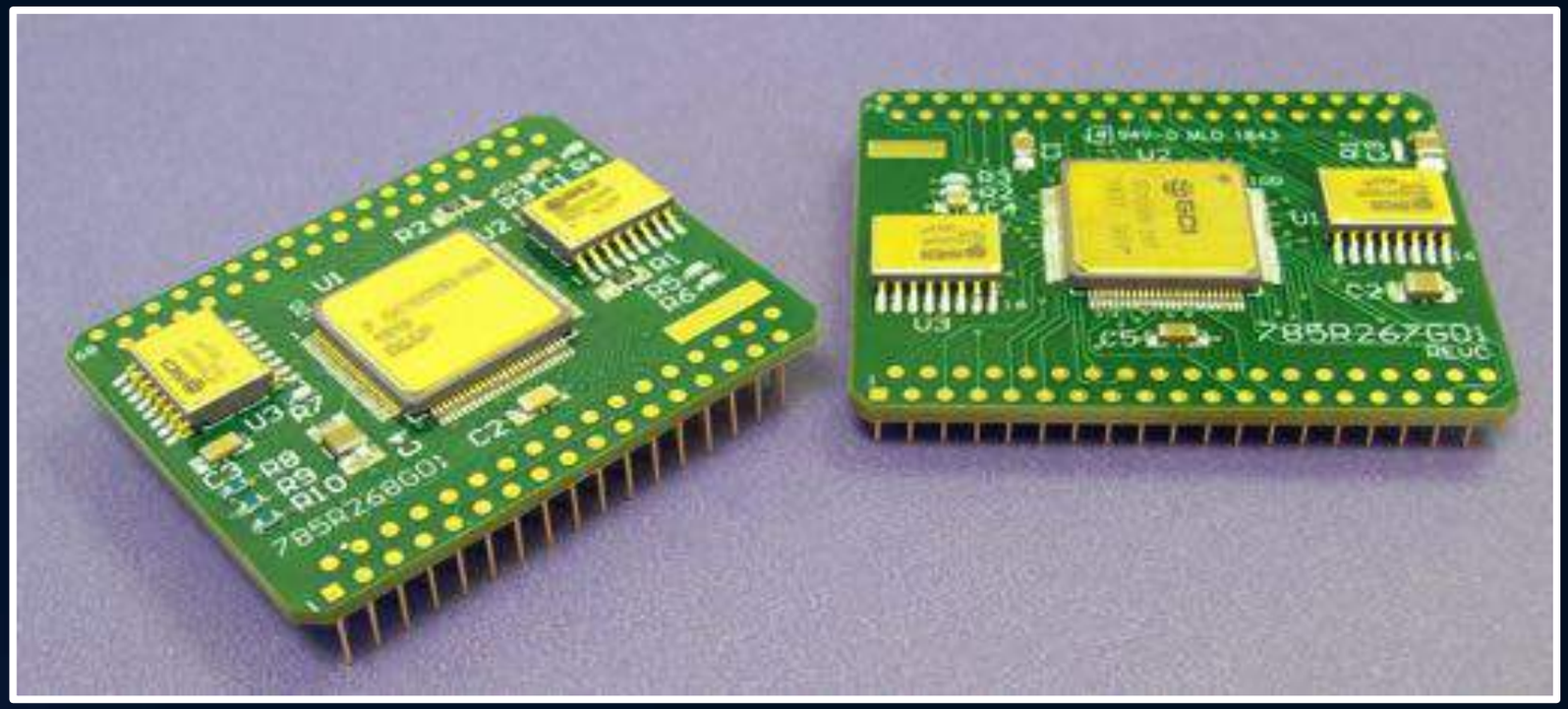




Test Board and Socket for Manual Input of the Test Vectors

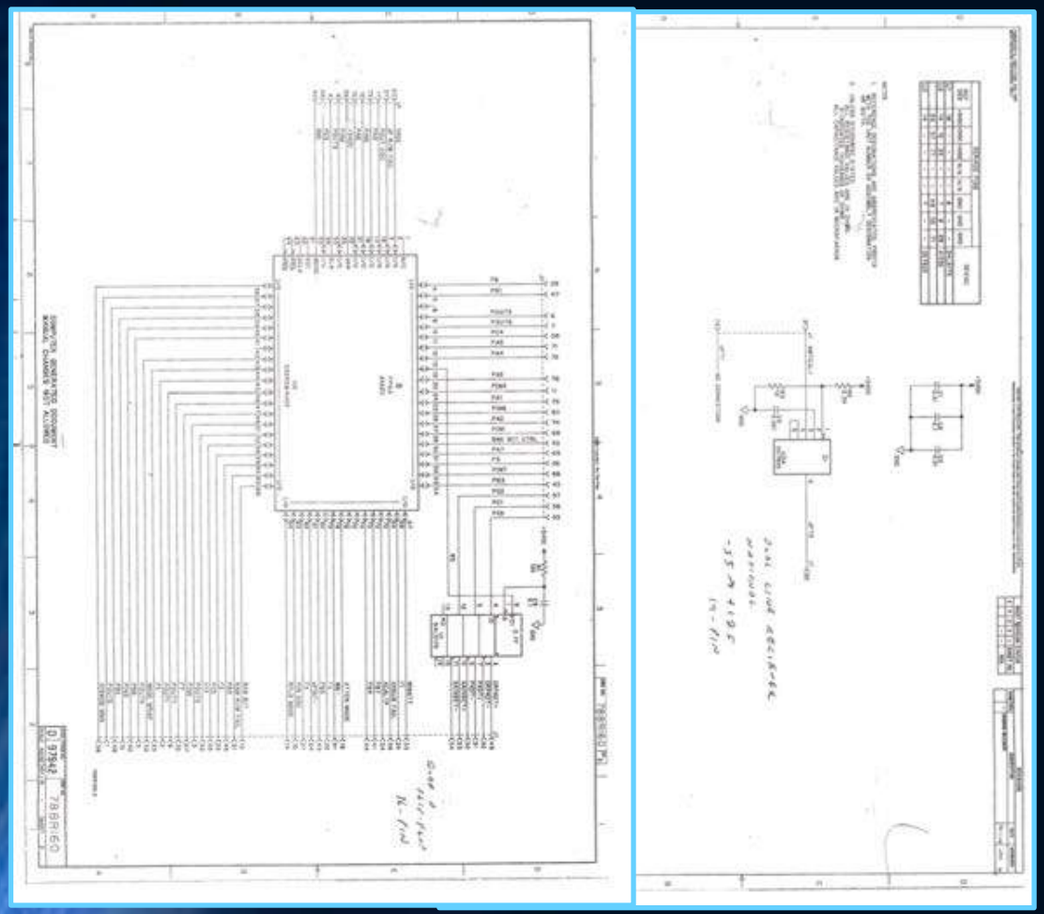
- Multi-Chip Module (MCM) is Manufactured From Extracted Die using GCI's *DER*™ & *DEER*™ Processes
- Plastic Components (above left) Represent Actual Franchised Donor IC's used in Final MCM (Plastic Components are Positioned Identically to Bare Die seen to above Right)

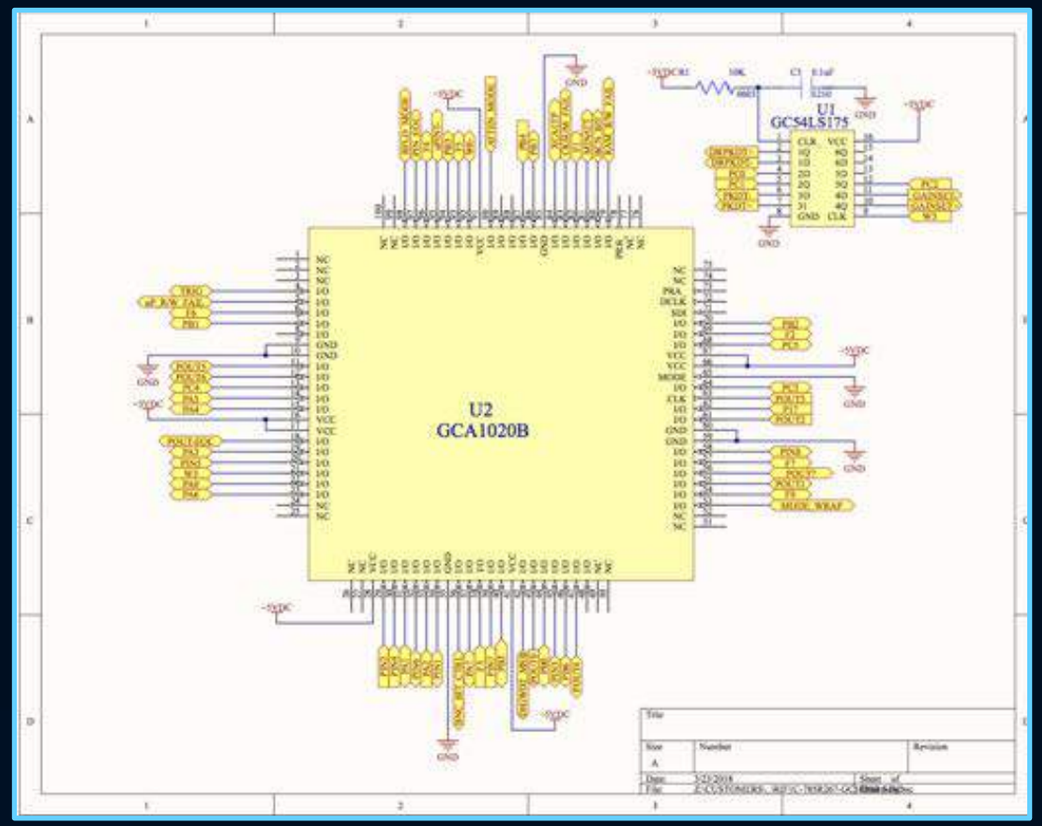
GCI Reverse Engineered CCA Substrates



- RAM I/O Interface Assembly and Microprocessor RAM Interface Assembly– 68-Pin and 76-Pin Circuit Card Assembly Substrates to Support F-16 Radar
- **Reference:** Original Contractor Source Control Drawing (SCD)
- **Problem Statement:** Device is no Longer Supported by Original Component Manufacturer yet still in Demand for Respective Circuit Card Assembly (CCA)

GCI Reverse Engineered CCA Substrates

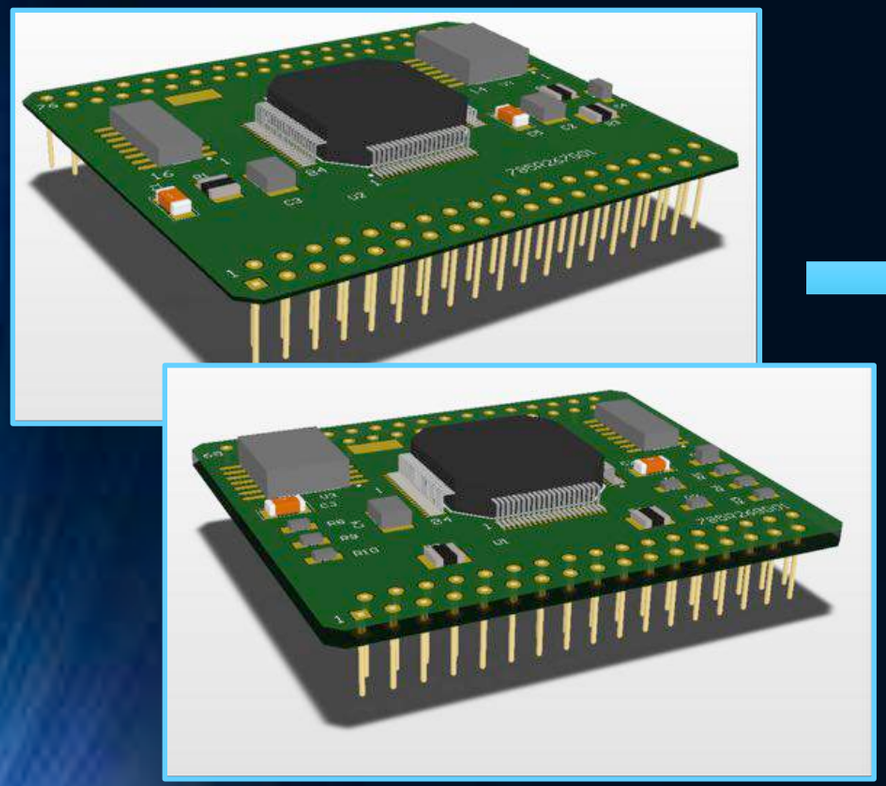




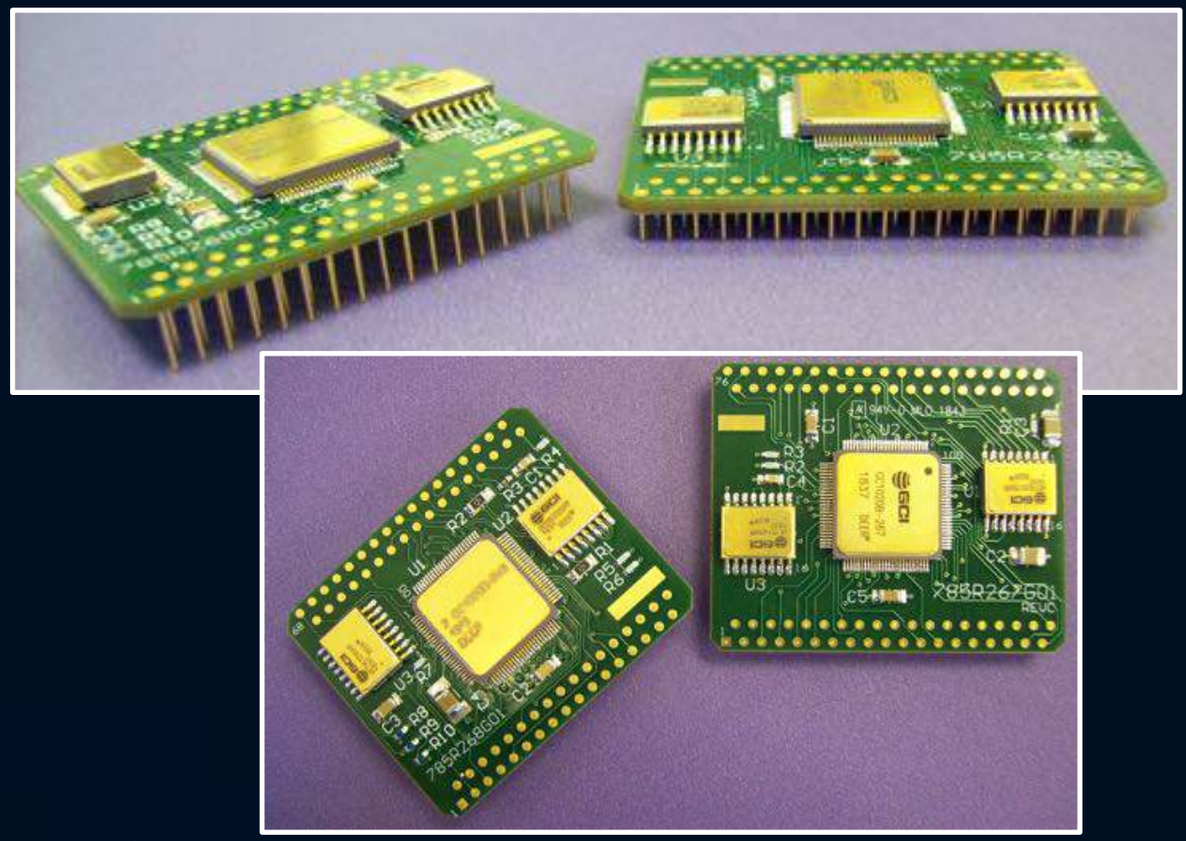
RAM I/O and Microprocessor Interface Assemblies – Original Source Control Drawing Schematics and Requirements are Converted into New Software for Schematic-to-Layout Development of New Circuit Card Assembly

GCI Reverse Engineered CCA Substrates

CAD Prototype Model



Finished CCA Product



RAM I/O and Microprocessor Interface Assemblies

- CAD Model is Converted into actual CCA Modules using GCI Technology
- Manufacture can be Resolved with either Franchised Bare Die Purchase or Franchised Die Extracted from Packaged Donor Devices

GCI Re-Engineered 500W Power Amplifier

500W Power Amplifier

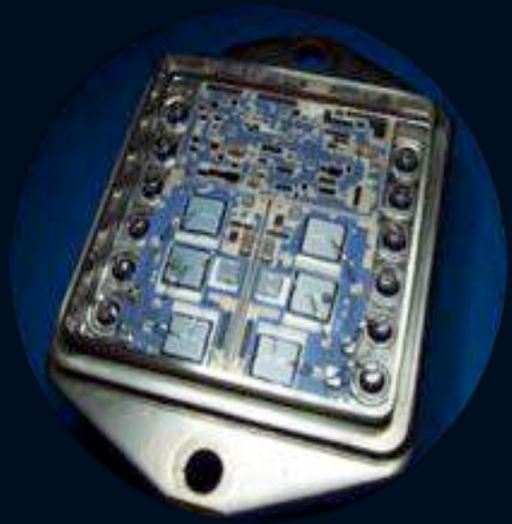
500W Power Amplifier

- +/- 75V, 30A - Circuit Redesigned to Deliver 57% More Power
- 12 Pin Power DIP Package

Reference: Original Component Manufacturer (OCM) Datasheet

GCI Re-Engineered 500W Power Amplifier

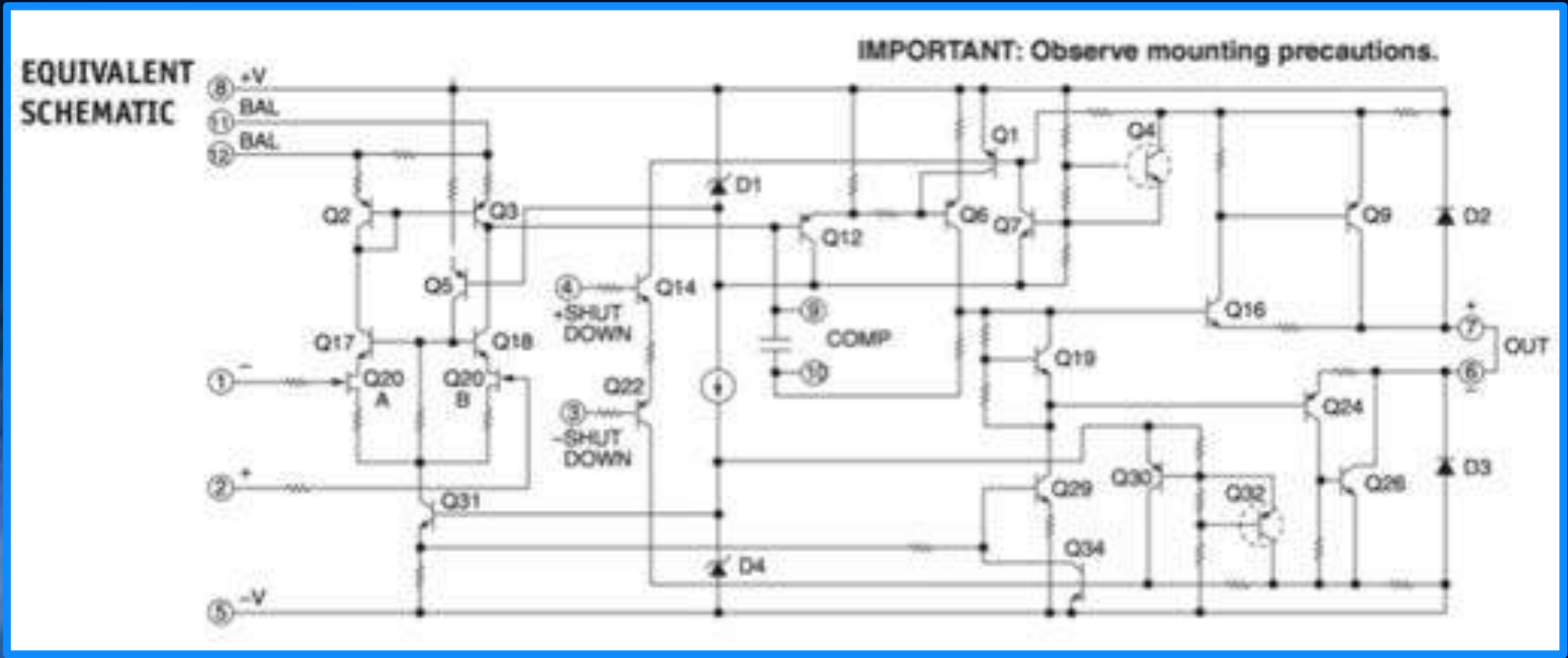
- Implemented within F-16 Antenna Radar Steering
- IC Redesign Cost $20K – Avoided ~$3M System Redesign
- IC specified for maximum temperature of +85°C…**YET**…was originally demonstrated to operate up to +125°C, and was successfully used in a +125°C avionics application for many years
- 2018 Design Revision ICs required for replacement units no longer worked near +125°C
- GCI engineered new design and created a solution that restored the power at +125°C
- Ogden Air Logistics Center (OO-ALC) at Hill AFB confirmed that the redesigned IC passed their bench testing in June 2018



500W Power Amplifier

GCI Re-Engineered 500W Power Amplifier

Solution – Discussion with OEM Application Engineering and Subsequent Circuit Analysis Highlighted Key Discrete Transistors Operating in Sub-Threshold Mode Providing Circuit Temperature Protection to Ensure Operation in Safe Operating Area (SOA)

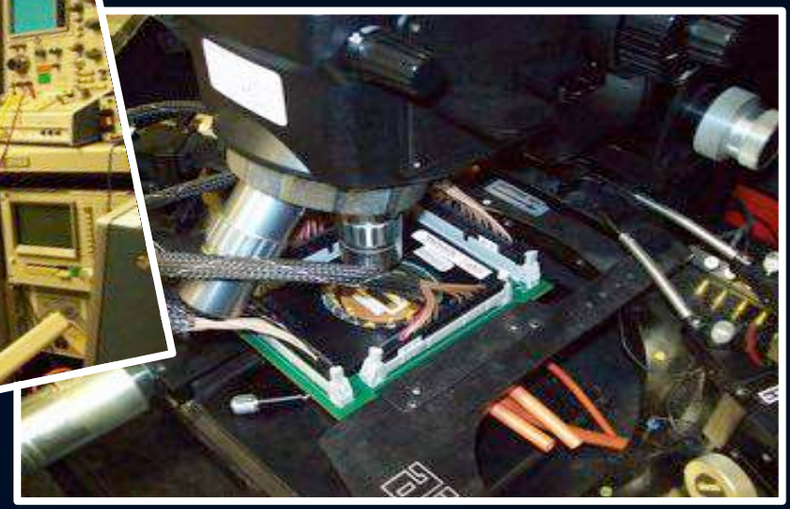


GCI Re-Engineered 500W Power Amplifier

Solution – An OEM Design Change due to the Retirement and Replacement of Two Transistors Caused the IC to Prematurely Shut Off while Still Well Within the SOA. The "New" Design Shut Down at 70% of the Sourcing Power and 63% of the Sinking Power.

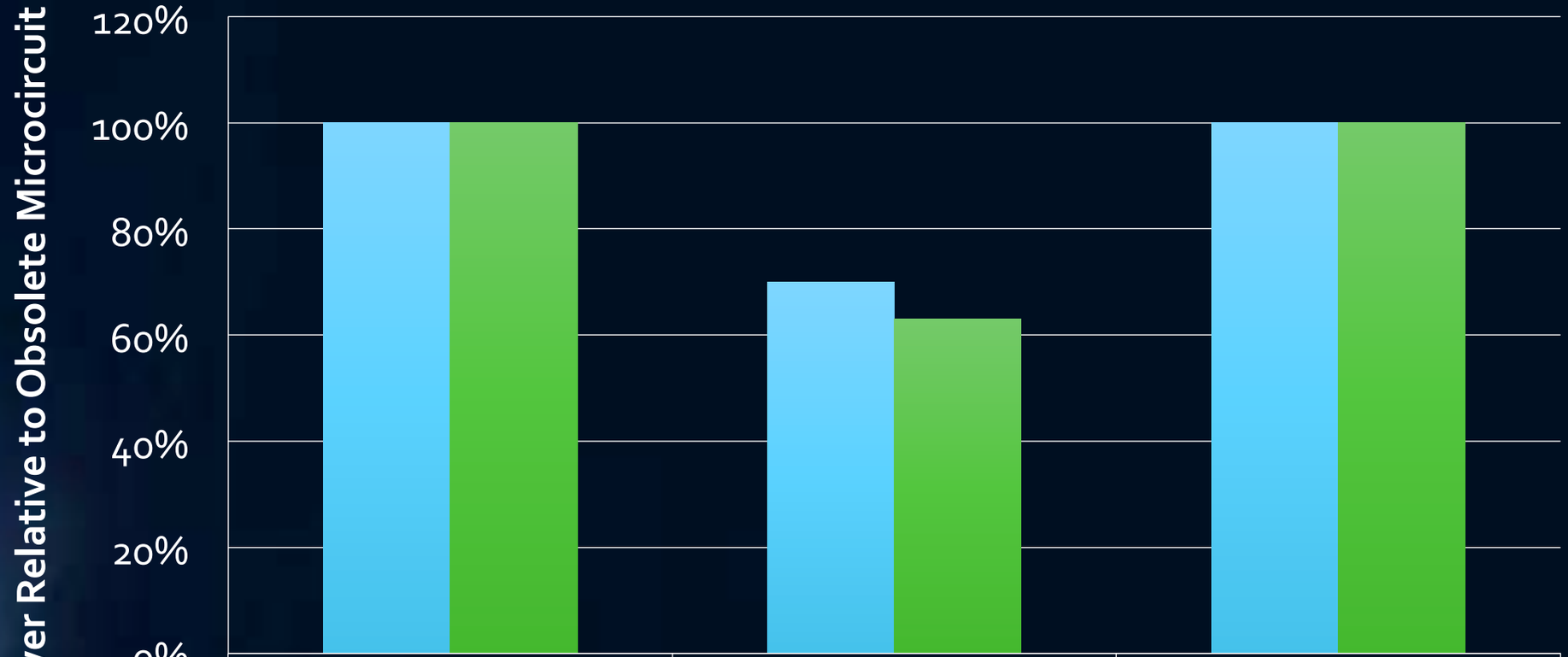
This Caused the IC to NOT Reliably Operate at +125°C.

GCI Executed a Circuit Design Modification Which Restored the SOA to it's Prior Power Range While Still in SOA



GCI Re-Engineered 500W Power Amplifier

Power Amp Power Relative to Original Design



	Obsolete IC Performance	New IC Revision Performance	GCI Modified IC Performance
Sourcing Power	100%	70%	100%
Sinking Power	100%	63%	100%

GCI Re-Engineered 500W Power Amplifier

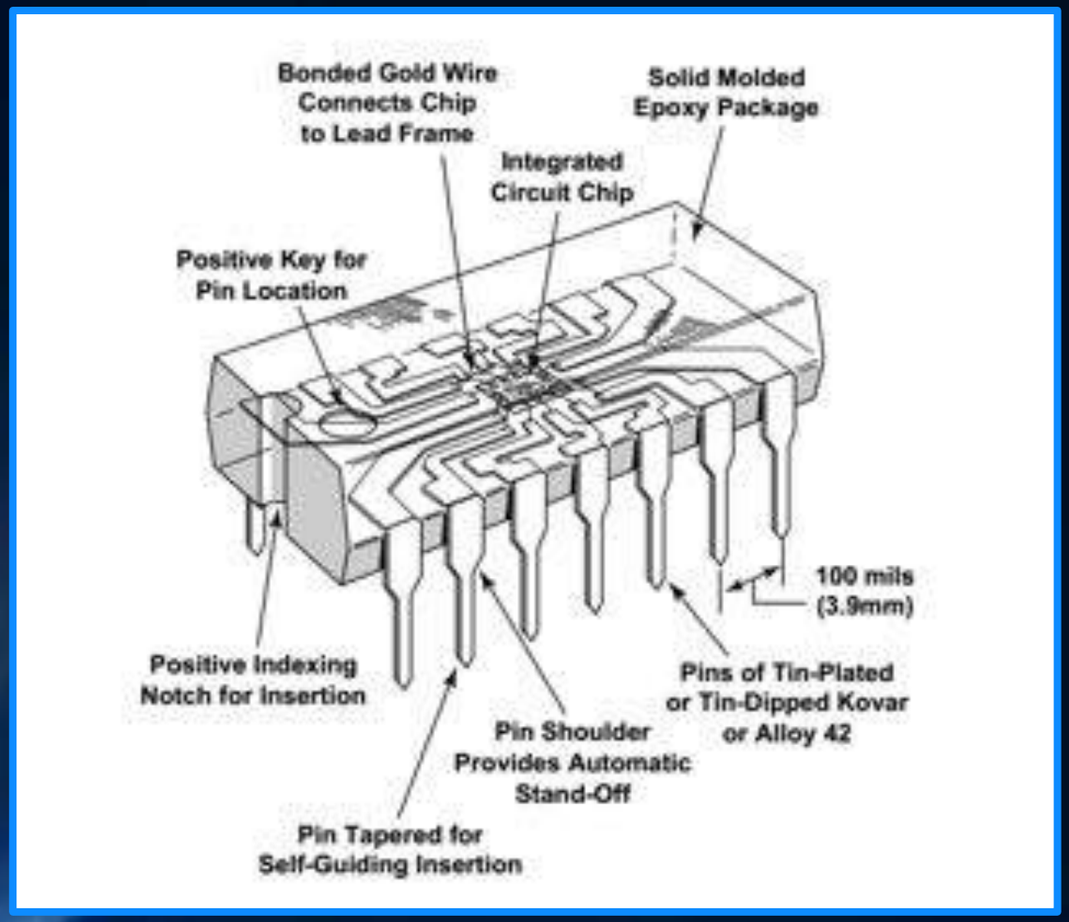
Estimated ROI: >200:1 by Avoiding ~$3.0M Avionics Radar System Design, or $20K total cost and $2.98M in Cost Savings

GCI's ***DER™*** and ***DEER™*** Technologies and Benefits

- ***DER™*** - Die Extraction and Re-Assembly: Removal of Franchised Die from either Plastic or Ceramic Package for Re-Packaging within any other Package.
- ***DEER™*** – ***DER™*** Process, but with Gold Ball Remnant Removal Followed by ENEPIG Die Pad Processing (Electroless Nickel, Electroless Palladium, and Immersion Gold Plating)
- Increased High-Temperature IC Reliability (150°C - 250°C Exposure) due to Ceramic Package Integrity and Removal of Gold Bond to Aluminum Die Pad Interface
- Increased Operating Temperatures due to Greater Heat Transfer Coefficient for Ceramic Package vs. Plastic Package
- Creating Obsolescence Solutions by Increasing Franchised Inventory Selection of Potential Donor Stock (larger Package Selection Possibilities of Desired Component)
- Available Franchised Die Inventory for Multi-Chip Modules or Prototype Requirements

Typical Integrated Circuit (IC) Architecture

The Various Elements of a Plastic Packaged IC Include:
the Die, Leadframe, Leads, and Plastic Encapsulation

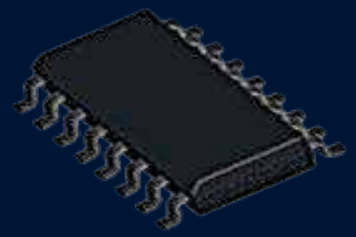


Franchised
Donor IC
Device

Cut Away
of Above
Package

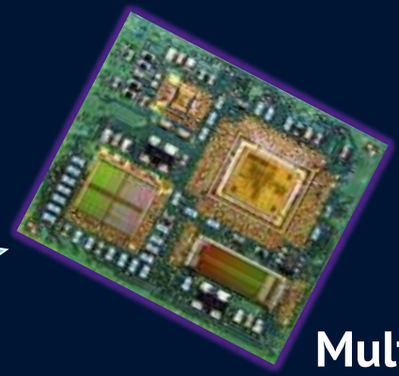
DER™: Die Extraction And Re-Assembly

If one Package Footprint is Obsolete, but the Die can still be Located in Another Package Footprint, or the Die is in an Undesirable Package, the Die can be Extracted and Re-assembled into the Desired Footprint (*DER*™)

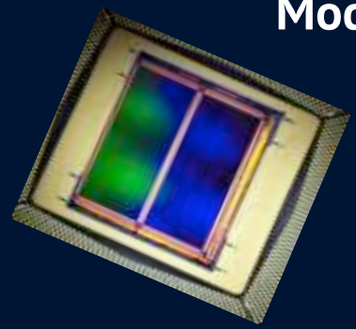


Franchised Donor IC Device

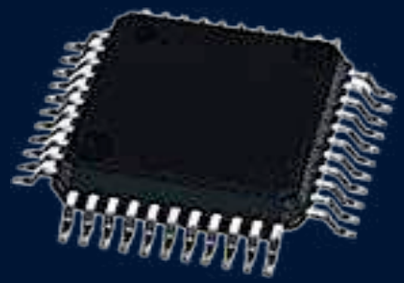
Extracted Die



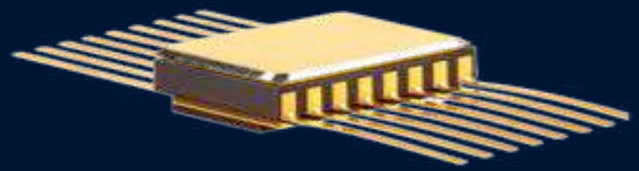
Multi-Chip Module



Ceramic CQFP

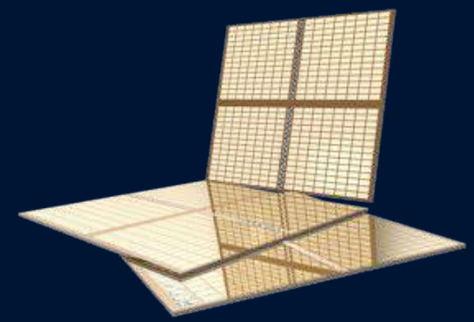


Plastic PQFP



Ceramic Flatpack

Or the *DER*™ Process Can be Used to Inventory Functional Die

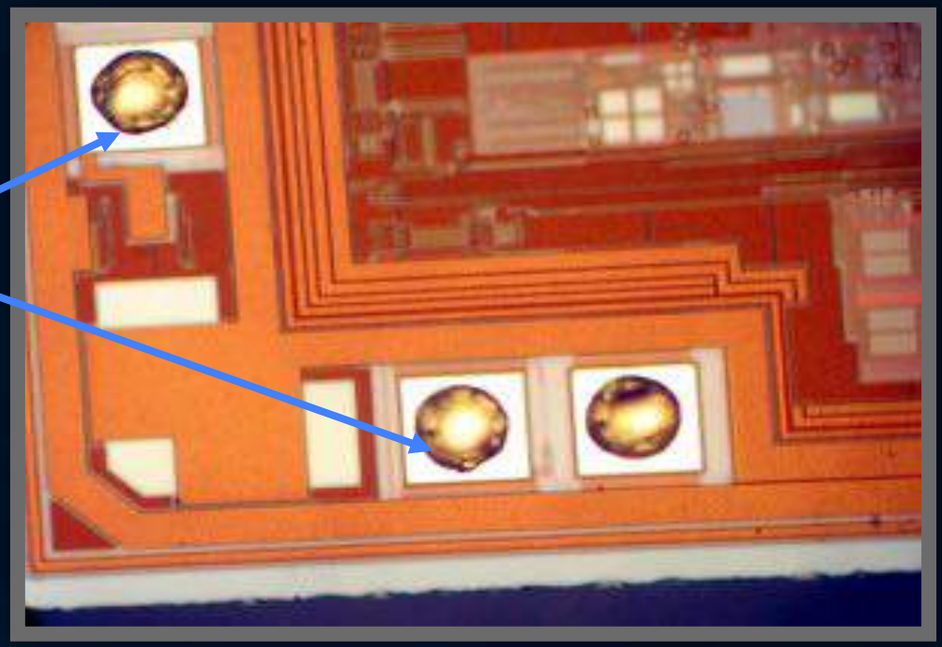


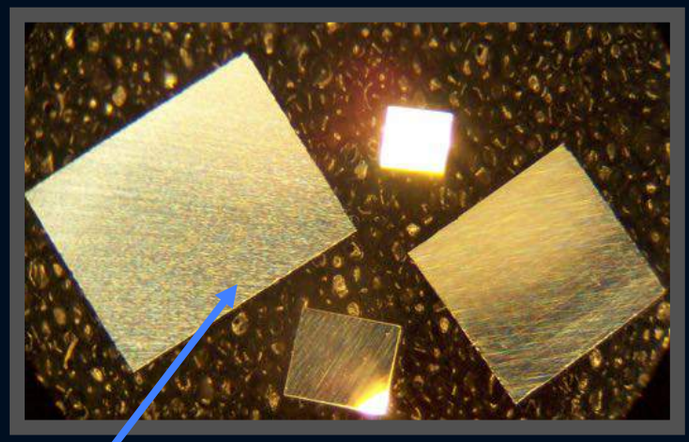
GCI's *DER*™ Technology Up Close

- GCI's Extraction Technology Provides Very Clean Front-Side and Back-Side Surfaces
- *DER*™ Relies on Chemical and Mechanical Processes Which Are No More Aggressive Than Those Used During Wafer Fabrication

No Inadvertent Etching of Bond Pads

Die Surface Free of Contaminants





Die Back-Side Surface Free of Contaminants and Returned to Original Mirror Finish

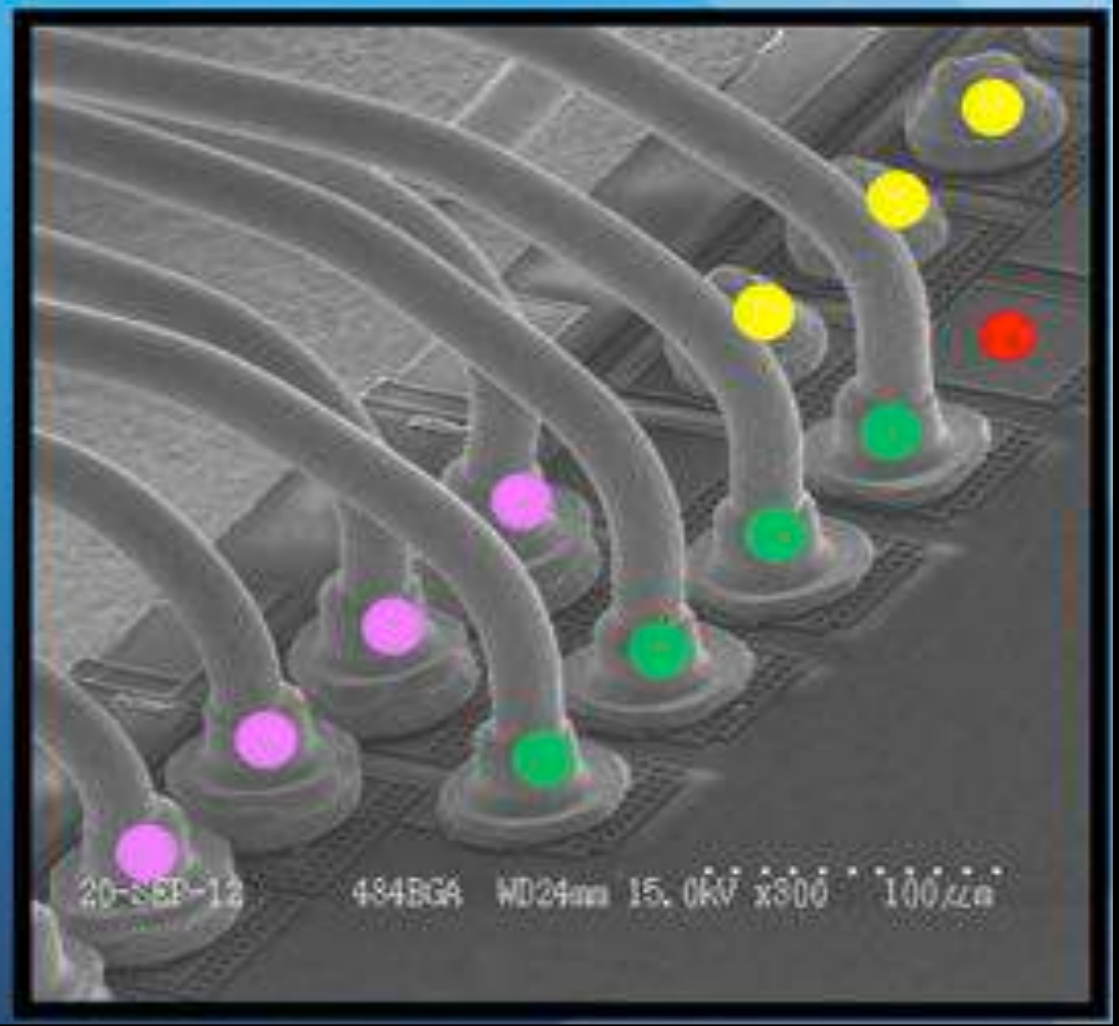
SEM Image of Compound Single Bonds

New Bond Mapping Options Available for Same Die

Multiple Chip Configurations for the Same Die Can be Achieved with Optional Bondouts

Note Four (4) Bond Options:

- Originally Non-Bonded Pad Still Not Bonded
- Originally Non-Bonded Pad Now Bonded
- Previously Bonded Pad Now Not Bonded
- Previously Bonded Pad With a New Compound Bond



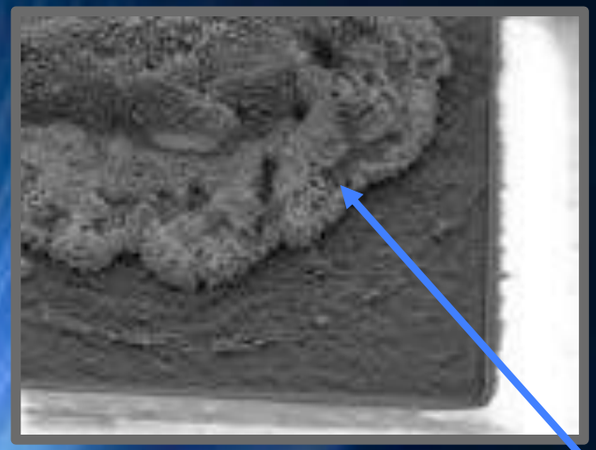
GCI's *DER™* U.S. DoD MIL-STD 883 Qualification

F-16 P/N (GEN#)	Original Package	New Package	Counterfeit Analysis	Variability Analysis	Reliability Study	DER	Hermetic Assembly	SMD Military 3-T Electrical	100% Screen/ Group A	QCI Group B	QCI Group C 2000 Hour Life Test	QCI Group D	4000 Hour Life Test Scheduled Completion
AT28C64B *Memory Device*	*28-pin SOIC Plastic*	*Ceramic-28 Pin SideBraze*	Authorized Distributor - Franchised	PASSED	PASSED	100%	100%	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED
XC4013XL *Field Programmable Gate Array*	*160-pin TQFP Plastic*	*Ceramic-144 CQFP*	Authorized Distributor - Franchised	PASSED	PASSED	100%	100%	PASSED	PASSED	PASSED	PASSED	PASSED	SEE * BELOW

- U.S. Department of Defense (DoD) MIL-STD 883 Testing
  - Nominal MIL-STD-883 Life Test Requirement of 1000 hours extended to 4000 hours at 125°C
  - IC Burn-In and Life Test Boards Designed for Maximum I/O Signal Level, I/O Loads and VDD Supply Voltage
- *XC4013XL FPGA: Solder Seal Solution with Brazed Sealing Ring Superior to Low-Temperature or High-Temperature Sealing Glass (for Hermetic Lid Sealing)

GCI's *DEER*™ Process Improvements

- Pad Re-Conditioning Using Gold Ball Removal Followed by ***ENEPIG*** (*Electroless Nickel, Electroless Palladium, Immersion Gold*) Plating
  - Potential Original Poor Ball Bond Quality/Reliability is Removed
  - Subsequent Bonding is Non-Compound with Highly Consistent and Reliable Bond Pull Strength
  - New Bond Pad Surface ***Eliminates*** Possibility of Kirkendall Voiding with Gold Bond Wire at Operating Temperatures Above 150°C



General Appearance of Kirkendall or Horsting Voiding at Bond Pad Location

Specifically, at Gold Ball to Aluminum Bond Pad Interface, the following Intermetallic Compounds can be formed:

Au_5Al_2, Au_4Al, Au_2Al, $AuAl_2$

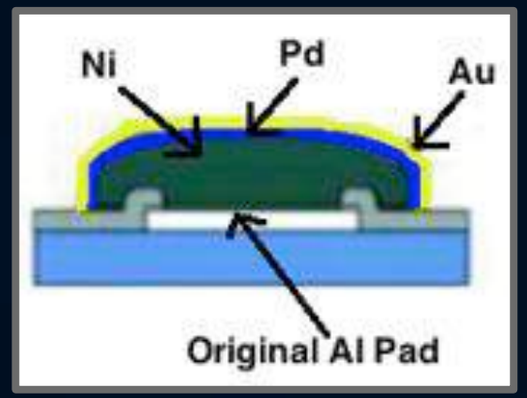
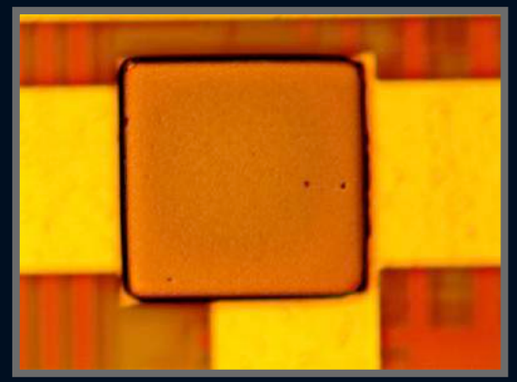


Illustration of *ENEPIG* Pad Plating



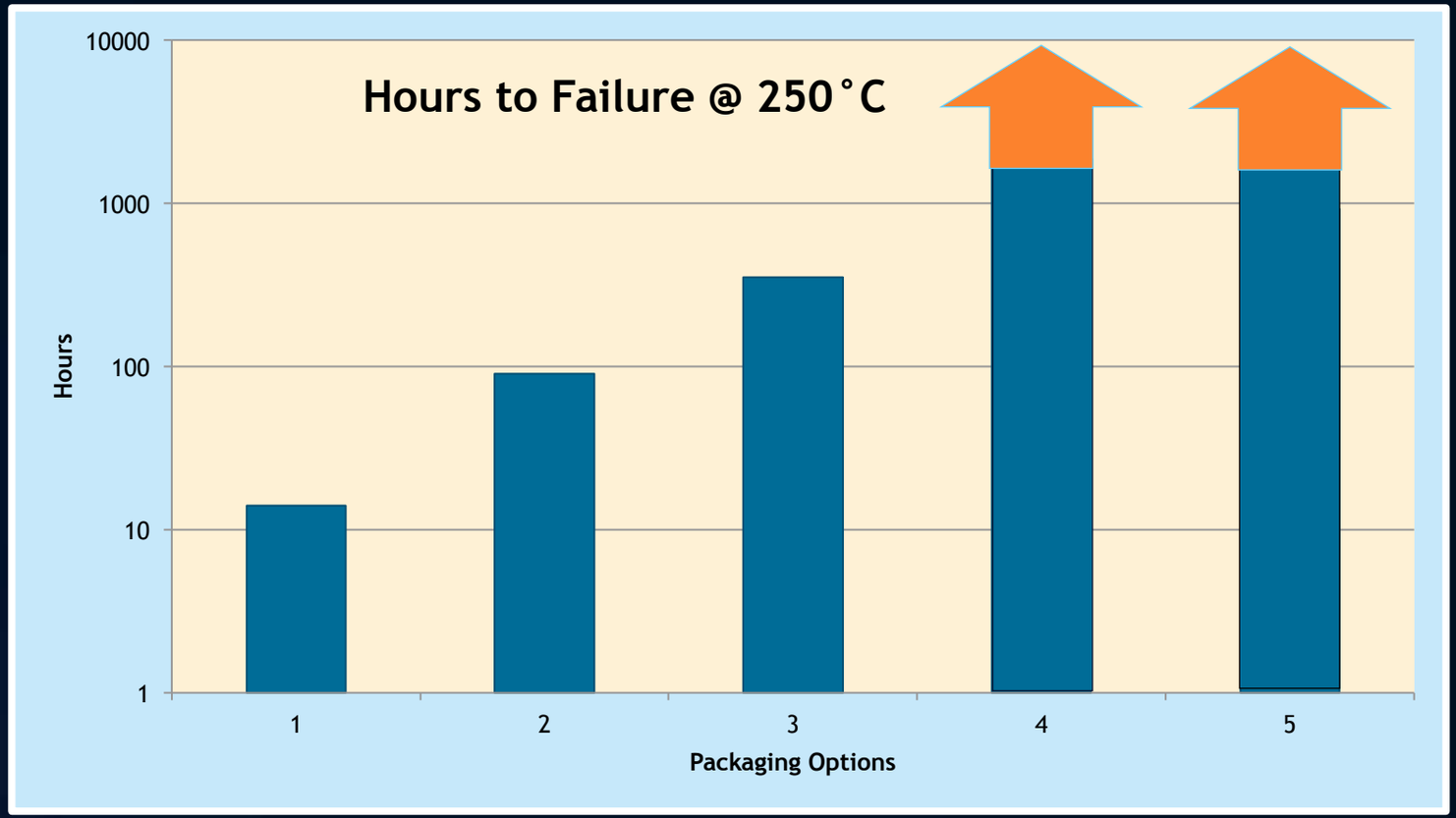
Optical Photo of Actual *ENEPIG* Plated Die Pad

DEER™ Gold Ball Removal, Pad Re-Plating with Electroless Ni/Pd/Au Process (***ENEPIG***)

Aluminum Pad Reconditioning for an Extracted Die

(Target Total Plate Up is 4 – 5 µm)

Ni/Pd/Au Pad *DEER*™ Re-Plating Performance at 250°C



Packaging Option Key:

1 – Standard Plastic	(25h)
2 – Extraction, Standard Ceramic Assembly (*DER*™)	(95h)
3 – Extraction, Hi-Temp Ceramic Assembly (*DER*™)	(600h)
4 – Extraction, Ni/Pd/Au Process, Standard Ceramic Assembly (*DEER*™)	(+2500h)
5 – Extraction, Ni/Pd/Au Process, Hi-Temp Ceramic Assembly (*DEER*™)	(+6000h)

Accomplishments

- RIF 1 (Rapid Innovation Fund) Awarded - $2.75 million contract to produce 20+ IC Component Obsolescence Solutions across DoD - FA8615-17-C-6053 was awarded through USAF/AFMC/ AFLCMC AF LIFE CYCLE Program Engineer Program Engineer
- RIF 2 (Rapid Innovation Fund) Awarded - $2.94 million contract to produce FPGA obsolescence solutions using GCI's **DEER™** process - AFLCMC17-9.e.-P-747
- AFRL Study ($350K) – ***DER™*** Evaluation and Variability Study
- SBIR Phase I, II ($150K, $750K respectively) – Characterize, Optimize, and Qualify ***DER™*** & ***DEER™***
- AFWERX SBIR Phase I – Reverse Engineering on Digital Timing Generator Microcircuit for F-16 Radar
- STTR awarded Fall 2016 ($150K) - Collaborated with University of Colorado Springs, CO for High-Temperature Reliability Study of ***DEER™*** - Air Force Research Laboratory (AFRL)
- NAVSEA Navy Program – Qualification of Serial 4K Memory Device for NSWC
- Trademarks Granted for ***DER™*** and ***DEER™*** Spring/Summer '17
- Currently have 12 Patents Granted, and 6 Pending

Summary of Key Points

- Many CCAs are Obsolete Because one or more Microcircuits (or ICs) on those CCAs is no Longer Available (IC Obsolescence Produces Next Higher Assembly Issues)
- GCI's Capabilities allow for Form, Fit, and Function (FFF) Drop-In Replacements for those Microcircuits, thus making these CCAs Available without Complete System Re-Design or Line Replacement Unit (LRU) Re-Design
- GCI does not Design Original Microcircuits, but Acquires Original Design Manufacturer (ODM) Microcircuits and Develops Reverse Engineering Methods to Allow Development of a Component, Designed to Perform in the Required Conditions and Mandatory Specifications while Meeting FFF Requirements
- **The Die Extraction and Re-Assembly Technologies (*DER*™ & *DEER*™) Continues to Provide High-Temperature and Obsolescence Solutions and are Now Tools to Help Resolve Circuit Card Assembly Obsolescence**
- Billions of Dollars of Potential Cost Savings in DoD and other Applications can be Realized Through these Approaches

Contact Information

Erick Spory
President & CTO
Erick.Spory@GCI-Global.com
Office: +1 (719) 573-6777 x104
Cell: +1 (719) 649-0947

DMSMS Booth #630

www.GCI-Global.com