ELECENG 2EI4
Project 4 – CMOS XOR Gate

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Summary

Logic gates are the fundamental building blocks of digital circuits, primarily composed of transistors such as MOSFETs or BJTs. This project focuses on the MOSFET-based implementation of logic gates.

Before designing a logic gate, it is important to understand how MOSFETs function as voltage-controlled switches. Applying a specific voltage to the gate terminal determines whether current flows between the source and drain terminals. NMOS transistors conduct when a high voltage is applied to the gate, while PMOS transistors conduct when the gate voltage is low [1].

By combining NMOS and PMOS transistors, CMOS logic (Complementary MOS) is created, ensuring that only one type conducts at a time. CMOS circuits consist of a Pull-Up Network (PUN) made of PMOS transistors and a Pull-Down Network (PDN) made of NMOS transistors. This structure improves efficiency and reduces power consumption.

Using these principles, an XOR gate can be designed with CMOS logic, using the complementary behavior of MOSFETs to achieve the desired logic function.

Design

CMOS uses negative logic, meaning the XOR gate's Boolean expression needs to be simplified using DeMorgan's theorem.

Table 1: Truth table for the XOR gate

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

DeMorgan's Theorem applies two inversions to the Boolean expression and then distributes one, converting AND to OR, and vice versa, to get the complementary logic.

$$F = A \oplus B$$

$$F = \bar{A}B + A\bar{B}$$

$$F = \overline{\overline{\bar{A}B + A\bar{B}}}$$

$$F = \overline{\overline{(\bar{A}B)} \cdot \overline{(A\bar{B})}}$$

$$F = \overline{\overline{(\bar{A}B)} \cdot \overline{(A\bar{B})}}$$

$$F = \overline{(A + \bar{B}) \cdot (\bar{A} + B)}$$

$$F = \overline{AB + \overline{A}\overline{B}}$$

Once the Boolean expression for the XOR gate has been simplified, it can be implemented using the pull-down and pull-up network. CMOS logic indicates that N-MOSFETs bridge a LOW connection, and P-MOSFETs bridge a HIGH connection. The pull-down network contains inputs A in series with B, which is in parallel with inputs $\bar{A}$ in series with $\bar{B}$. This is mirrored and implemented in the pull-up network using P-MOSFETs. When mirroring the networks, we must invert the series connections to parallel and parallel connections to series. With the final Boolean expression made, the circuit can be modelled. The final XOR CMOS circuit uses a total of 12 MOSFETs, including 2 needed for each of the inversions for inputs A and B.

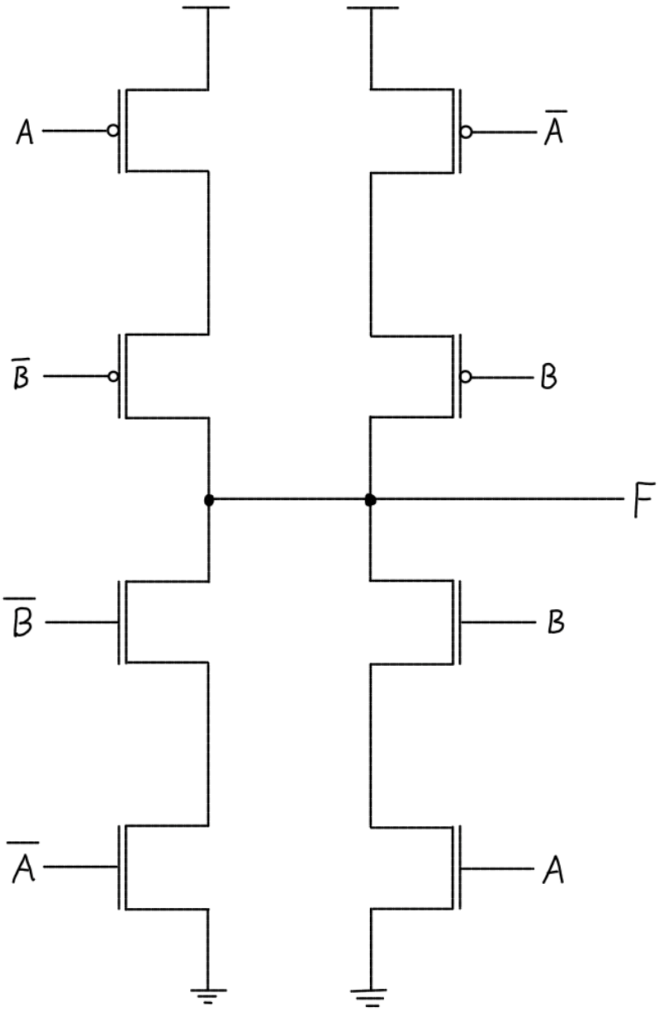

Figure 1: Circuit schematic of CMOS XOR gate

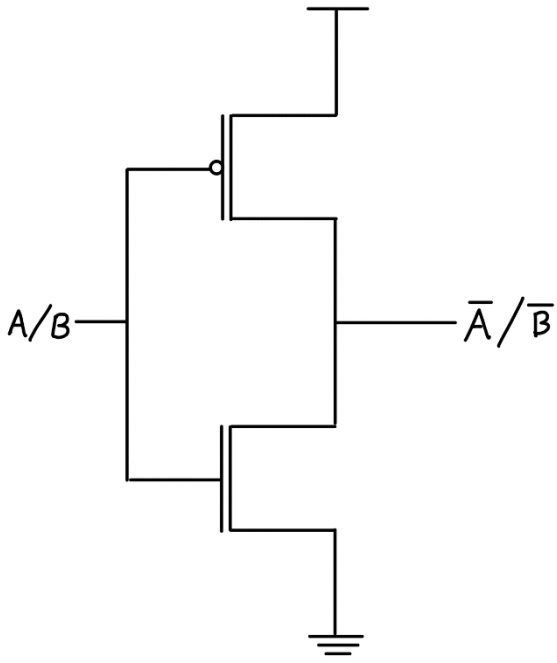

Figure 2: Circuit schematic of CMOS inverter

Ideal Sizing

Determining the ideal sizing of this XOR gate allows us to minimize the delay for this logic output to be updated. To minimize the delay for this circuit, it requires it to be symmetric, which means the ratio between the pull-down network and pull-up network should be 1:1. This ensures both networks have the smallest delay possible.

$$\tau_{PHL} = 0.69 R_N C_L = 4.14 C_L$$

$$\tau_{PLH} = 0.69 R_P C_L = 4.14 C_L$$

$$R_N \propto \frac{1}{k}$$

$$k' = k\left(\frac{W}{L}\right)$$

By examining the relationship for the time delay, we know the conduction of electrons happens quicker in N-MOS than the conduction of holes in P-MOS. Electron conduction happens faster by a factor of 2.5, this is because the electron mobility ratio of electrons to holes is 2.5:1. Therefore, the size ratio for both N-MOS and P-MOS cannot be the same, since P-MOS will have a larger equivalent resistance, which would increase the time delay. The ideal ratio between P-MOS and N-MOS transistors is 2.5:1, which would result in the following size ratio:

$\left(\frac{W}{L}\right)_P = \frac{5}{1}$ and $\left(\frac{W}{L}\right)_N = \frac{2}{1}$.

The worst-case time delay involves 2 MOSFETs through any branch of the XOR gate. From the pull-up network, all transistors have a resistance of ½R, so the worst-case time delay is $(\tau_{PLH}) = 2 * \tau_{ref}$, and from the pull-down network, since the circuit is symmetric, the worst-case time delay is $(\tau_{PHL}) = 2 * \tau_{ref}$. In both cases, the time delay is double the reference time delay, which means transistors on both sides have double the resistance needed. To decrease the resistance of the transistors by a factor of 2, their size ratio needs to be multiplied by a factor of 2. This makes the ideal size of the MOSFETs to be 2n for the PDN and 2p for the PUN or

$\left(\frac{W}{L}\right)_P = \frac{10}{1}$ and $\left(\frac{W}{L}\right)_N = \frac{4}{1}$.

However, the size parameters, width and length, are fixed physical parameters set by the IC manufacturer and cannot be changed. The only other option to implement the ideal size is to put multiple transistors in parallel with each other to half the on resistance. However, we cannot implement this since the circuit requires 12 MOSFETs, which is all the MOSFETs available to us, which means we cannot implement the ideal sizes in our scenario. Since we cannot optimize this circuit with its ideal size, its propagation time will be double that of τ_{ref}.

Testing

The circuit model uses 12 MOSFETs, 6 NMOS and 6 PMOS. As a result, every pin on the CD4007B IC chip was used.

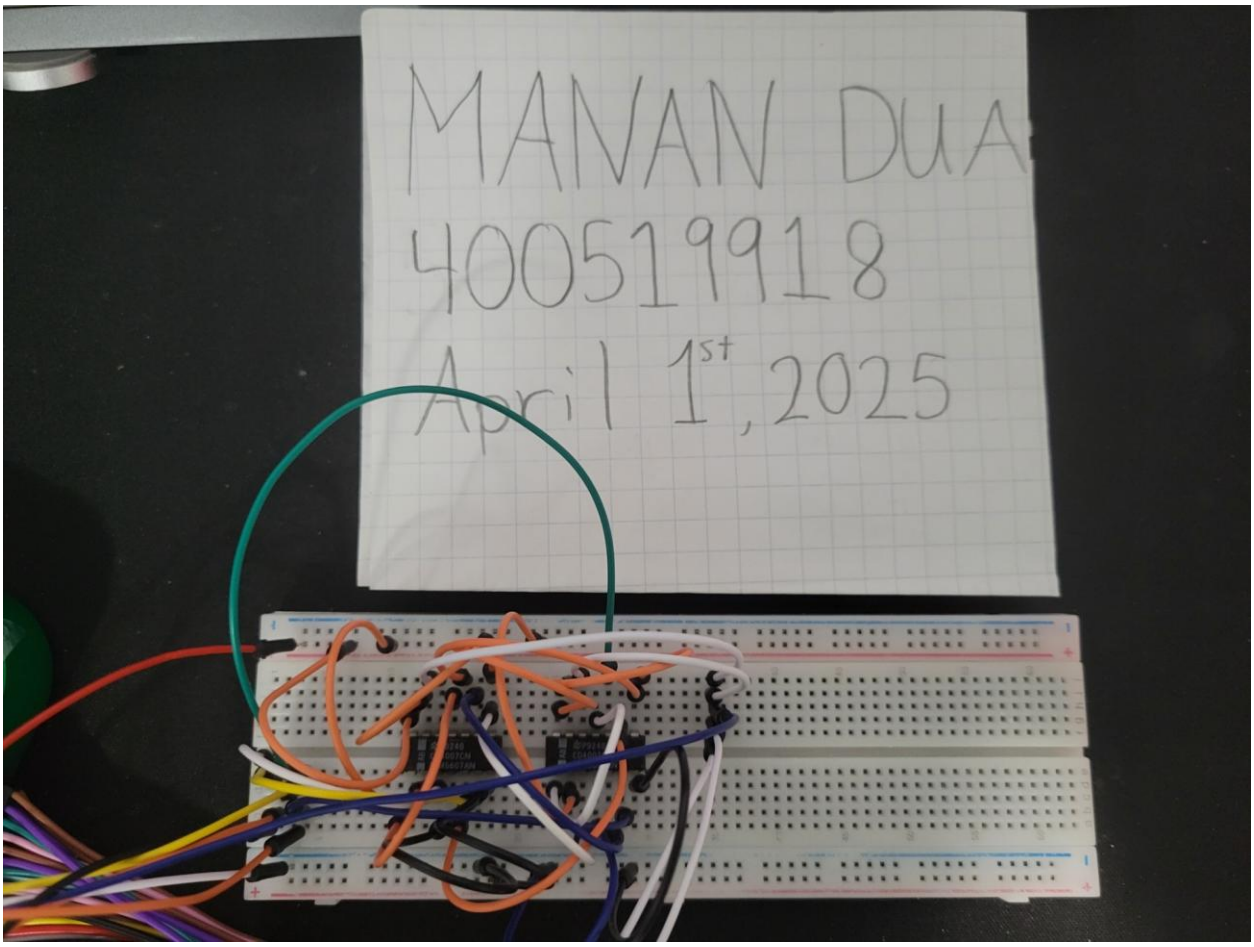

Figure 3: Physical circuit of CMOS XOR gate

Functional Testing

For testing the functionality of the CMOS XOR gate, 2 square waves input with 2.5V amplitude and 2.5V offset were inputted at terminals A and B, with terminal A having a frequency of 100Hz and terminal B having a frequency of 50Hz. This ensures we are able to see the output at every given possibility of the truth table. Additionally, digital IO pins were placed at both inputs as well as the outputs to visualize the logic states. Pin 1 is connected to terminal A, pin 2 is connected to terminal B and pin 3 is connected to the output. When both outputs are logic low or logic high, the output is logic low, and when only one input is high and the other is low, the output is logic high.

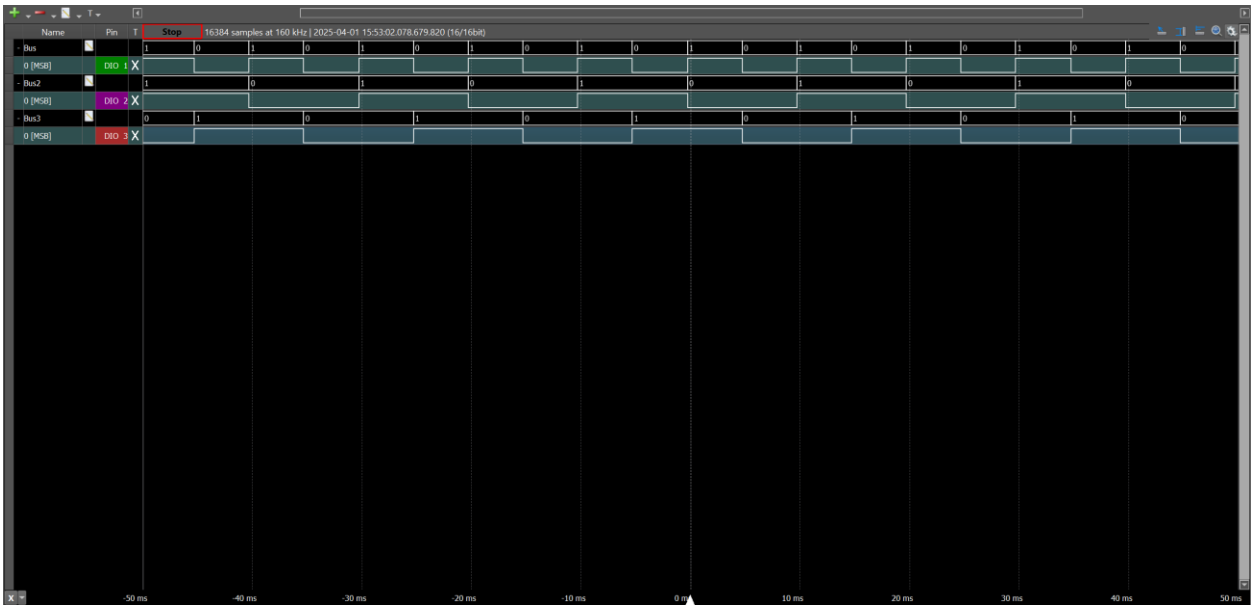

Figure 4: Logic analysis of the CMOS XOR gate

Static Testing

For static testing, we set one of the inputs to logic high (+5V) and the second input to be a square wave between 0V and 5V. With the static input connected to input A, V_H = 5.01V and V_L = 0.042V and when the inputs are swapped, there is little to no change with V_H = 5.02V and V_L = 0.041V. However, since this is a logic gate with only two states, these values are rounded to V_H = 5V and V_L = 0V, which indicate a logic high and logic low, respectively.

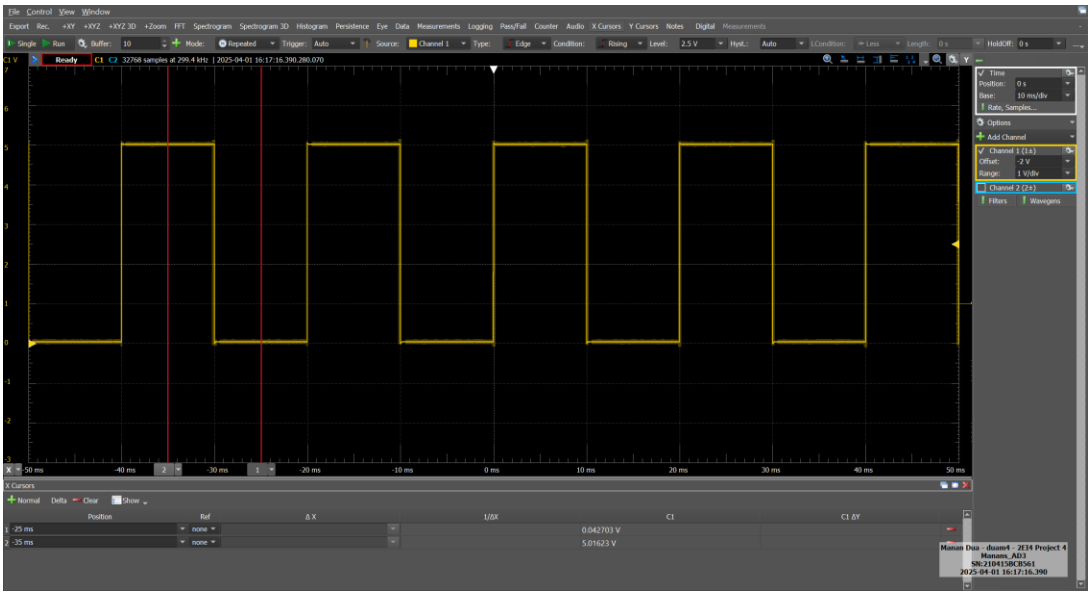

Figure 5: V_H and V_L measured with input A fixed at 5V

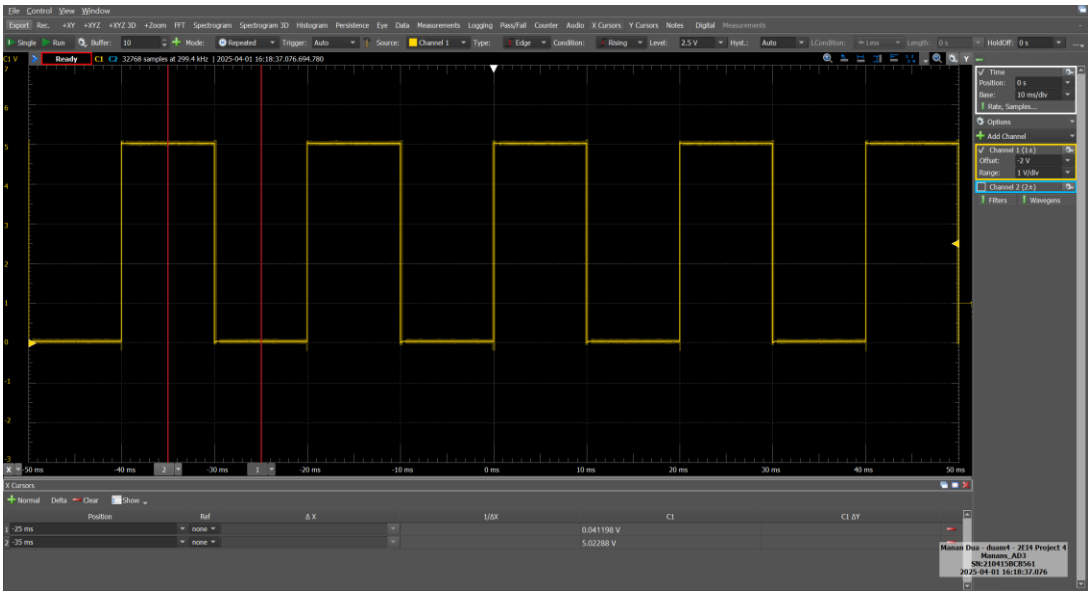

Figure 6: V_H and V_L measured with input B fixed at 5V

Timing

To measure the transition delay between low to high and high to low, a 100nF capacitor is connected to the output and the voltage is measured across it. Additionally, input voltage B was set to logic high (+5V), and input A was set to a square wave between 0V and 5V. From the produced waveform, it was determined that τ_{rise} = 353us and τ_{fall} = 330us. Next, we can determine the high-to-low propagation delay by measuring the time between the input pulse reaching 50% of its transition from low to high and 50% of its transition from high to low. From Figure 8, it was determined that τ_{PLH} =158us and from Figure 9 τ_{PHL} = 175us. τ_P can be found using the following formula: $\tau_P = \frac{\tau_{PLH}+\tau_{PHL}}{2} = \frac{158+175}{2} = 166us.$

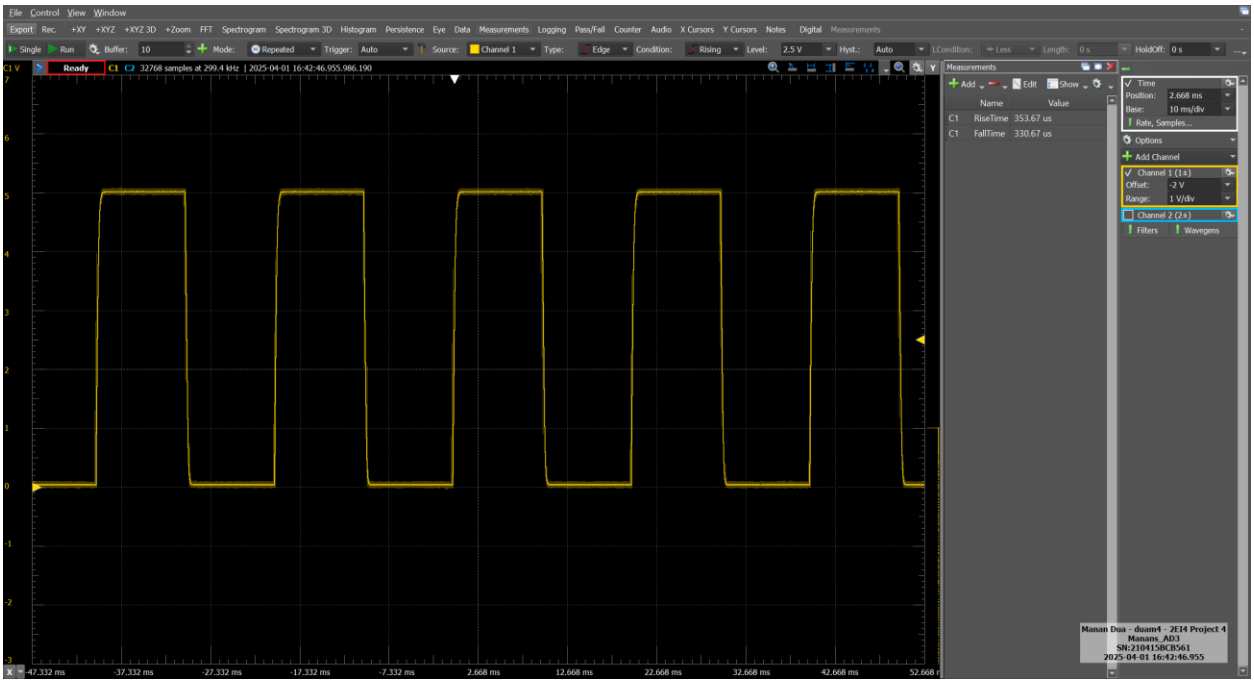

Figure 7: Circuit output with 100nF capacitor connected at the output

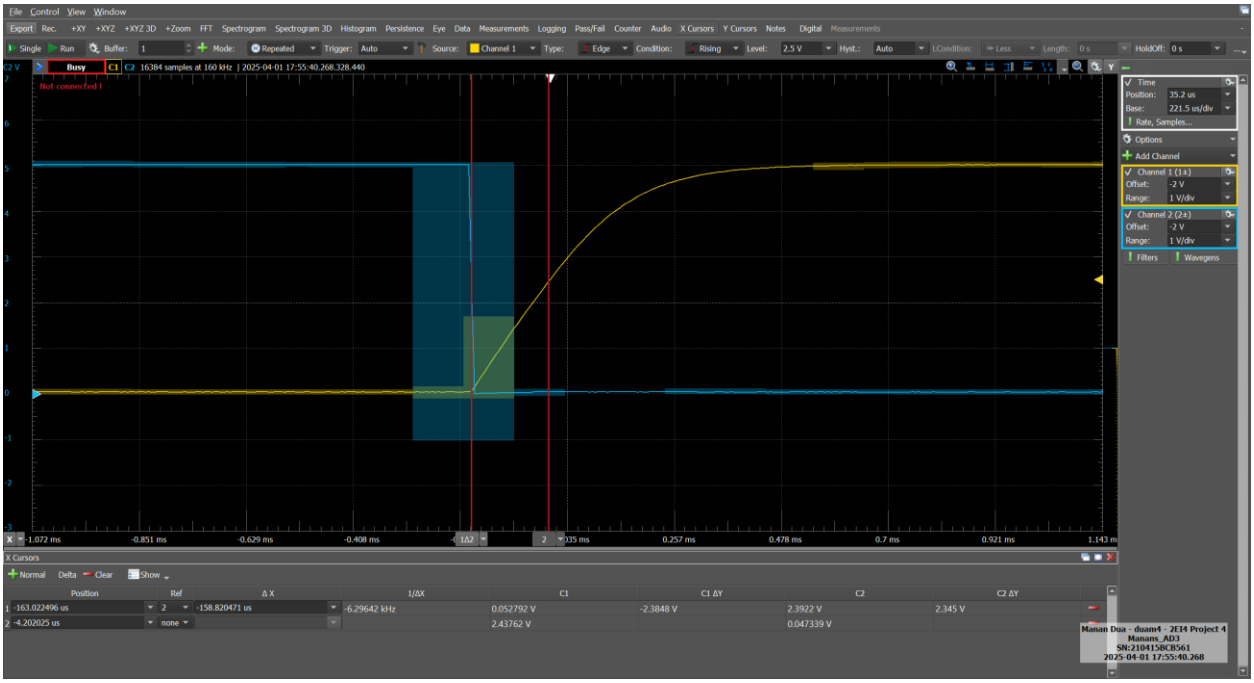

Figure 8: Zoomed plot of input and output waves with cursors to measure τ_{PLH}

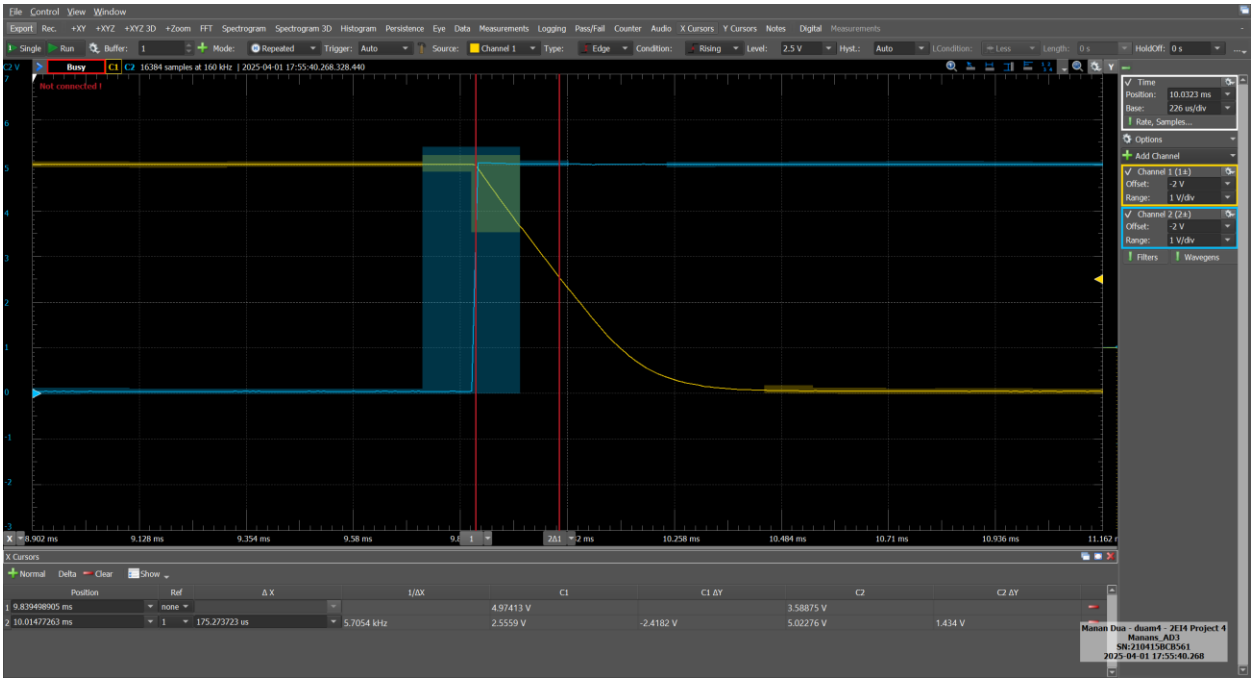

Figure 9: Zoomed plot of input and output waves with cursors to measure τ_{PHL}

Bonus

A pass transistor is a transistor used as a switch to control the flow of current in a The transistor "passes" current from its input to its output based on a control signal applied to its gate [2]. A pass transistor can be used to construct an XOR gate by controlling how input signals are selectively transmitted based on transistor switching. In a pass transistor logic implementation of XOR, NMOS and PMOS transistors are used to conditionally pass one input based on the value of the other input. When B = 0, the circuit passes A to the output, and when B = 1, the circuit passes A' to the output.

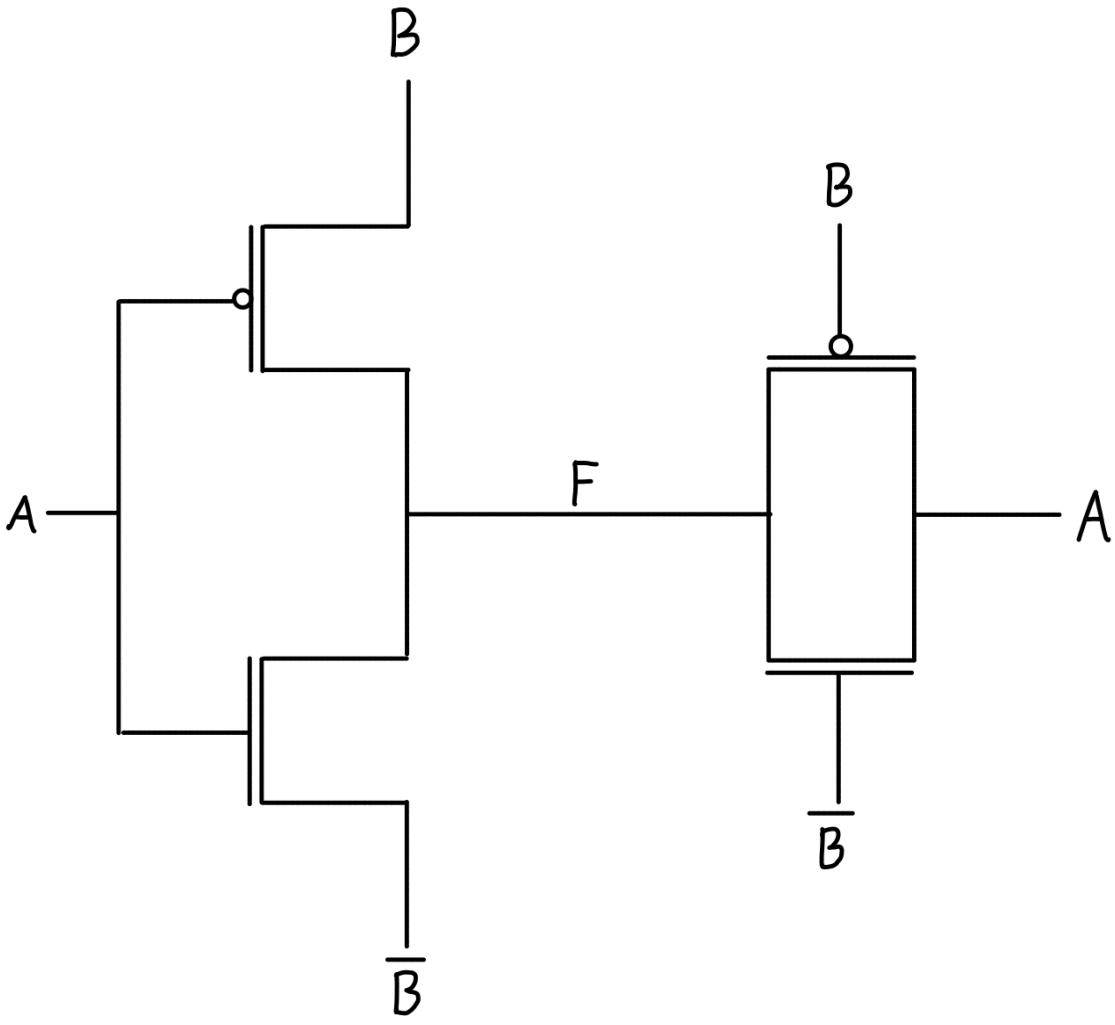

Figure 10: Circuit schematic of CMOS XOR gate with pass transistors

Testing

This new circuit only uses 6 total MOSFETs, 4 for the actual logic gate and 2 for an inverter. This is significantly lower than the original circuit, making it easier to implement.

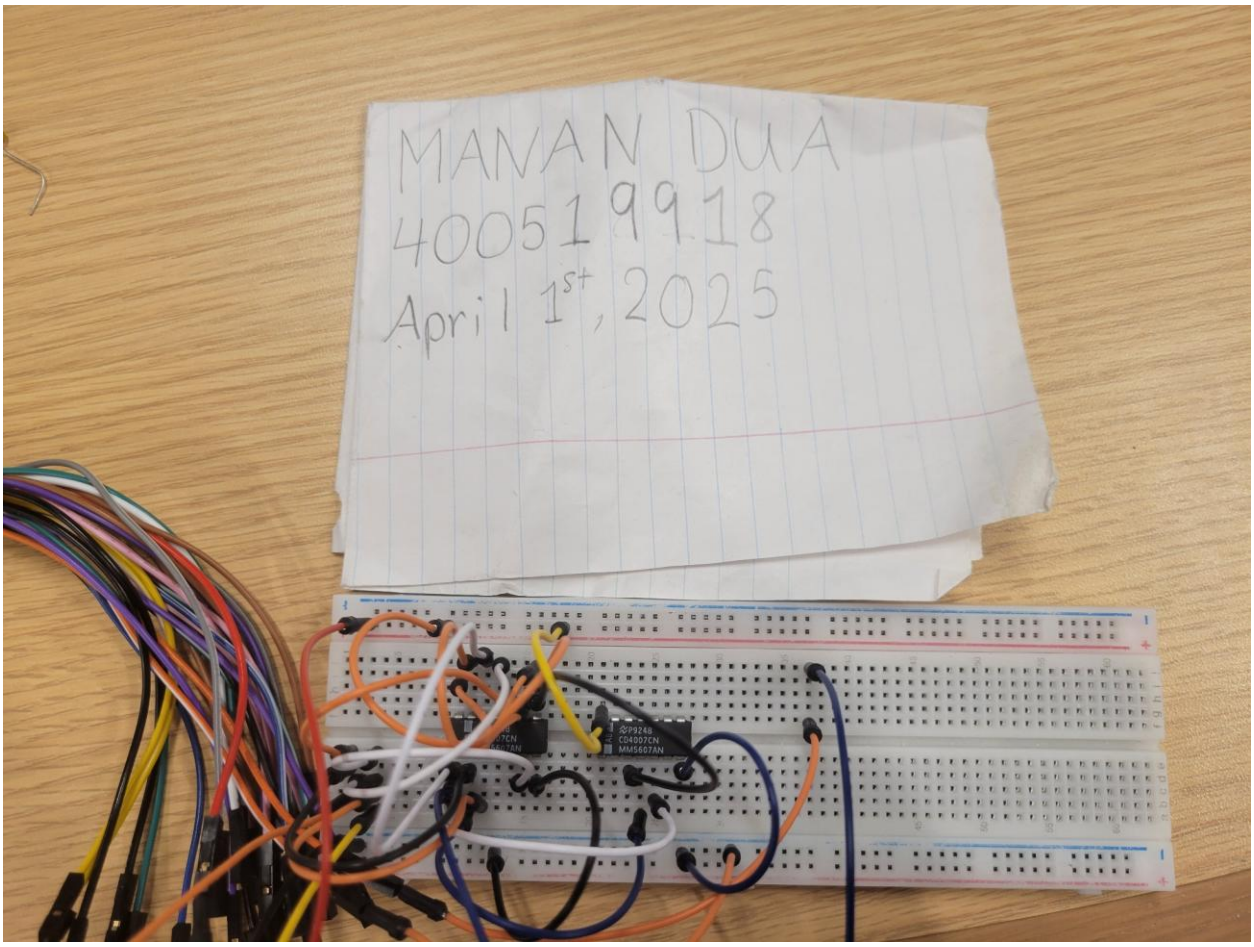

Figure 11: Physical circuit of CMOS XOR gate with pass transistors

Functional Testing

By building this circuit, we can verify that the circuit produces the correct output based on the truth table of the XOR gate using the logic analyzer on the AD3. Similar to the first circuit, the inputs receive a square wave with an amplitude of 2.5V and offset of 2.5V. Input A receives a wave with a frequency of 100Hz and input B receives and input of 50Hz. GPIO pin 1 is connected to terminal A, pin 2 is connected to terminal B and pin 3 is connected to the output. When both outputs are logic low or logic high, the output is logic low, and when only one input is high and the other is low, the output is logic high.

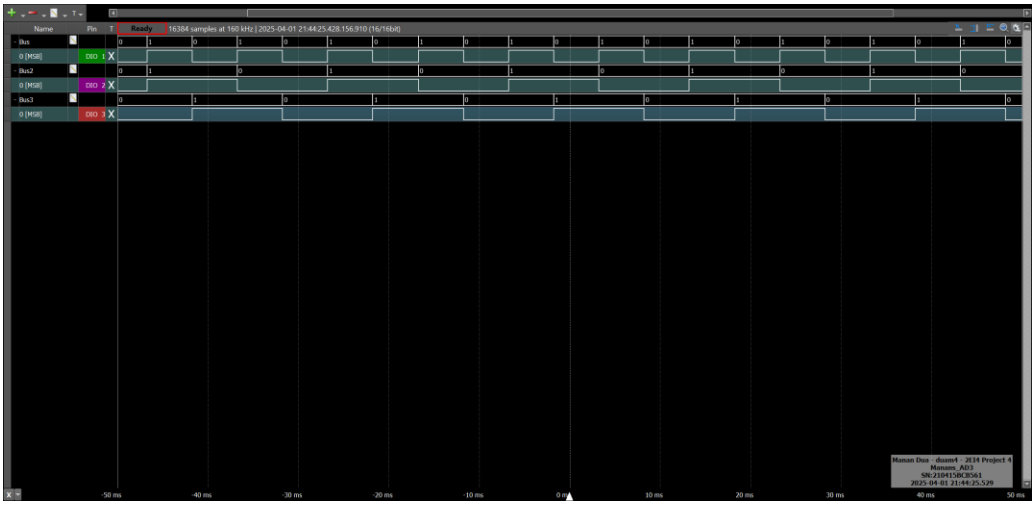

Figure 12: Logic analysis of the CMOS XOR gate with pass transistors

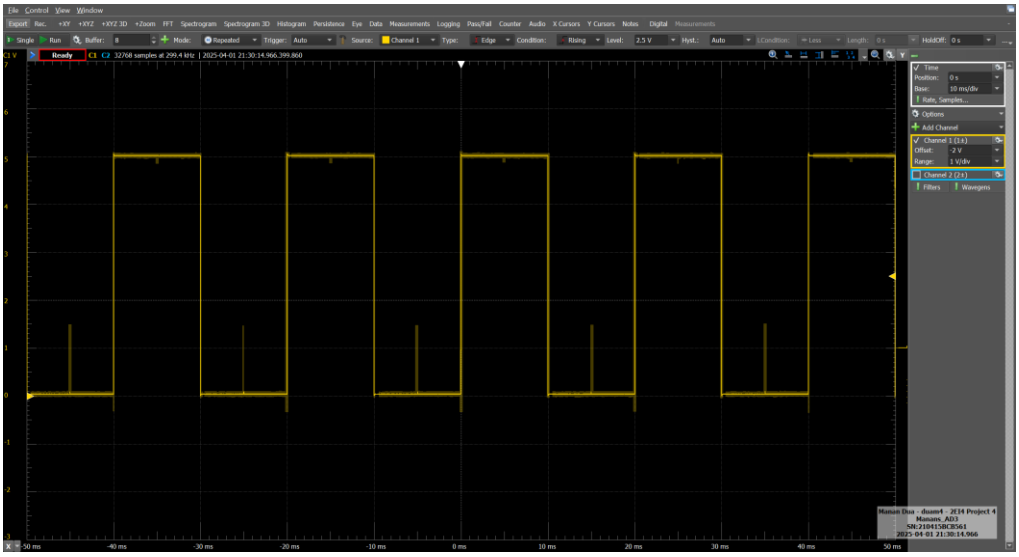

Figure 13: Oscilloscope output of CMOS XOR gate with pass transistors

Static Testing

Analyzing the output using the oscilloscope, we can measure V_H and V_L. From Figure 14, we can see that V_H = 5.01V and V_L = 0.06V, this value was the same with either input A or B fixed at +5V. Since this is a logic gate with only two states, these values are rounded to V_H = 5V and V_L = 0V.

Figure 14: V_H and V_L measured with input A fixed at 5V

Timing

Connecting the 100nF capacitor at the output allows us to measure the rise time and fall time of the circuit. τ_{rise} = 167us and τ_{fall} = 334us. Comparing these values to the initial circuit, the rise time is significantly lower, but the fall time is relatively the same. This can be attributed to the pass transistor, which has two MOSFETs in parallel, reducing their resistance and allowing it to rise more quickly. Whereas the other side which bridges a low connection does not have a pass transistor, so the resistance is the same, which is why the fall time is unchanged.

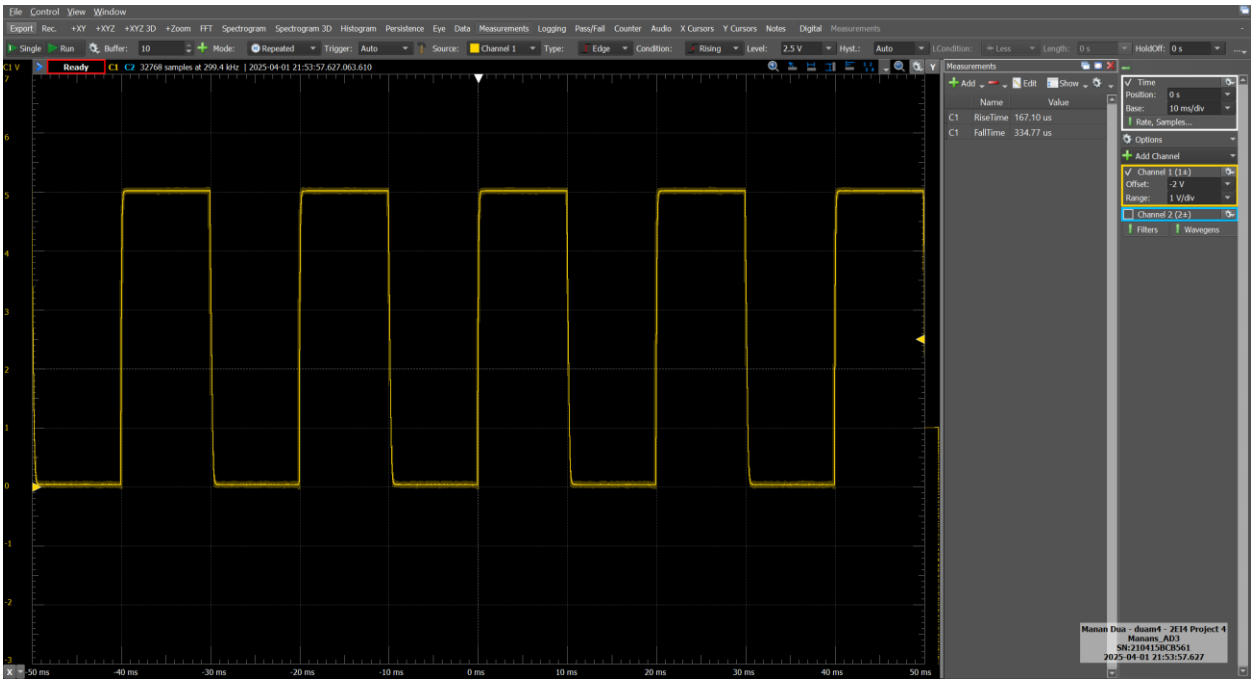

Figure 15: Circuit output with a 100nF capacitor connected to the output

Zooming into the plot, we can use cursors to find τ_{PLH} and τ_{PHL}. Once again, we can determine the high-to-low propagation delay by measuring the time between the input pulse reaching 50% of its transition from low to high and 50% of its transition from high to low. From Figure 16, we find that τ_{PLH} = 63us and from Figure 17, τ_{PHL} = 185us. τ_P can be found using the following formula: $\tau_P = \frac{\tau_{PLH}+\tau_{PHL}}{2} = \frac{63+185}{2} = 124us$. Comparing these values to the initial circuit, τ_{PLH} is significantly lower, whereas τ_{PHL} is relatively the same, τ_P is also lower due to the τ_{PLH} value. Similarly, this happens because of the pass transistor, which has two MOSFETs in parallel, resistance their capacitance and allowing it to rise more quickly, reducing its overall propagation delay.

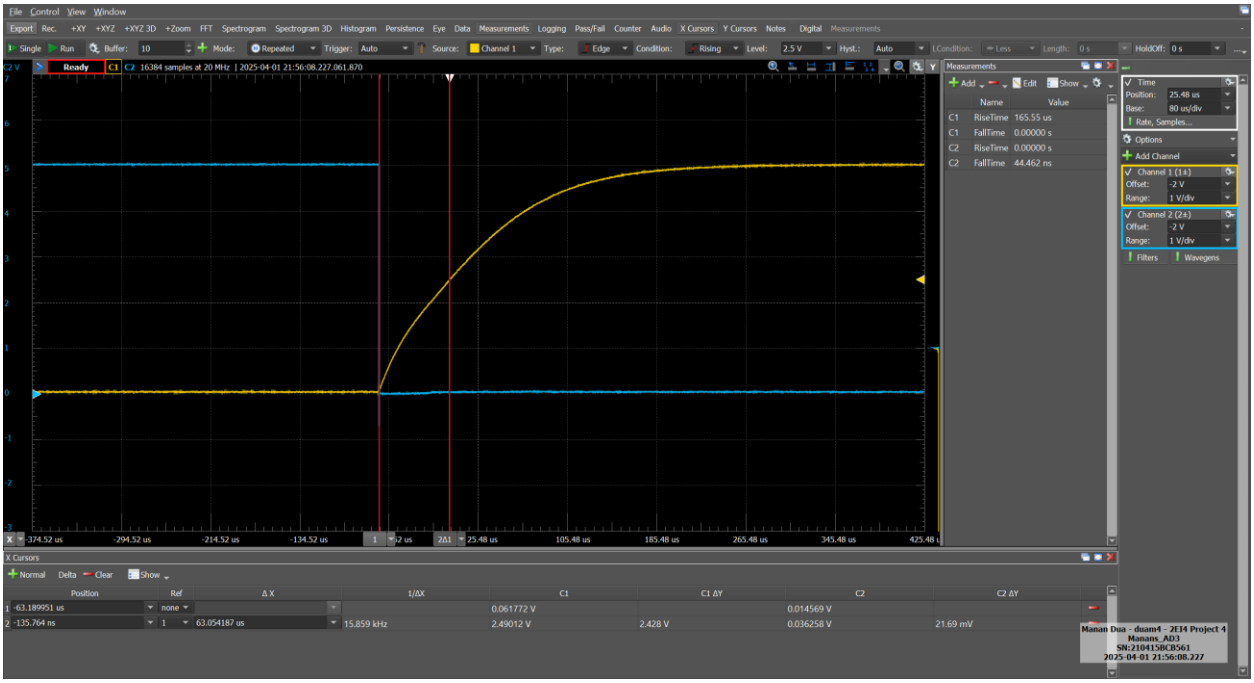

Figure 16: Zoomed plot of input and output waves with cursors to measure τ_{PLH}

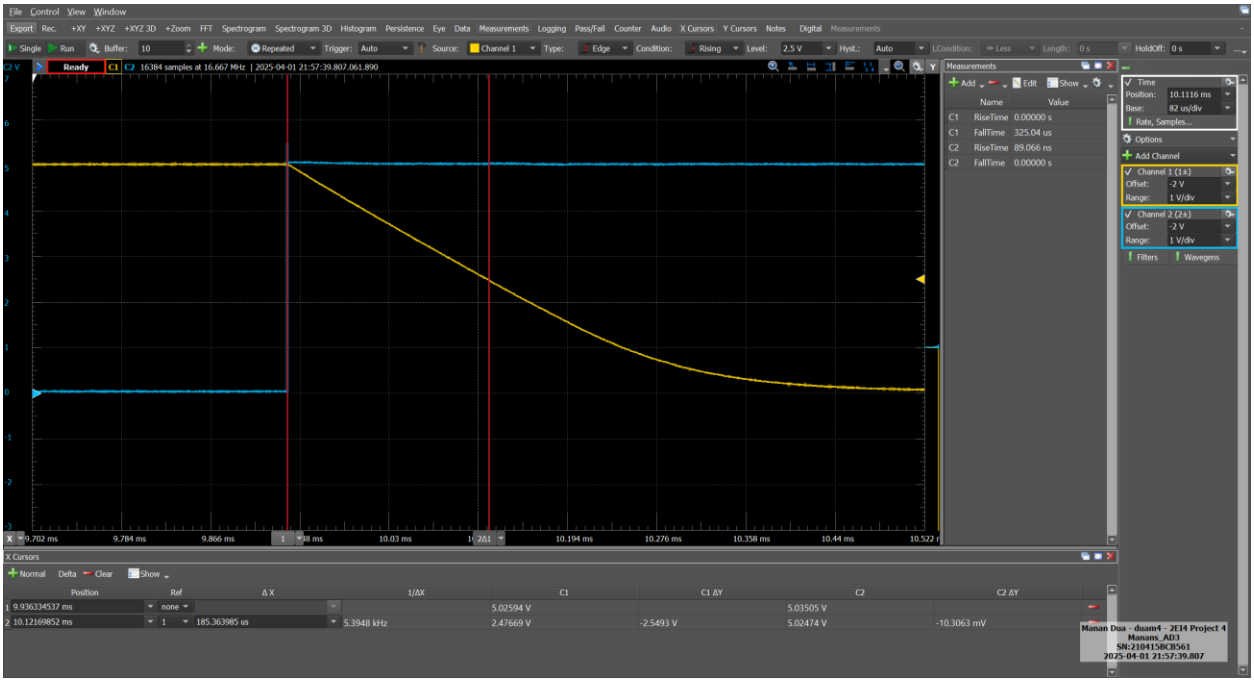

Figure 17: Zoomed plot of input and output waves with cursors to measure τ_{PHL}

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.

[2] R. Keim, “Introduction to Pass-Transistor Logic,” *Allaboutcircuits.com*, Dec. 18, 2018. https://www.allaboutcircuits.com/technical-articles/introduction-to-pass-transistor-logic/ (accessed Apr. 02, 2025).