ELECENG 2EI4
Project 5 – Digital-to-Analog Converter

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1 Summary

The objective of Design Project #5 is to design, simulate, and construct a 3-bit Digital-to-Analog Converter (DAC) with a full-scale analog voltage of V_{FS} = 5 V. The DAC design incorporates three digital input bits, with the weight of each bit determined by the ratio of the full-scale analog voltage to the total number of possible digital values for that bit. This setup ensures a proportional relationship between the output voltage and the sum of the input bits, each weighted according to its value. The design must not draw more than 1uA from the input bit lines. The design includes a weighted resistor network, which is then connected to a non-inverting unity-gain buffer.

2 Design

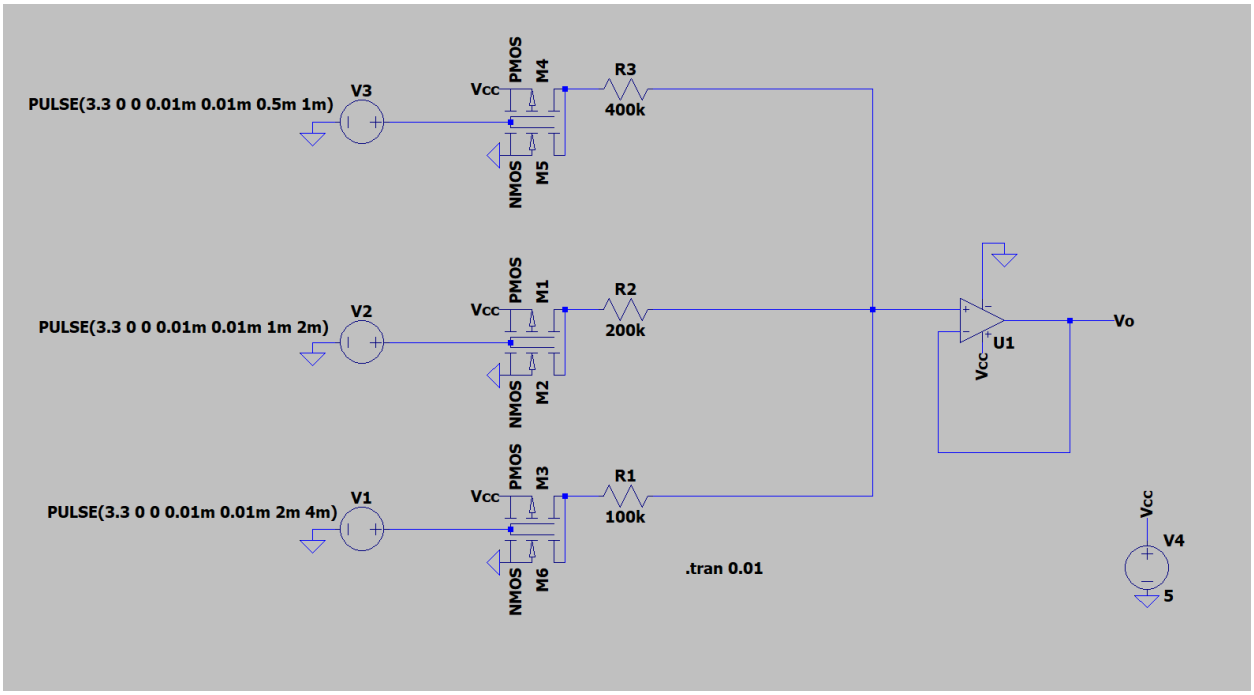

Figure 1: Circuit schematic of the Digital-to-Analog converter

The Digital-to-Analog Converter (DAC) circuit shown in the diagram converts a 3-bit digital input into a corresponding analog output voltage. The core of the design is a weighted resistor network, where each resistor value is determined by the binary weight of the corresponding digital input bit. This ensures that the output voltage is a proportional sum of the input bits, each multiplied by its respective weight. The resistors are labeled R1, R2, and R3, and they are arranged in a way that reflects the binary values of the input bits.

Each pulse generator (V1, V2, V3) represents the three digital bits. These pulses control the voltages that feed into both a P-MOS and N-MOS, which bridge either a high or low signal to the resistive network, creating the desired weighted sum for each bit. The MOSFETs are added to keep the current drawn from the data lines 0A, as the gate of a MOSFET draws minimal current. However, in doing so, the voltage is inverted due to the P-MOS source/gate being the highest potential and the N-MOS source/gate being the lowest potential. However, this doesn't affect the functionality of the DAC, it just interprets 5V as logic 0 and 0V as logic 1. The resulting voltage from the resistive network is then passed to a non-inverting unity-gain buffer. The op-amp buffer serves two purposes: it maintains the signal and isolates the output from the rest of the circuit, making the current through the op-amp close to 0A. This isolation is crucial to prevent loading effects, ensuring that the DAC operates accurately without interference from the rest of the circuit.

The resistors are selected to correspond to specific bits in the DAC by being in powers of 2 relative to a reference resistor value (R_{REF}). The resistor values follow a sequence of increasing powers of 2, ensuring that each bit contributes a weighted sum based on its binary significance. The bit weights are as follows:

- The LSB corresponds to a resistance of $R_1 = R_{REF}$
- The next bit corresponds to $R_2 = 2 * R_{REF}$
- The MSB corresponds to $R_3 = 4 * R_{REF}$

This scaling ensures that each resistor is weighed appropriately to match its corresponding bit in the binary system, and so the resulting output voltage reflects the correct binary sum.

R_{REF} = 100kΩ, this value was chosen such that the resistors are within the specified component kits.

$R_1 = 2^0(R_{REF})$ = 100kΩ ← made using 100kΩ resistor

$R_2 = 2^1(R_{REF})$ = 200kΩ ← made using 150kΩ + 2 x 24.9kΩ resistors in series

$R_3 = 2^2(R_{REF})$ = 400kΩ ← made using 4 x 100kΩ resistors in series

Reference(s) for Circuit Design

[1] W. Storr, "Binary Weighted Digital to Analogue Converter," Basic Electronics Tutorials, Jun. 10, 2022. https://www.electronics-tutorials.ws/combination/digital-to-analogue-converter.html (accessed Apr. 08, 2025).

[2] Simply Put, "Making a DAC Using a Resistor Ladder Op-Amp Weighted Summing Amplifier - Simply Put," *Youtube.com*, May 04, 2020. https://www.youtube.com/watch?v=kLUrVIhzeAY (accessed Apr. 08, 2025).

3 Measurement and Analysis

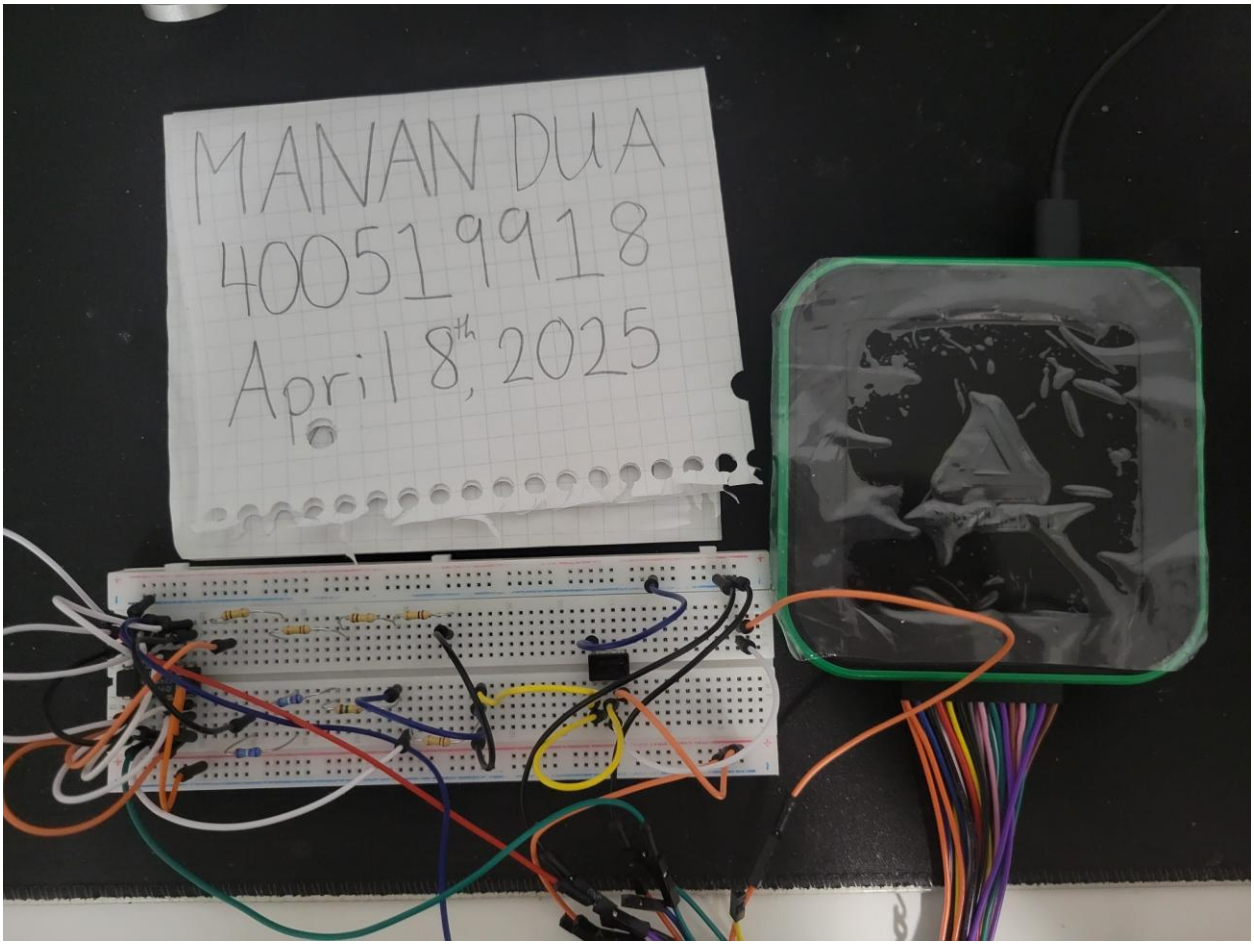

Figure 2: Physical circuit of the Digital-to-Analog converter

To test the circuit, the digital inputs were configured using the pattern functionality in the Waveforms software, with the input configuration shown in the figure below. Power supplies were used to provide +5 V to the operational amplifiers, and an oscilloscope was used to measure the output of the Digital-to-Analog circuit. Since there were not enough waveform outputs on the AD3, the GPIO pins were used for the pulse output. However, when using the pattern generator, these GPIO outputs are limited to 3.3V, which is lower than the project specification of 5V. However, this should not affect the functionality of the circuit.

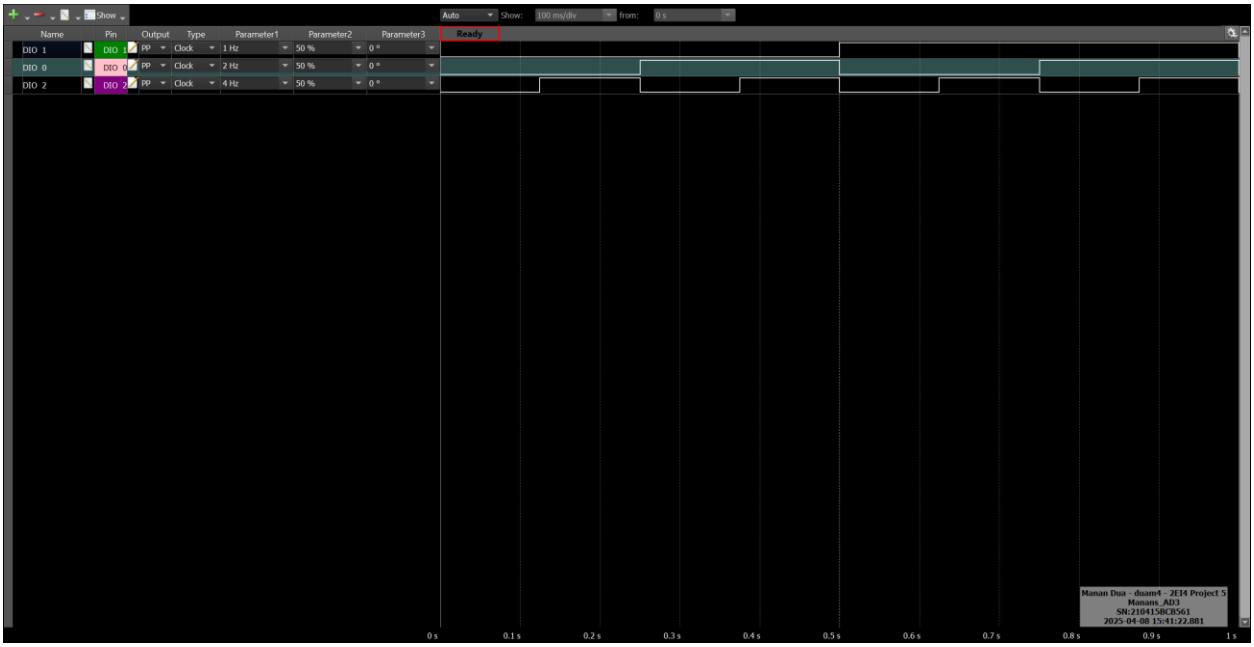

Figure 3: Digital Input Configuration using the Pattern Generator

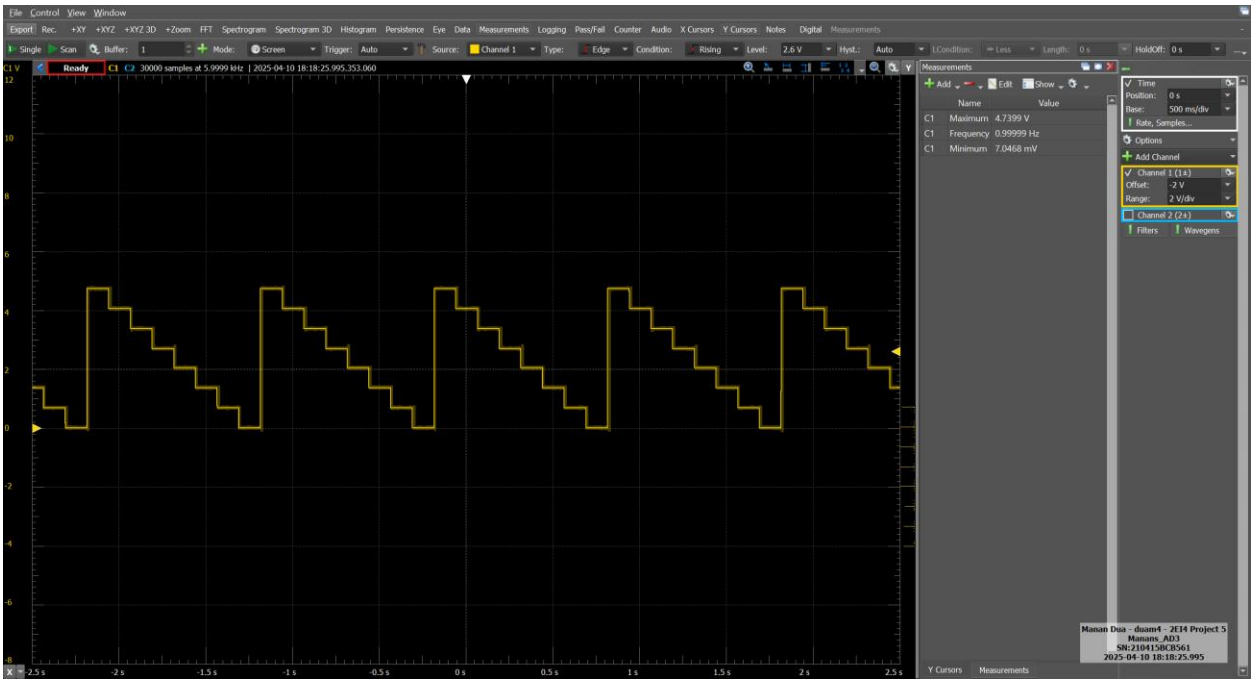

Figure 4: Oscilloscope output from the circuit

3.1 Gain Error

The gain error represents the difference between the experimental and expected gain, serving as a measure of the circuit's amplification accuracy. To calculate the gain error, we will find the difference between the expected peak voltage and the measured peak voltage, then divide that by the expected peak voltage. Since this circuit uses a unity-gain buffer, it is expected to have a gain of 1. Given that the voltage into the non-inverting input of the op-amp is 5V, the output from the op-amp is also 5V, however, there may be some error in the gain with a real op-amp. The circuit requirements are to have a full-scale voltage of 5V. When using cursors, it is found that the actual full-scale voltage is approximately 4.74V. When using the circuit requirements, the gain error can be calculated to be:

$$Error = \frac{V_{Expected} - V_{Actual}}{V_{Expected}} = \frac{5V - 4.74V}{5V} = 5.2\%.$$

3.2 Maximum Differential Non-Linearity

Maximum Differential Non-Linearity (MDNL) refers to the largest deviation between the ideal and actual change in the output of a digital-to-analog converter (DAC) as the input changes incrementally between two adjacent code values. For an ideal DAC, each step should have the same size, representing a constant change in voltage or current. However, in a real-world converter, these steps can vary slightly due to imperfections, which results in differential non-linearity. To calculate the MDNL, we first need to determine the ideal voltage, which is the voltage per step. This is found by dividing the total voltage by the total number of steps. For example, with a full-scale voltage of 5 V and 8 steps ($2^{3\ bits}$), the ideal voltage per step is:

$$V_{ideal} = \frac{Full\ Scale\ Voltage}{2^n - 1} = \frac{5V}{7} = 0.714V$$

Actual voltage per step, measured using cursors on the output waveform: $V_{actual} = 0.697V$

Once the ideal voltage is determined, we can calculate the MDNL by finding the difference between the ideal voltage and the measured step voltage and then dividing that difference by the ideal voltage:

$$MDNL = \frac{|V_{Ideal} - V_{Actual}|}{V_{Ideal}} = \frac{|0.7143V - 0.697V|}{0.7143V} = 0.0242 = 2.42\%.$$

The Maximum Differential Non-Linearity (MDNL) is 2.42% of the ideal step size in this case, which indicates the deviation from the ideal voltage step for this particular DAC.

3.3 Offset Error

Offset error refers to a consistent deviation in the output of a system, such as an Analog-to-Digital Converter (ADC) or Digital-to-Analog Converter (DAC), even when the input signal is ideally zero. Specifically, the offset error is the difference between the actual output and the expected output when the input is zero or at its reference voltage.

For example, when the expected output is 0V, using cursors, the actual output is measured as 7.05 mV. This deviation represents the constant offset in the system. The cause of the offset error can often be traced to imperfections in the system's components, such as op-amps, resistors, voltage drops caused by MOSFETs or other elements in the circuit. Therefore, with this circuit, the offset error of the circuit is 7.05 mV.

4 Discussion

4.1 Origins of errors

The errors observed in the circuit's output can occur from several factors. These include faulty connections in the wiring, limitations of the AD3 output, and inaccuracies in the resistor values. Faulty wire connections introduced noise that affected the circuit's performance. Additionally, as mentioned before, the output limitations of the AD3, specifically the Digital I/O's restriction to 3.3V, did not meet the 5V input requirement specified in the project manual. Simulating this circuit reveals that when the input voltage is set to the correct 5V specification, the output of the circuit remains unchanged, regardless of whether the threshold voltage of the MOSFETs is exceeded, as it is in the case of using 3.3V.

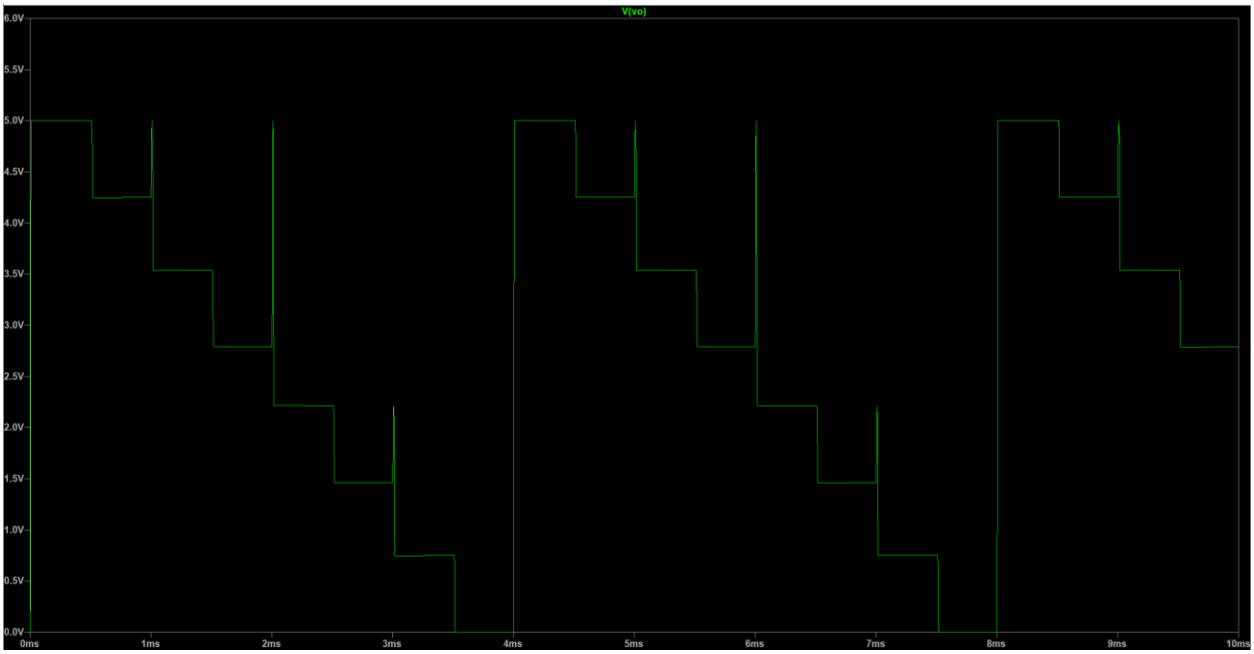

Figure 5: Simulated circuit output with input voltage as 5V

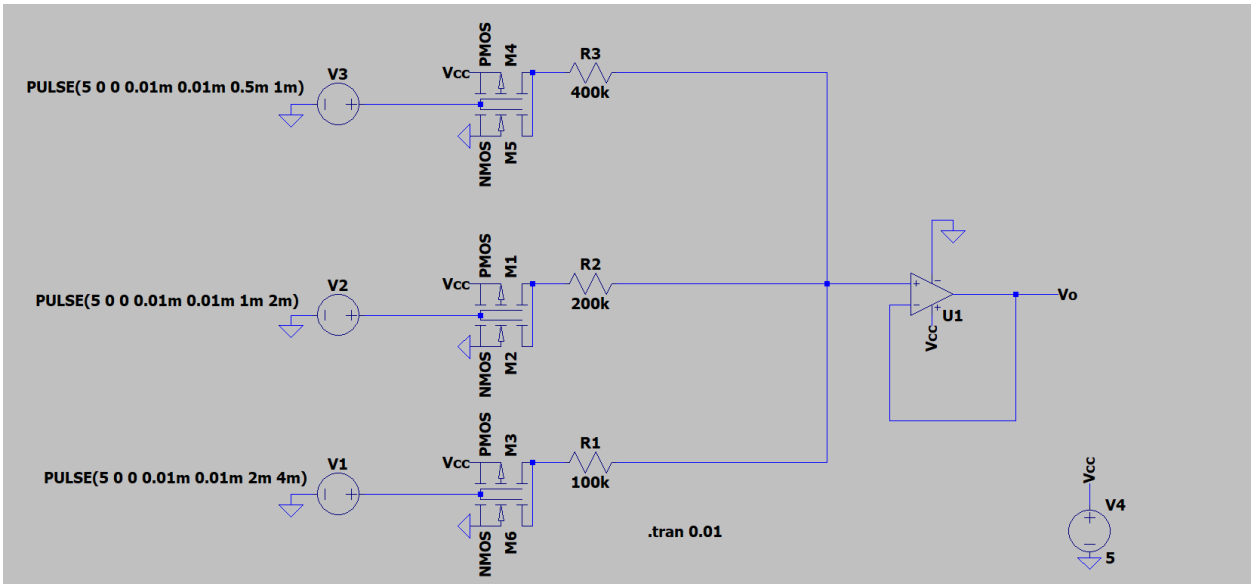

Figure 6: Circuit schematic with 5V input sources

Additionally, we were limited to the components in our 2EI4 and 2CI4 kits, where we only have a small number of resistors, op-amps and transistors, restricting the combinations of the resistor network. Increasing the values of the resistors would have led to a smaller drop across the MOSFETs and a more accurate output. If there had been no such limitation, I would have selected higher-value components to improve the accuracy of the circuit's output.

4.2 Alternate Designs

In my project, I compared several Digital-to-Analog Converter (DAC) circuits, including different types of resistor ladder networks, such as the binary weighted resistor network and the R-2R ladder network. I ultimately chose the binary weighted resistor network for my project due to its simplicity and ease of understanding, especially for a 3-bit system. This project allows each digital input bit to be directly associated with a specific resistor value, making the calculation of the output voltage straightforward and reducing the complexity of the design.

The other approach I examined was the R-2R ladder network. The R-2R arrangement has several benefits, most notably that it needs only two resistor values, R and 2R. This can lead to improved matching and less sensitivity to resistor tolerances, which becomes increasingly valuable when scaling the design up for higher resolutions. Although the R-2R ladder network can be designed to provide better performance in terms of component matching and error minimization, the binary weighted resistor network was selected for this project because the simple relationship between binary weights and resistor values made the design and implementation much simpler to perform for the 3-bit specification.