ELEC ENG 2EI4
Project 2– Voltage Controlled Switch

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Ideal switches

An ideal switch is a theoretical standard in electrical systems that specifies parameters for best performance. An ideal switch's properties include having a zero on-state resistance, which allows current to flow without voltage drop or power loss while maximizing efficiency and decreasing heat dissipation. Additionally, to avoid accidental leakage current and keep correct circuit isolation in the open state, it must have infinite off-state resistance. Furthermore, an ideal switch should be able to manage any voltage difference between its terminals without breaking down or showing nonlinear behaviour, ensuring expected operation regardless of the voltage applied. Finally, its on-state resistance must be constant and independent of voltage variations across its terminals, ensuring consistent performance.

Switch non-idealities

However, real switches do not perfectly follow these ideal properties due to physical and electrical limitations. These imperfections can impact their performance and reliability, making it important to consider their effects in practical applications. These non-idealities can be measured to be taken into account when completing theoretical calculations.

1. **Non-Zero On-State Resistance:**
   When closed, real switches have a small but finite resistance, known as contact resistance. This resistance can cause a voltage drop and power dissipation, which is especially noticeable in high-current applications.
2. **Finite Off-State Resistance:**
   In the open state, real switches may allow a small leakage current due to finite insulation resistance, leading to unintended current flow.
3. **Limited voltage range:**
   Real switches have a limited voltage range beyond which they may fail or show nonlinear behaviour.
4. **Not Bidirectional:**
   In real switches, their internal resistance may vary depending on the voltage applied and the direction of the flow of current, meaning they may only operate in a single direction.

Test plan

Switch 1

The first non-ideality is the non-zero resistance at the on state of the switch, applying a small voltage drop between the terminals since a real switch has a quantifiable resistance. For switch 1, this can be tested by measuring the voltage at the nodes before and after the switch and calculating the voltage difference. This can be done by connecting V_1 to 5V, $V_{control}$ to 0V, V_{supply} to 5V and connecting a resistor with a known voltage to V_2 and ground. By measuring the potential at V_2, which is the potential across the resistor and treating this as a voltage divider, the internal resistance of the switch can be calculated. For this and all other tests requiring a load resistor, I will be using a 10kΩ resistor, this is because using a larger resistor value would make the voltage drop across the MOSFETs lower, however, it isn't too large, so it guarantees a measurable voltage drop. The next non-ideality is that in the off state, some current is expected to leak due to the switch's finite but large resistance. For switch 1, this can be calculated by connecting V_1 to 5V, $V_{control}$ to 5V, and V_{supply} to 5V, connecting a known resistor to V_2, measuring the voltage across it, and calculating the current using Ohm's law. This is the leakage current of the MOSFET in the off state. The next non-ideality is that a switch will only operate with an input voltage within its specific range. For switch 1, this can be measured by supplying a sinusoidal voltage to V_1 from 0V to 5V, setting $V_{control}$ to 0, and measuring the potential at V2, and observing the output to determine the threshold for which the switch will operate normally. The last non-ideality is that a switch cannot conduct bidirectionally. For switch 1, this can be measured similarly to first non-ideality, but by now applying the voltage at V_2 and connecting a pull-down resistor to V_1 and measuring the potential at the resistor and calculating the internal resistance of the switch in the reverse direction using a current divider.

Switch 2

Measuring the on-state resistance for switch 2, follows a similar procedure to switch 1, but now we have to measure the voltage drop across both output terminals of the device. This can be done by first connecting V_1 to 5V, $V_{control}$ to 0V, V_{supply} to 5V and measuring the voltage at Va and calculating its forward resistance, then switching $V_{control}$ to 5V and measuring the voltage at V_B and calculating its forward resistance. This method also requires connecting a pull-down resistor to V_A and V_B. To measure the off state current leakage in switch 2, we must measure the leakage current at both output terminals in their respective off states. This can be done with the same parameters as switch 1, but by first setting $V_{control}$ to 0V and measuring the leakage current at V_B with a pull-down resistor, then setting $V_{control}$ to 5V and measuring the leakage current at V_A with a pull-down resistor. To measure the operating voltage of switch 2, we must measure the resistance and observe the output at both output terminals. This can be done by supplying a sinusoidal voltage to V_1 from 0V to 5V, connecting $V_{control}$ to 0 and measuring the voltage at V_A with a pulldown resistor and using a voltage divider, then switching $V_{control}$ to 5V and measuring the voltage at V_B with a pulldown resistor and using a voltage divider. The last non-ideality is that a switch cannot conduct bidirectionally. For switch 2, this can be measured similarly to first non-ideality, but by now supplying the voltage at V_A and V_B and connecting a pull-down resistor to V_1 and measuring the potential at the resistor and calculating the internal resistance of the switch in the reverse direction from both terminals independently using a voltage divider.

Switch Type 1

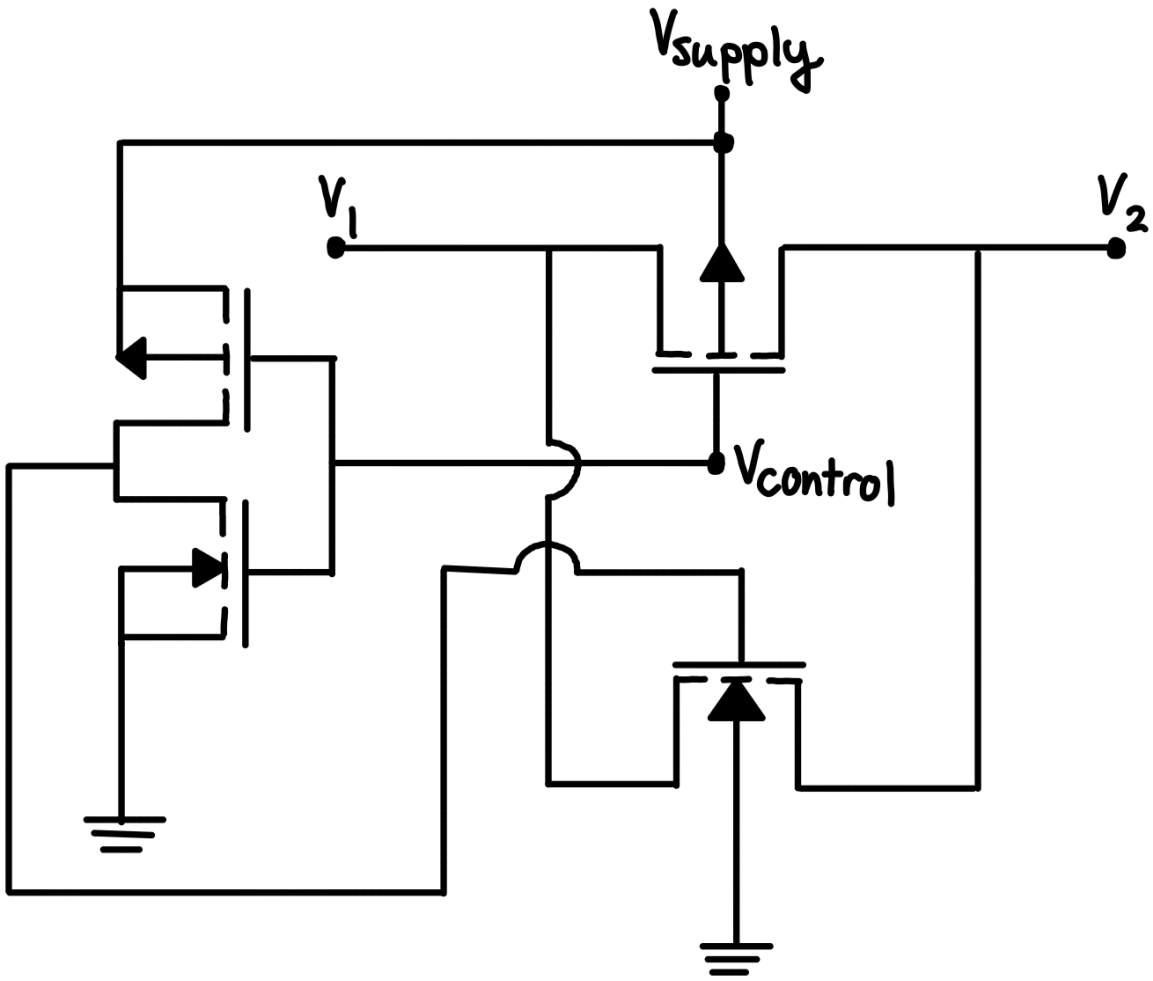

Figure 1: Hand-drawn Schematic of circuit of switch type 1

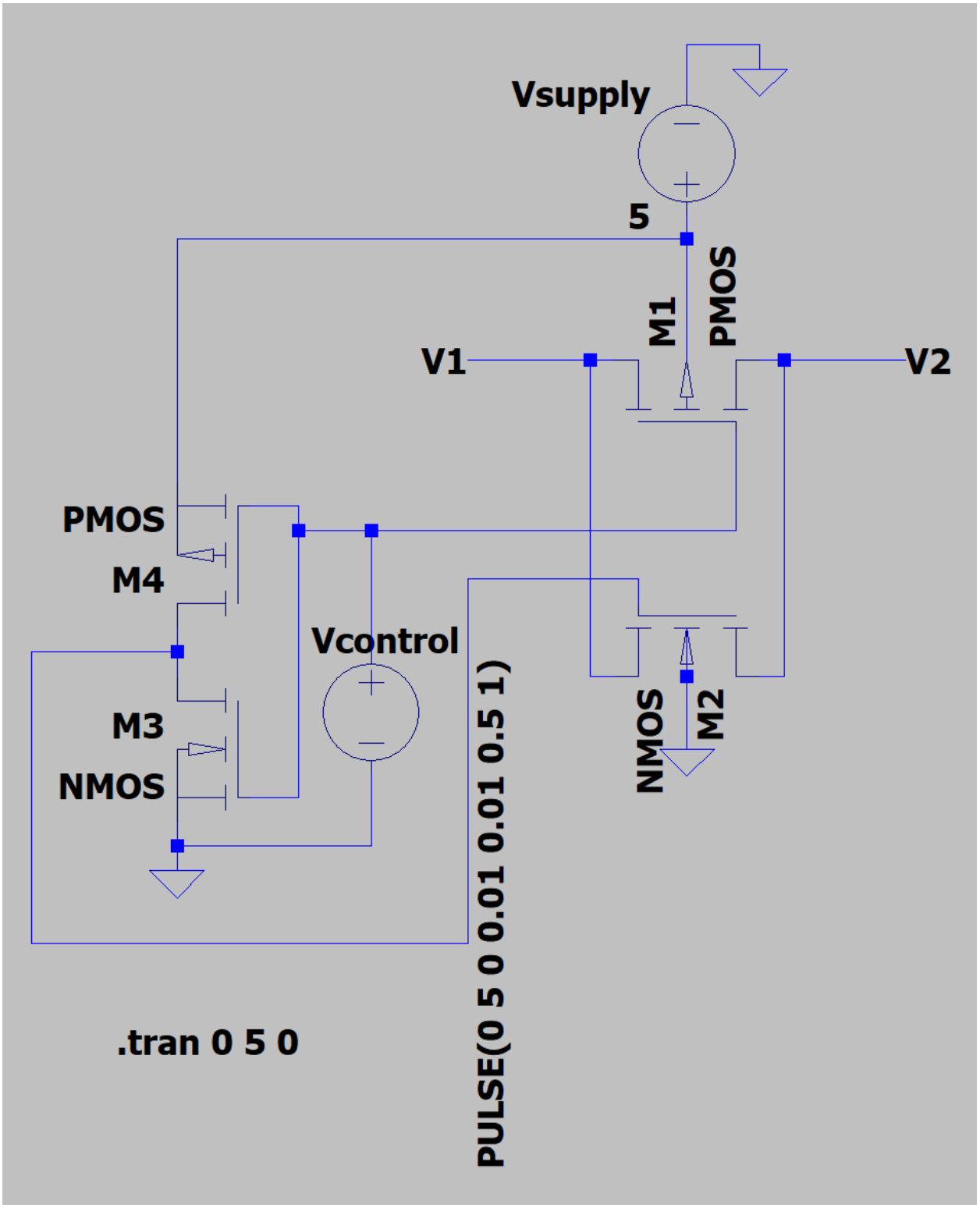

Figure 2: LTSpice schematic of circuit of switch type 1

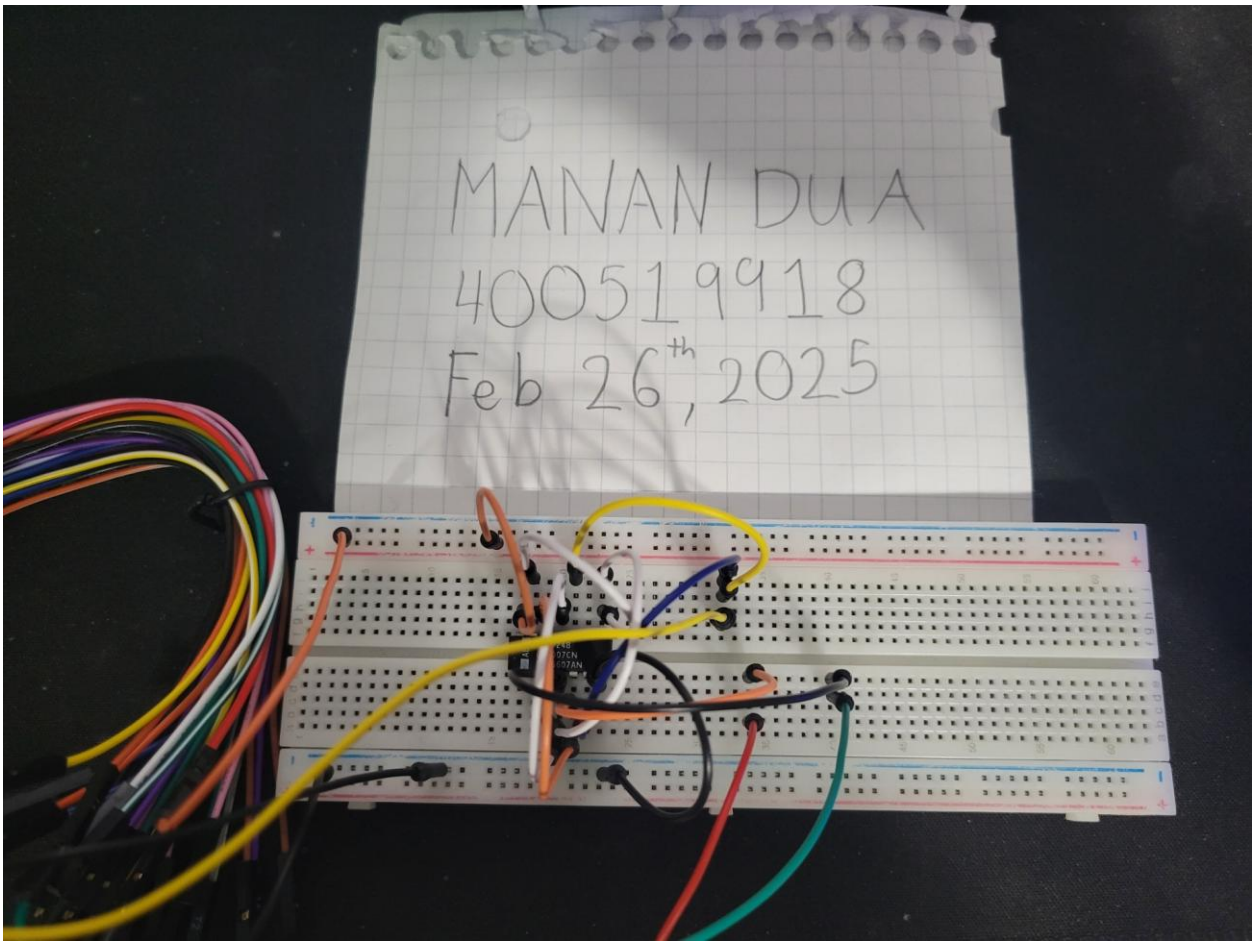

Figure 3: Physical circuit of switch type 1

ON Resistance

To measure ON resistance, a resistor can be added to one of the terminals of switch and a voltage source to the other. Using this resistor the current and voltage drop across the switch can be measured, which can be used to calculate the ON resistance.

Test Conditions:

$V_{supply} = 5V$

$V_1 = 5V$

$V_{control} = 0V$

- There is a 10kΩ pull-down resistor connected to V_2

Figure 4: Voltage at pull-down resistor connected to V_2 with $V_{control} = 0V$

From this, V_2 is found to be around 4.75V

This means $V_2 = V_1(\frac{10k\Omega}{10k\Omega + R_{on}})$

$R_{on} = \frac{5V(10k\Omega)}{4.75V} - 10k\Omega = 526\Omega$

Leakage Current

To measure Leakage current in the OFF state, the voltage at V_1 should still be applied, however the switch should now be off, this way we can measure the voltage drop across the switch in its off state and measure its resistance.

Test Conditions:

$V_{supply} = 5V$

$V_1 = 5V$

$V_{control} = 5V$

- There is a 10kΩ pull-down resistor connected to V_2

Figure 5: Voltage at pull-down resistor connected to V_2 with $V_{control} = 5V$

From this V_2 is found to be around 19.2mV

From this, using Ohm's law, the current can be calculated to be $I = \frac{19.2mV}{10k\Omega} = 1.92\mu A$

This gives the switch an OFF resistance of $R_{off} = \frac{5V(10k\Omega)}{19.2mV} - 10k\Omega = 2.59M\Omega$

Voltage Range

To test the operating voltage range of the switch, a sinusoidal wave can be inputted to one of the switch terminals and measured at the other to see at which voltages the switch operates properly.

Test Conditions:

$V_{supply} = 5V$

$V_1 = 5V_{PP}$ sinusoidal wave at 10Hz, 2.5V offset

$V_{control} = 0V$

- There is a 10kΩ pull-down resistor connected to V_2

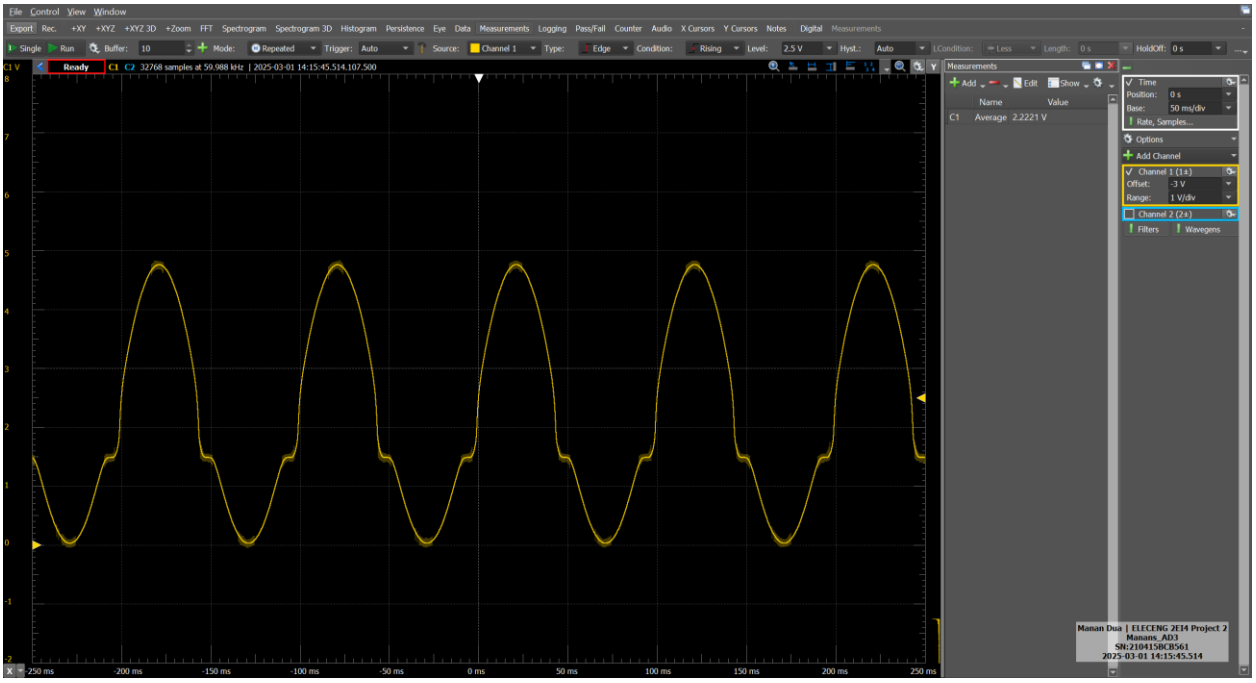

Figure 6: Voltage at pull-down resistor connected to V_2 with sinusoidal input

The switch operates at most of the range between 0V and 5V. However, there is some deviation at around 2.4V. This is likely to be the switching voltage where the switch has an intermediate state between on and off due to the threshold voltages of the MOSFETs and differences in resistance between the NMOS and PMOS.

Bidirectional operation

To test if the switch operates in any direction, the terminal that the input voltage was connected to in previous tests can be swapped to the other terminal and both forward and reverse ON resistances can be calculated. The forward ON resistance was already found in the first non-ideality so, now reverse ON resistance can be calculated.

Test Conditions:

$V_{supply} = 5V$

$V_2 = 5V$

$V_{control} = 0V$

- Voltage is being measured at V_1
- There is a 10kΩ pull-down resistor connected to V_1

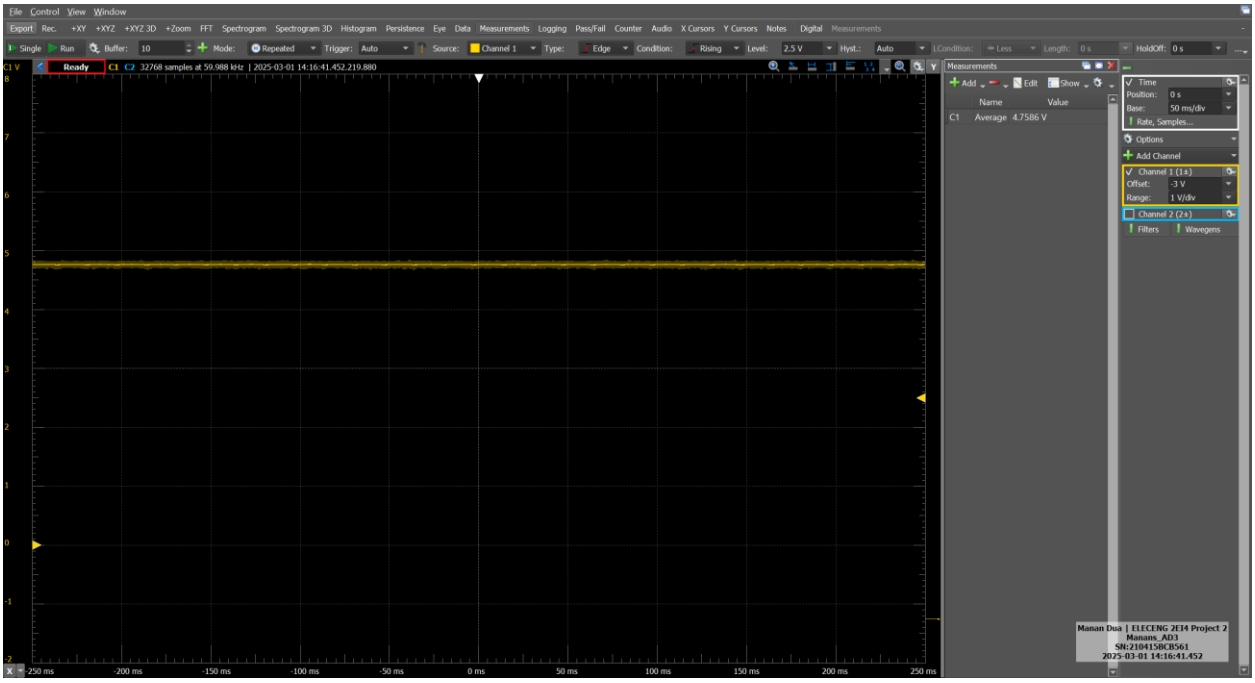

Figure 7: Voltage at pull-down resistor connected to V_1 with input at V_2

From this, V_2 is found to be around 4.76V

This means $R_{on} = \frac{5V(10k\Omega)}{4.76V} - 10k\Omega = 504\Omega$

The graph produced is very similar to the first non-ideality and has similar resistances, which means the switch operates in both directions.

Theoretical explanation

The design of the switch is based on a Transmission Gate which is a bilateral switch consisting of NMOS and PMOS transistors controlled by externally applied voltage levels [2]. To test this circuit, V_{supply} was set to 5V, $V_{!}$ was set to a $5V_{PP}$ sinusoidal wave at 10Hz, and $V_{control}$ was set to a $5V_{PP}$ square wave at 1Hz.

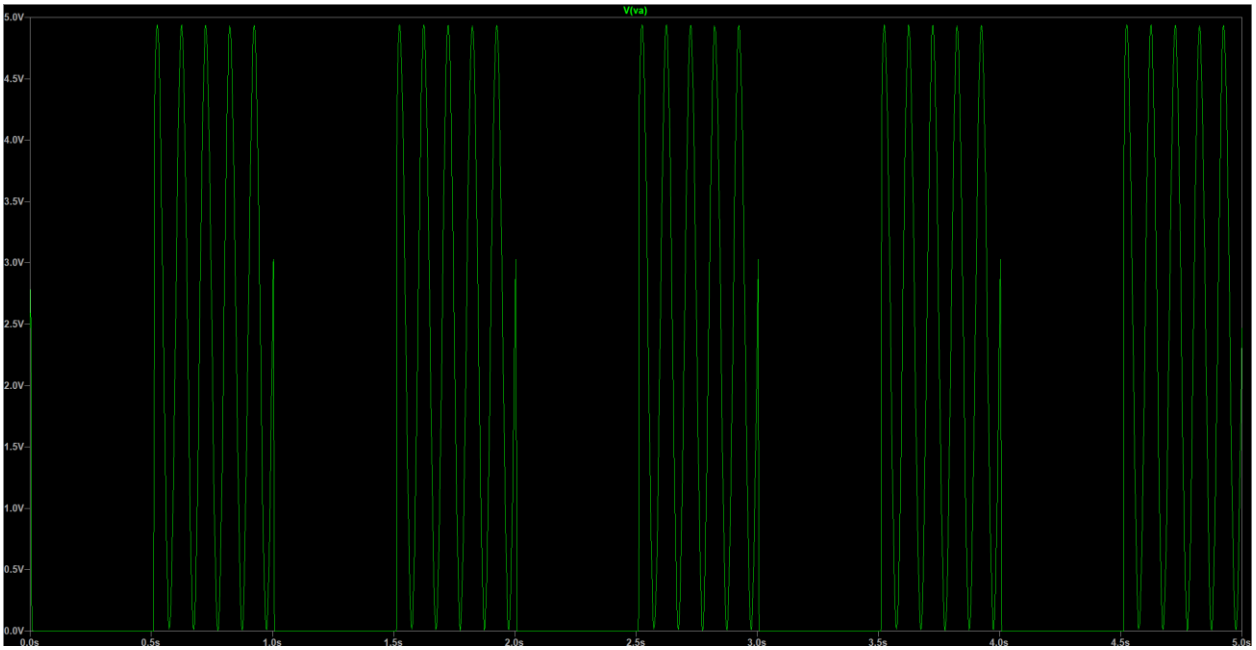

Figure 8: LTSpice simulation of the circuit

For both MOSFETs to be on at the same time, the NMOS needs to be provided the inverse of $V_{control}$. This is what the additional two MOSFETs are on the left of the schematic. With the NMOS and PMOS connected in series with the inverted output connected to both of their drains and their gates tied together to $V_{control}$, only one of the MOSFETs is guaranteed to be on at a time, shorting their drain to either ground or V_{supply}. When $V_{control}$ is on, the PMOS is in cutoff and the NMOS is saturating, shorting the drain to ground, which is the inverse of $V_{control}$. Similarly, if $V_{control}$ is off, the PMOS is in saturation and the NMOS is in cutoff, shorting the drain to 5V, which is the inverse of $V_{control}$.

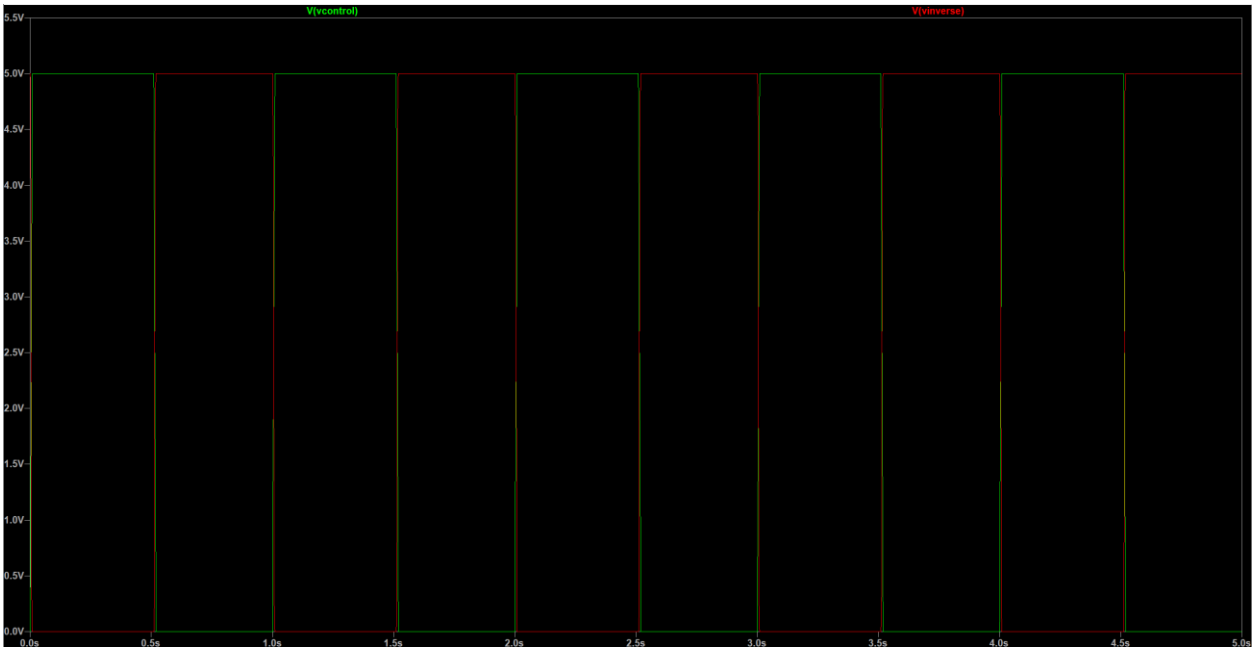

Figure 9: plot of $V_{control}$ and $V_{inverted}$

To measure the ON resistance of the switch, a pull-down resistor needed to be added to one of the terminals to measure the current through the switch. However, changing the load resistance changes the voltage drop across the switch and the current through the switch. This means the resistance of the switch changes depending on the load resistance.

Voltage at V_2 with load resistance of 940kΩ:

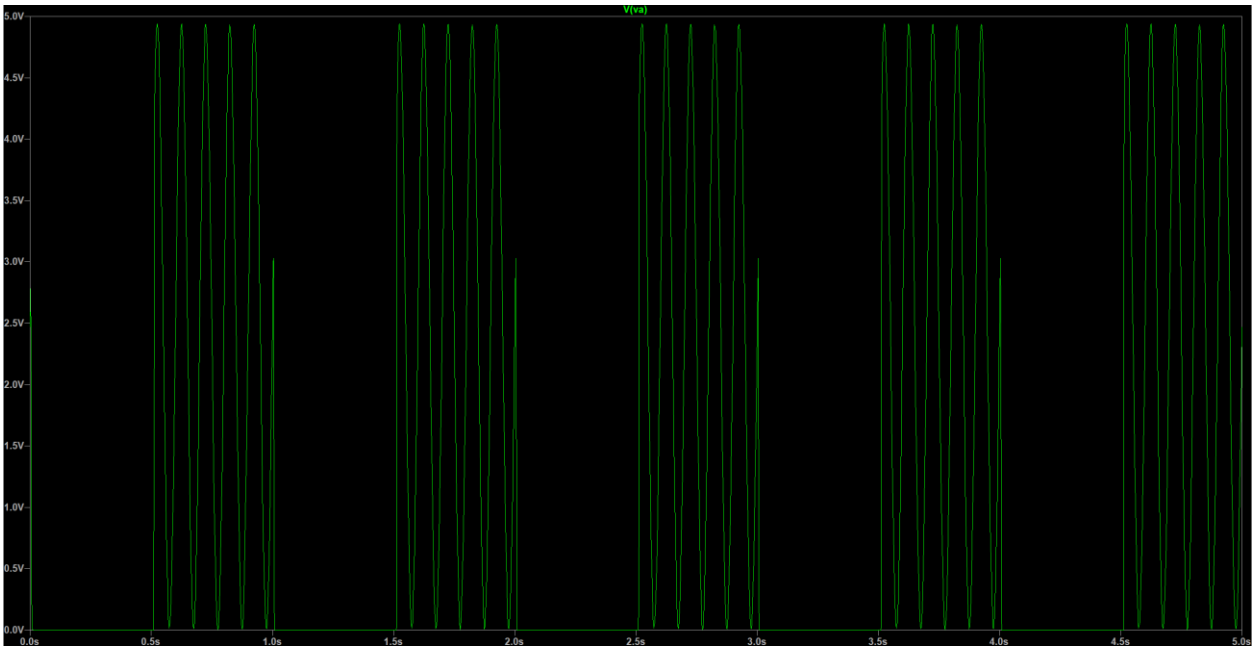

Figure 10: Simulation output with 940kΩ pull-down resistor

Voltage at V_2 with load resistance of 10kΩ:

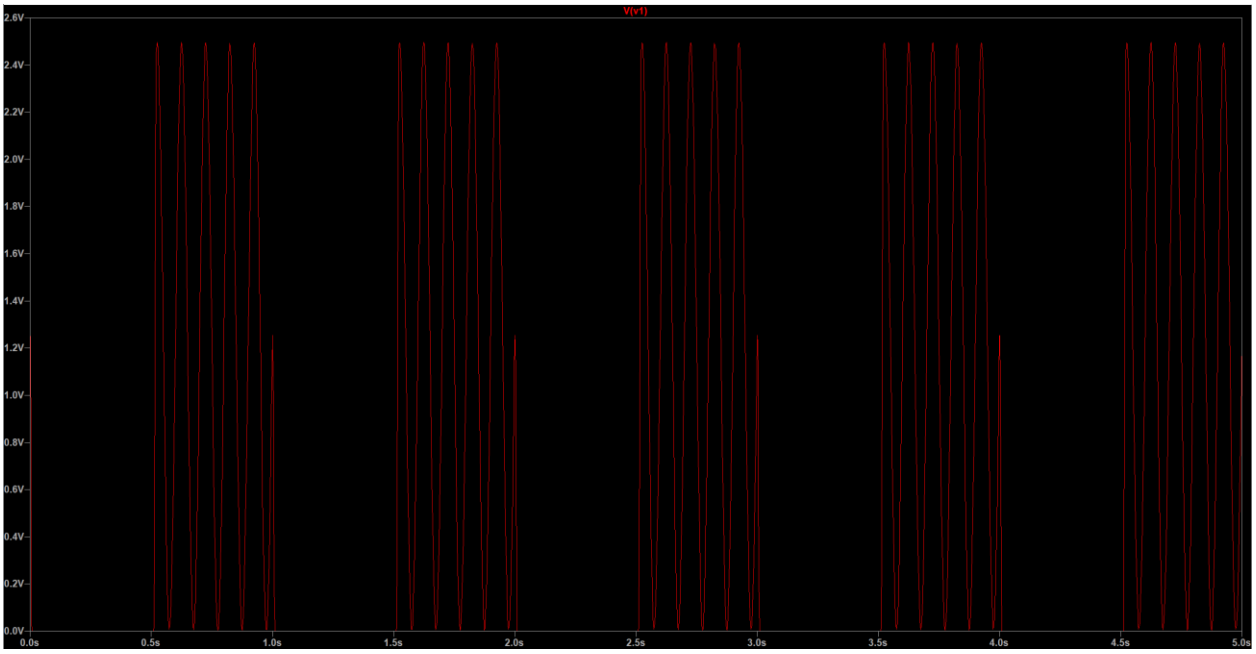

Figure 11: Simulation output with 10kΩ pull-down resistor

This would explain why the ON resistance seemed unusually high. It's also noticeable that the actual measurement and simulation do not line up, since LTSpice indicates a much larger voltage drop of 2.5V, which would give $R_{on} = \frac{5V(10k\Omega)}{2.5V} - 10k\Omega = 10k\Omega$. This could be due to LTSpice having different parameters of the MOSFETs. Since I used a 10kΩ resistor, the current flowing through it was very small, which made the resistance of the switch higher. The switch ideally should have an internal resistance of 2-3Ω [2]. Based on the work completed in lab 3, I found that the NMOS had the parameters: V_T = 1.8V and K = $0.4767\frac{mA}{V^2}$, and the PMOS had the parameters: V_T = -1.73V and K = $0.5725\frac{mA}{V^2}$.

The leakage current is theoretically 0A from the cutoff definition of the MOSFET. However, the hardware cannot be perfectly ideal and there will be a small amount of current leaking. However, the LTSpice MOSFETs do not have the same parameters as the physical IC and show a different voltage drop with the switch off. Adding cursors to the simulation shows that the voltage drop across the switch is around 150nV. This would give a leakage current of: $I = \frac{150nV}{10k\Omega} = 15pA$. This is much smaller than what was observed, again due to the physical MOSFETs having different parameters.

The switch contains both a PMOS and NMOS in parallel with each other and both on at the same time so that the switch can operate with any voltage range between the highest and lowest potential connected to their bulks respectively. This is because if the threshold voltage is not met for one of the MOSFETS, it guarantees the other MOSFET to be on since there is both a PMOS, which has a negative threshold voltage, and an NMOS, which has

a positive threshold voltage. This means no matter the voltage applied, one of the MOSFETs will be on. This can be shown through a simulation of the circuit when supplying a sinusoidal wave to V_1 and measuring the potential at V_2. Based on this, the voltage range for which the switch operates is almost all voltages between 0 and 5V. However, there is a little bit of inconsistency at 2.4V from the results. This is likely due to the MOSFETs having an intermediate state where they are not fully conducting. This may be because the NMOS conducts positive voltage slightly worse than a PMOS, making it a "poor 1" [1]. Additionally, the MOSFETs have a small internal capacitance that would change the output voltage at a sudden change in the capacitor's voltage. The simulated results do not show this likely because the software does not consider these discrepancies between the PMOS and NMOS.

The switch is designed to operate in any direction, since the bulk of the MOSFETs are not tied to the source, allowing them to be symmetrical and allow current to flow in any direction. The simulation in LTSpice also confirms this as the voltage supply can be connected to either V_1 or V_2 and the output is normal in both directions.

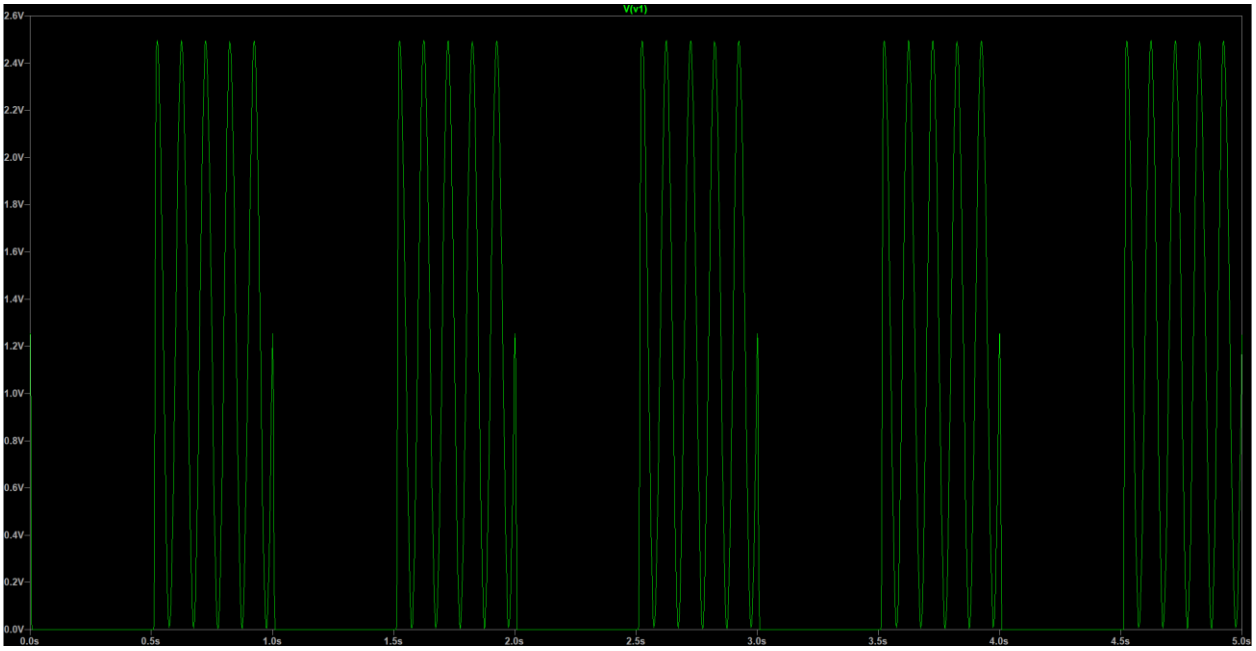

Figure 12: Simulation output at V_1 with input signal at V_2

This graph now has the voltage supplied at V_2 and measuring at V_1. Comparing this graph with the previous graph, using a 10kΩ pull down resistor, shows the output is the same, indicating the switch will operate in any direction, and with any voltage.

Design Trade-offs

This switch design is quite complex as it requires 4 MOSFETs and according to the pinout of the CD4007 IC, the remaining 2 MOSFETs may not be able to be used separately, making those additional MOSFETs a waste. The chip costs $0.92, and we are only able to use 4 of the 6 MOSFETs based on how the IC is wired and how this circuit is designed, making large-scale applications expensive and wasteful. Another trade-off is the poor performance of the NMOS since it introduces an inconsistency at a certain voltage. This could be solved by just removing the NMOS from the circuit, which would also remove the need for an inverter, however, the circuit may no longer operate at the full voltage range, so the change would not make the circuit better.

Switch type 2

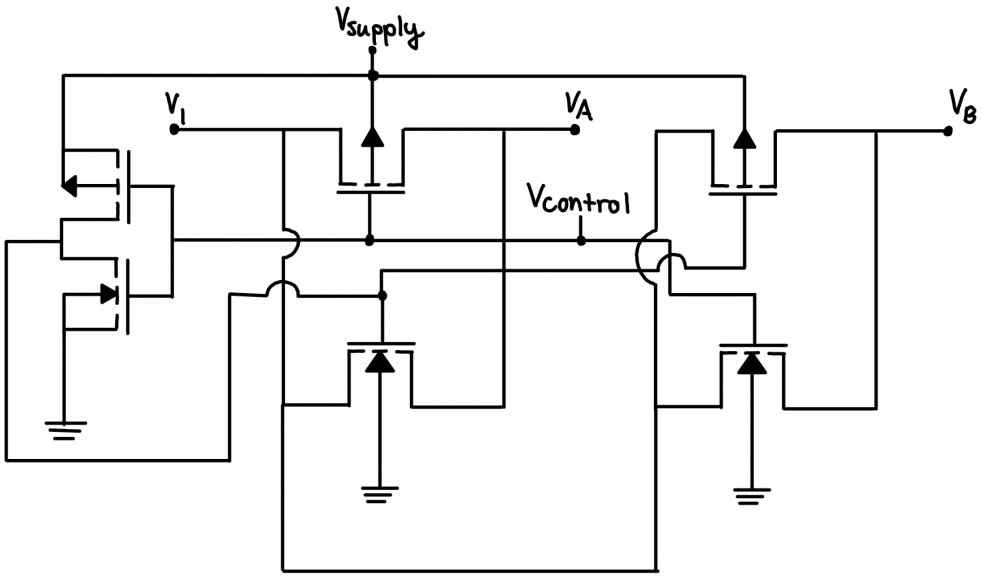

Figure 13: Hand-drawn Schematic of circuit of switch type 2

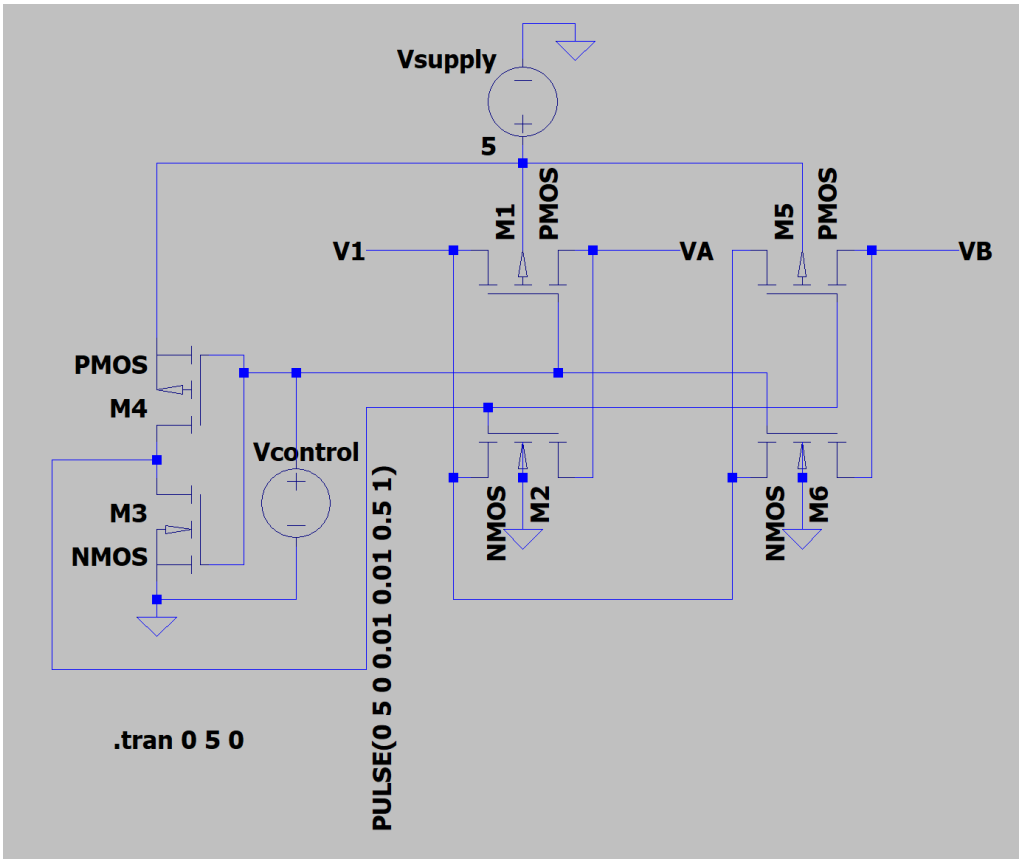

Figure 14: LTSpice Schematic of circuit of switch type 2

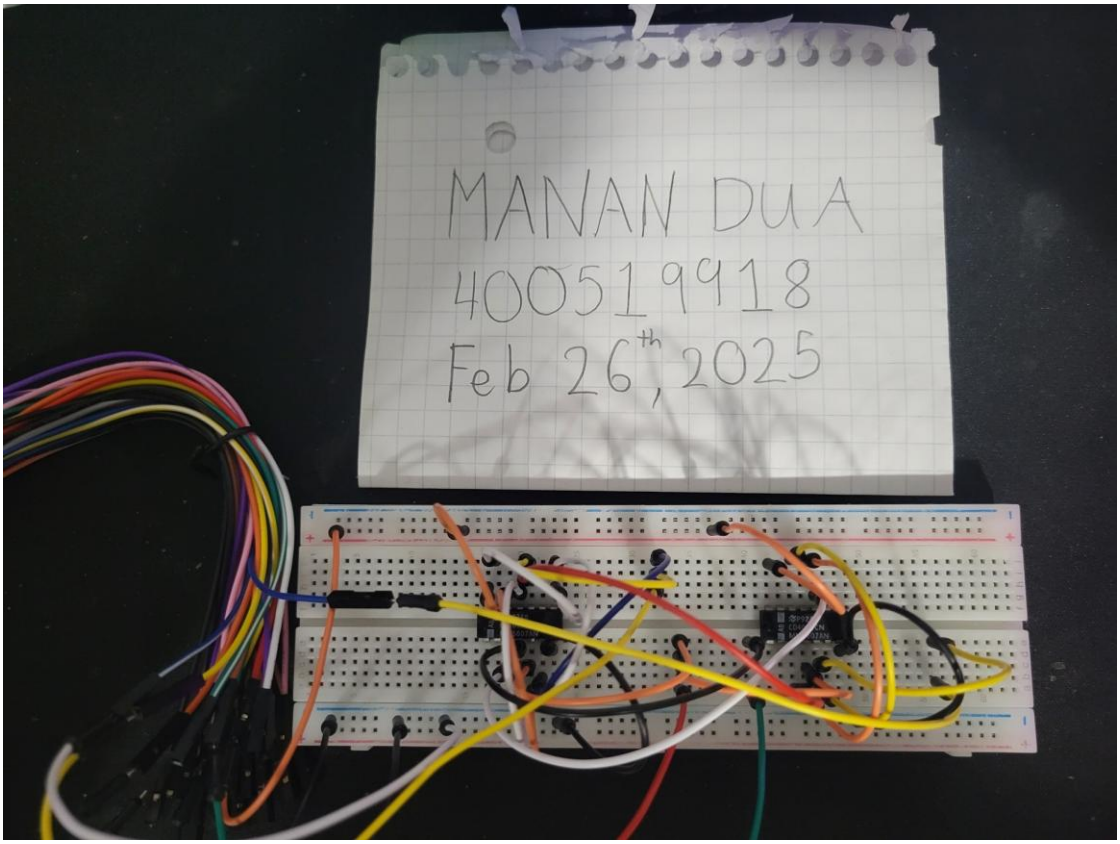

Figure 15: Physical circuit of switch type 2

For testing this circuit at terminals V_A and V_B, channel 1 (yellow) will be connected to V_A, and channel 2 (blue) will be connected to V_B.

ON Resistance

Since this switch now has two output terminals, we must check the ON resistance on both terminals. The procedure is the same as the first switch, but now adding a pull-down resistor to V_A and V_B and measuring the voltage across both terminals with both $V_{control}$ situations.

Test Conditions:

$V_{control} = 0V$

$V_{supply} = 5V$

$V1 = 5V$

- The 10kΩ pull down resistor is connected to V_A and V_B

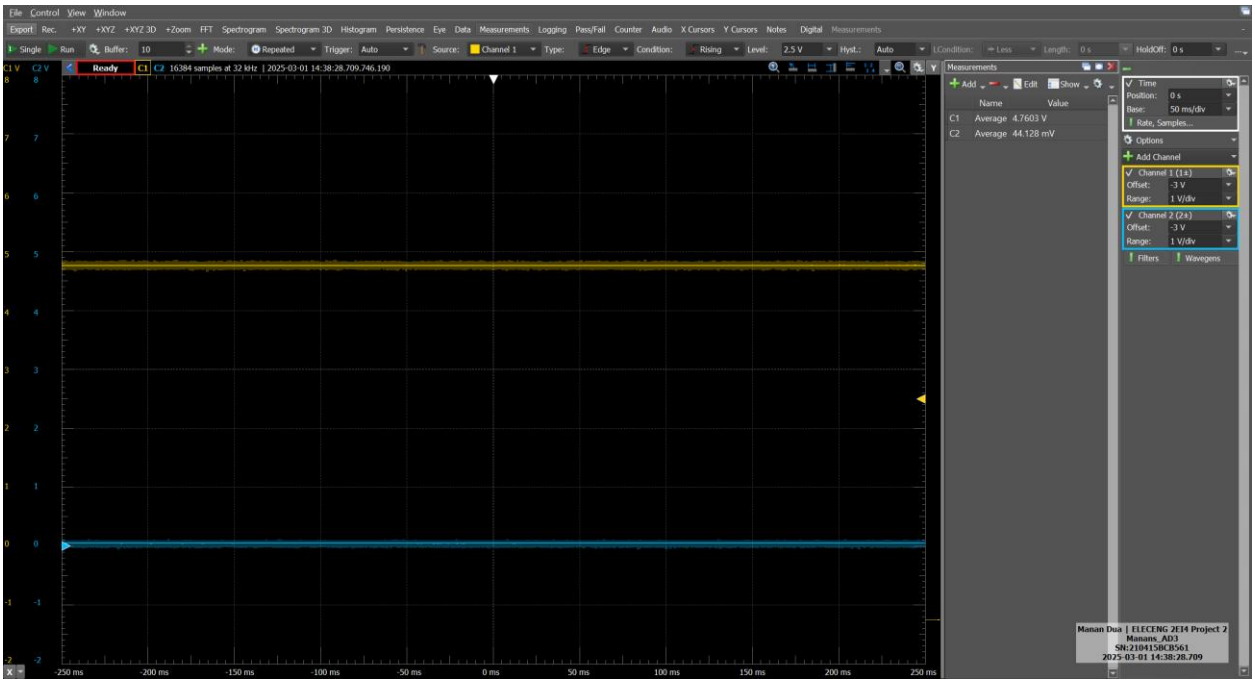

Figure 16: Output of physical circuit at V_A (yellow) and V_B (blue) with $V_{control} = 0V$

From this, V_A is found to be around 4.76V

This means $V_A = V_1(\frac{10k\Omega}{10k\Omega+R_{on}})$

$R_{on} = \frac{5V(10k\Omega)}{4.76V} - 10k\Omega = 504\Omega$

Next, set

$V_{control} = 5V$

$V_{supply} = 5V$

$V_1 = 5V$

- The 10kΩ pull-down resistor is connected to V_A and V_B

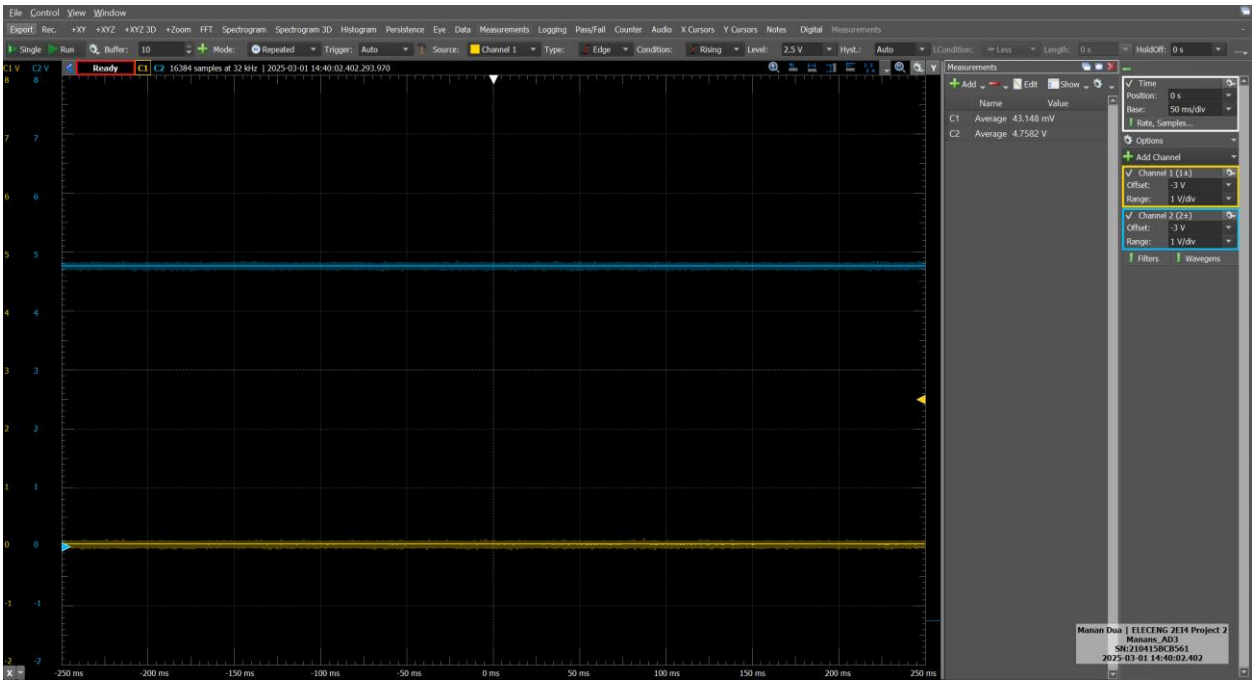

Figure 17: Output of physical circuit at V_A (yellow) and V_B (blue) with $V_{control} = 5V$

From this, V_B is found to be around 4.76V

This means $V_B = V_1(\frac{10k\Omega}{10k\Omega+R_{on}})$

$R_{on} = \frac{5V(10k\Omega)}{4.76V} - 10k\Omega = 504\Omega$

The resistance across either of the output terminals of the switch is identical, meaning the difference in voltage in either output will be the same.

Leakage Current

Since this switch will always be connected to either of the terminals, we need to check the current being leaked at the terminal that is off. First measure the voltage of V_B when it is off, then measure the voltage at V_A.

Test Conditions:

$V_{control} = 0V$

$V_{supply} = 5V$

V1 = 5V

- The 10kΩ pull-down resistor is connected to V_A and V_B

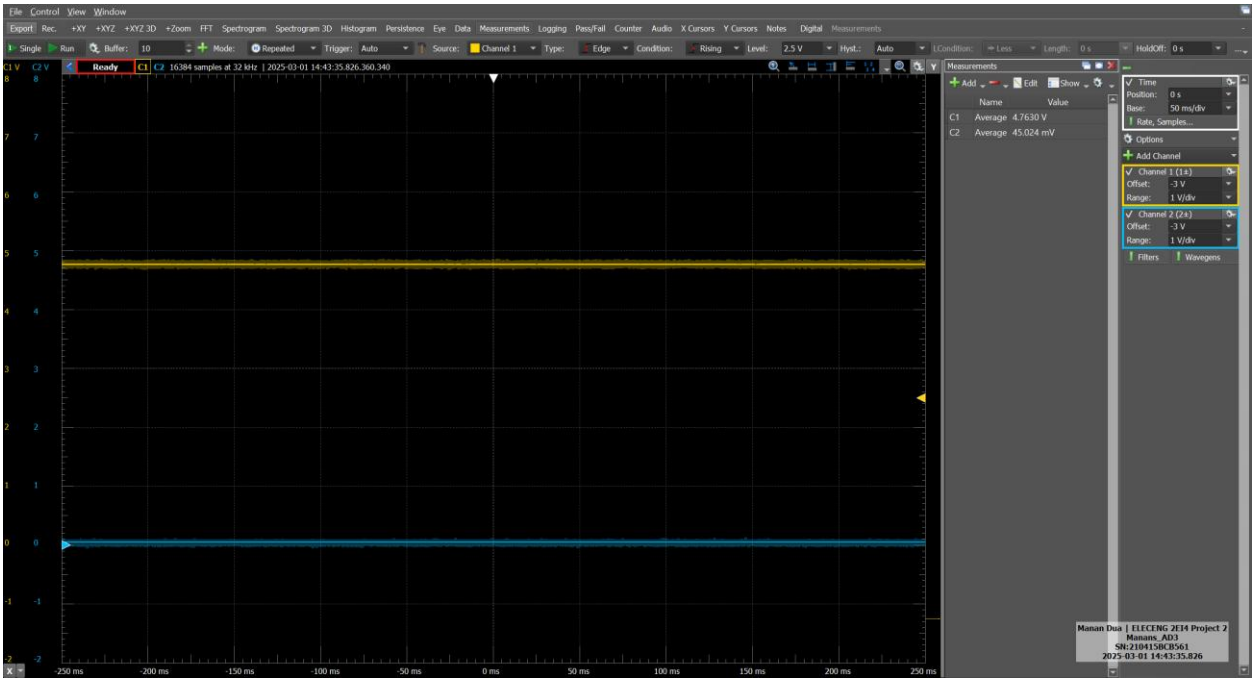

Figure 18: Output of physical circuit at V_A (yellow) and V_B (blue) with $V_{control} = 0V$

The voltage at V_B is found to be around 45.0mV

From this, using Ohm's law, the current can be calculated to be $I = \frac{45.0mV}{10k\Omega} = 4.5\mu nA$

This gives the switch an OFF resistance of $R_{off} = \frac{5V(10k\Omega)}{45.0mV} - 10k\Omega = 1.10M\Omega$

Now set

$V_{control}$ = 5V

V_{supply} = 5V

V_1 = 5V

The 10kΩ pull-down resistor is connected to V_A and V_B

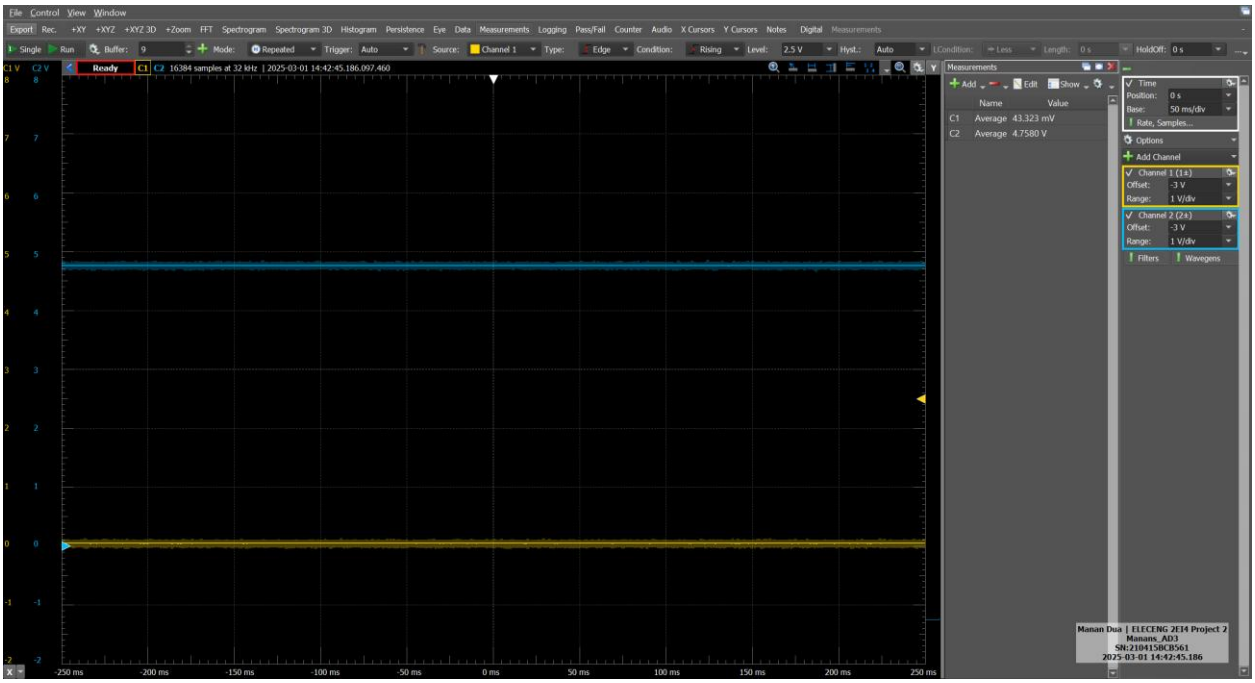

Figure 18: Output of physical circuit at V_A (yellow) and V_B (blue) with $V_{control}$ = 5V

The voltage at V_A is found to be around 43.3mV

From this, using Ohm's law, the current can be calculated to be $I = \frac{43.3mV}{10k\Omega} = 4.33\mu A$

This gives the switch an OFF resistance of $R_{off} = \frac{5V(10k\Omega)}{43.3mV} - 10k\Omega = 1.14M\Omega$

Voltage Range

The voltage range needs to be checked on both output terminals of the switch. The procedure follows supplying V_1 with $5V_{pp}$ sinusoidal wave at 10Hz with 2.5V offset, V_{supply} to 5V, and first supplying $V_{control}$ to 0V and starting by measuring the voltage at V_A.

Test Conditions:

$V_{supply} = 5V$

$V_1 = 5V_{PP}$ sinusoidal wave at 10Hz, 2.5V offset

$V_{control} = 0V$

There is also a 10kΩ pull-down resistor connected to V_A

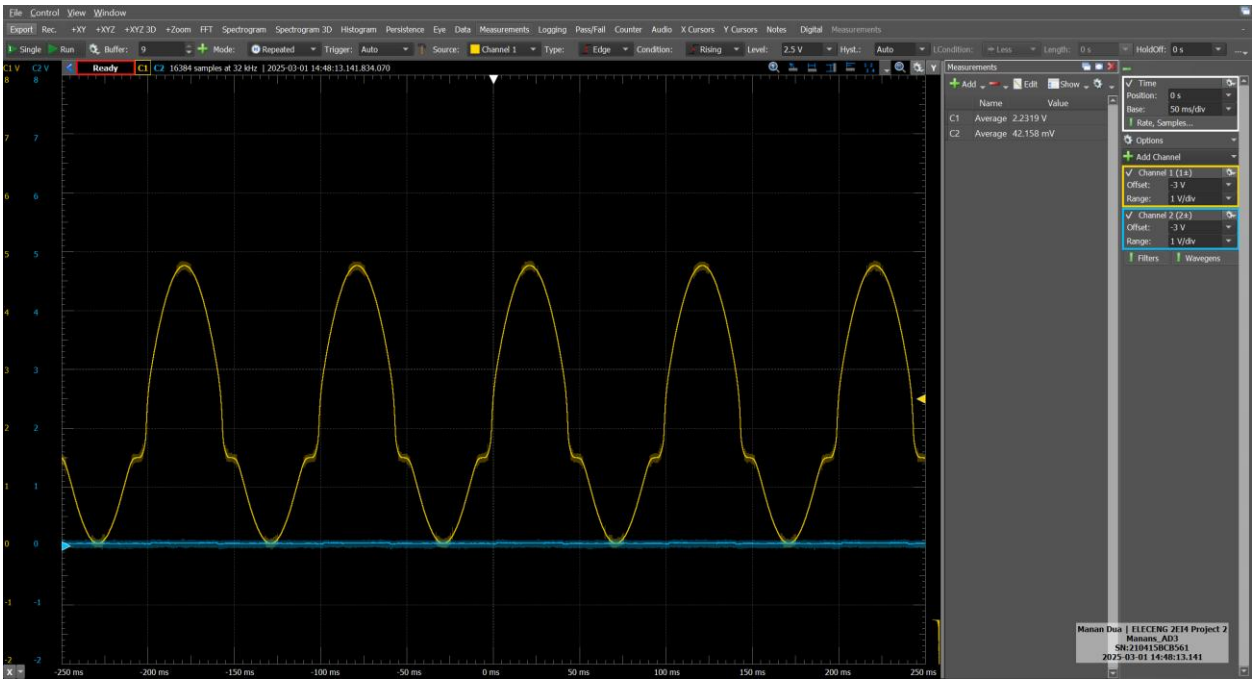

Figure 19: Voltage at pull-down resistor connected to V_A (yellow) with sinusoidal input

Next we have to supply $V_{control}$ with 5V to connect the switch to V_B.

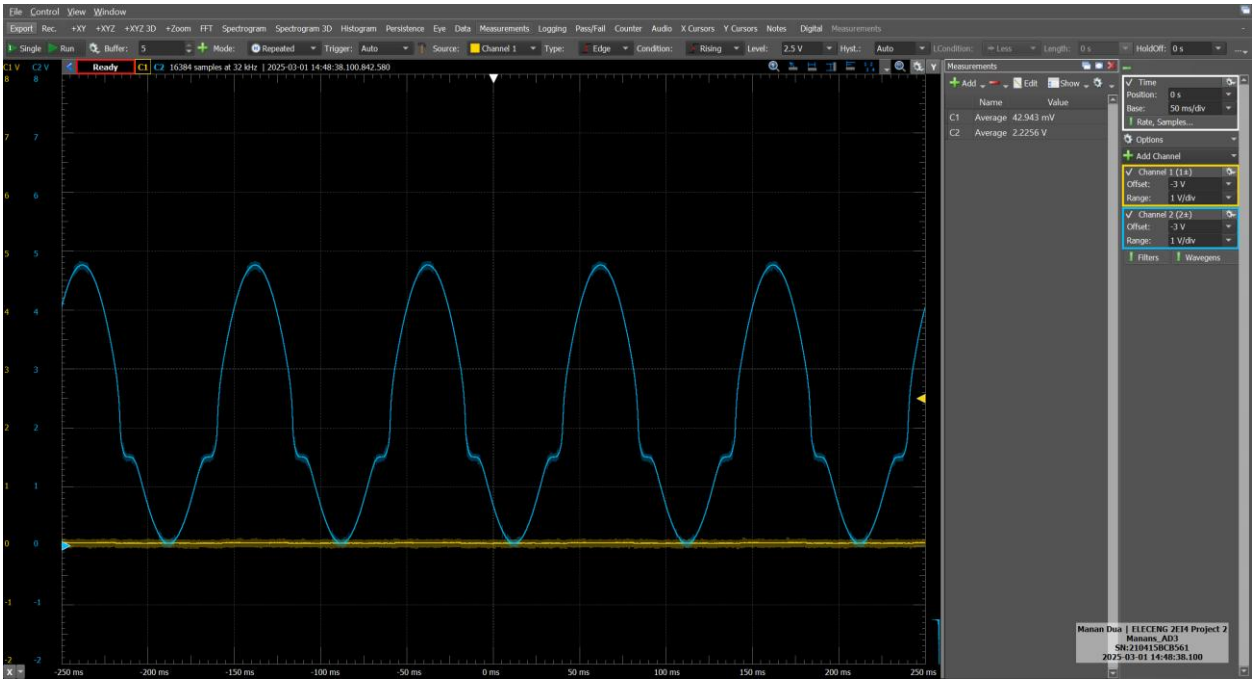

Figure 20: Voltage at pull-down resistor connected to V_B (blue) with sinusoidal input

Similarly, to switch 1, both output terminals support an input voltage across 0V to 5V, with the same inconsistency at around 2.4V.

Bidirectional Operation

To test the bidirectionality of the switch, we can remove the voltage supply from V_1 and connect it to either V_A or V_B. Note that the switch can only ever provide a connection to V_1, not the other nodes. i.e. V_A cannot be connected to V_B.

First, connect the supply to V_A and the voltmeter to V_1.

Test Conditions:

$V_{control} = 0V$

$V_{supply} = 5V$

$V_A = 5V$

The 10kΩ pull-down resistor is connected to V_1

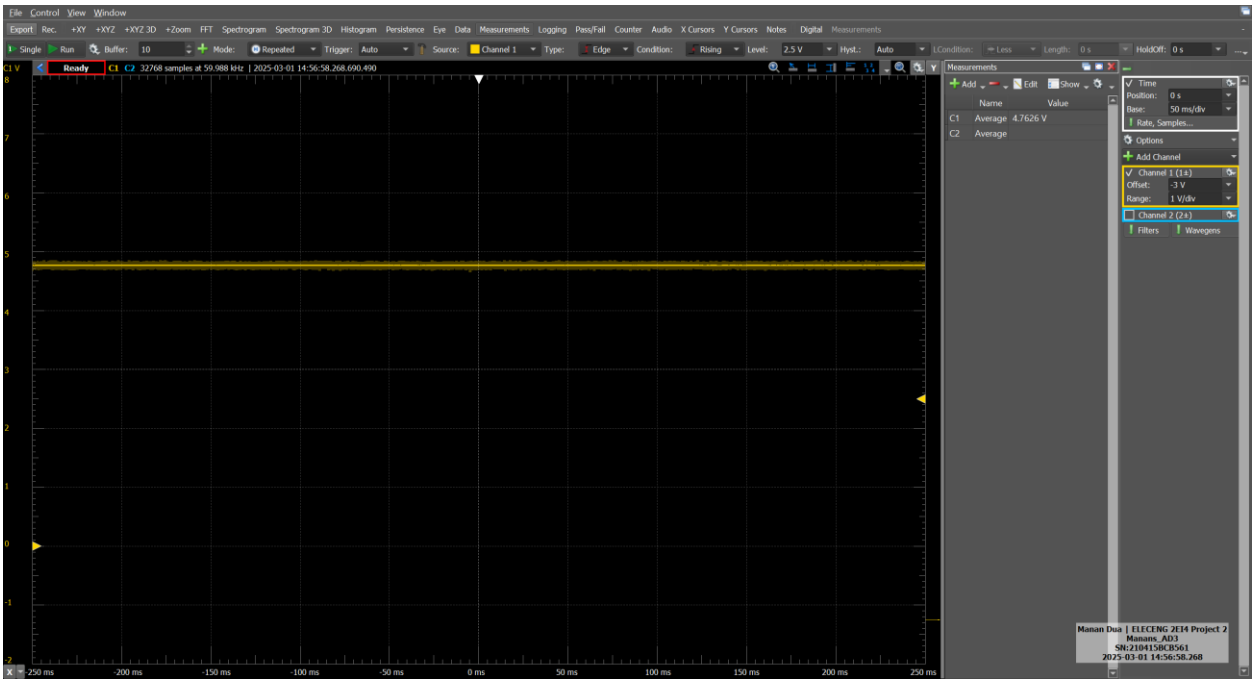

Figure 21: Voltage at V_1 with input connected to V_A

From this, V_2 is found to be around 4.76V

This means $R_{on} = \frac{5V(10k\Omega)}{4.76V} - 10k\Omega = 504\Omega$

Now swap the voltage supply to V_B and set $V_{control}$ to 5V.

Figure 22: Voltage at V_1 with input connected to V_B

From this, V_2 is found to be around 4.76V

This means $R_{on} = \frac{5V(10k\Omega)}{4.76V} - 10k\Omega = 504\Omega$

Both show a voltage of 4.76V, which means in either direction, the resistance of the switch is around 504Ω.

Theoretical explanation

The second switch is very similar to the first switch, but it has an additional transmission gate connected with an inverted $V_{control}$ signal to the first [3]. This allows for switching between two terminals, since if one transmission gate is off, the other will be on due to the inverted control signal, allowing it to conduct with one of two terminals. To test this circuit, V_{supply} was set to 5V, $V_!$ was set 5V, and $V_{control}$ was set to a $5V_{PP}$ square wave at 1Hz.

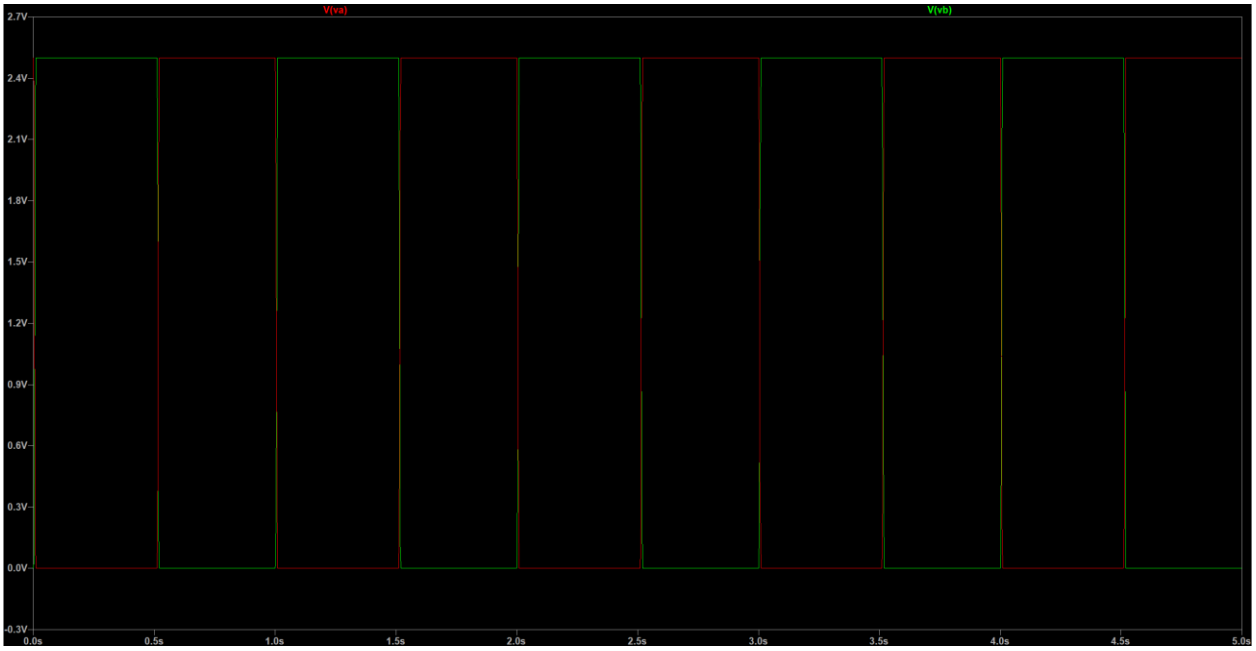

Figure 23: Simulation output at V_A and V_B

As shown in the simulation graph, only one of the outputs is ever bridged to V_1 at a time.

The theoretical results are very similar to the first switch but just require a repeat of steps due to the additional output terminal of the switch.

The ON resistance was also measured in this switch with a 10kΩ pull down resistor connected to the respective terminal to keep measurements consistent.

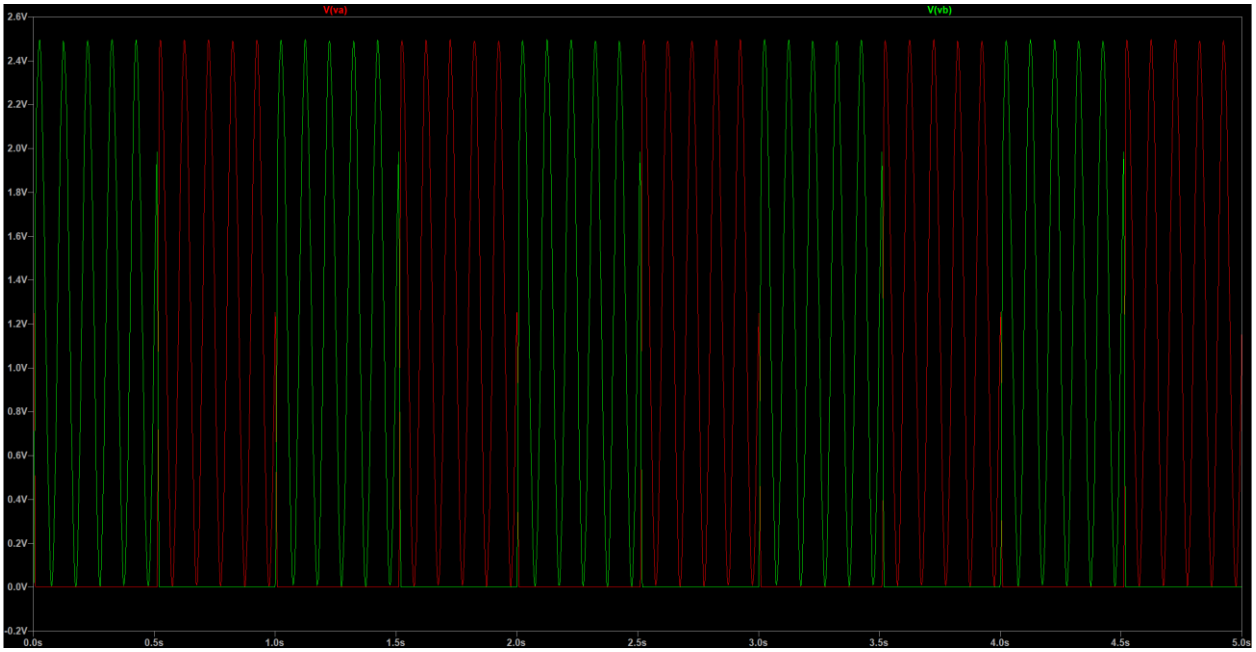

Figure 24: Simulation output at V_A and V_B with sinusoidal input

Similar to the first switch, the voltage drop across both output terminals of the switch is roughly 2.5V. This means that the current flowing to either output would experience the same resistance of roughly $R_{on} = \frac{5V(10k\Omega)}{2.5V} - 10k\Omega = 10k\Omega$. This is much higher than the resistance actually measured, due to the simulated MOSFETs having different characteristics. But ideally, the resistance across the switch would be 0Ω.

Similar to the first switch, the leakage current is theoretically 0A from the cutoff definition of the MOSFET. However, the hardware cannot be perfectly ideal and there will be a small amount of current leaking. Additionally, the LTSpice MOSFETs do not have the same parameters as the physical IC and show a different voltage drop with the switch off. Adding cursors to the simulation shows that the voltage drop across the switch is around 150nV at V_A and 148nV at V_B. This would give a leakage current at V_A of: $I = \frac{150nV}{10k\Omega} = 15pA$, and a leakage current at V_B of: $I = \frac{148nV}{10k\Omega} = 14.8pA$.

Since the only modification of this switch was the additional transmission gate, the properties stay the same, just repeated for each terminal. Meaning the voltage range for which the switch operates is also almost all voltages between 0 and 5V with the same inconsistency at 2.4V from the results.

The switch is also designed to operate in any direction, since the bulk of the MOSFETs are not tied to the source, allowing them to be symmetrical and allow current to flow in any direction. The simulation in LTSpice also confirms this as the voltage supply can be connected to either V_A or V_B with different frequencies and the output measured at V_1 remains at the same voltage.

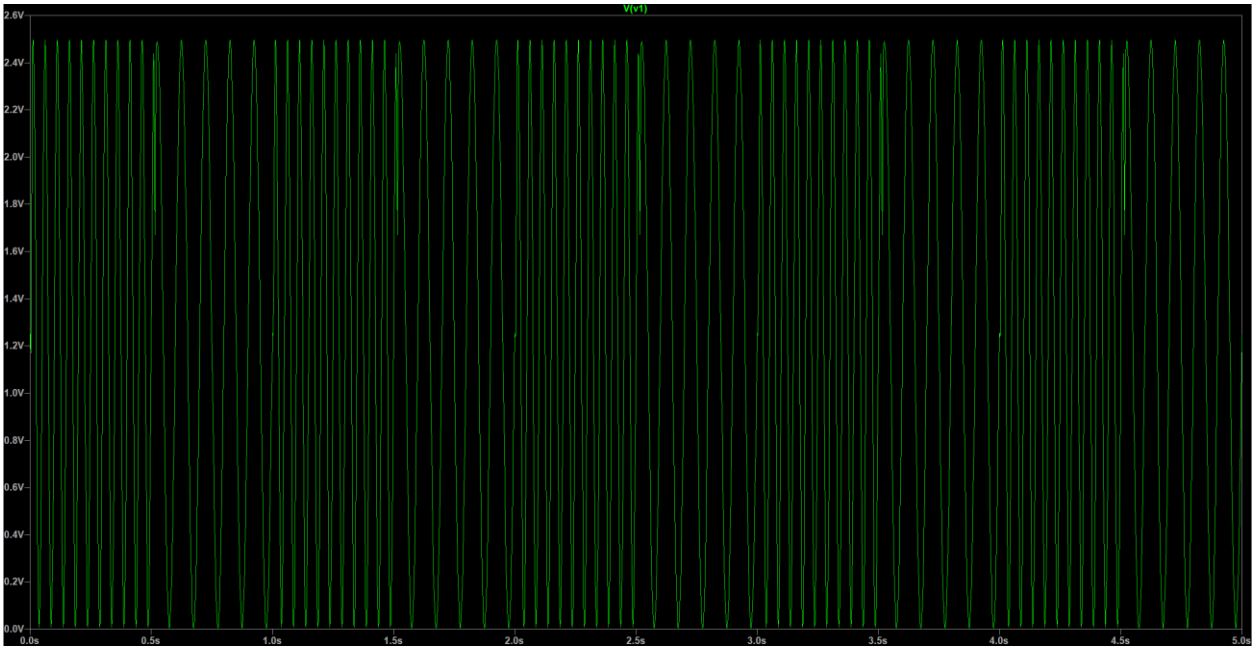

Figure 25: Simulation output at V_1 with alternating sinusoidal inputs from V_A and V_B

In this test, V_A is a $5V_{PP}$ sinusoidal wave at 10Hz, and V_B is a $5V_{PP}$ sinusoidal wave at 20Hz. From the graph it is clear when the frequency changes when being bridged with either V_A or V_B,, which is when $V_{control}$ is toggled.

Design Trade-offs

This switch is even more complex than switch 1. Due to how the IC is wired, it required 2 ICs to create this circuit. Doubling the cost of production ($1.88) but only adding 2 more MOSFETs. This switch also has the same inconsistency with operating voltage, but now it has it on two terminals. This switch operates similarly to a multiplexer, so it makes having current in the reverse direction impractical since connecting a voltage to either V_A or V_B will only bridge the connection to V_1 and not the other terminal.

References

[1] "CD4007UB Types," Texas Instruments, https://www.ti.com/lit/ds/symlink/cd4007ub-mil.pdf?ts=1735331598739&ref_url=https%253A%252F%252Fwww.google.com%252F (accessed Feb. 27, 2025).

[2] W. Storr, "Transmission gate as a CMOS bilateral switch," Basic Electronics Tutorials, https://www.electronics-tutorials.ws/combination/transmission-gate.html (accessed Feb. 26, 2025).

[3] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.