



Arab Academy for Science, Technology & Maritime Transport

College of Engineering and Technology

EXAMINATION PAPER

Department: Computer Engineering

Date: 30-December 2020

Course Title: Digital Electronics

Time allowed: 2 Hours

Course Code: CC 341

Lecturer: Prof. Dr. Mohamed T. El-Sonni

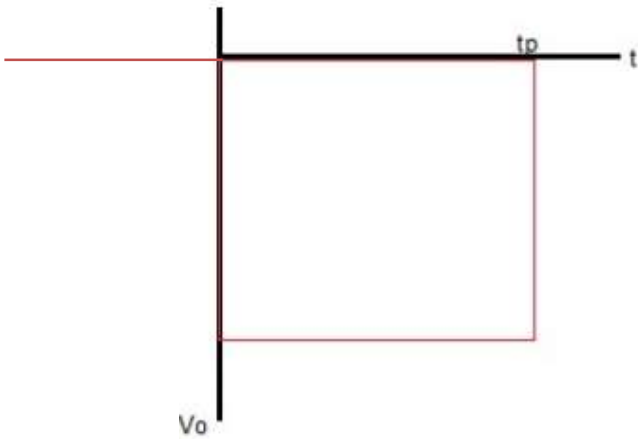
Student's Name : -----

Student's Department :----- Reg.# : -----

Question #	Marks	
	Available	Actual
1	3	
2	3	
3	3	
4	3	
5	2	
6	3	
7	3	
Total	20	
Lecturer	Name: Prof. Dr. Mohamed T. El-Sonni	
	Signature:	
	Date: 30 December 2020	

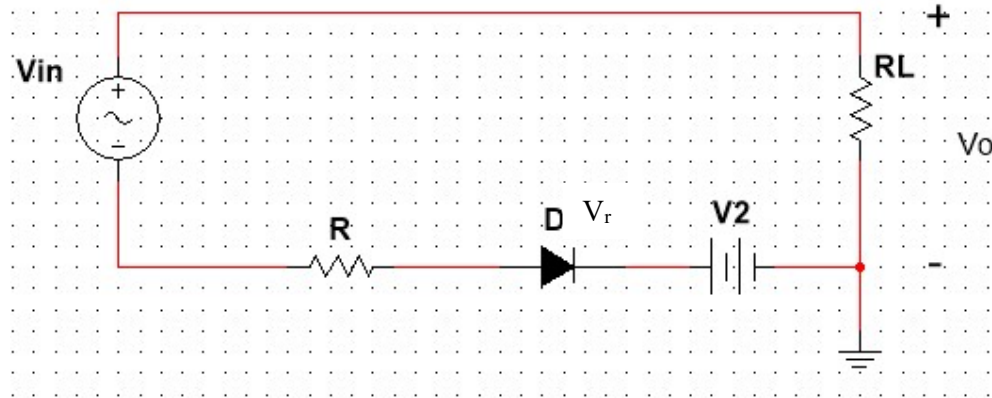
Question 1: [Linear wave shaping]

A negative pulse of 6V amplitude is applied to an RC high-pass filter circuit with $R = 22\text{K}\Omega$ and $C = 0.47\text{ }\mu\text{F}$. Sketch the output waveform and Specify V_o ($0 \leq t < t_p$), $V_o(t_p+)$, $V_o(t_p-)$ and V_o ($t > t_p$) when:
 $t_p = 10.34\text{ msec}$.

Symbol	Formula / Condition	Calculations / Results	Units
Fall time = t_r			
V_o ($0 \leq t < t_p$)			
$V_1 = V_o(t_p-)$			
$V_2 = V_o(t_p+)$			
V_o ($t > t_p$)			
Draw RC high-pass filter circuit			
Draw output waveform			

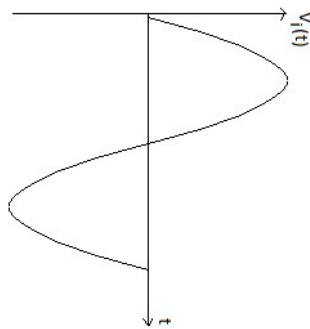
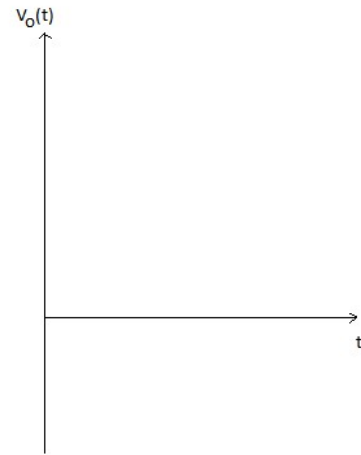
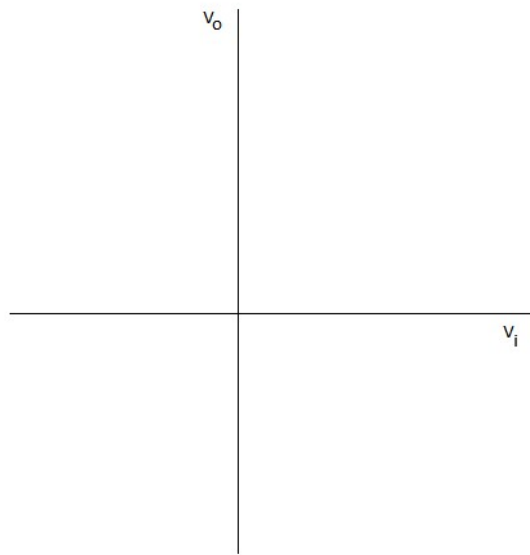
Question 2: [Non-linear wave shaping]

For the following circuits, draw the appropriate transfer characteristic output voltage.
 Know that $V_{\max} > V_r$ and $R_L = 2R$



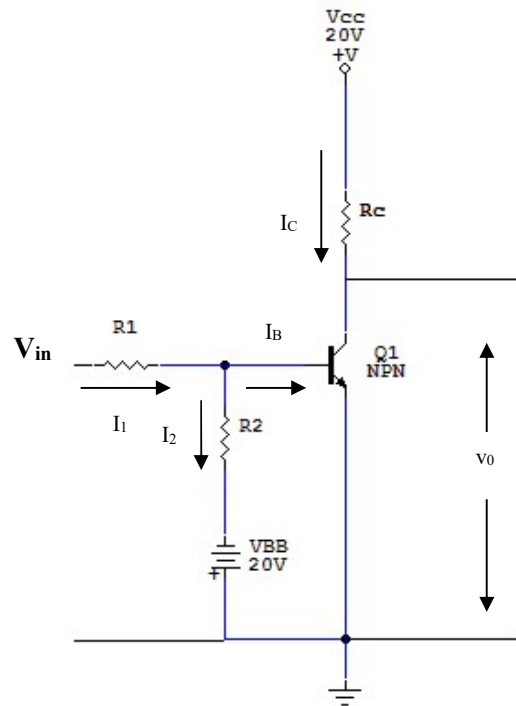
D is ON:

D is OFF:

Break point:

Question 3: [Switching characteristic of devices]

Design a Common Emitter transistor switch operating with $V_{CC}=20\text{V}$ and $V_{BB}=20\text{V}$. The transistor is expected to operate at $I_{C(\text{sat})}=5\text{mA}$, $h_{FE(\text{min})}=25$, $V_{CE(\text{sat})}=0.2\text{V}$, $V_{BE(\text{sat})}=0.7\text{V}$.

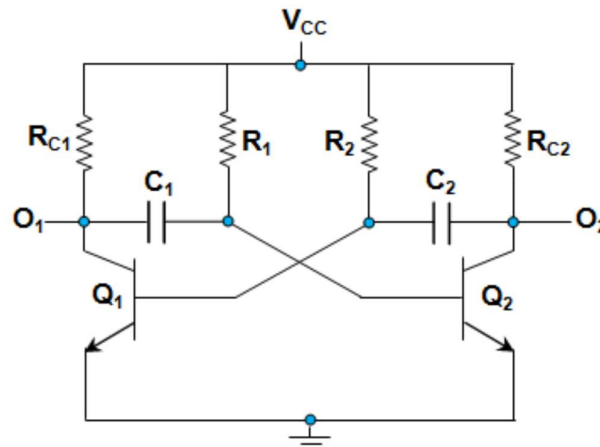
**Solution:**

Symbol	Formula / Condition	Calculation / Result	Units
$R_C =$			
$I_{B(\text{min})} =$			
$I_{B(\text{sat})} =$			
$I_2 =$			
$R_2 =$			
$I_1 =$			
$R_1 =$			
$V_i \text{ (high level)} =$			

at V_i (low level) =0			
$V_B =$			
Q is in cut-off?			

Question 4: [Astable multivibrator]

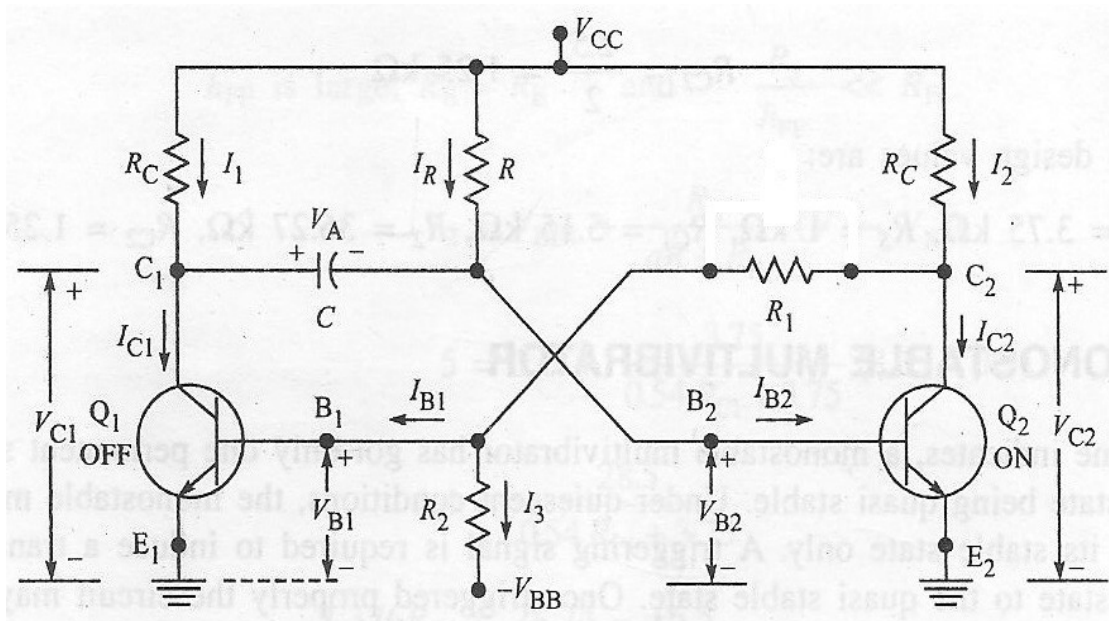
Design an astable multivibrator, assuming that silicon devices with $h_{FE(min)} = 45$ are used. Also assume that $V_{CC} = 12V$, $I_{C(sat)} = 5\text{ mA}$. Let the desired frequency of oscillations be 5 KHz and the required duty cycle 70%. For transistor used, $V_{CE(sat)} = 0.2V$, $V_{BE(sat)} = V_{\sigma} = 0.7V$.

**Solution:**

Symbol	Formula / Condition	Calculation / Result	Units
R_C			
$I_B (min)$			
$I_B (sat)$			
$R_1 = R_2 = R$			
For an unsymmetric a-stable multivibrator ($T_1 \neq T_2$) It is required to fix the component values of R_1 , R_2 , C_1 and C_2 let $R_1 = R_2 = R$			
T_1			
T_2			
C_1			
C_2			

Question 5: [Monostable multivibrator]

Diagnose the following circuit when a component is short circuited (S.C) and when a component is open circuited (O.C).

**Solution:**

R1	C1	R2	Vb1	Vc1	Vb2	Vc2	Q1	Q2
S.C			$V_{c2}=0.2$	V_{cc}	>0.7	V_{ceSat}	off	on
o.c			<0.7 or $-V_{bb}?$	V_{cc}	>0.7	V_{ceSat}	off	on
	S.C		>0.7 or $V_{ce}-IR1$	V_{b2}	>0.7	V_{ceSat}	off	on
	O.C							
		S.C						
		O.C						

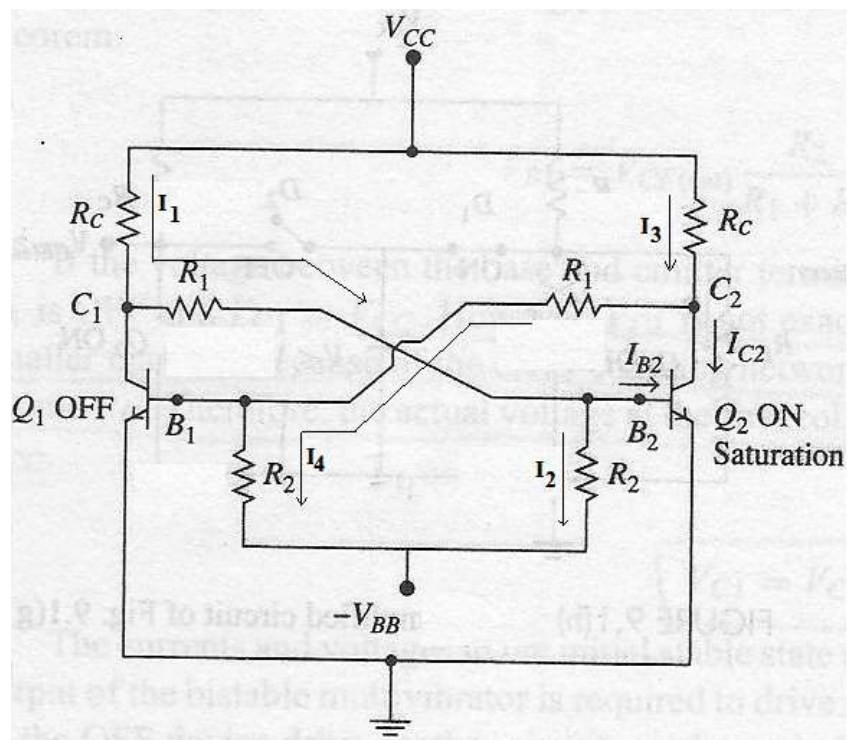
Answer the following multiple choice questions:

- 1) The base emitter voltage in a saturation region is _____
 - a) Greater than 7V
 - b) Almost to 0.7V
 - c) Less than 0.7V
 - d) **Cannot be predicted**
- 2) Bistable circuit is also known as _____
 - a) Latch
 - b) Gate
 - c) **Flip-flop**
 - d) Bidirectional circuit
- 3) What is a square wave generator?
 - a) Flip-flop
 - b) Bi-stable multivibrator
 - c) **Astable multivibrator**
 - d) Monostable multivibrator
- 4) Monostable multivibrators can be used as
 - a) Pulse generator
 - b) **Pulse stretcher**
 - c) Pulse looser
 - d) Pulse motor

Question 6:

Design a fixed-bias binary multivibrator with $h_{FE} = 50$.

The circuit parameters are $V_{CC} = 12\text{V}$, $V_{BB} = -12\text{V}$, $I_C = 5\text{ mA}$, $V_{CE(\text{sat})} = 0.3\text{V}$, $V_{BE(\text{sat})} = 0.7\text{V}$.



Symbol	Formula / Condition	Calculation / Result	Units
R_C			
I_2			
R_2			
$I_{B2(\text{min})}$			
$I_{B2(\text{sat})}$			
I_1			
$I_B (\text{min})$			
V_{B1}			

Question 7: [Logic Gates]**Draw the following Circuits and Complete The Truth Tables:****PMOS NOR gate:**

V ₁	V ₂	O/P
Low	Low	
Low	High	
High	Low	
High	High	

CMOS NAND:

V ₁	V ₂	O/P
Low	Low	
Low	High	
High	Low	
High	High	

74 series two input Transistor Transistor Logic NAND Gate:

V ₁	V ₂	O/P
Low	Low	
Low	High	
High	Low	
High	High	