WbXbc Manual

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Overview

TBD

Integration Parameters

This section specifies the integration parameters to configure the WbXbc components. Each WbXbc component supports a subset of the parameters listed below.

ITR_CNT

The number of initiator bus interfaces to be offered by the WbXbc component

TGT_CNT

The number of target bus interfaces to be offered by the WbXbc component

ADDR_WIDTH

Width of all address busses (ADR_I and ADR_0)

ITR_ADDR_WIDTH

Width of the initiator address bus(ses) (ADR_I), in case it differs from the target address bus(es) (ADR_O)

SEL_WIDTH

Number data select lines of all initiator and target busses (SEL_I and SEL_O)

ITR_SEL_WIDTH

Number of data select lines of the initiator bus (SEL_I), in case it from the target bus (SEL_O)

DATA_WIDTH

Width of all data busses (initiator and target, read and write direction)

ITR_DATA_WIDTH

Width of the initiator's data busses (read and write direction

TGA_WIDTH

Number of tags associated with the address busses of the initiator and the target (TGA_I and TGA_O)

TGC_WIDTH

Number of tags associated with the cycle indicators (CYC_I and CYC_O) of thw initiator and the target (TGC_I and TGC_O)

TGRD_WIDTH

Number of tags assoociated with the read data busses of the initiator and the target (TGD_O and TGD_I)

TGWD_WIDTH

Number of tags associated with the write data busses of the initiator and the target (TGD_I and TGD_O)

BIG_ENDIAN

Selects the endianess of the design (1=big endian, 0=little endian)

Interface Signals

All WbXbc components share common interface signals, which are described in this chapter. Most of these signals refer directly to the Wishbone specification [1].

General Signals (SYSCON)

clk_i

Common clock input for all Wishbone interfaces

itr_clk_i

clock input for all initiator busses. Target busses must be clocked by synchronous and subdivided clock.

tgt_clk_i

clock input for all target busses. Initiator busses must be clocked by synchronous and subdivided clock.

itr2tgt_sync_i

This signal indicates a common positive clock edge of the initiator clock and the synchronous and subdivided target clock.

tgt2itr_sync_i

This signal indicates a common positive clock edge of the targert clock and the synchronous and subdivided initiator clock.

async_rst_i

An optional asynchronous reset signal for all sequential logic. This reset signal may assert asynchronously, but must deassert synchronously. If no asynchrounous reset is implemented, this input must be tied to zero.

sync_rst_i

A synchronous reset signal as required by the Wishbone specification (RST_I). For WbXBC components, this synchronous reset is not required, if an asynchronous reset is provided. If no synchrounous reset is implemented, this input must be tied to zero.

Initiator Bus Signals

itr_cyc_i

TBD

itr_stb_i

TBD

itr_we_i

TBD

itr_lock_i
TBD

itr_sel_i
TBD

itr_adr_i
TBD

itr_dat_i
TBD

itr_tga_i
TBD

itr_tgc_i
TBD

itr_tgd_i
TBD

itr_ack_o
TBD

itr_err_o
TBD

itr_rty_o
TBD

itr_stall_o
TBD

itr_dat_o
TBD

itr_tgd_o
TBD

Target Bus Signals

tgt_cyc_o
TBD

tgt_stb_o
TBD

tgt_we_o
TBD

tgt_lock_o
TBD

tgt_sel_o
TBD

tgt_adr_o
TBD

tgt_dat_o
TBD

tgt_tga_o
TBD

tgt_tgc_o
TBD

tgt_tgd_o
TBD

tgt_ack_i
TBD

tgt_err_i
TBD

tgt_rty_i
TBD

tgt_stall_i
TBD

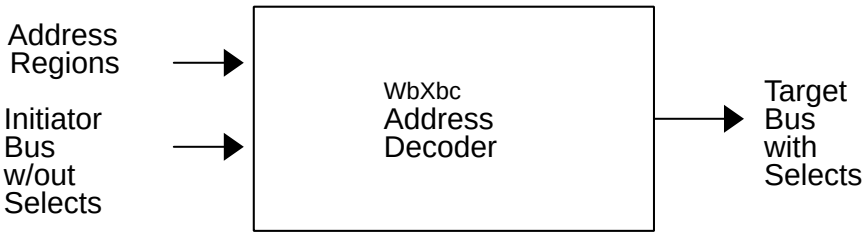
tgt_dat_i
TBD

tgt_tgd_i
TBD

Crossbar Switch components

TBD

WbXbc Address Decoder



This module implements an address decoder for the Wishbone protocol. It propagates accesses from the initiator bus to the target bus and adds a set of address tags which selecting the target block.

Integration Parameters

Parameter	Default Value	Description
TGT_CNT	4	number of target addresses to decode
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Target Address Regions			
region_addr	(TGT_CNT*ADDR_WIDTH)-1:0	input	target address
region_mask	(TGT_CNT*ADDR_WIDTH)-1:0	input	selects relevant address bits (1: relevant, 0: ignored)
Initiator Interface			
itr_cyc_i		input	bus cycle indicator

Signal	Range	Direction	Description
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
itr_tga_tgtsel_o	TGT_CNT-1:0	output	target select tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

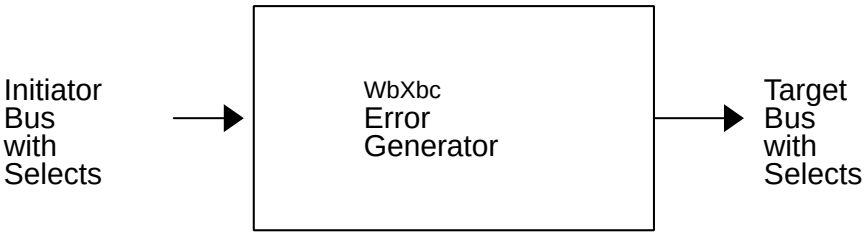
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
TGT_CNT	4	iVerilog, Yosys			
ADDR_WIDTH	16				
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Error Generator



This module implements an error generator or dummy target for the pipelined Wishbone protocol. It propagates accesses from the initiator to the target bus, but intercepts accesses without a target, signaling an error condition to the initiator. The target association is determined by a set of address tags, generated by the address decoder.

Integration Parameters

Parameter	Default Value	Description
TGT_CNT	4	number of target busses
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tga_tgtsel_i	TGT_CNT-1:0	input	target select tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
itr_tga_tgtsel_o	TGT_CNT-1:0	output	target select tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags

Signal	Range	Direction	Description
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

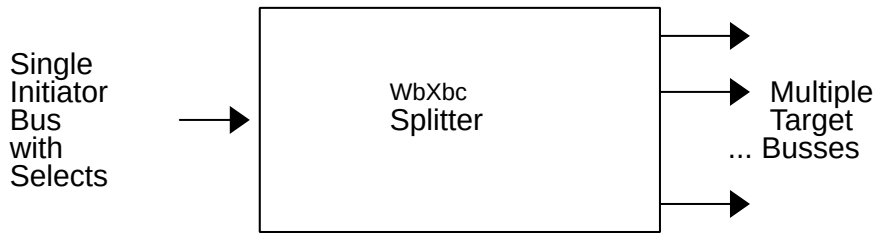
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
TGT_CNT	4	iVerilog, Yosys			
ADDR_WIDTH	16				
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Splitter



This module implements a bus splitter for the pipelined Wishbone protocol. Accesses from the initiator bus are propagated to one of the target busses. The target busses are selected by a set of address tags, generated by the address decoder.

Integration Parameters

Parameter	Default Value	Description
TGT_CNT	4	number of target busses
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tga_tgtsel_i	TGT_CNT-1:0	input	target select tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags

Signal	Range	Direction	Description
Target Interfaces			
tgt_cyc_o	TGT_CNT-1:0	output	concatinated bus cycle indicators
tgt_stb_o	TGT_CNT-1:0	output	concatinated access requests
tgt_we_o	TGT_CNT-1:0	output	concatinated write enables
tgt_lock_o	TGT_CNT-1:0	output	concatinated bus cycle locks
tgt_sel_o	(TGT_CNT*SEL_WIDTH)-1:0	output	concatinated write data selects
tgt_adr_o	(TGT_CNT*ADDR_WIDTH)-1:0	output	concatinated write data selects
tgt_dat_o	(TGT_CNT*DATA_WIDTH)-1:0	output	concatinated write data busses
tgt_tga_o	(TGT_CNT*TGA_WIDTH)-1:0	output	concatinated address tags
tgt_tgc_o	(TGT_CNT*TGC_WIDTH)-1:0	output	concatinated bus cycle tags
tgt_tgd_o	(TGT_CNT*TGWD_WIDTH)-1:0	output	concatinated write data tags
tgt_ack_i	TGT_CNT-1:0	input	concatinated bus cycle acknowledges
tgt_err_i	TGT_CNT-1:0	input	concatinated error indicators
tgt_rty_i	TGT_CNT-1:0	input	concatinated retry requests
tgt_stall_i	TGT_CNT-1:0	input	concatinated access delays
tgt_dat_i	(TGT_CNT*DATA_WIDTH)-1:0	input	concatinated read data busses
tgt_tgd_i	(TGT_CNT*TGRD_WIDTH)-1:0	input	concatinated read data tags

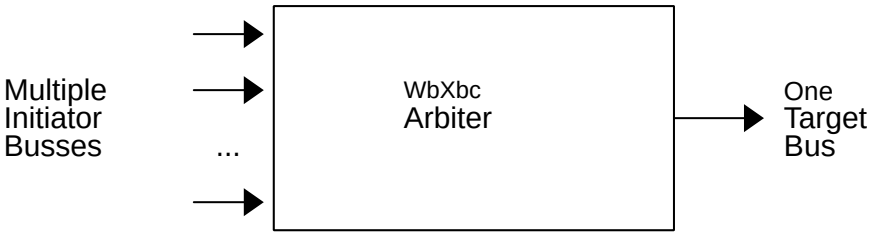
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
TGT_CNT	4	iVerilog, Yosys			
ADDR_WIDTH	16				
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Arbiter



This module implements a bus arbiter for the pipelined Wishbone protocol. Accesses from multiple initiator busses are arbitrated and propagated to the target bus. Each initiator bus can request bus accesses at two priority levels. The priority levels are selected via a set of address tags. Access requests of equal priority are arbitrated with a fixed priority (initiator 0 has the higheest priority).

Integration Parameters

Parameter	Default Value	Description
ITR_CNT	4	number of initiator busses
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of write data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i	ITR_CNT-1:0	input	concatinated bus cycle indicators
itr_stb_i	ITR_CNT-1:0	input	concatinated access requests

Signal	Range	Direction	Description
itr_we_i	ITR_CNT-1:0	input	concatinated write enables
itr_lock_i	ITR_CNT-1:0	input	concatinated bus cycle locks
itr_sel_i	(ITR_CNT*SEL_WIDTH)-1:0	input	concatinated write data selects
itr_adr_i	(ITR_CNT*ADDR_WIDTH)-1:0	input	concatinated address busses
itr_dat_i	(ITR_CNT*DATA_WIDTH)-1:0	input	concatinated write data busses
itr_tga_i	(ITR_CNT*TGA_WIDTH)-1:0	input	concatinated address tags
itr_tga_prio_i	ITR_CNT-1:0	input	concatinated access priorities
itr_tgc_i	(ITR_CNT*TGC_WIDTH)-1:0	input	concatinated bus cycle tags
itr_tgd_i	(ITR_CNT*TGWD_WIDTH)-1:0	input	concatinated write data tags
itr_ack_o	ITR_CNT-1:0	output	concatinated bus cycle acknowledges
itr_err_o	ITR_CNT-1:0	output	concatinated error indicators
itr_rty_o	ITR_CNT-1:0	output	concatinated retry requests
itr_stall_o	ITR_CNT-1:0	output	concatinated access delays
itr_dat_o	(ITR_CNT*DATA_WIDTH)-1:0	output	concatinated read data buses
itr_tgd_o	(ITR_CNT*TGRD_WIDTH)-1:0	output	concatinated read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

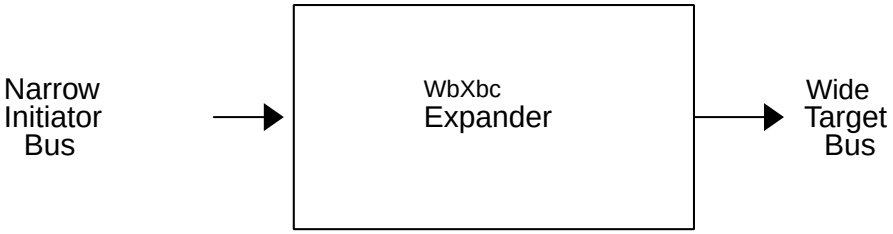
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
ITR_CNT	4	iVerilog, Yosys			
ADDR_WIDTH	16				
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Expander



This module connects a pipelined Wishbone initiator to a target with wider data busses (twice the width of the initiator's data busses).

Integration Parameters

Parameter	Default Value	Description
ITR_ADDR_WIDTH	16	width of the initiator address bus
ITR_DATA_WIDTH	16	width of each initiator data bus
ITR_SEL_WIDTH	2	number of initiator data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags
BIG_ENDIAN	1	endianess of the component

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	ITR_SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ITR_ADDR_WIDTH-1:0	input	address bus
itr_dat_i	ITR_DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	(ITR_SEL_WIDTH*2)-1:0	output	write data selects
tgt_adr_o	ITR_ADDR_WIDTH-2:0	output	write data selects
tgt_dat_o	(ITR_DATA_WIDTH*2)-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge

Signal	Range	Direction	Description
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	(ITR_DATA_WIDTH*2)-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

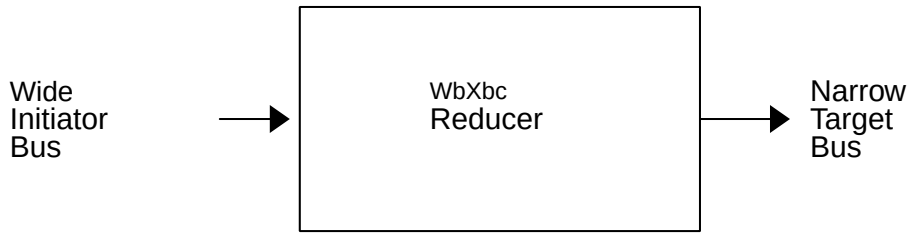
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
TGT_ADDR_WIDTH	16	iVerilog, Yosys			
TGT_DATA_WIDTH	16				
TGT_SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				
BIG_ENDIAN	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Reducer



This module connects a pipelined Wishbone initiator to a target with narrower data busses (half the width of the initiator's data busses). Initiator bus accesses may be converted into two consecutive accesses to the target bus.

Integration Parameters

Parameter	Default Value	Description
ITR_ADDR_WIDTH	16	width of the initiator address bus
ITR_DATA_WIDTH	16	width of each initiator data bus
ITR_SEL_WIDTH	2	number of initiator data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags
BIG_ENDIAN	1	endianess of the component

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			

Signal	Range	Direction	Description
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	(ITR_SEL_WIDTH/2)-1:0	output	write data selects
tgt_adr_o	ITR_ADDR_WIDTH:0	output	write data selects
tgt_dat_o	(ITR_DATA_WIDTH/2)-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	(ITR_DATA_WIDTH/2)-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

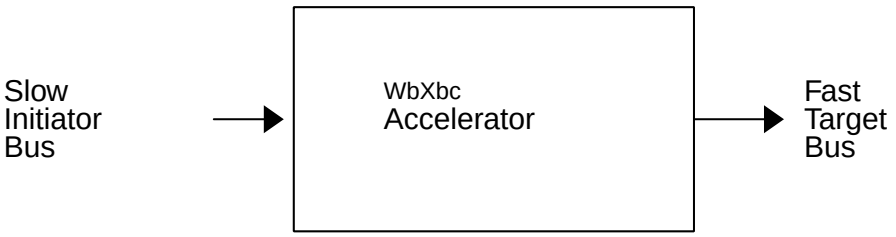
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
TGT_ADDR_WIDTH	16	iVerilog, Yosys			
TGT_DATA_WIDTH	16				
TGT_SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				
BIG_ENDIAN	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Accelerator



This module connects a pipelined Wishbone initiator, running at a higher frequency to a target, running at a lower frequency.

Integration Parameters

Parameter	Default Value	Description
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags
REG_ITR	0	register initiator bus inputs

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
tgt_clk_i		input	target clock
tgt2itr_sync_i		input	clock sync signal
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle

Signal	Range	Direction	Description
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

Section Interface Signals gives a detailed description of each slignal listed above.

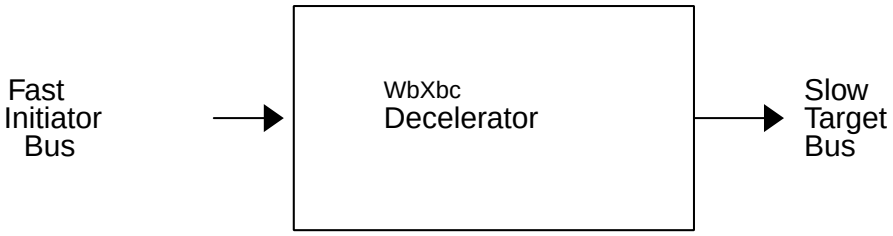
Verification Status

Configuration	Linting	Simulation	Formal	FPGA
Default Configuration				

Configuration		Linting	Simulation	Formal	FPGA
ADDR_WIDTH	16	iVerilog, Yosys			
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				
REG_ITR	0				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Decelerator



This module connects a pipelined Wishbone initiator, running at a higher frequency to a target, running at a lower frequency:.

Integration Parameters

Parameter	Default Value	Description
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags
REG_ITR	0	register initiator bus inputs
REG_TGT	0	register target bus inputs

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
itr_clk_i		input	initiator clock
itr2tgt_sync_i		input	clock sync signal
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge

Signal	Range	Direction	Description
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

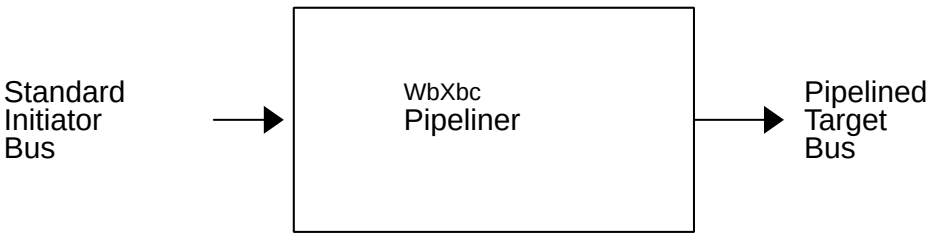
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
ADDR_WIDTH	16	iVerilog, Yosys			
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				
REG_ITR	0				
REG_TGT	0				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Pipeliner



This module connects a standard protocol Wishbone initiator to a pipelined target.

Integration Parameters

Parameter	Default Value	Description
ADDR_WIDTH	16	width of the address bus

Parameter	Default Value	Description
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable

Signal	Range	Direction	Description
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
ADDR_WIDTH	16	iVerilog, Yosys			
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Standardizer

This module connects a pipelined Wishbone initiator to a standard protocol target.

Integration Parameters

Parameter	Default Value	Description
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags

Signal	Range	Direction	Description
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADDR_WIDTH-1:0	output	write data selects
tgt_dat_o	DATA_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DATA_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

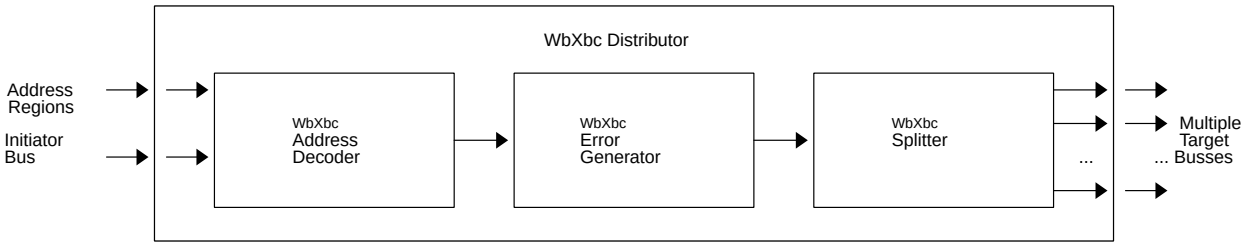
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
ADDR_WIDTH	16	iVerilog, Yosys			
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Distributor



This module implements an address decoder for the Wishbone protocol. It propagates accesses from the initiator bus to the target bus and adds a set of address tags which selecting the target block.

Integration Parameters

Parameter	Default Value	Description
TGT_CNT	4	number of target busses
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Target Address Regions			
region_addr	(TGT_CNT*ADDR_WIDTH)-1:0	input	target address
region_mask	(TGT_CNT*ADDR_WIDTH)-1:0	input	selects relevant address bits
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle

Signal	Range	Direction	Description
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADDR_WIDTH-1:0	input	address bus
itr_dat_i	DATA_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DATA_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interfaces			
tgt_cyc_o	TGT_CNT-1:0	output	concatinated bus cycle indicators
tgt_stb_o	TGT_CNT-1:0	output	concatinated access requests
tgt_we_o	TGT_CNT-1:0	output	concatinated write enables
tgt_lock_o	TGT_CNT-1:0	output	concatinated bus cycle locks
tgt_sel_o	(TGT_CNT*SEL_WIDTH)-1:0	output	concatinated write data selects
tgt_adr_o	(TGT_CNT*ADDR_WIDTH)-1:0	output	concatinated write data selects
tgt_dat_o	(TGT_CNT*DATA_WIDTH)-1:0	output	concatinated write data busses
tgt_tga_o	(TGT_CNT*TGA_WIDTH)-1:0	output	concatinated address tags
tgt_tgc_o	(TGT_CNT*TGC_WIDTH)-1:0	output	concatinated bus cycle tags
tgt_tgd_o	(TGT_CNT*TGWD_WIDTH)-1:0	output	concatinated write data tags
tgt_ack_i	TGT_CNT-1:0	input	concatinated bus cycle acknowledges
tgt_err_i	TGT_CNT-1:0	input	concatinated error indicators
tgt_rty_i	TGT_CNT-1:0	input	concatinated retry requests
tgt_stall_i	TGT_CNT-1:0	input	concatinated access delays
tgt_dat_i	(TGT_CNT*DATA_WIDTH)-1:0	input	concatinated read data busses
tgt_tgd_i	(TGT_CNT*TGRD_WIDTH)-1:0	input	concatinated read data tags

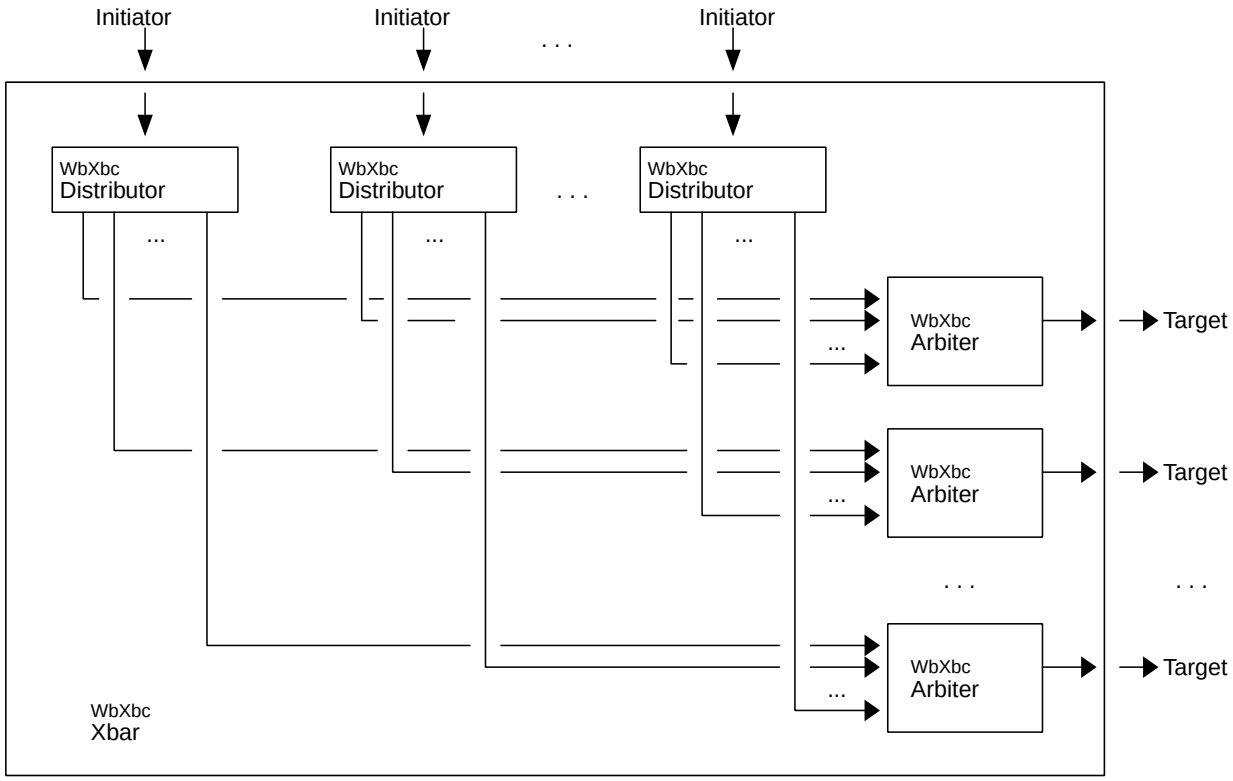
Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration		Linting	Simulation	Formal	FPGA
Default Configuration					
TGT_CNT	4	iVerilog, Yosys			
ADDR_WIDTH	16				
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

WbXbc Xbar



This module implements a full crossbar switch between a set of initator busses and a set of target busses, all using the pipelined Wishbone protocol.

Integration Parameters

Parameter	Default Value	Description
ITR_CNT	4	number of initiator busses
TGT_CNT	4	number of target busses
ADDR_WIDTH	16	width of the address bus
DATA_WIDTH	16	width of each data bus
SEL_WIDTH	2	number of data select lines
TGA_WIDTH	1	number of address tags
TGC_WIDTH	1	number of cycle tags
TGRD_WIDTH	1	number of read data tags
TGWD_WIDTH	1	number of write data tags

Section Integration Parameters gives a detailed description of each parameter listed above.

Interface Signals

Signal	Range	Direction	Description
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Target Address Regions			
region_addr	(TGT_CNT*ADDR_WIDTH)-1:0	input	target address
region_mask	(TGT_CNT*ADDR_WIDTH)-1:0	input	selects relevant address bits
Initiator Interface			
itr_cyc_i	ITR_CNT-1:0	input	concatinated bus cycle indicators
itr_stb_i	ITR_CNT-1:0	input	concatinated access requests
itr_we_i	ITR_CNT-1:0	input	concatinated write enables
itr_lock_i	ITR_CNT-1:0	input	concatinated bus cycle locks
itr_sel_i	(ITR_CNT*SEL_WIDTH)-1:0	input	concatinated write data selects
itr_adr_i	(ITR_CNT*ADDR_WIDTH)-1:0	input	concatinated address busses
itr_dat_i	(ITR_CNT*DATA_WIDTH)-1:0	input	concatinated write data busses
itr_tga_i	(ITR_CNT*TGA_WIDTH)-1:0	input	concatinated address tags
itr_tga_prio_i	ITR_CNT-1:0	input	concatinated access priorities
itr_tgc_i	(ITR_CNT*TGC_WIDTH)-1:0	input	concatinated bus cycle tags
itr_tgd_i	(ITR_CNT*TGWD_WIDTH)-1:0	input	concatinated write data tags

Signal	Range	Direction	Description
itr_ack_o	ITR_CNT-1:0	output	concatinated bus cycle acknowledges
itr_err_o	ITR_CNT-1:0	output	concatinated error indicators
itr_rty_o	ITR_CNT-1:0	output	concatinated retry requests
itr_stall_o	ITR_CNT-1:0	output	concatinated access delays
itr_dat_o	(ITR_CNT*DATA_WIDTH)-1:0	output	concatinated read data buses
itr_tgd_o	(ITR_CNT*TGRD_WIDTH)-1:0	output	concatinated read data tags
Target Interfaces			
tgt_cyc_o	TGT_CNT-1:0	output	concatinated bus cycle indicators
tgt_stb_o	TGT_CNT-1:0	output	concatinated access requests
tgt_we_o	TGT_CNT-1:0	output	concatinated write enables
tgt_lock_o	TGT_CNT-1:0	output	concatinated bus cycle locks
tgt_sel_o	(TGT_CNT*SEL_WIDTH)-1:0	output	concatinated write data selects
tgt_adr_o	(TGT_CNT*ADDR_WIDTH)-1:0	output	concatinated write data selects
tgt_dat_o	(TGT_CNT*DATA_WIDTH)-1:0	output	concatinated write data busses
tgt_tga_o	(TGT_CNT*TGA_WIDTH)-1:0	output	concatinated address tags
tgt_tgc_o	(TGT_CNT*TGC_WIDTH)-1:0	output	concatinated bus cycle tags
tgt_tgd_o	(TGT_CNT*TGWD_WIDTH)-1:0	output	concatinated write data tags
tgt_ack_i	TGT_CNT-1:0	input	concatinated bus cycle acknowledges
tgt_err_i	TGT_CNT-1:0	input	concatinated error indicators
tgt_rty_i	TGT_CNT-1:0	input	concatinated retry requests
tgt_stall_i	TGT_CNT-1:0	input	concatinated access delays
tgt_dat_i	(TGT_CNT*DATA_WIDTH)-1:0	input	concatinated read data busses
tgt_tgd_i	(TGT_CNT*TGRD_WIDTH)-1:0	input	concatinated read data tags

Section Interface Signals gives a detailed description of each slignal listed above.

Verification Status

Configuration	Linting	Simulation	Formal	FPGA
Default Configuration				

Configuration		Linting	Simulation	Formal	FPGA
ITR_CNT	4	iVerilog, Yosys			
TGT_CNT	4				
ADDR_WIDTH	16				
DATA_WIDTH	16				
SEL_WIDTH	2				
TGA_WIDTH	1				
TGC_WIDTH	1				
TGRD_WIDTH	1				
TGWD_WIDTH	1				

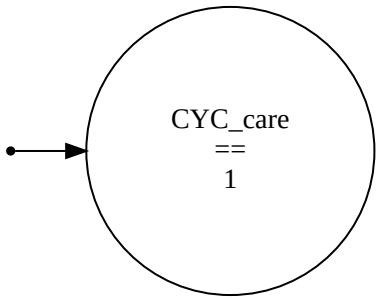
All lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

My Interpretation of the Pipelined Wishbone Protocol Spec

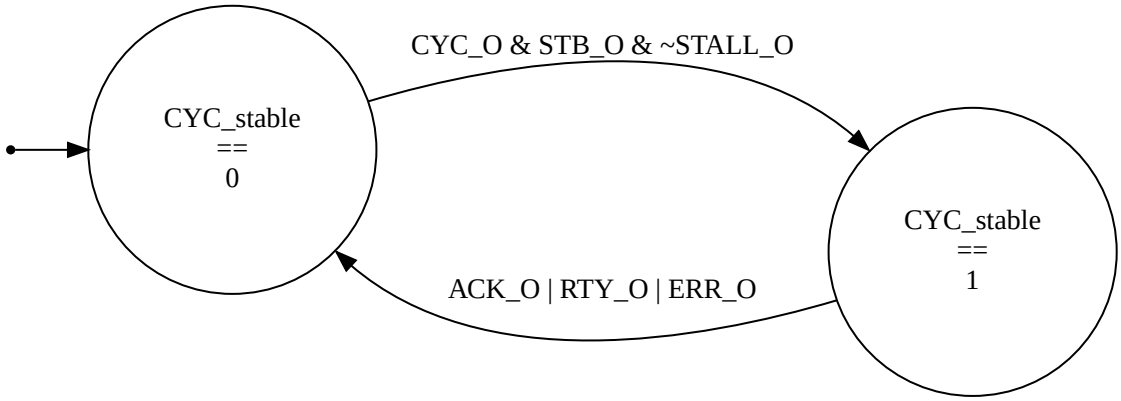
Protocol Signals Driven by the Initiator

Cycle Indicator: `CYC_O`, `CYC_I`

Care Condition

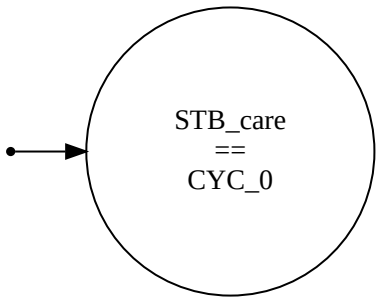


Stable Condition

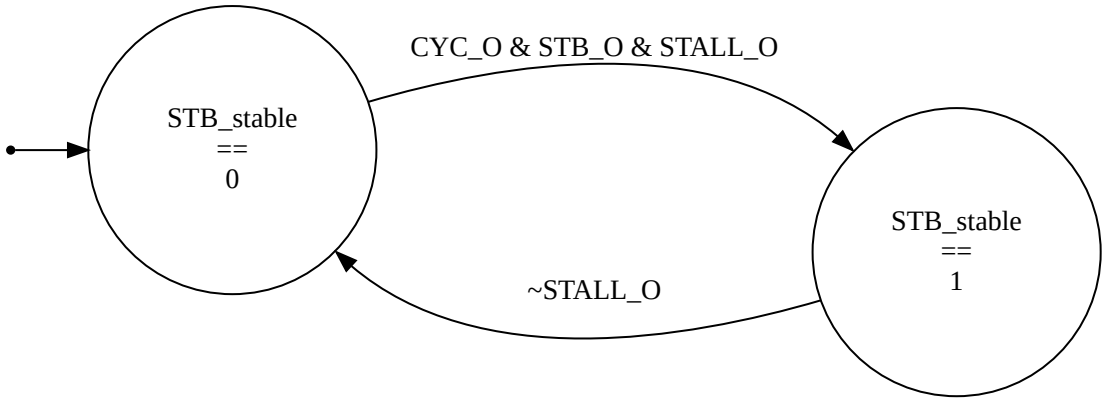


Transfer Request: `STB_O`, `STB_I`

Care Condition

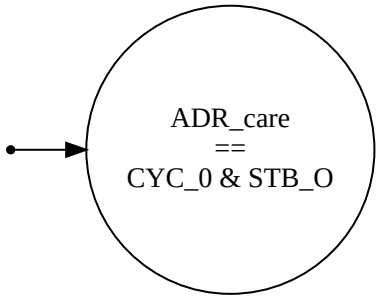


Stable Condition

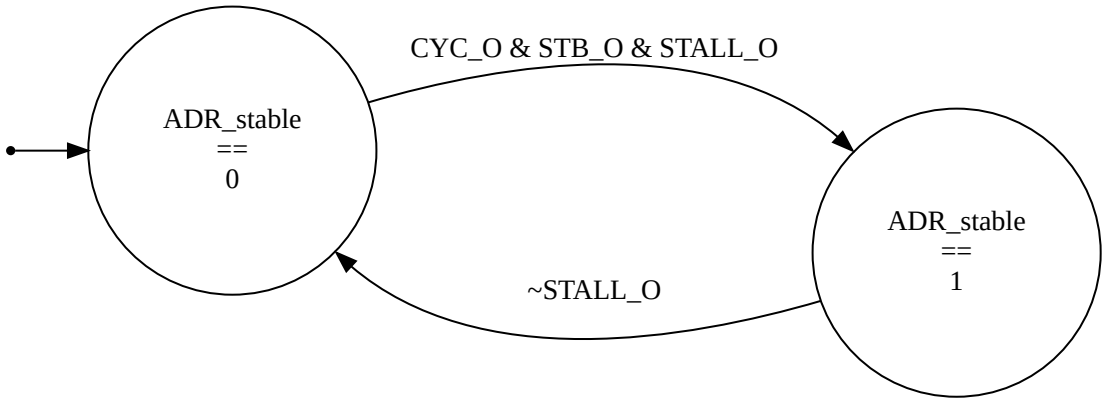


Address Bus: `ADR_O`, `ADR_I`

Care Condition

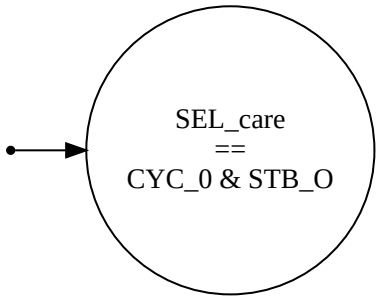


Stable Condition

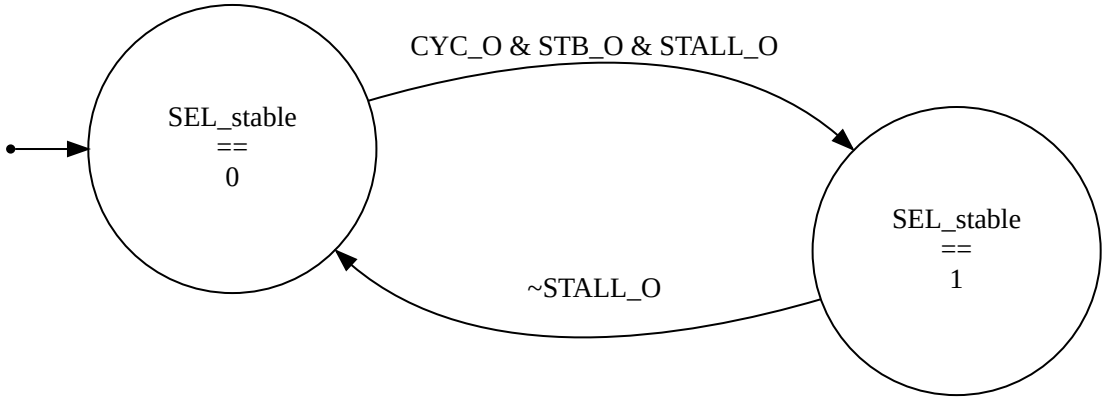


Data Select: `SEL_O`, `SEL_I`

Care Condition

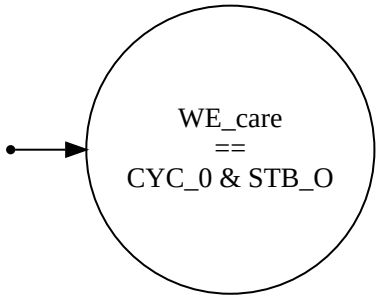


Stable Condition



Data Direction: `WE_O`, `WE_I`

Care Condition

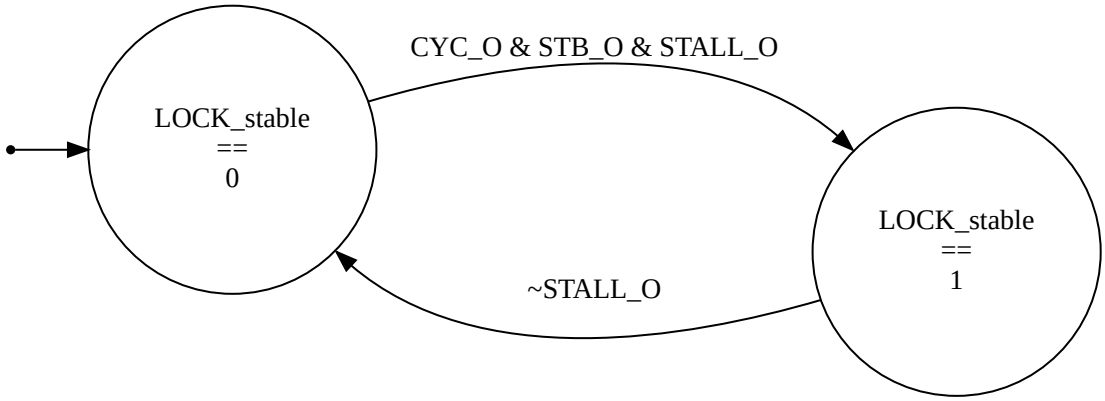


Stable Condition

Target Lock: `LOCK_O`, `LOCK_I`

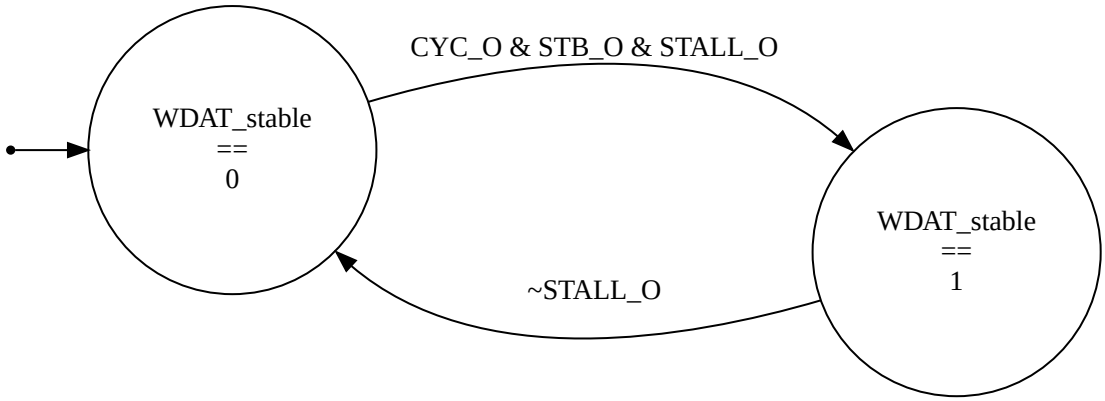
Care Condition

Stable Condition



Write Data: `DAT_O`, `DAT_I`

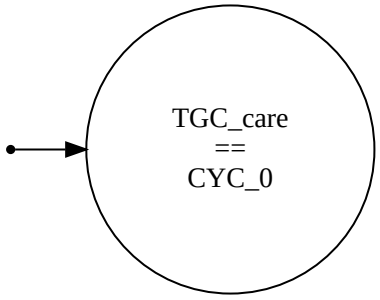
Care Condition



Stable Condition

Cycle Tags: TGC_O, TGC_I

Care Condition

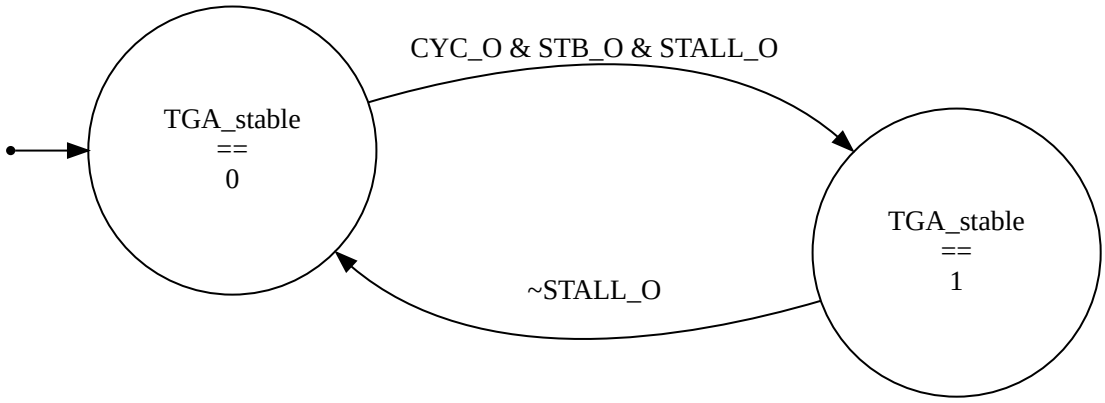


Stable Condition

Address Tags: TGA_O, TGA_I

Care Condition

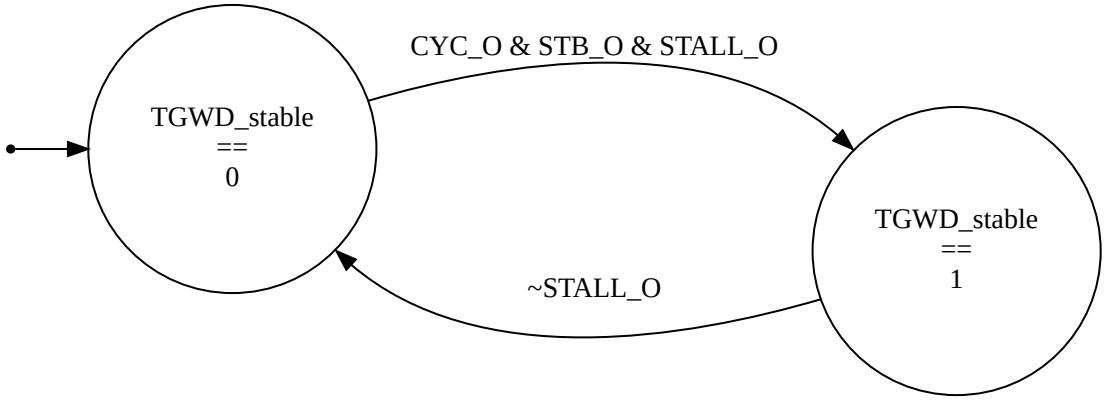
Stable Condition



Write Data Tags: TGD_O, TGD_I

Care Condition

Stable Condition

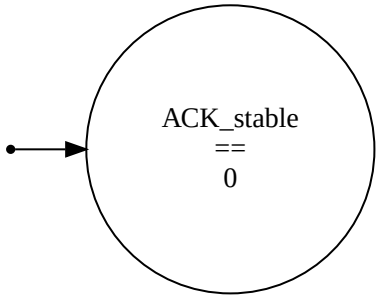


Protocol Signals Driven by the Target

Transfer Completion Indicator: `ACK_O`, `ACK_I`

Care Condition

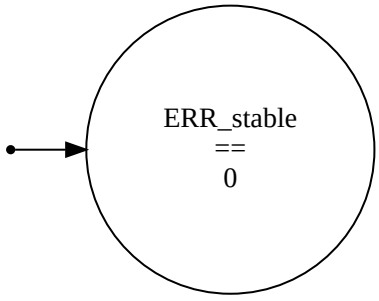
Stable Condition



Permanent Error Indicator: `ERR_O`, `ERR_I`

Care Condition

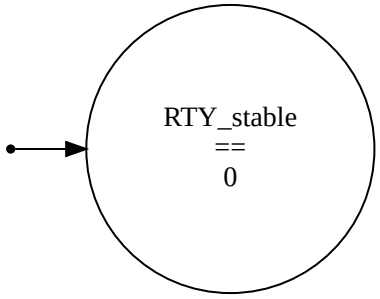
Stable Condition



Temporary Error Indicator: `RTY_O`, `RTY_I`

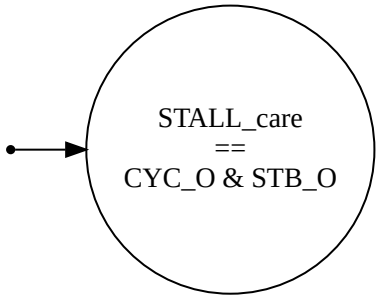
Care Condition

Stable Condition

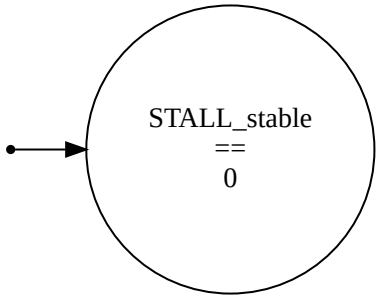


Transfer Delay: STALL_O, STALL_I

Care Condition



Stable Condition



Read Data: DAT_O, DAT_I

Care Condition

Stable Condition

Read Data Tags: TGD_O, TGD_I

Care Condition

Stable Condition

Bibliography

1. *Wishbone B4*. Open Cores, 2010.
2. S. Williams, “Icarus Verilog.” http://iverilog.icarus.com/ .
3. C. Wolf, “Yosys Open SYnthesis Suite.” http://www.clifford.at/yosys/ .


```
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