WbXbc Manual

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Contents

Revision History

Date	Change
October 6, 2018	Preliminary release

1 Overview

WbXbc stands for "**W**ish**b**one **crossb**ar **c**omponents". It is a collection of soft IP blocks for building customized crossbar switches. As all WbXbc blocks interconnect via a common interface (pipelined Wishbone protocol [1]), they can be easily arranged to fulfil application specific performance or size requirements. An example of different ways a set of Wishbone initiators may be connected to a set of Wishbone targets shown in Figure 1-1. The four implementations differ in the number of concurrent bus accesses they support and in the amount of logic gates they require. The WbXbc components in this example are described in Section 4 "Crossbar Switch components".

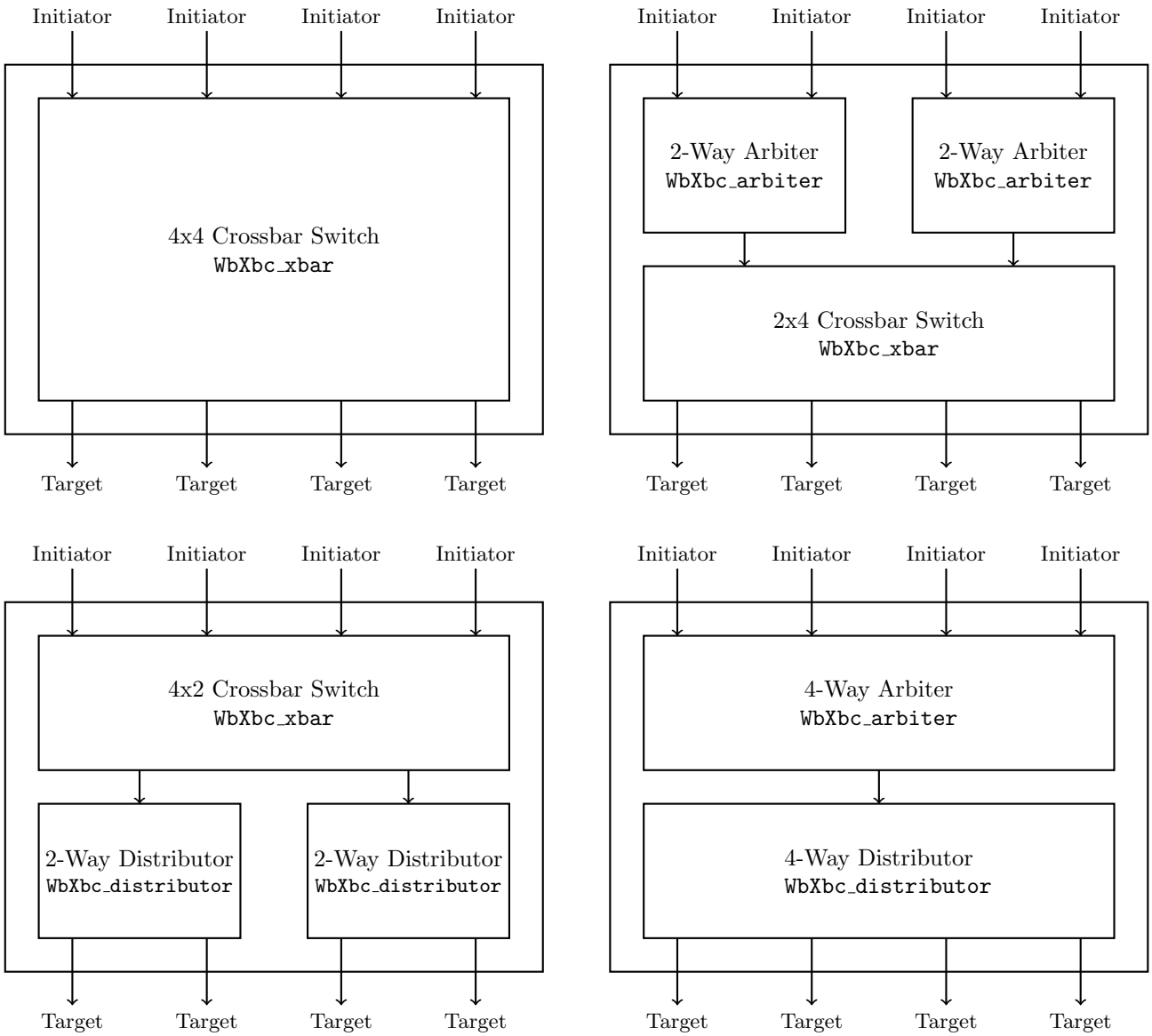

Figure 1-1: Examples of Different Crossbar Implementations

2 Integration Parameters

This section specifies the integration parameters to configure the WbXbc components. Each WbXbc component supports a subset of the parameters listed below.

`ITR_CNT`
: The number of initiator bus interfaces to be offered by the WbXbc component

`TGT_CNT`
: The number of target bus interfaces to be offered by the WbXbc component

`ADR_WIDTH`
: Width of all address busses (`ADR_I` and `ADR_O`)

`ITR_ADR_WIDTH`
: Width of the initiator address bus(ses) (`ADR_I`), in case it differs from the target address bus(es) (`ADR_O`)

`SEL_WIDTH`
: Number data select lines of all initiator and target busses (`SEL_I` and `SEL_O`)

`ITR_SEL_WIDTH`
: Number of data select lines of the initiator bus (`SEL_I`), in case it from the target bus (`SEL_O`)

`DAT_WIDTH`
: Width of all data busses (initiator and target, read and write direction)

`ITR_DAT_WIDTH`
: Width of the initiator's data busses (read and write direction

`TGA_WIDTH`
: Number of tags associated with the address busses of the initiator and the target (`TGA_I` and `TGA_O`)

`TGC_WIDTH`
: Number of tags associated with the cycle indicators (`CYC_I` and `CYC_O`) of thw initiator and the target (`TGC_I` and `TGC_O`)

`TGRD_WIDTH`
: Number of tags assoociated with the read data busses of the initiator and the target (`TGD_O` and `TGD_I`)

`TGWD_WIDTH`
: Number of tags associated with the write data busses of the initiator and the target (`TGD_I` and `TGD_O`)

`BIG_ENDIAN`
: Selects the endianess of the design (1=big endian, 0=little endian)

3 Interface Signals

All WbXbc components share common interface signals, which are described in this chapter. Most of these signals refer directly to the Wishbone specification [1].

Some WbXbc components offer multiple of instances of a particular interface type (e.g. the WbXbx Splitter offers multiple Wishbone target interfaces, the WbXbc Arbiter offers multiple Wishbone initiator interfaces). In these cases, the interfaces are concatinated on a signal by signal basis. For instance, a set of concatinated Wishbone initiator interfaces shares a single `itr_adr_i` bus signal. The individual bus signals are concatinated as a whole (see Figure 3-1). The order of the signal concatination is consistent throughout all interface signals.

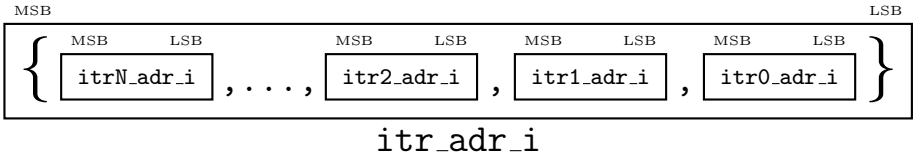

Figure 3-1: Concatination of Interface signals

3.1 Address Region Descriptors

`region_adr_i`
: Target region descriptors (base addresses).

  The address range of each bus target is determined by a base address and an address mask. An address `itr_adr_i` is within the range of the n-th bus target if

$$\begin{array}{c} \texttt{itr\_adr\_i[ADR\_WIDTH-1:0] |} \\ \texttt{region\_msk\_i[(ADR\_WIDTH*(}n\texttt{+1))-1:ADR\_WIDTH*}n\texttt{]} \\ \equiv \\ \texttt{region\_adr\_i[(ADR\_WIDTH*(}n\texttt{+1))-1:ADR\_WIDTH*}n\texttt{] |} \\ \texttt{region\_msk\_i[(ADR\_WIDTH*(}n\texttt{+1))-1:ADR\_WIDTH*}n\texttt{]} \end{array}$$

`region_msk_i`
: Target region descriptors (address masks).
  See `region_adr_i`.

3.2 General Signals (SYSCON)

`clk_i`
: Common clock input for all Wishbone interfaces.
  This clock input corresponds to signal `CLK_I` of the Wishbone specification [1].

`itr_clk_i`
: Clock input for all initiator busses.
  Target busses must be clocked by synchronous and subdivided clock. This clock input corresponds to signal `CLK_I` of the Wishbone specification [1].

`tgt_clk_i`
: Clock input for all target busses.
Initiator busses must be clocked by synchronous and subdivided clock.
This clock input corresponds to signal `CLK_I` of the Wishbone specification [1].

`itr2tgt_sync_i`
: Clock phase indicator for for the WbXbc Decelerator component.
This signal indicates a common positive clock edge of the initiator clock and the synchronous and subdivided target clock (see Figure 3-2).

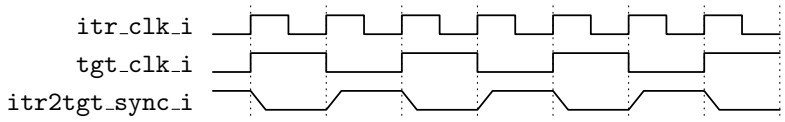

Figure 3-2: `itr2tgt_sync_i` Timing Example

`tgt2itr_sync_i`
: Clock phase indicator for for the WbXbc Accelerator component.
This signal indicates a common positive clock edge of the target clock and the synchronous and subdivided initiator clock (see Figure 3-3).

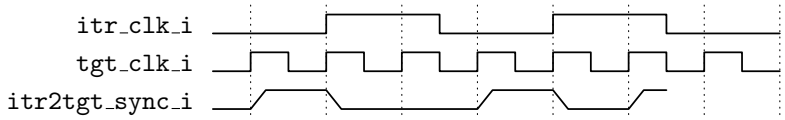

Figure 3-3: `tgt2itr_sync_i` Timing Example

`async_rst_i`
: Optional asynchronous reset input for all sequential logic.
This reset signal may assert asynchronously, but must deassert synchronously.
If no asynchrounous reset is implemented, this input must be tied to zero.

`sync_rst_i`
: Synchronous reset input.
For WbXBC components, this synchronous reset is not required, if an asynchronous reset is provided. If no synchrounous reset is implemented, this input must be tied to zero. This reset input corresponds to signal `RST_I` of the Wishbone specification [1].

3.3 Initiator Bus Signals

`itr_cyc_i`
: Cycle indicator input.
This input signal corresponds to signal `CYC_I` of the Wishbone specification [1].

`itr_stb_i`
: Strobe input.
This input signal corresponds to signal `STB_I` of the Wishbone specification [1].

`itr_we_i`
: Write enable input.
This input signal corresponds to signal `WE_I` of the Wishbone specification [1].

`itr_lock_i`
: Cycle lock input.
This input signal corresponds to signal `LOCK_I` of the Wishbone specification [1].

`itr_sel_i`
: Write data select inputs.
These input signals correspond to bus `SEL_I` of the Wishbone specification [1].

`itr_adr_i`
: Address bus.
These input signals correspond to bus `ADR_I` of the Wishbone specification [1].

`itr_dat_i`
: Write data bus.
These input signals correspond to bus `DAT_I` of the Wishbone specification [1].

`itr_tga_i`
: Address bus tags.
These input signals correspond to bus `TGA_I` of the Wishbone specification [1].

`itr_tgc_i`
: Cycle tags.
These input signals correspond to bus `TGC_I` of the Wishbone specification [1].

`itr_tgd_i`
: Write data tags.
These input signals correspond to bus `TGD_I` of the Wishbone specification [1].

`itr_ack_o`
: Acknowlede output.
This output signal corresponds to signal `ACK_O` of the Wishbone specification [1].

`itr_err_o`
: Error indicator output.
This output signal corresponds to signal `ERR_O` of the Wishbone specification [1].

`itr_rty_o`
: Retry output.
This output signal corresponds to signal `RTY_O` of the Wishbone specification [1].
For all WbXbc components this signal serves as indicator for a lost bus arbitration.

`itr_stall_o`
: Pipeline stall output.
This output signal corresponds to signal `STALL_O` of the Wishbone specification [1].

`itr_dat_o`
: Read data bus.
These output signals correspond to bus `DAT_O` of the Wishbone specification [1].

`itr_tgd_o`
: Read data tags.
These output signals correspond to bus `TGD_O` of the Wishbone specification [1].

3.4 Target Bus Signals

`tgt_cyc_o`
: Cycle indicator output.
This output signal corresponds to signal `CYC_O` of the Wishbone specification [1].

`tgt_stb_o`
: Strobe output.
This output signal corresponds to signal `STB_O` of the Wishbone specification [1].

`tgt_we_o`
: Write enable output.
This output signal corresponds to signal `WE_O` of the Wishbone specification [1].

`tgt_lock_o`
: Cycle lock output.
This output signal corresponds to signal `LOCK_O` of the Wishbone specification [1].

`tgt_sel_o`
: Write data select outputs.
These output signals correspond to bus `SEL_O` of the Wishbone specification [1].

`tgt_adr_o`
: Address bus.
These output signals correspond to bus `ADR_O` of the Wishbone specification [1].

`tgt_dat_o`
: Write data bus.
These output signals correspond to bus `DAT_O` of the Wishbone specification [1].

`tgt_tga_o`
: Address bus tags.
These output signals correspond to bus `TGA_O` of the Wishbone specification [1].

`tgt_tgc_o`
: Cycle tags.
These output signals correspond to bus `TGC_O` of the Wishbone specification [1].

`tgt_tgd_o`
: Write data tags.
These output signals correspond to bus `TGD_O` of the Wishbone specification [1].

`tgt_ack_i`
: Acknowlede input.
This input signal corresponds to signal `ACK_I` of the Wishbone specification [1].

`tgt_err_i`
: Error indicator input.
This input signal corresponds to signal `ERR_I` of the Wishbone specification [1].

`tgt_rty_i`
: Retry input.
This output signal corresponds to signal `RTY_I` of the Wishbone specification [1].
For all WbXbc components this signal serves as indicator for a lost bus arbitration.

`tgt_stall_i`
: Pipeline stall input.
This input signal corresponds to signal `STALL_I` of the Wishbone specification [1].

`tgt_dat_i`
: Read data bus.
These input signals correspond to bus `DAT_I` of the Wishbone specification [1].

`tgt_tgd_i`
: Read data tags.
These input signals correspond to bus `TGD_I` of the Wishbone specification [1].

4 Crossbar Switch components

The WbXbc tontains components to connect Wishbone intefaces of various types. Table 4-1 summarizes the components, which are currently available. Detailed descriptions are given in the following sections.

Table 4-1: List of WbXbc Components

Component	Decription
WbXbc_address_decoder	Decodes the initiator address and generates tags selecting the target memory.
WbXbc_error_generator	Generates an error response, if no target is selected.
WbXbc_splitter	Connects an initiator bus to a set of targets. Tatgets are selected based on tags.
WbXbc_arbiter	Propagates a bus cycle from one of many initiator interfaces to a single target.
WbXbc_expander	Connects an initiator bus to a target with a wider data bus.
WbXbc_reducer	Connects an initiator bus to a target with a narrower data bus.
WbXbc_accelerator	Connects an initiator bus to a target running at a higher clock frequency.
WbXbc_decellerator	Connects an initiator bus to a target running at a lower clock frequency.
WbXbc_pipeliner	Connects a standard Wishbone interface to a pipelined target.
WbXbc_standardizer	Connects a pipelined Wishbone interface to a standard target.
WbXbc_distributor	Connects an initiator bus to a set of targets. Tatgets are selected based on the address.
WbXbc_xbar	Preassembled full crossbar switch.

4.1 WbXbc Address Decoder (`WbXbc_addesss_decoder`)

This module implements an address decoder for the Wishbone protocol. It propagates accesses from the initiator bus to the target bus and adds a set of address tags which selecting the target block (see Figure 4-1).

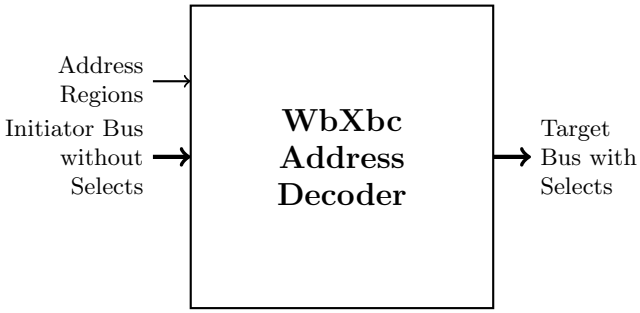

Figure 4-1: Block Diagram of the WbXbc Address Decoder

4.1.1 Integration Parameters

The WbXbc Address Decoder supports the integration parameters listed in Table 4-2. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-2: Integration Parameters of the WbXbc Address Decoder

Parameter	Default	Decription
`TGT_CNT`	4	Number of target addresses to decode
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags

4.1.2 Interface Signals

Table 4-3 lists the interface signals of the WbXbc Address Decoder. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-3: Interface Signals of the WbXbc Address Decoder

Signal	Range	Direction	Decription
Target Address Regions			
region_adr_i	(TGT_CNT*ADR_WIDTH)1:0	input	target address regions
region_msk_i	(TGT_CNT*ADR_WIDTH)1:0	input	selects relevant address bits 1: relevant, 0: ignored)
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
itr_tga_tgtsel_o	TGT_CNT-1:0	output	target select tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.1.3 Verification Status

Table 4-4 provides an overview of the verification status of the WbXbc Address Decoder. Lint checks have been done with the Icarus Verilog simulator [2] and

the Yosys synthesis tool [3].

Table 4-4: Verification Status of the WbXbc Address Decoder

Configuration	Linting	Simulation	Formal	FPGA
Default: ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.2 WbXbc Error Generator (WbXbc_error_generator)

This module implements an error generator or dummy target for the pipelined Wishbone protocol. It propagates accesses from the initiator to the target bus, but intercepts accesses without a target, signaling an error condition to the initiator. The target association is determined by a set of address tags, generated by the address decoder (see Figure 4-2).

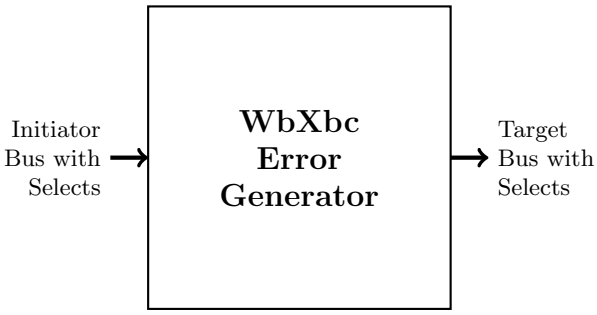

Figure 4-2: Block Diagram of the WbXbc Error Generator

4.2.1 Integration Parameters

The WbXbc Error Generator supports the integration parameters listed in Table 4-5. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-5: Integration Parameters of the WbXbc Error Generator

Parameter	Default	Decription
TGT_CNT	4	Number of target addresses to decode
ADR_WIDTH	16	Width of the address bus
DAT_WIDTH	16	Width of each data bus
SEL_WIDTH	2	Number of data select lines
TGA_WIDTH	1	Number of address tags
TGC_WIDTH	1	Number of cycle tags
TGRD_WIDTH	1	Number of read data tags
TGWD_WIDTH	1	Number of write data tags

4.2.2 Interface Signals

Table 4-6 lists the interface signals of the WbXbc Error Generator. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-6: Interface Signals of the WbXbc Error Generator

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tga_tgtsel_i	TGT_CNT-1:0	input	target select tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
itr_tga_tgtsel_o	TGT_CNT-1:0	output	target select tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.2.3 Verification Status

Table 4-7 provides an overview of the verification status of the WbXbc Error Generator. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-7: Verification Status of the WbXbc Error Generator

Configuration	Linting	Simulation	Formal	FPGA
Default: ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.3 WbXbc Splitter (`WbXbc_splitter`)

This module implements a bus splitter for the pipelined Wishbone protocol. Accesses from the initiator bus are propagated to one of the target busses. The target busses are selected by a set of address tags, generated by the address decoder (see Figure 4-3).

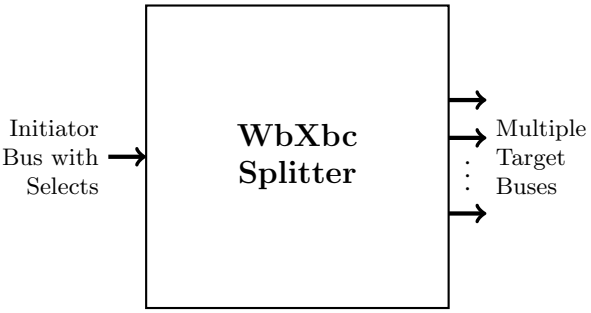

Figure 4-3: Block Diagram of the WbXbc Splitter

4.3.1 Integration Parameters

The WbXbc Splitter supports the integration parameters listed in Table 4-8. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-8: Integration Parameters of the WbXbc Splitter

Parameter	Default	Decription
`TGT_CNT`	4	Number of target busses
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags

4.3.2 Interface Signals

Table 4-9 lists the interface signals of the WbXbc Splitter. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-9: Interface Signals of the WbXbc Splitter

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tga_tgtsel_i	TGT_CNT-1:0	input	target select tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o	TGT_CNT-1:0	output	concatinated bus cycle indicators
tgt_stb_o	TGT_CNT-1:0	output	concatinated access requests
tgt_we_o	TGT_CNT-1:0	output	concatinated write enables
tgt_lock_o	TGT_CNT-1:0	output	concatinated bus cycle locks
tgt_sel_o	(TGT_CNT*SEL_WIDTH)-1:0	output	concatinated write data selects
tgt_adr_o	(TGT_CNT*ADR_WIDTH)-1:0	output	concatinated write data selects
tgt_dat_o	(TGT_CNT*DAT_WIDTH)-1:0	output	concatinated write data busses
tgt_tga_o	(TGT_CNT*TGA_WIDTH))-1:0	output	concatinated address tags
tgt_tgc_o	(TGT_CNT*TGC_WIDTH)-1:0	output	concatinated bus cycle tags
tgt_tgd_o	(TGT_CNT*TGWD_WIDT)-1:0	output	concatinated write data tags
tgt_ack_i	TGT_CNT-1:0	input	concatinated bus cycle acknowledges
tgt_err_i	TGT_CNT-1:0	input	concatinated error indicators
tgt_rty_i	TGT_CNT-1:0	input	concatinated retry requests
tgt_stall_i	TGT_CNT-1:0	input	concatinated access delays
tgt_dat_i	(TGT_CNT*DAT_WIDTH-1):0	input	concatinated read data busses
tgt_tgd_i	(TGT_CNT*TGRD_WIDTH-1):0	input	concatinated read data tags

4.3.3 Verification Status

Table 4-10 provides an overview of the verification status of the WbXbc Splitter. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys

synthesis tool [3].

Table 4-10: Verification Status of the WbXbc Splitter

Configuration	Linting	Simulation	Formal	FPGA
Default: TGT_CNT 4 ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.4 WbXbc Arbiter (`WbXbc_arbiter`)

This module implements a bus arbiter for the pipelined Wishbone protocol. Accesses from multiple initiator busses are arbitrated and propagated to the target bus (see Figure 4-4). Each initiator bus can request bus accesses at two priority levels. The priority levels are selected via a set of address tags. Access requests of equal priority are arbitrated with a fixed priority (initiator 0 has the higheest priority).

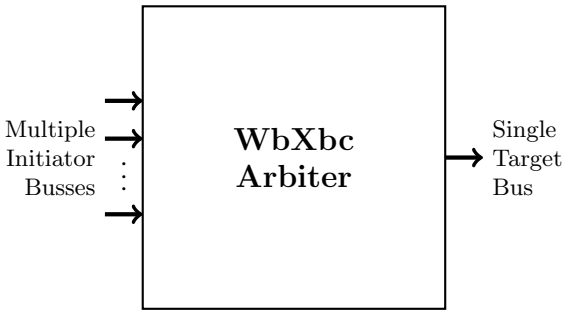

Figure 4-4: Block Diagram of the WbXbc Arbiter

4.4.1 Integration Parameters

The WbXbc Arbiter supports the integration parameters listed in Table 4-11. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-11: Integration Parameters of the WbXbc Arbiter

Parameter	Default	Decription
`ITR_CNT`	4	Number of initiator busses
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags

4.4.2 Interface Signals

Table 4-12 lists the interface signals of the WbXbc Arbiter. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-12: Interface Signals of the WbXbc Arbiter

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i	ITR_CNT-1:0	input	concatinated bus cycle indicators
itr_stb_i	ITR_CNT-1:0	input	concatinated access requests
itr_we_i	ITR_CNT-1:0	input	concatinated write enables
itr_lock_i	ITR_CNT-1:0	input	concatinated bus cycle locks
itr_sel_i	(ITR_CNT*SEL_WIDTH)-1:0	input	concatinated write data selects
itr_adr_i	(ITR_CNT*ADR_WIDTH)-1:0	input	concatinated address busses
itr_dat_i	(ITR_CNT*DAT_WIDTH)-1:0	input	concatinated write data busses
itr_tga_i	(ITR_CNT*TGA_WIDTH)-1:0	input	concatinated address tags
itr_tga_prio_i	ITR_CNT-1:0	input	concatinated access priorities
itr_tgc_i	(ITR_CNT*TGC_WIDTH)-1:0	input	concatinated bus cycle tags
itr_tgd_i	(ITR_CNT*TGWD_WIDTH)-1:0	input	concatinated write data tags
itr_ack_o	ITR_CNT-1:0	output	concatinated bus cycle acknowledges
itr_err_o	ITR_CNT-1:0	output	concatinated error indicators
itr_rty_o	ITR_CNT-1:0	output	concatinated retry requests
itr_stall_o	ITR_CNT-1:0	output	concatinated access delays
itr_dat_o	(ITR_CNT*DAT_WIDTH)-1:0	output	concatinated read data buses
itr_tgd_o	(ITR_CNT*TGRD_WIDTH)-1:0	output	concatinated read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.4.3 Verification Status

Table 4-13 provides an overview of the verification status of the WbXbc Arbiter. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys

synthesis tool [3].

Table 4-13: Verification Status of the WbXbc Arbiter

Configuration	Linting	Simulation	Formal	FPGA
Default: ITR_CNT 4 ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.5 WbXbc Expander (`WbXbc_expander`)

This module connects a pipelined Wishbone initiator to a target with twice the data bus width (see Figure 4-5).

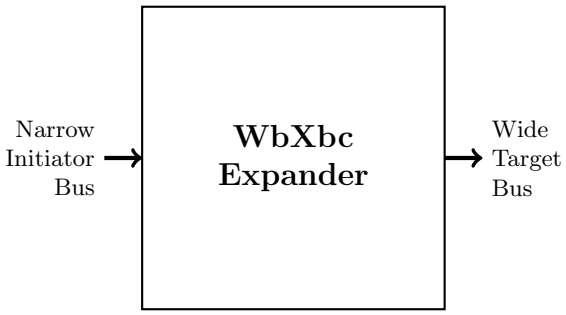

Figure 4-5: Block Diagram of the WbXbc Expander

4.5.1 Integration Parameters

The WbXbc Expander supports the integration parameters listed in Table 4-14. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-14: Integration Parameters of the WbXbc Expander

Parameter	Default	Decription
ITR_ADR_WIDTH	16	Width of the address bus
ITR_DAT_WIDTH	16	Width of each data bus
ITR_SEL_WIDTH	2	Number of data select lines
TGA_WIDTH	1	Number of address tags
TGC_WIDTH	1	Number of cycle tags
TGRD_WIDTH	1	Number of read data tags
TGWD_WIDTH	1	Number of write data tags
BIG_ENDIAN	1	Endianess of the component

4.5.2 Interface Signals

Table 4-15 lists the interface signals of the WbXbc Expander. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-15: Interface Signals of the WbXbc Expander

Signal	Range	Direction	Decription
Target Address Regions			
region_addr_i	(TGT_CNT*ADR_WIDTH)1:0	input	target address
region_mask_i	(TGT_CNT*ADR_WIDTH)1:0	input	selects relevant address bits (1: relevant, 0: ignored)
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	ITR_SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ITR_ADR_WIDTH-1:0	input	address bus
itr_dat_i	ITR_DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	(ITR_SEL_WIDTH*2)-1:0	output	write data selects
tgt_adr_o	ITR_ADR_WIDTH-2:0	output	write data selects
tgt_dat_o	(ITR_DAT_WIDTH*2)-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.5.3 Verification Status

Table 4-16 provides an overview of the verification status of the WbXbc Expander. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-16: Verification Status of the WbXbc Expander

Configuration	Linting	Simulation	Formal	FPGA
Default: ITR_ADR_WIDTH 16 ITR_DAT_WIDTH 16 ITR_SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1 BIG_ENDIAN 1	iVerilog [2] Yosis [3]			

4.6 WbXbc Reducer (`WbXbc_reducer`)

This module connects a pipelined Wishbone initiator to a target with half the data bus width (see Figure 4-6). Initiator bus accesses may be converted into two consecutive accesses to the target bus.

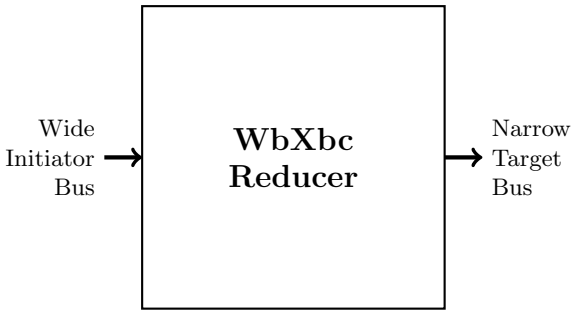

Figure 4-6: Block Diagram of the WbXbc Reducer

4.6.1 Integration Parameters

The WbXbc Reducer supports the integration parameters listed in Table 4-17. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-17: Integration Parameters of the WbXbc Reducer

Parameter	Default	Decription
`ITR_ADR_WIDTH`	16	Width of the address bus
`ITR_DAT_WIDTH`	16	Width of each data bus
`ITR_SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags
`BIG_ENDIAN`	1	Endianess of the component

4.6.2 Interface Signals

Table 4-18 lists the interface signals of the WbXbc Reducer. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-18: Interface Signals of the WbXbc Reducer

Signal	Range	Direction	Decription
Target Address Regions			
region_addr_i	(TGT_CNT*ADR_WIDTH)1:0	input	target address
region_mask_i	(TGT_CNT*ADR_WIDTH)1:0	input	selects relevant address bits (1: relevant, 0: ignored)
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	ITR_SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ITR_ADR_WIDTH-1:0	input	address bus
itr_dat_i	ITR_DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	(ITR_SEL_WIDTH/2)-1:0	output	write data selects
tgt_adr_o	ITR_ADR_WIDTH:0	output	write data selects
tgt_dat_o	(ITR_DAT_WIDTH/2)-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.6.3 Verification Status

Table 4-19 provides an overview of the verification status of the WbXbc Reducer. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-19: Verification Status of the WbXbc Reducer

Configuration	Linting	Simulation	Formal	FPGA
Default: ITR_ADR_WIDTH 16 ITR_DAT_WIDTH 16 ITR_SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1 BIG_ENDIAN 1	iVerilog [2] Yosis [3]			

4.7 WbXbc Accelerator (`WbXbc_accelerator`)

This module connects a pipelined Wishbone initiator, running at a higher frequency to a target, running at a lower frequency (see Figure 4-7).

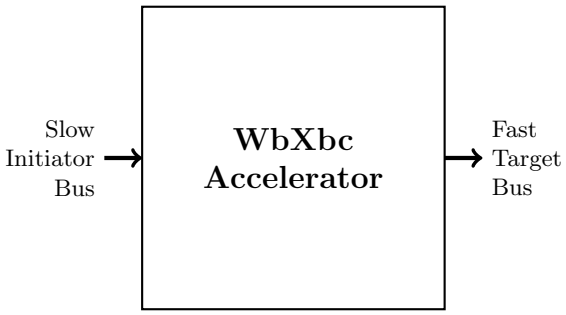

Figure 4-7: Block Diagram of the WbXbc Accelerator

4.7.1 Integration Parameters

The WbXbc Accelerator supports the integration parameters listed in Table 4-20. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-20: Integration Parameters of the WbXbc Accelerator

Parameter	Default	Decription
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags
`REG_ITR`	0	Register initiator bus inputs

4.7.2 Interface Signals

Table 4-21 lists the interface signals of the WbXbc Accelerator. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-21: Interface Signals of the WbXbc Accelerator

Signal	Range	Direction	Decription
Clock and Reset			
tgt_clk_i		input	target clock
tgt2itr_sync_i		input	clock sync signal
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.7.3 Verification Status

Table 4-22 provides an overview of the verification status of the WbXbc Accelerator. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys

synthesis tool [3].

Table 4-22: Verification Status of the WbXbc Accelerator

Configuration	Linting	Simulation	Formal	FPGA
Default: ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1 REG_ITR 0	iVerilog [2] Yosis [3]			

4.8 WbXbc Decelerator (`WbXbc_decelerator`)

This module connects a pipelined Wishbone initiator, running at a higher frequency to a target, running at a lower frequency (see Figure 4-8).

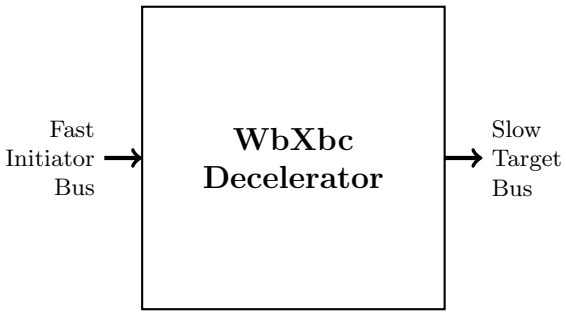

Figure 4-8: Block Diagram of the WbXbc Decelerator

4.8.1 Integration Parameters

The WbXbc Decelerator supports the integration parameters listed in Table 4-23. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-23: Integration Parameters of the WbXbc Decelerator

Parameter	Default	Decription
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags
`REG_ITR`	0	Register initiator bus inputs
`REG_TGT`	0	Register target bus inputs

4.8.2 Interface Signals

Table 4-24 lists the interface signals of the WbXbc Decelerator. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-24: Interface Signals of the WbXbc Decelerator

Signal	Range	Direction	Decription
Clock and Reset			
itr_clk_i		input	initiator clock
itr2tgt_sync_i		input	clock sync signal
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.8.3 Verification Status

Table 4-25 provides an overview of the verification status of the WbXbc Decelerator. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys

synthesis tool [3].

Table 4-25: Verification Status of the WbXbc Decelerator

Configuration	Linting	Simulation	Formal	FPGA
Default: ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1 REG_ITR 0 REG_TGT 0	iVerilog [2] Yosis [3]			

4.9 WbXbc Pipeliner (`WbXbc_pipeliner`)

This module connects a standard protocol Wishbone initiator to a pipelined target (see Figure 4-9).

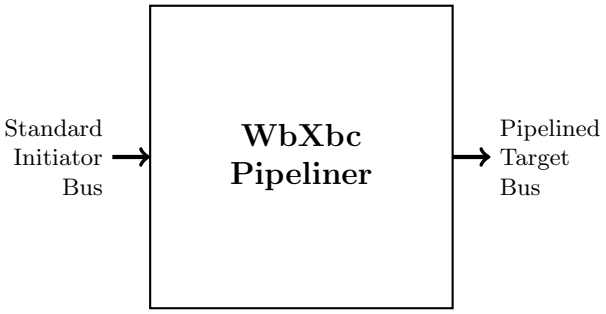

Figure 4-9: Block Diagram of the WbXbc Pipeliner

4.9.1 Integration Parameters

The WbXbc Pipeliner supports the integration parameters listed in Table 4-26. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-26: Integration Parameters of the WbXbc Pipeliner

Parameter	Default	Decription
ADR_WIDTH	16	Width of the address bus
DAT_WIDTH	16	Width of each data bus
SEL_WIDTH	2	Number of data select lines
TGA_WIDTH	1	Number of address tags
TGC_WIDTH	1	Number of cycle tags
TGRD_WIDTH	1	Number of read data tags
TGWD_WIDTH	1	Number of write data tags

4.9.2 Interface Signals

Table 4-27 lists the interface signals of the WbXbc Pipeliner. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-27: Interface Signals of the WbXbc Pipeliner

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.9.3 Verification Status

Table 4-28 provides an overview of the verification status of the WbXbc Pipeliner. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-28: Verification Status of the WbXbc Pipeliner

Configuration	Linting	Simulation	Formal	FPGA
Default: ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.10 WbXbc Standardizer (`WbXbc_standardizer`)

This module connects a pipelined Wishbone initiator to a standard protocol target (see Figure 4-10).

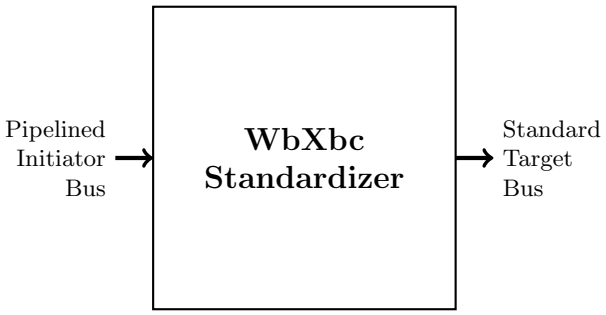

Figure 4-10: Block Diagram of the WbXbc Standardizer

4.10.1 Integration Parameters

The WbXbc Standardizer supports the integration parameters listed in Table 4-29. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-29: Integration Parameters of the WbXbc Standardizer

Parameter	Default	Decription
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags

4.10.2 Interface Signals

Table 4-30 lists the interface signals of the WbXbc Standardizer. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-30: Interface Signals of the WbXbc Standardizer

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o		output	bus cycle indicator
tgt_stb_o		output	access request
tgt_we_o		output	write enable
tgt_lock_o		output	uninterruptable bus cycle
tgt_sel_o	SEL_WIDTH-1:0	output	write data selects
tgt_adr_o	ADR_WIDTH-1:0	output	write data selects
tgt_dat_o	DAT_WIDTH-1:0	output	write data bus
tgt_tga_o	TGA_WIDTH-1:0	output	address tags
tgt_tgc_o	TGC_WIDTH-1:0	output	bus cycle tags
tgt_tgd_o	TGWD_WIDTH-1:0	output	write data tags
tgt_ack_i		input	bus cycle acknowledge
tgt_err_i		input	error indicator
tgt_rty_i		input	retry request
tgt_stall_i		input	access delay
tgt_dat_i	DAT_WIDTH-1:0	input	read data bus
tgt_tgd_i	TGRD_WIDTH-1:0	input	read data tags

4.10.3 Verification Status

Table 4-31 provides an overview of the verification status of the WbXbc Standardizer. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-31: Verification Status of the WbXbc Standardizer

Configuration	Linting	Simulation	Formal	FPGA
Default: ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.11 WbXbc Distributor (`WbXbc_distributor`)

This module combines an an and a or the pipelined Wishbone protocol (see Figure 4-11).

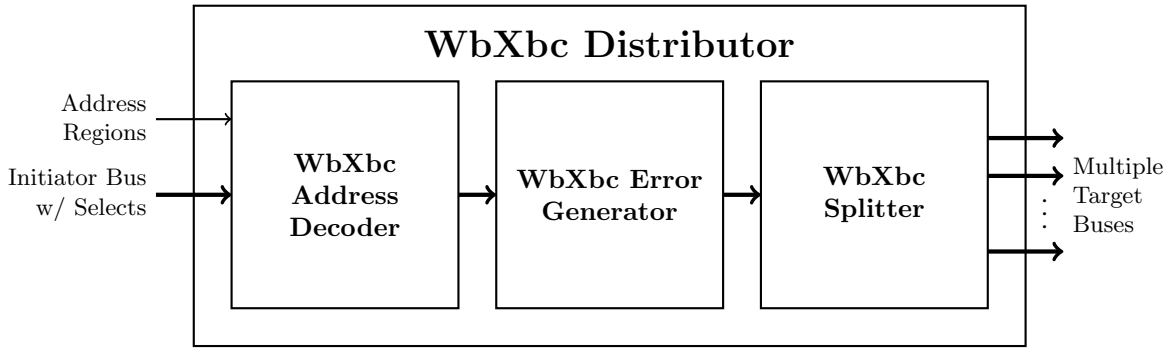

Figure 4-11: Block Diagram of the WbXbc Distributor

4.11.1 Integration Parameters

The WbXbc Distributor supports the integration parameters listed in Table 4-32. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-32: Integration Parameters of the WbXbc Distributor

Parameter	Default	Decription
`TGT_CNT`	4	Number of target busses
`ADR_WIDTH`	16	Width of the address bus
`DAT_WIDTH`	16	Width of each data bus
`SEL_WIDTH`	2	Number of data select lines
`TGA_WIDTH`	1	Number of address tags
`TGC_WIDTH`	1	Number of cycle tags
`TGRD_WIDTH`	1	Number of read data tags
`TGWD_WIDTH`	1	Number of write data tags

4.11.2 Interface Signals

Table 4-33 lists the interface signals of the WbXbc Distributor. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-33: Interface Signals of the WbXbc Distributor

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Target Address Regions			
region_adr_i	(TGT_CNT*ADR_WIDTH)1:0	input	target address regions
region_msk_i	(TGT_CNT*ADR_WIDTH)1:0	input	selects relevant address bits (1: relevant, 0: ignored)
Initiator Interface			
itr_cyc_i		input	bus cycle indicator
itr_stb_i		input	access request
itr_we_i		input	write enable
itr_lock_i		input	uninterruptable bus cycle
itr_sel_i	SEL_WIDTH-1:0	input	write data selects
itr_adr_i	ADR_WIDTH-1:0	input	address bus
itr_dat_i	DAT_WIDTH-1:0	input	write data bus
itr_tga_i	TGA_WIDTH-1:0	input	address tags
itr_tgc_i	TGC_WIDTH-1:0	input	bus cycle tags
itr_tgd_i	TGWD_WIDTH-1:0	input	write data tags
itr_ack_o		output	bus cycle acknowledge
itr_err_o		output	error indicator
itr_rty_o		output	retry request
itr_stall_o		output	access delay
itr_dat_o	DAT_WIDTH-1:0	output	read data bus
itr_tgd_o	TGRD_WIDTH-1:0	output	read data tags
Target Interface			
tgt_cyc_o	TGT_CNT-1:0	output	concatinated bus cycle indicators
tgt_stb_o	TGT_CNT-1:0	output	concatinated access requests
tgt_we_o	TGT_CNT-1:0	output	concatinated write enables
tgt_lock_o	TGT_CNT-1:0	output	concatinated bus cycle locks
tgt_sel_o	(TGT_CNT*SEL_WIDTH)-1:0	output	concatinated write data selects
tgt_adr_o	(TGT_CNT*ADR_WIDTH)-1:0	output	concatinated write data selects
tgt_dat_o	(TGT_CNT*DAT_WIDTH)-1:0	output	concatinated write data busses
tgt_tga_o	(TGT_CNT*TGA_WIDTH))-1:0	output	concatinated address tags
tgt_tgc_o	(TGT_CNT*TGC_WIDTH)-1:0	output	concatinated bus cycle tags
tgt_tgd_o	(TGT_CNT*TGWD_WIDT)-1:0	output	concatinated write data tags
tgt_ack_i	TGT_CNT-1:0	input	concatinated bus cycle acknowledges
tgt_err_i	TGT_CNT-1:0	input	concatinated error indicators
tgt_rty_i	TGT_CNT-1:0	input	concatinated retry requests
tgt_stall_i	TGT_CNT-1:0	input	concatinated access delays
tgt_dat_i	(TGT_CNT*DAT_WIDTH-1):0	input	concatinated read data busses
tgt_tgd_i	(TGT_CNT*TGRD_WIDTH-1):0	input	concatinated read data tags

4.11.3 Verification Status

Table 4-34 provides an overview of the verification status of the WbXbc Distributor. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-34: Verification Status of the WbXbc Distributor

Configuration	Linting	Simulation	Formal	FPGA
Default: TGT_CNT 4 ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

4.12 WbXbc Xbar (`WbXbc_xbar`)

This module implements a full crossbar switch between a set of initator busses and a set of target busses, all using the pipelined Wishbone protocol. The WbXbc Xbar consists nd omponents (see Figure 4-12).

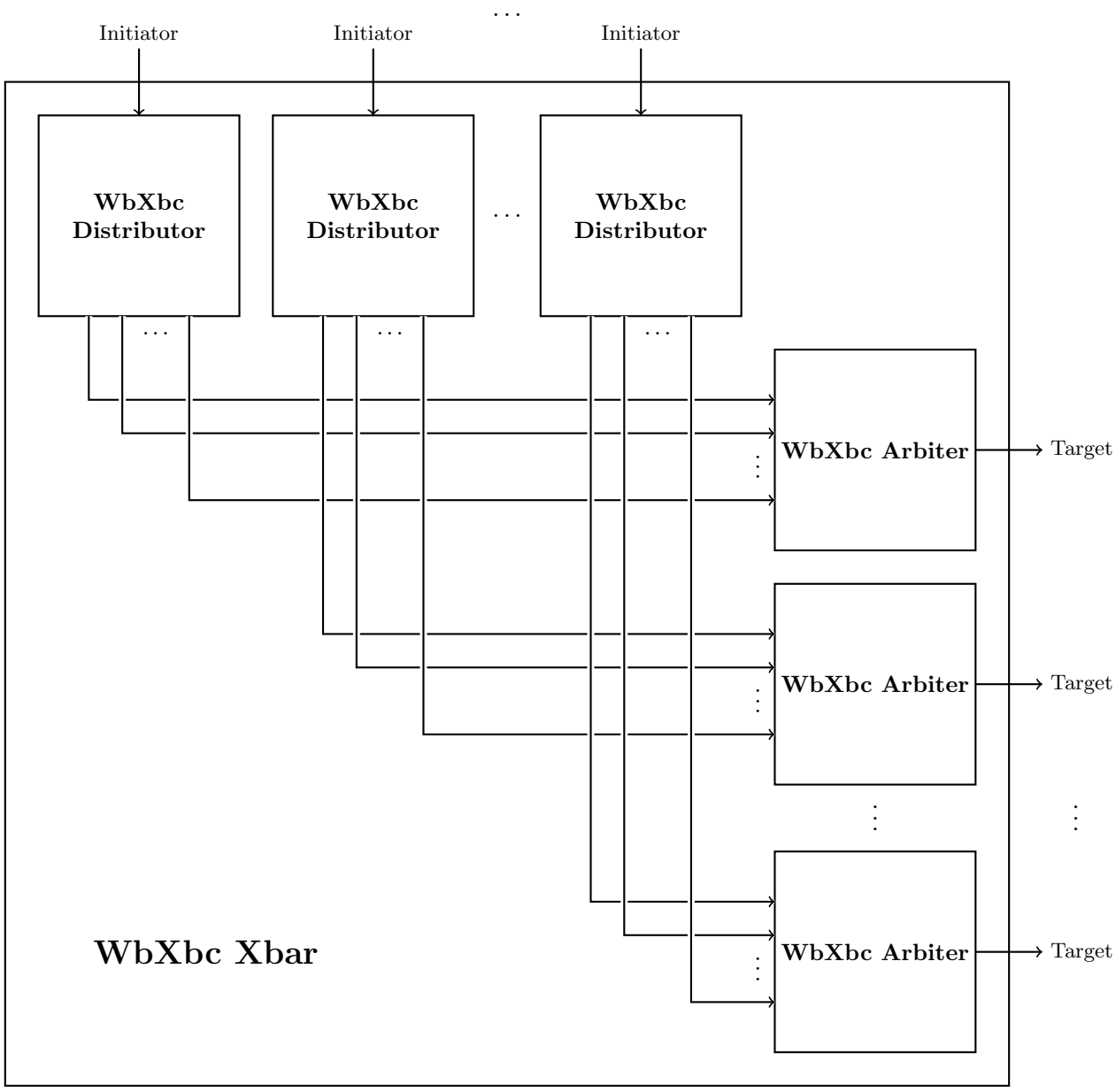

Figure 4-12: Block Diagram of the WbXbc Xbar

4.12.1 Integration Parameters

The WbXbc Xbar supports the integration parameters listed in Table 4-35. See Section 2 "Integration Parameters" for a detailed description of all integration parameters.

Table 4-35: Integration Parameters of the WbXbc Xbar

Parameter	Default	Decription
ITR_CNT	4	Number of initiator busses
TGT_CNT	4	Number of target busses
ADR_WIDTH	16	Width of the address bus
DAT_WIDTH	16	Width of each data bus
SEL_WIDTH	2	Number of data select lines
TGA_WIDTH	1	Number of address tags
TGC_WIDTH	1	Number of cycle tags
TGRD_WIDTH	1	Number of read data tags
TGWD_WIDTH	1	Number of write data tags

4.12.2 Interface Signals

Table 4-36 lists the interface signals of the WbXbc Xbar. See Section 3 "Interface Signals" for a detailed description of all interface signals.

Table 4-36: Interface Signals of the WbXbc Xbar

Signal	Range	Direction	Decription
Clock and Reset			
clk_i		input	module clock
async_rst_i		input	asynchronous reset
sync_rst_i		input	synchronous reset
Target Address Regions			
region_adr_i	(TGT_CNT*ADR_WIDTH)1:0	input	target address
region_msk_i	(TGT_CNT*ADR_WIDTH)1:0	input	selects relevant address bits (1: relevant, 0: ignored)

...continued

Table 4-36: Interface Signals of the WbXbc Xbar

Signal	Range	Direction	Decription
Initiator Interface			
itr_cyc_i	ITR_CNT-1:0	input	concatinated bus cycle indicators
itr_stb_i	ITR_CNT-1:0	input	concatinated access requests
itr_we_i	ITR_CNT-1:0	input	concatinated write enables
itr_lock_i	ITR_CNT-1:0	input	concatinated bus cycle locks
itr_sel_i	(ITR_CNT*SEL_WIDTH)-1:0	input	concatinated write data selects
itr_adr_i	(ITR_CNT*ADR_WIDTH)-1:0	input	concatinated address busses
itr_dat_i	(ITR_CNT*DAT_WIDTH)-1:0	input	concatinated write data busses
itr_tga_i	(ITR_CNT*TGA_WIDTH)-1:0	input	concatinated address tags
itr_tga_prio_i	ITR_CNT-1:0	input	concatinated access priorities
itr_tgc_i	(ITR_CNT*TGC_WIDTH)-1:0	input	concatinated bus cycle tags
itr_tgd_i	(ITR_CNT*TGWD_WIDTH)-1:0	input	concatinated write data tags
itr_ack_o	ITR_CNT-1:0	output	concatinated bus cycle acknowledges
itr_err_o	ITR_CNT-1:0	output	concatinated error indicators
itr_rty_o	ITR_CNT-1:0	output	concatinated retry requests
itr_stall_o	ITR_CNT-1:0	output	concatinated access delays
itr_dat_o	(ITR_CNT*DAT_WIDTH)-1:0	output	concatinated read data buses
itr_tgd_o	(ITR_CNT*TGRD_WIDTH)-1:0	output	concatinated read data tags
Target Interface			
tgt_cyc_o	TGT_CNT-1:0	output	concatinated bus cycle indicators
tgt_stb_o	TGT_CNT-1:0	output	concatinated access requests
tgt_we_o	TGT_CNT-1:0	output	concatinated write enables
tgt_lock_o	TGT_CNT-1:0	output	concatinated bus cycle locks
tgt_sel_o	(TGT_CNT*SEL_WIDTH)-1:0	output	concatinated write data selects
tgt_adr_o	(TGT_CNT*ADR_WIDTH)-1:0	output	concatinated write data selects
tgt_dat_o	(TGT_CNT*DAT_WIDTH)-1:0	output	concatinated write data busses
tgt_tga_o	(TGT_CNT*TGA_WIDTH))-1:0	output	concatinated address tags
tgt_tgc_o	(TGT_CNT*TGC_WIDTH)-1:0	output	concatinated bus cycle tags
tgt_tgd_o	(TGT_CNT*TGWD_WIDT)-1:0	output	concatinated write data tags
tgt_ack_i	TGT_CNT-1:0	input	concatinated bus cycle acknowledges
tgt_err_i	TGT_CNT-1:0	input	concatinated error indicators
tgt_rty_i	TGT_CNT-1:0	input	concatinated retry requests
tgt_stall_i	TGT_CNT-1:0	input	concatinated access delays
tgt_dat_i	(TGT_CNT*DAT_WIDTH-1):0	input	concatinated read data busses
tgt_tgd_i	(TGT_CNT*TGRD_WIDTH-1):0	input	concatinated read data tags

4.12.3 Verification Status

Table 4-37 provides an overview of the verification status of the WbXbc Xbar. Lint checks have been done with the Icarus Verilog simulator [2] and the Yosys synthesis tool [3].

Table 4-37: Verification Status of the WbXbc Xbar

Configuration	Linting	Simulation	Formal	FPGA
Default: ITR_CNT 4 TGT_CNT 4 ADR_WIDTH 16 DAT_WIDTH 16 SEL_WIDTH 2 TGA_WIDTH 1 TGC_WIDTH 1 TGRD_WIDTH 1 TGWD_WIDTH 1	iVerilog [2] Yosis [3]			

References

[1] Wishbone b4. http://cdn.opencores.org/downloads/wbspec_b4.pdf, 2010.

[2] Stephen Williams. Icarus verilog. http://iverilog.icarus.com/.

[3] Clifford Wolf. Yosys open synthesis suite. http://www.clifford.at/yosys/.