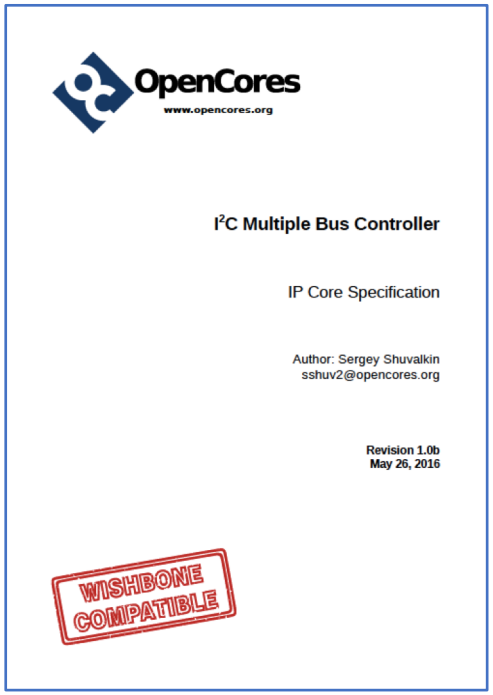
ECE 745

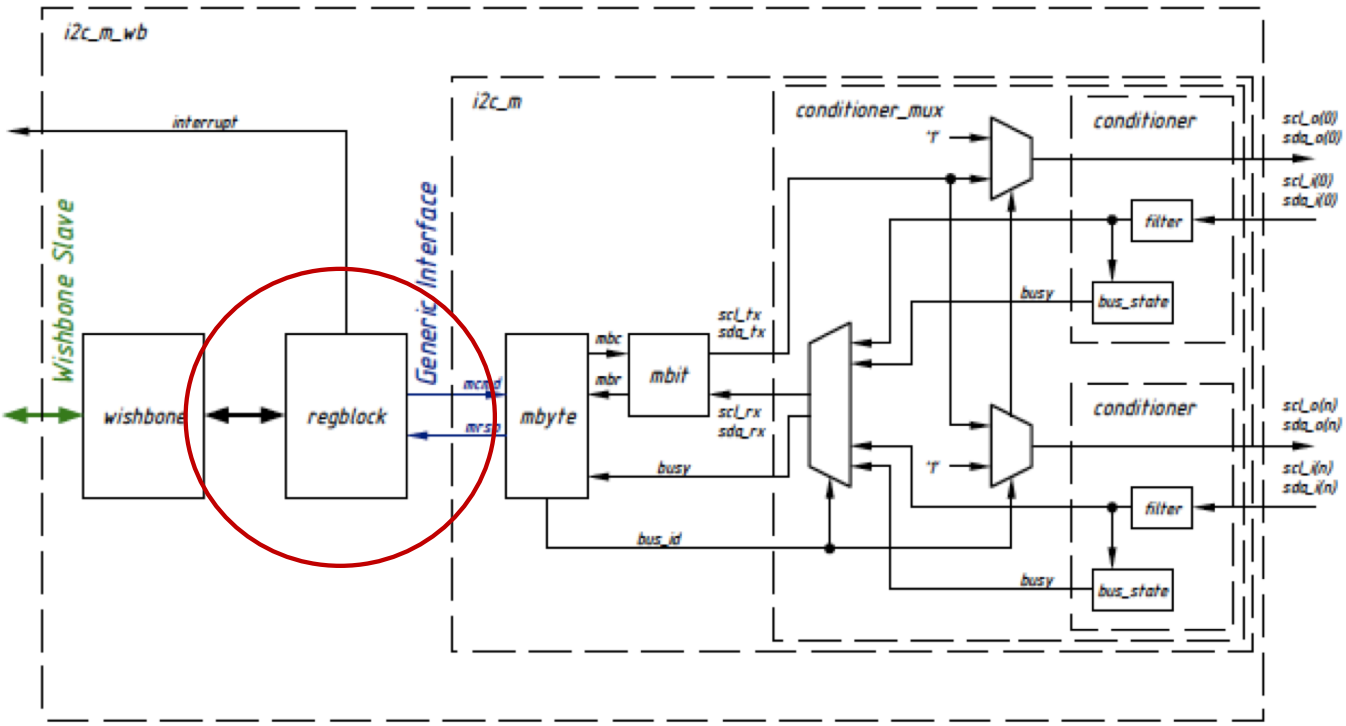
ASIC Verification

Project 3 Assignment – I2CMB Test Plan and Coverage



Create a Test Plan from the I2CMB Specification

Example of Where Bugs May Reside



Register Testing

5 Registers

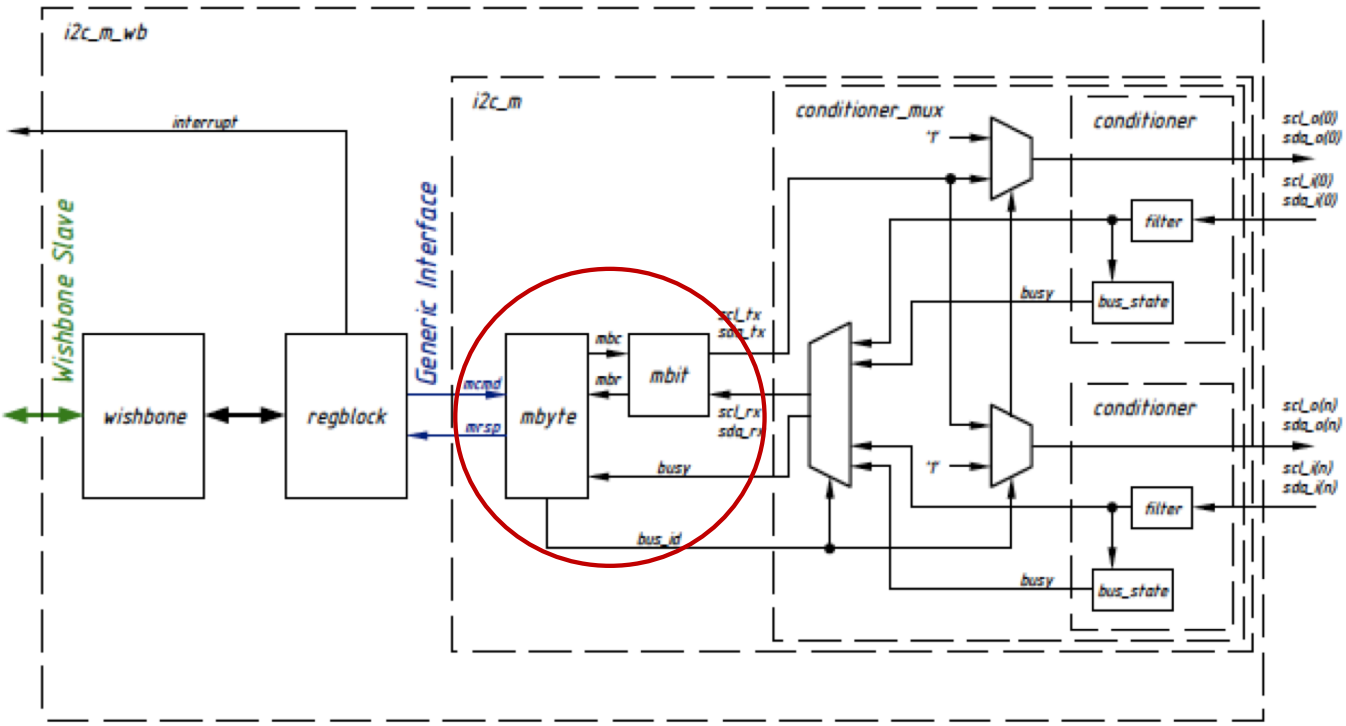
Wishbone and Avalon-MM based top level modules of IICMB controller (`iicmb_m_wb.vhd` and `iicmb_m_av.vhd`) contain a register block with the following registers. Note, that the sequencer based top level (`iicmb_m_sq.vhd`) does without them.

Name	Offset	Access	Description
CSR	0x00	R/W	Control/Status Register
DPR	0x01	R/W	Data/Parameter Register
CMDR	0x02	R/W	Command Register
FSMR	0x03	RO	FSM States Register

Table 15: IICMB registers

- Addresses valid?
- Response to invalid addresses?
- Register or field aliasing?
- Register and field default values?
- Register access permissions enforced?
- Register fields accurate
  - Purpose, access permissions,

Example of Where Bugs May Reside



FSM Flow Testing

- State values in register correct?
- State transitioning valid?
- All states covered?
- All transitions covered?

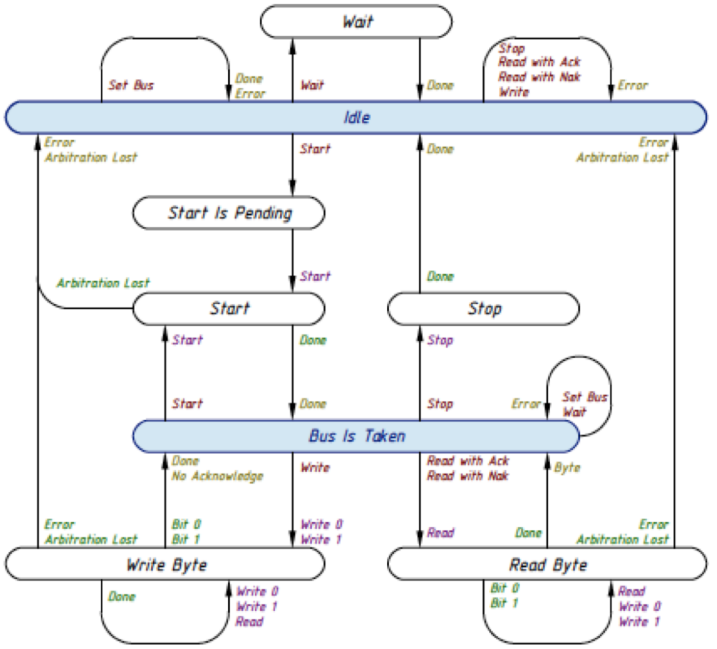
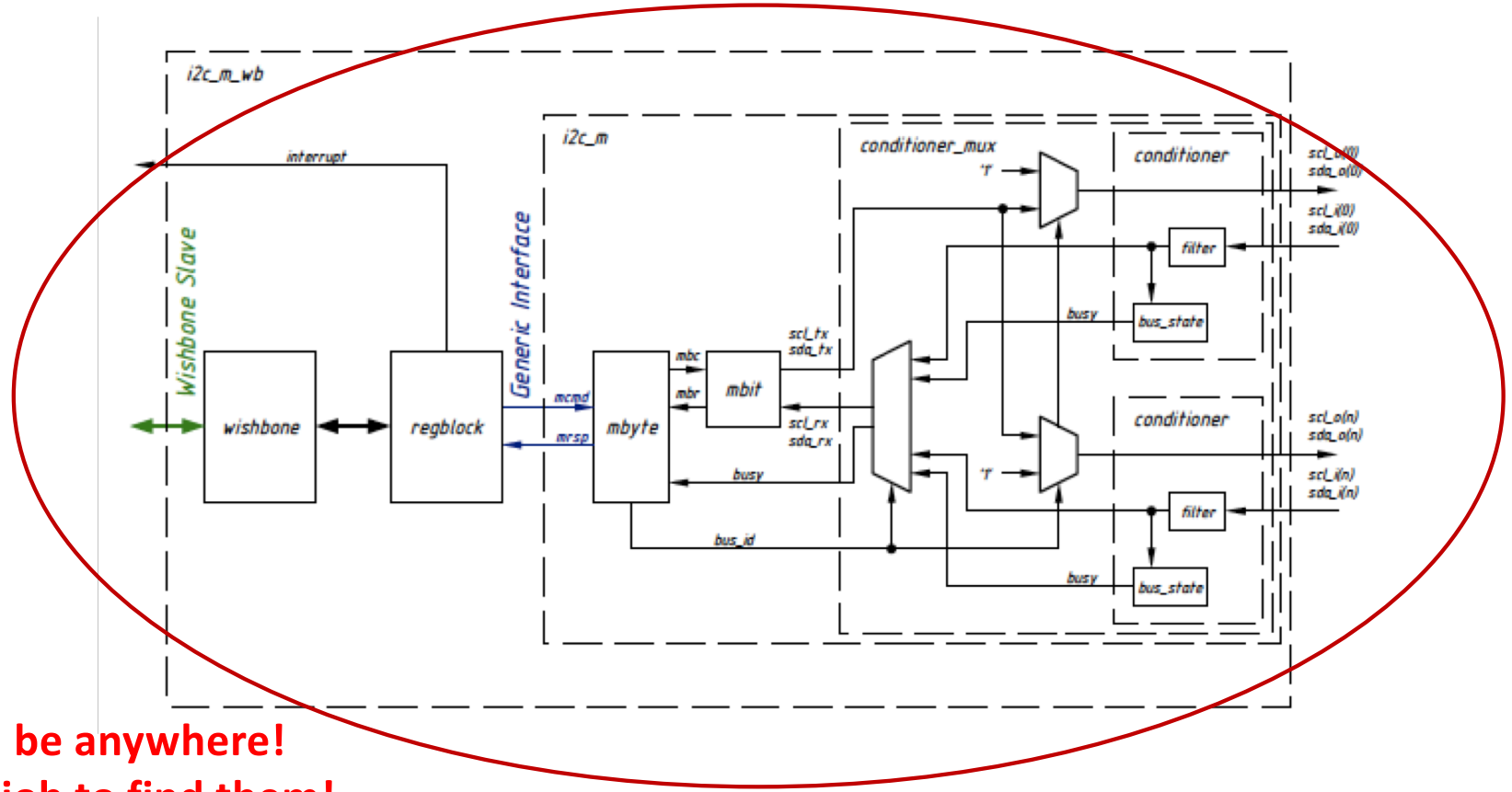


Figure 3: Byte-level FSM

Example of Where Bugs May Reside



Bugs can be anywhere!
It's your job to find them!

Provided in Assignment

- On Moodle – project_3_provided_files
  - Updated layered_testbench example with coverage and assertions
  - Example Test Plan: test_plan_layered_testbench.xml

Project Setup Instructions

1. In your project_benches directory:
   - Copy your proj_2 project directory to proj_3 directory
2. In the ece745_projects/proj_3/sim directory
   - Place a copy of the provided test plan example with the name i2cmb_test_plan.xls
3. Run ‘make debug’ to compile and run the proj_3 bench
   - Simulation should run as in proj_2

Project 3 Completion Instructions

1. Review the I2CMB Specification
2. Identify areas where potential bugs may reside in the design
3. Select a mechanism for ensuring feature has been tested
   - Functional coverage covergroup, coverpoint, cross, transition coverage, etc.
   - Directed tests
   - Code coverage
4. Implement the covergroups
   - Within predictor, coverage component, agent, etc.
5. Ensure coverage within test plan links to coverage in the simulation

Project 3 Requirements

- Completed i2cmb_test_plan.xls spreadsheet within ece745_projects/docs directory that includes
  - All features to be tested. Each feature in a separate row.
  - The following columns completed for each entry
    - Number, Section, Description, Link, Type, Weight, Goal
- Test plan must successfully
  - Import into Questa
  - Convert to UCDB
  - Merge with simulation coverage
  - Link all test plan links to simulation coverage structures

- Test plan to contain 20 items
  - Five related to register testing
  - Fifteen from other areas of design
- Mix of the following coverage types
  - Covergroups, coverpoints with bins, cross coverage, code coverage
- Covergroups, coverpoints, and crosses must be defined in test bench for linking with test plan

Project 3 Grading Criteria

- Test plan thoroughness
  - Identification of where bugs may reside within I2CMB
- Test plan structure
  - Well organized
  - Clear descriptions of each test plan item, row
  - Easy to understand
- Test plan links
  - All test plan items of covergroups/coverpoints/crosses type must successfully link to content in simulation

Project Submission

- Submit by 11:59pm on Sunday, March 30th
- Single tar file
  - Containing: ece745_projects directory and all sub-directories
    - Project_benches directory should include lab_1, proj_1, proj_2 and proj_3 sub-directories
  - Named: <unityId>_p3.tar
  - Execute ‘make clean’ in sim directory before creating tar file