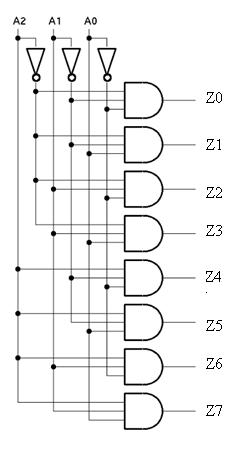
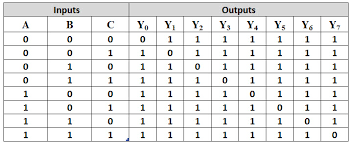
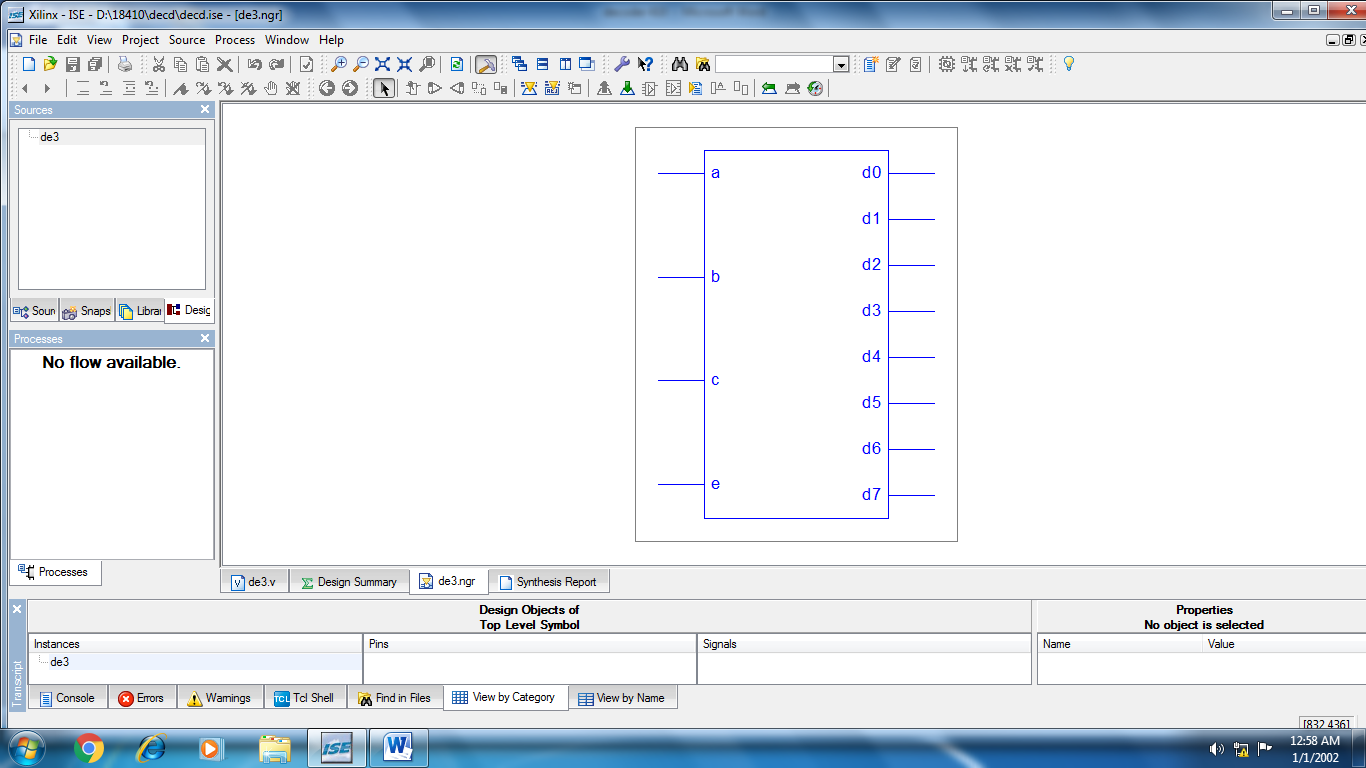
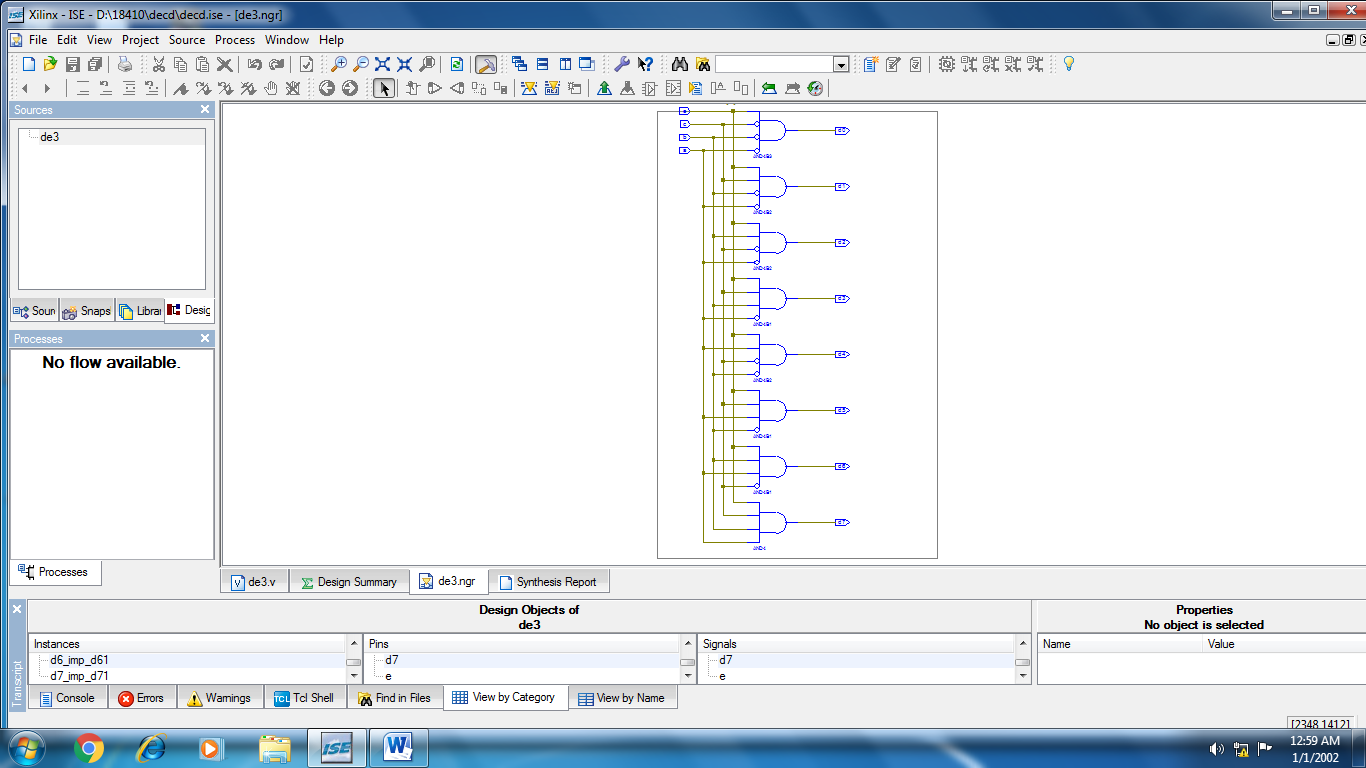
**CIRCUIT DIAGRAM AND TRUTH TABLE:**





**RTL SCHEMATIC:**

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**TEST BENCH PROGRAM:**

moduleder\_tb\_v;

// Inputs

reg a;

reg b;

reg c;

reg e;

// Outputs

wire d0;

wire d1;

wire d2;

wire d3;

wire d4;

wire d5;

wire d6;

wire d7;

// Instantiate the Unit Under Test (UUT)

de3uut (.a(a), .b(b), .c(c), .e(e), .d0(d0), .d1(d1), .d2(d2), .d3(d3), .d4(d4), .d5(d5), .d6(d6),.d7(d7));

// Initialize Inputs

a = 0;b = 0;c = 0;e = 1;#100;

a = 0;b = 0;c = 1;e = 1;#100;

a = 0;b = 1;c = 0;e = 1;#100;

a = 0;b = 1;c = 1;e = 1;#100;

a = 1;b = 0;c = 0;e = 1;#100;

a = 1;b = 0;c = 1;e = 1;#100;

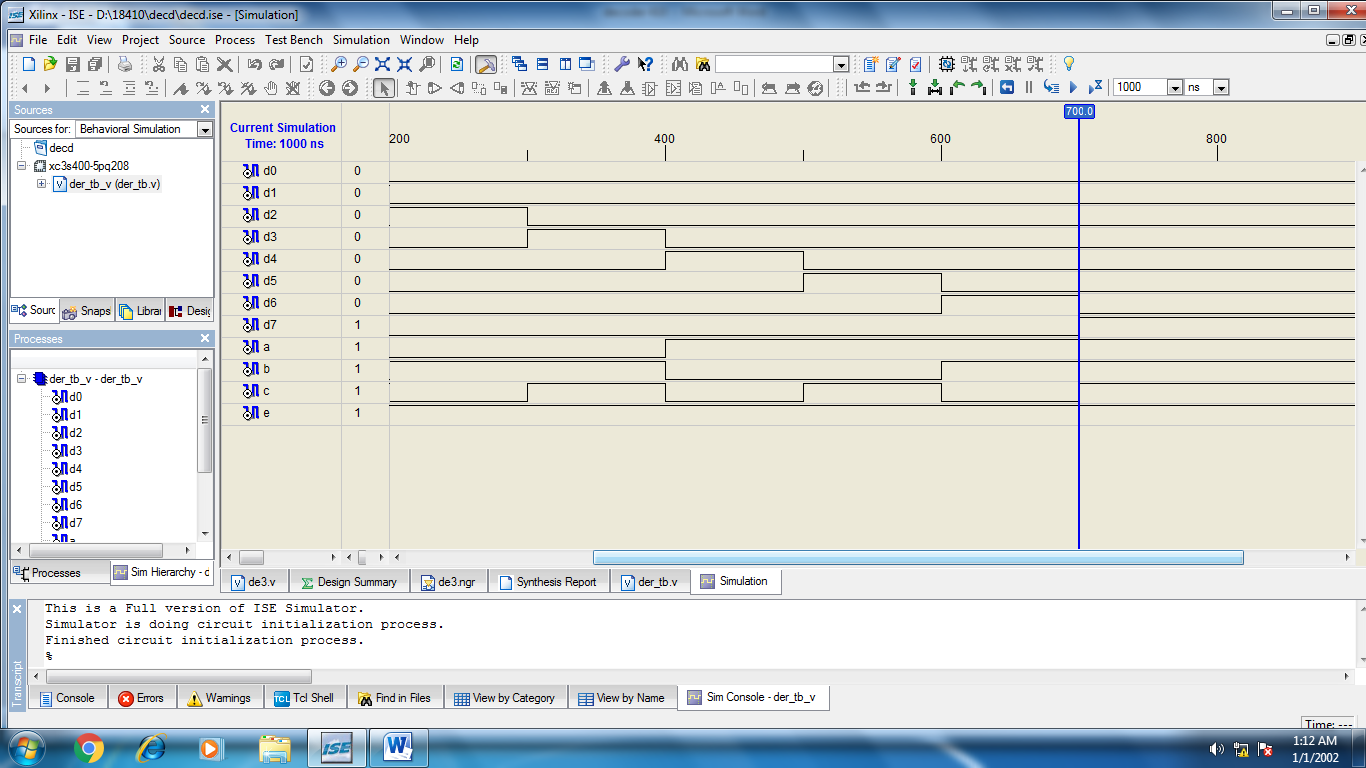
a = 1;b = 1;c = 0;e = 1;#100;

a = 1;b = 1;c = 1;e = 1;

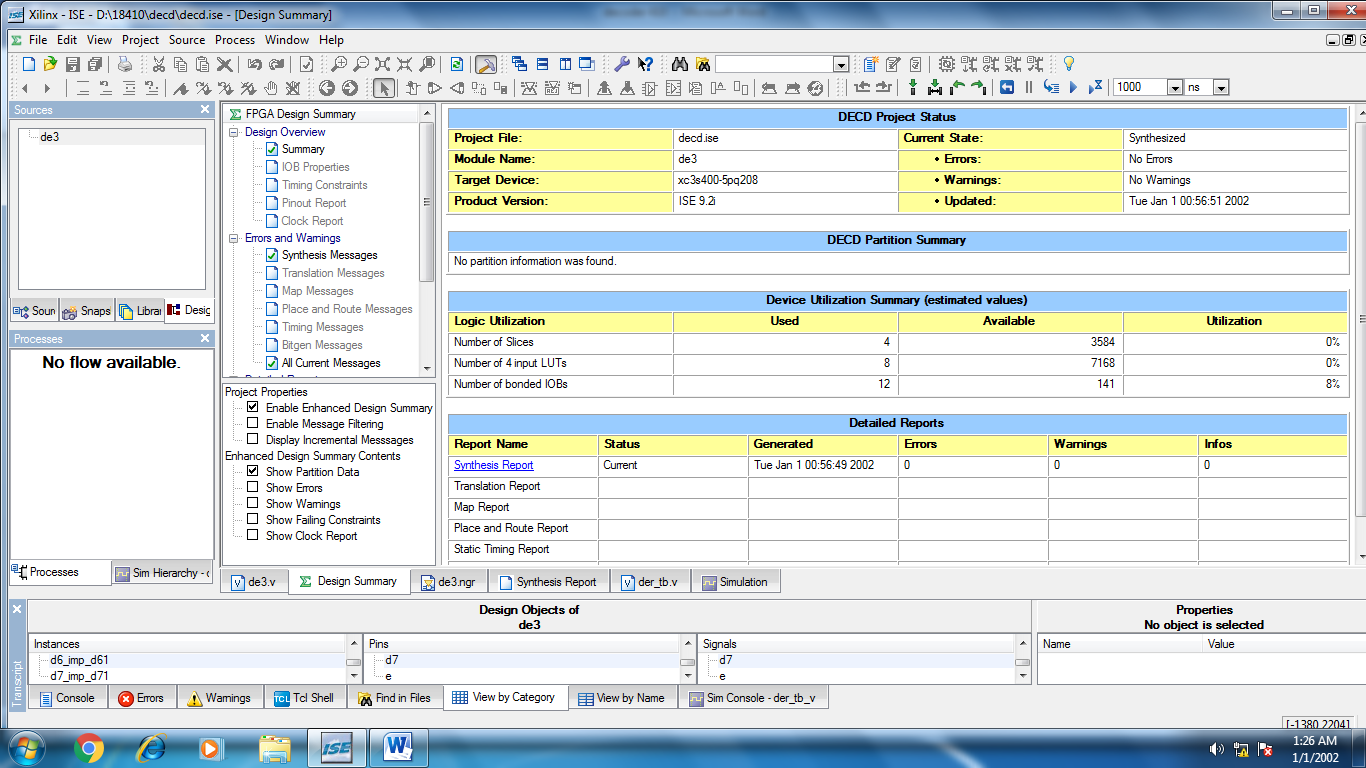
end

endmodule

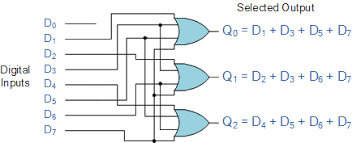
**SIMULATION WAVEFORM:**

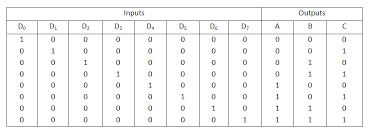


**DESIGN SUMMARY:**

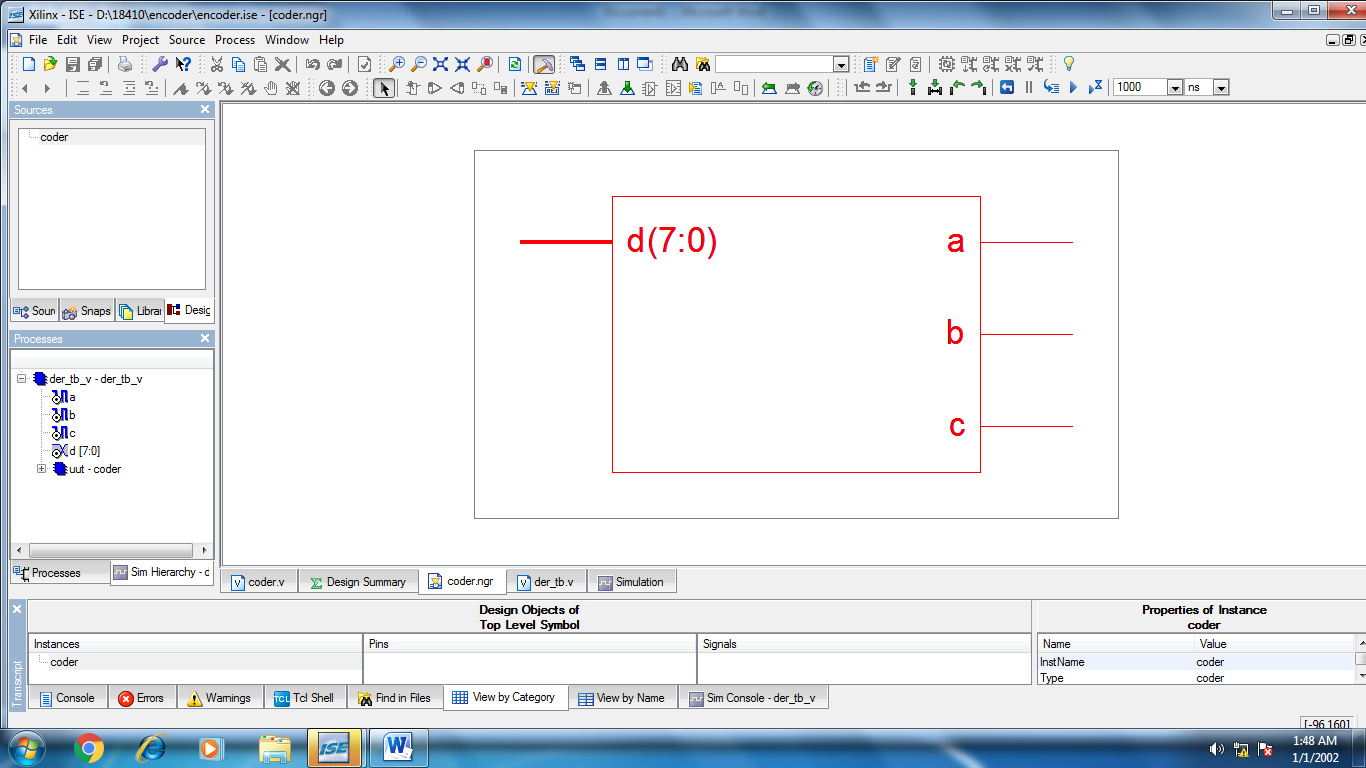


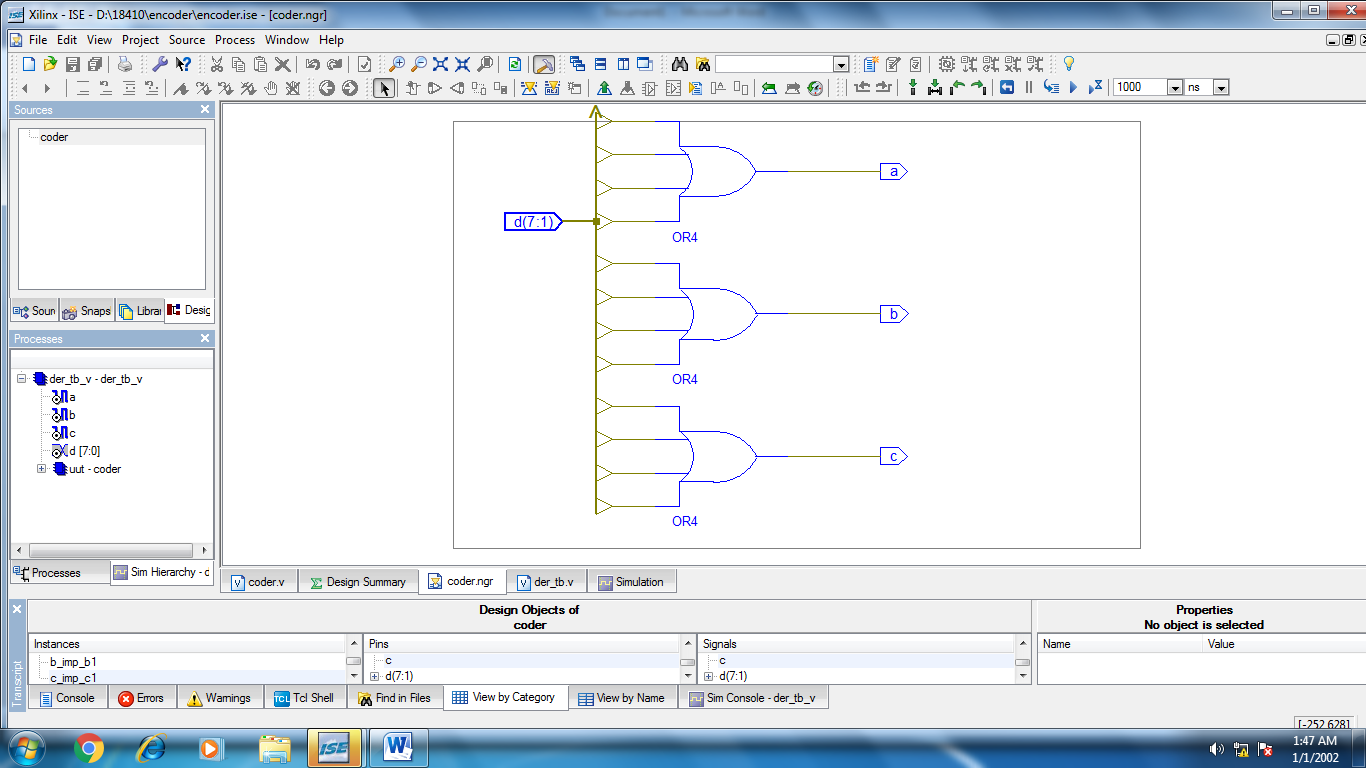
**CIRCUIT DIAGRAM AND TRUTH TABLE:**

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**RTL SCHEMATIC:**

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**TEST BENCH WAVE FORM:**

moduleder\_tb\_v;

// Inputs

reg [7:0] d;

// Outputs

wire a;

wire b;

wire c;

// Instantiate the Unit Under Test (UUT)

Coderuut(.d(d), .a(a), .b(b), .c(c));

initial begin

// Initialize Inputs

d[0]=1;d[1]=0;d[2]=0;d[3]=0;d[4]=0;d[5]=0;d[6]=0;d[7]=0;#100;

d[0]=0;d[1]=1;d[2]=0;d[3]=0;d[4]=0;d[5]=0;d[6]=0;d[7]=0;#100;

d[0]=0;d[1]=0;d[2]=1;d[3]=0;d[4]=0;d[5]=0;d[6]=0;d[7]=0;#100;

d[0]=0;d[1]=0;d[2]=0;d[3]=1;d[4]=0;d[5]=0;d[6]=0;d[7]=0;#100;

d[0]=0;d[1]=0;d[2]=0;d[3]=0;d[4]=1;d[5]=0;d[6]=0;d[7]=0;#100;

d[0]=0;d[1]=0;d[2]=0;d[3]=0;d[4]=0;d[5]=1;d[6]=0;d[7]=0;#100;

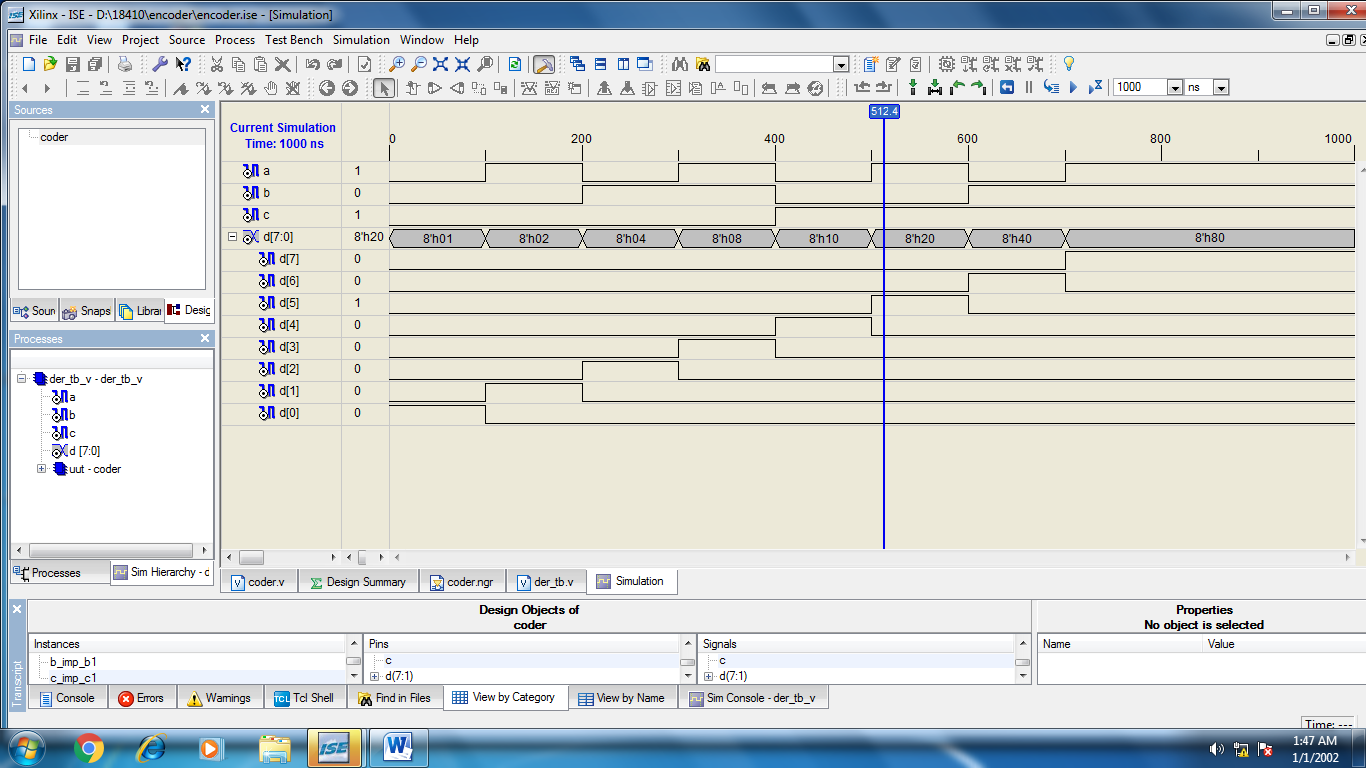
d[0]=0;d[1]=0;d[2]=0;d[3]=0;d[4]=0;d[5]=0;d[6]=1;d[7]=0;#100;

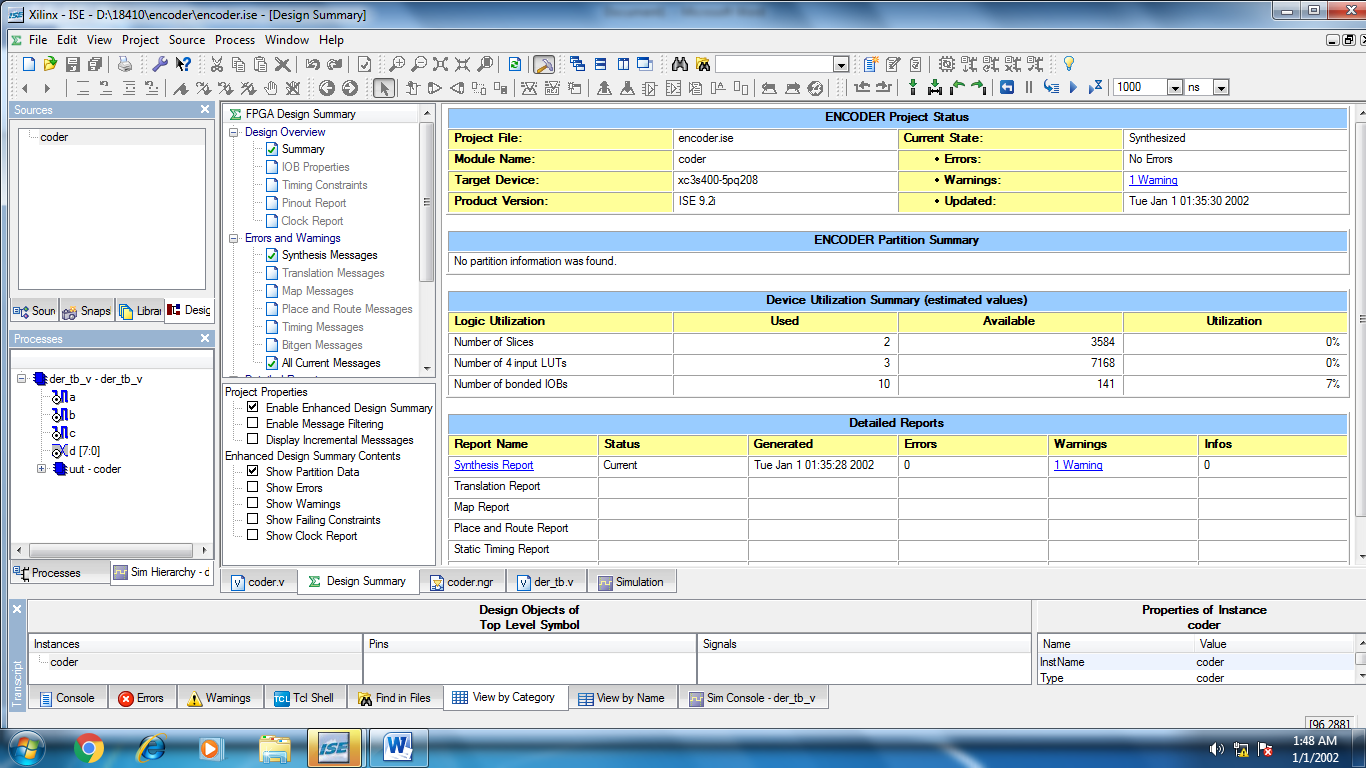
d[0]=0;d[1]=0;d[2]=0;d[3]=0;d[4]=0;d[5]=0;d[6]=0;d[7]=1;

end

endmodule

**SIMULATION WAVEFORM:**

****

**DESIGN SUMMARY:**