



MICROCHIP

PIC18F2455/2550/4455/4550

PIC18F2455/2550/4455/4550 Rev. A3 Silicon Errata

The PIC18F2455/2550/4455/4550 parts you have received conform functionally to the Device Data Sheet (DS39632B), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18F2455/2550/4455/4550 silicon.

The following silicon errata apply only to PIC18F2455/2550/4455/4550 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2455	01 0010 011	00010
PIC18F2550	01 0010 010	00010
PIC18F4455	01 0010 001	00010
PIC18F4550	01 0010 000	00010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

2. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written.

Work around

Do not write to TMR1H/TMR3H while Timer1/Timer3 is running, or else write to TMR1L/TMR3L immediately following a write to TMR1H/TMR3H.

Do not write to TMR1H/TMR3H and then wait for another event before also updating TMR1L/TMR3L.

3. Module: MSSP

In Slave Transmit mode, when a transmission is initiated, the SSPBUF register may be written for up to 10 T_{CY} before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

PIC18F2455/2550/4455/4550

4. Module: Interrupts

If a high priority interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of TEMP before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where Fd is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where Fd is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming: If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software in the same manner as is done with low priority interrupts. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead.
2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C Compiler documentation for details.

If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as "low priority" by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

The following code snippet demonstrates the work around using the C18 compiler:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

5. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>), or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 1, ECCPASE bit operations are performed on the W register.

EXAMPLE 1:

MOVF	ECCP1AS, W
BTFSC	WREG, ECCPASE
BRA	SHUTDOWN_ROUTINE

6. Module: ECCP

ECCP1 configured for auto-shutdown with Comparator 1 corrupts the PWM duty cycle pulse. In addition, it does not always synchronize the pulse to the beginning of the period and the end of the pulse can occur at any time within the period.

Work around

None.

7. Module: ECCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4550 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F4550 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

PIC18F2455/2550/4455/4550

8. Module: A/D

The A/D offset is greater than the specified limit in Table 28-28 of the Device Data Sheet. The updated conditions and limits are shown in **bold** text in Table 1.

Work around

Three workarounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

**TABLE 1: A/D CONVERTER CHARACTERISTICS: PIC18F2455/2550/4455/4550 (INDUSTRIAL)
PIC18LF2455/2550/4455/4550 (INDUSTRIAL)**

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	E _{OFF}	Offset Error	—	—	<±1.5	LSb	VREF = VREF+ and VREF-
A06	E _{OFF}	Offset Error	—	—	<±3.5	LSb	VREF = Vss and VDD

9. Module: DC Characteristics (BOR)

The values for parameter D005 (VBOR) in **Section 28.1 “DC Characteristics”** of the Device Data Sheet, when the trip point for BORV1:BORV0 = 11, are not applicable as the device may reset below the minimum operating voltage for the device.

Work around

None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39632B), the following clarifications and corrections should be noted.

None.

PIC18F2455/2550/4455/4550

REVISION HISTORY

Rev A Document (11/2004)

Original version of this document. Includes silicon issues 1 (EUSART), 2 (Timer1/Timer3), 3 (MSSP), 4 (Interrupts), 5-7 (ECCP), 8 (A/D) and 9 (DC Characteristics (BOR)).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELoQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, Migratable Memory, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rfLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta

Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston

Westford, MA
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose

Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Qingdao
Tel: 86-532-502-7355
Fax: 86-532-502-7205

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-2229-0061
Fax: 91-80-2229-0062

India - New Delhi
Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

Japan - Kanagawa
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Taiwan - Hsinchu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

EUROPE

Austria - Weis
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Ballerup
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Massy
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Ismaning
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

England - Berkshire
Tel: 44-118-921-5869
Fax: 44-118-921-5820