Reaction Time Game

Introduction

The Reaction Timer Single-Player game is a digital design project implemented on the Nexys DDR4 FPGA development board using Verilog HDL. It demonstrates how digital logic, finite state machines (FSMs), and timing control can be combined to create an interactive system. The project aims to measure and display a player's reaction time with high accuracy while showcasing the real-time processing capability of FPGA-based systems.

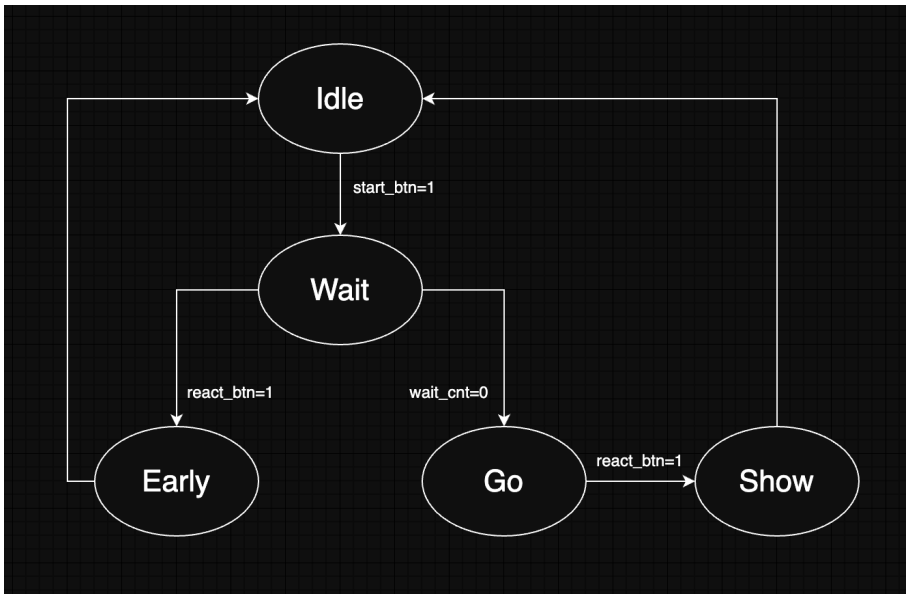
Objective

The objective of this project is to design and implement a reaction timer system that measures a player's response time in milliseconds. The system provides an engaging and practical way to apply digital design principles, state machines, and timing logic in a real-time FPGA environment.

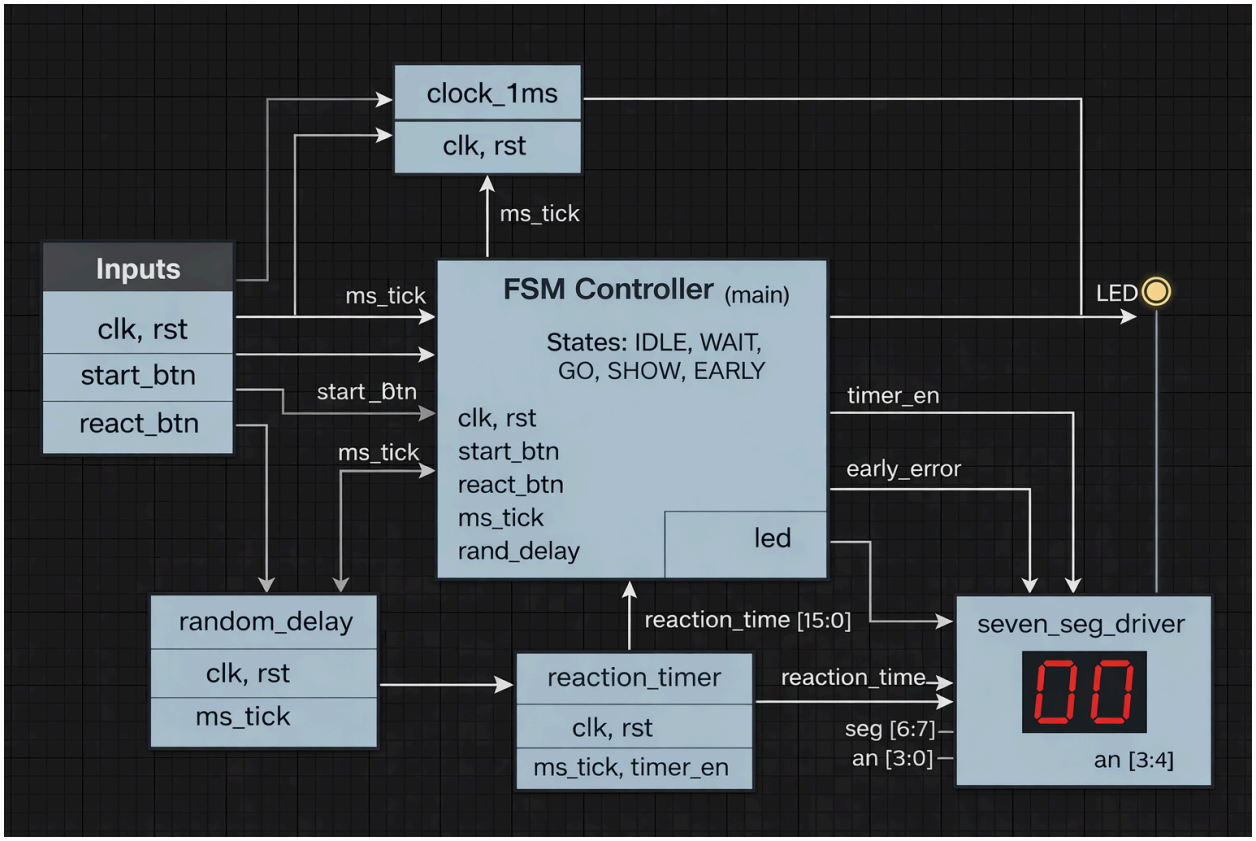
Basic Description/Workflow of the Game

1. The player clicks a button to start the game,
2. The LED turns ON after a random delay.
3. The player must press the reaction button as quickly as possible once the LED lights up.
4. If the player reacts before the LED turns on, the display shows "FAIL".
5. If the reaction is valid, the reaction time will be displayed on the 7-segment display.
6. To play again, the player flips a switch to restart the game.

State Diagram



Block Diagram



Features

- Implemented on the Nexys DDR4 FPGA using Verilog HDL.
- Utilizes Finite State Machine (FSM) for state control and game flow.
- Includes a clock divider, debouncing circuit, and pseudo-random delay generator.
- Operates using a 100 MHz FPGA system clock.
- Displays reaction time with millisecond accuracy on a 4-digit, 7-segment display.
- Incorporates an early start detection feature to prevent false triggers.

Compact and modular Verilog design, easily extendable for multiplayer versions.

Brief Overview of the model :

- Clock divider: Divides the 100 MHz system clock to generate a 1 ms tick signal for timing operations.
- Button Synchronizer & Edge Detector: Debounces and detects rising edges of `start_btn` and `react_btn` to trigger FSM transitions.
- Pseudo-Random Generator: Produces a varying delay value used to randomize the LED ON timing.
- Main FSM & Timers: Controls the sequence of game states, measures reaction time, and detects early responses.
- 7-Segment Display Driver: Converts numeric outputs (reaction time or error code) into corresponding 7-segment signals.
- LED Indicator: Signals the “GO” state when the player should react.