ECEN 714: Submission for LAB 3

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Contents (Rising and falling Delay, Delay Table, Input Capacitance and Cell18 files)

Inverter Delays:

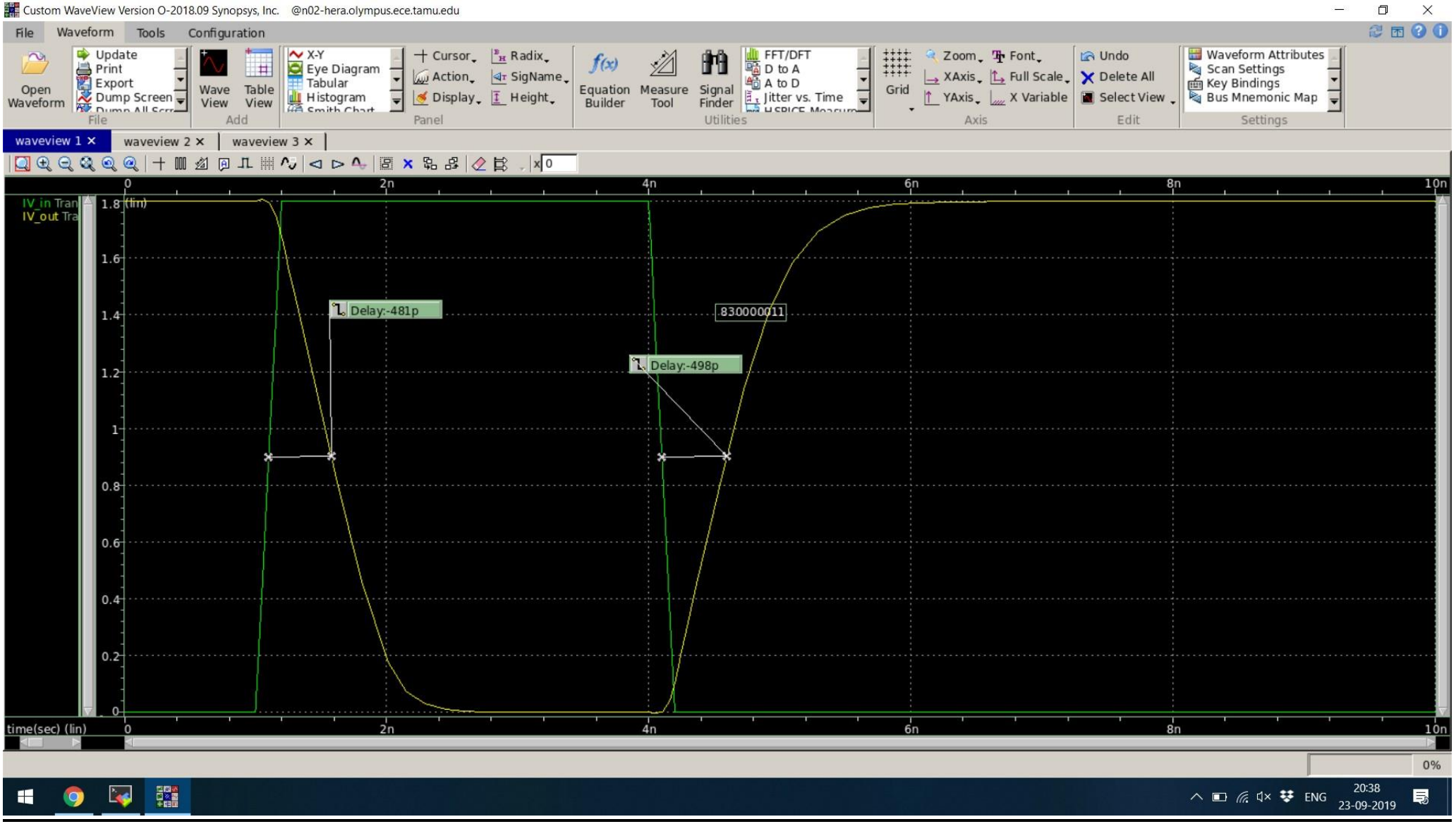


Figure 1 Rising and Falling delay for inverter with output capacitance at 100fF. The percentage difference between rising and falling delay is 3%.

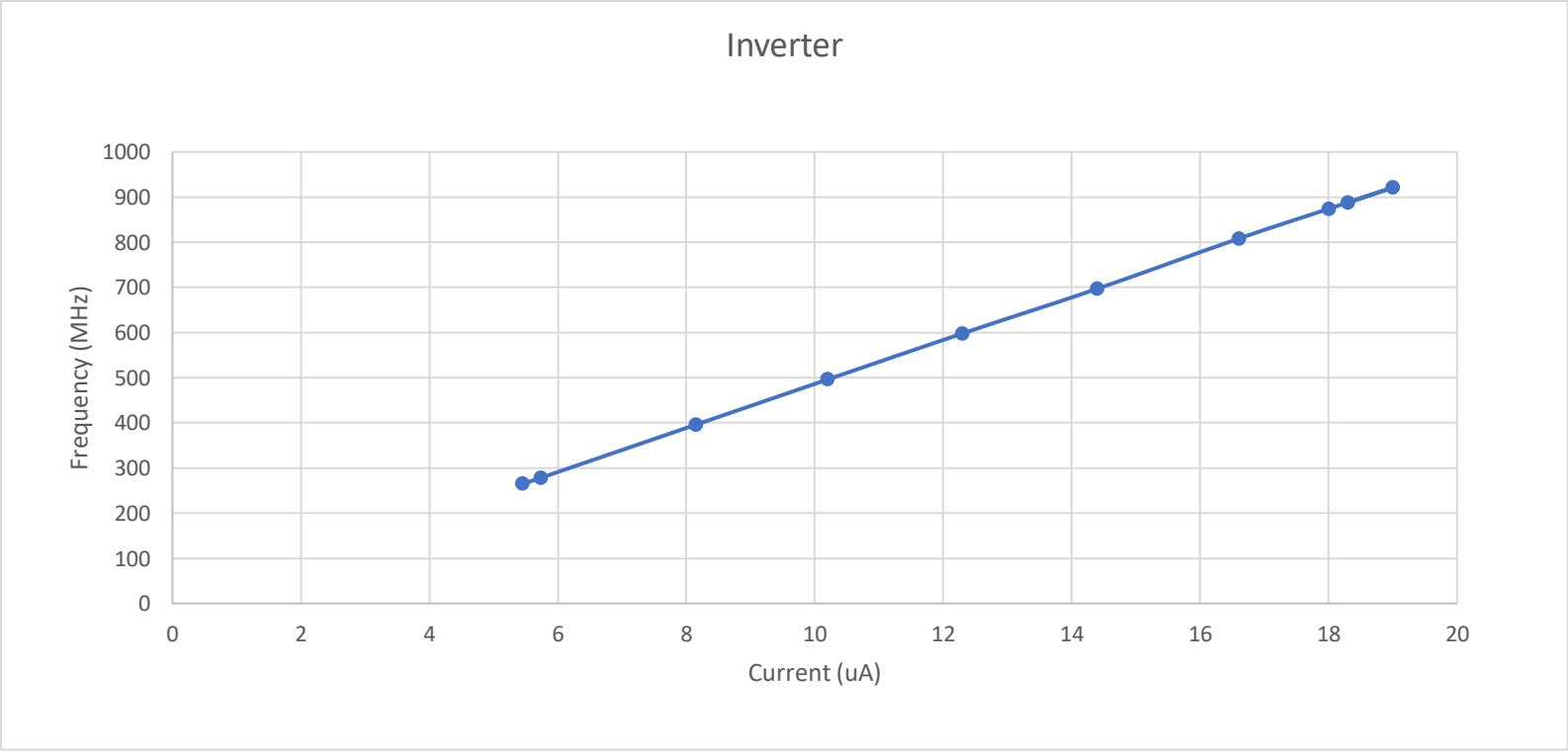
Delay Table for the Inverter:

Inverter:				
Capacitance (fF)	Rising Delay (ps)	Falling Delay(p)	Difference in Delay	Error %
1	-27.1	-45.2	-18.1	40.04424779
4.7	-53.3	-72.7	-19.4	26.68500688
8.8	-79.6	-95.1	-15.5	16.29863302
15	-109	-122	-13	10.6557377
30	-175	-188	-13	6.914893617
47	-249	-265	-16	6.037735849
65	-329	-345	-16	4.637681159
88	-430	-445	-15	3.370786517
90	-439	-451	-12	2.66075388

Input Capacitance for Inverter:

Current	Frequency	2*pi*F	Capacitance
5.45	265	1664.2	0.003274847
5.73	278	1745.84	0.003282088
8.15	396	2486.88	0.003277199
10.2	496	3114.88	0.003274604
12.3	598	3755.44	0.003275249

14.4	697	4377.16	0.003289804
16.6	808	5074.24	0.003271426
18	874	5488.72	0.003279453
19	921	5783.88	0.003284992
18.3	888	5576.64	0.003281546
		Avg Cap:	0.003279121



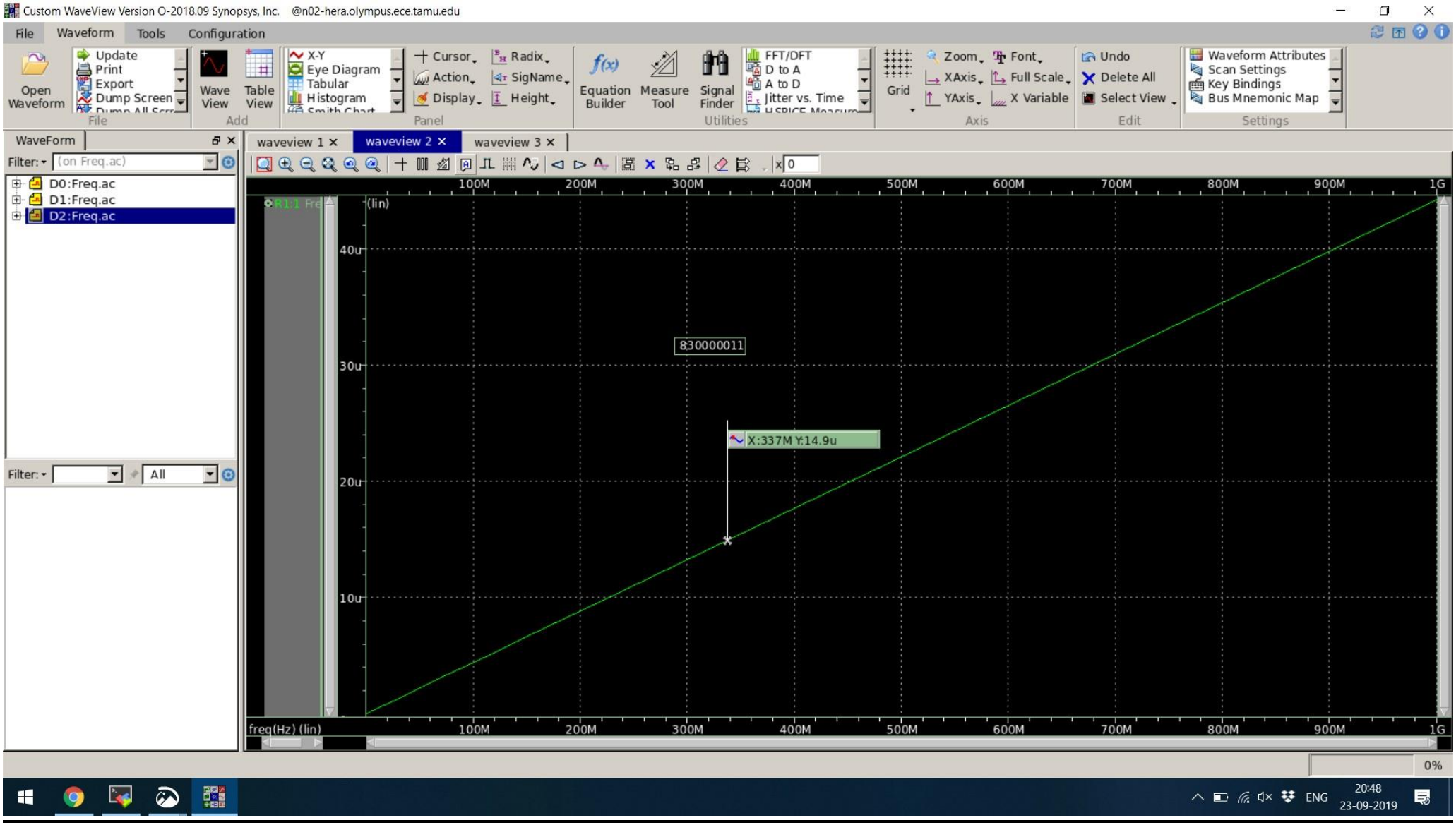


Figure 2 Plot of Frequency vs Current. Slope is proportional to the Input capacitance.

Cell18.spi file for Inverter:

```
//Spice netlist for an inverter
simulator lang=spectre
subckt ND (input1 input2 output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
            M2 output input VDD VDD tsmc18P w=wp l=lp
        M3 output input VSS VSS tsmc18N w=wn l=ln
            M4 output input VSS VSS tsmc18N w=wn l=ln
ends ND
```

Simulation file for Inverter:

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "/home/grads/m/mana/ecen454/Lab1/model18.spi"
include "/home/grads/m/mana/ecen454/Lab1/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

AC Simulation for Inverter:

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "/home/grads/m/mana/ecen454/Lab1/model18.spi"
include "/home/grads/m/mana/ecen454/Lab1/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (IV_in 0) vsource dc=0 mag=1

R1 (IV_in IV_in1) resistor r=0

X1 (IV_in1 IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

NAND Delays:

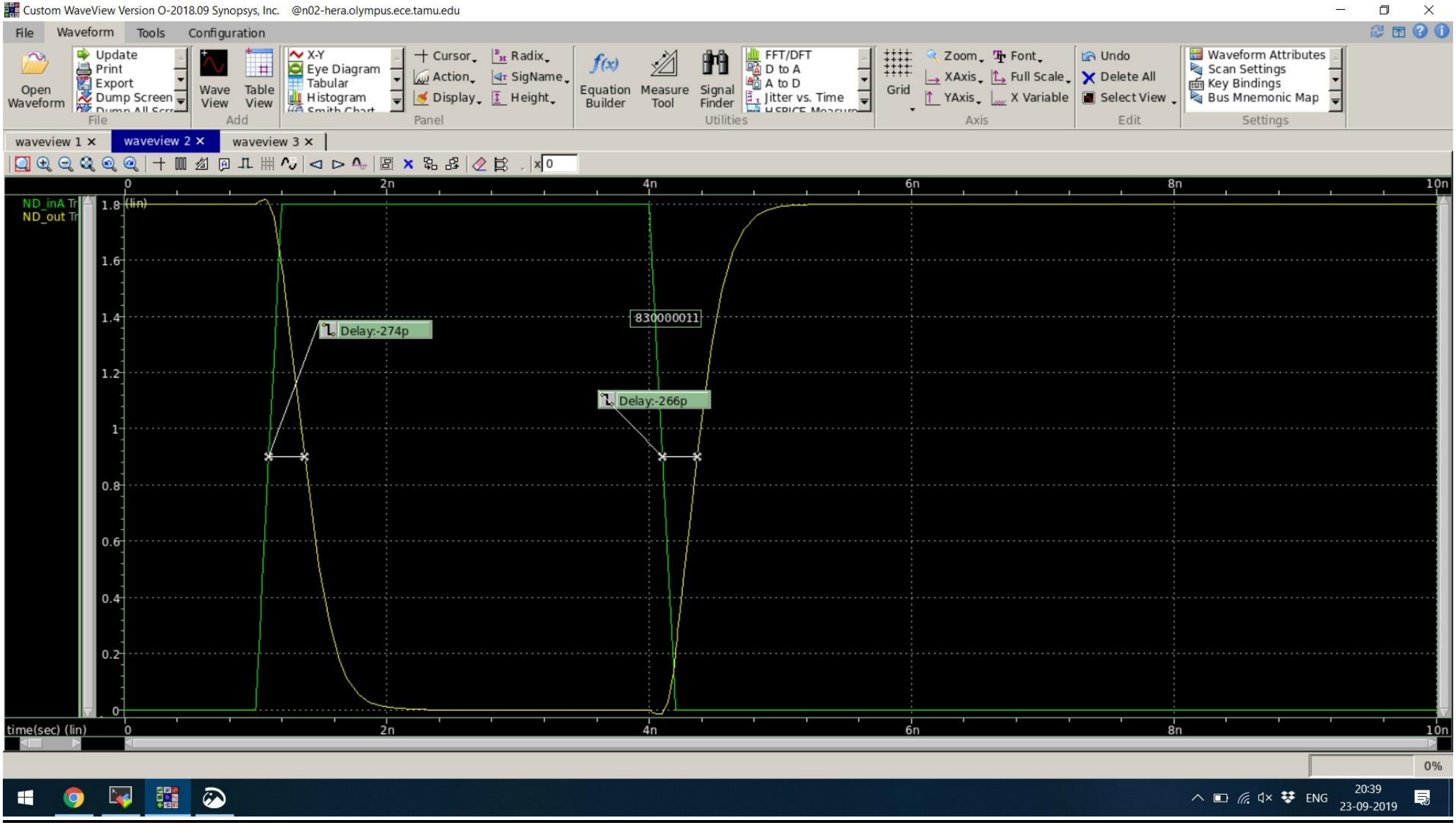


Figure 3 Rising and Falling delay for inverter with output capacitance at 100fF. The percentage difference between rising and falling delay is 3%.

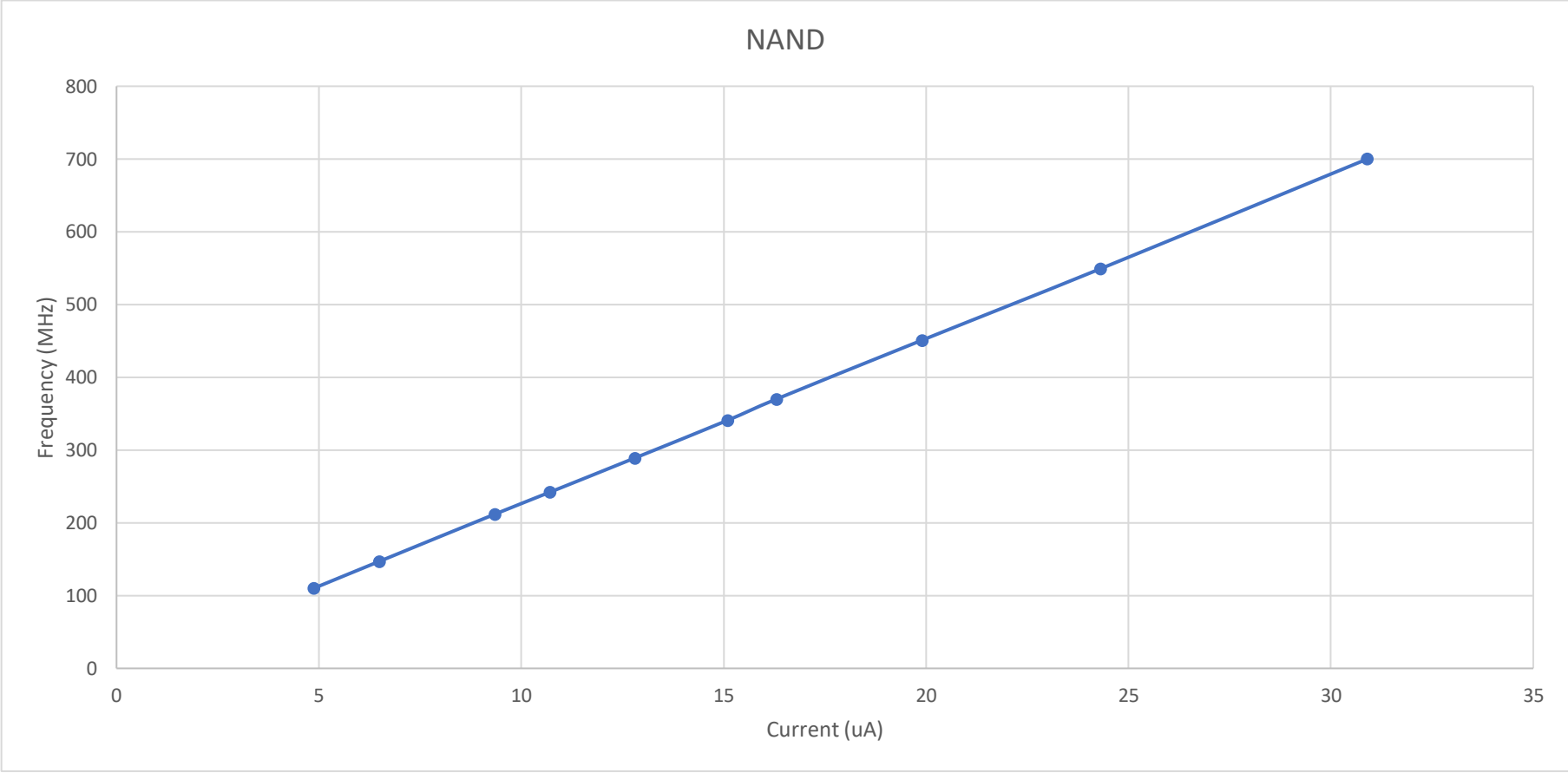
Delay Table for NAND:

Nand:				
Capacitance (fF)	Rising Delay (ps)	Falling Delay(p)	Difference in Delay	Error %
1	-36.9	-49.4	-12.5	25.30364372
4.7	-52.8	-64.5	-11.7	18.13953488
8.8	-67.7	-78.2	-10.5	13.42710997
15	-87	-95.6	-8.6	8.9958159
30	-126	-130	-4	3.076923077
47	-168	-169	-1	0.591715976
65	-212	-209	3	-1.435406699
88	-269	-262	7	-2.671755725
90	-274	-269	5	-1.858736059

Input Capacitance for NAND:

Current	Frequency	2*pi*F	Capacitance
4.87	110	690.8	0.007049797
6.49	147	923.16	0.007030201
9.35	212	1331.36	0.007022894
10.7	242	1519.76	0.007040585
12.8	289	1814.92	0.007052652
15.1	341	2141.48	0.007051198
16.3	370	2323.6	0.007014977
19.9	451	2832.28	0.007026141

24.3	549	3447.72	0.007048136
30.9	700	4396	0.007029117
		Avg Cap:	0.00703657



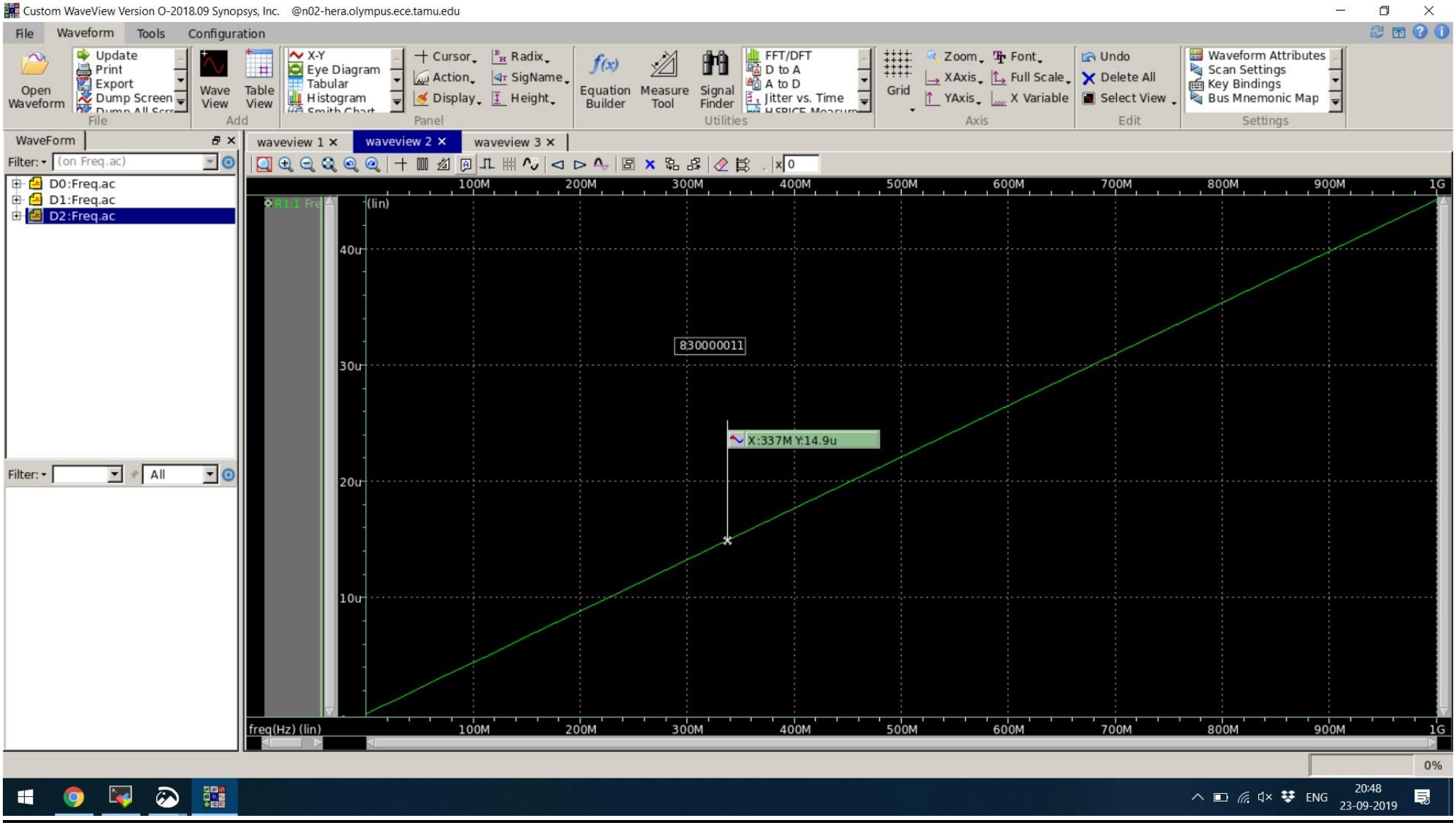


Figure 4 Plot of Frequency vs Current. Slope is proportional to the Input capacitance.

Cell18.spi for NAND:

```
//Spice netlist for an inverter
simulator lang=spectre
subckt ND (input1 input2 output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input1 VDD VDD tsmc18P w=wp l=lp
            M2 output input2 VDD VDD tsmc18P w=wp l=lp
        M3 output input1 A VSS tsmc18N w=wn l=ln
            M4 A input2 VSS VSS tsmc18N w=wn l=ln
ends ND
```

Simulation file for NAND:

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "/home/grads/m/mana/ecen454/Lab1/model18.spi"
include "/home/grads/m/mana/ecen454/Lab1/nand18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (ND_inA 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]
V2     (ND_inB 0) vsource dc = 1.8

X1 (ND_inA ND_inB ND_out vdd gnd) ND wp=1.8u lp=0.2u wn=1.0u ln=0.2u

R1 (ND_out 1) resistor r=1
C1 (1 0) capacitor c=90f

TransientAnalysis tran start=0 stop=10ns step=1ps
save ND_inA ND_out
```

AC Simulation for NAND:

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "/home/grads/m/mana/ecen454/Lab1/model18.spi"
```

```
include "/home/grads/m/mana/ecen454/Lab1/nand18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (ND_in 0) vsource dc=0 mag=1
V2     (ND_inB 0) vsource dc = 1.8

R1 (ND_in ND_inA) resistor r=0

X1 (ND_inA ND_inB ND_out vdd gnd) ND wp=1.8u lp=0.2u wn=1.0u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

Delays for XOR:

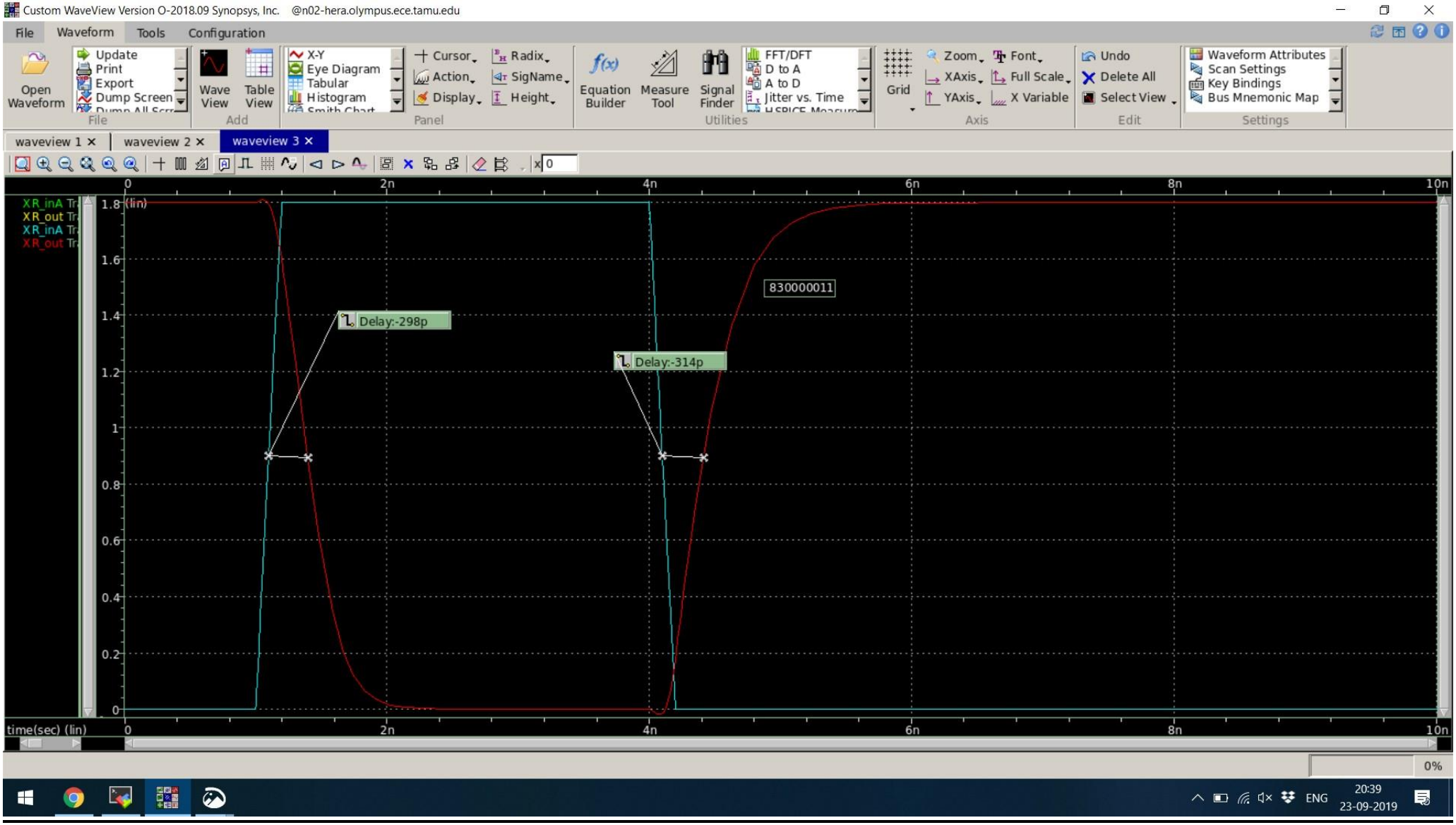


Figure 5 Rising and Falling delay for inverter with output capacitance at 100fF. The percentage difference between rising and falling delay is 5%.

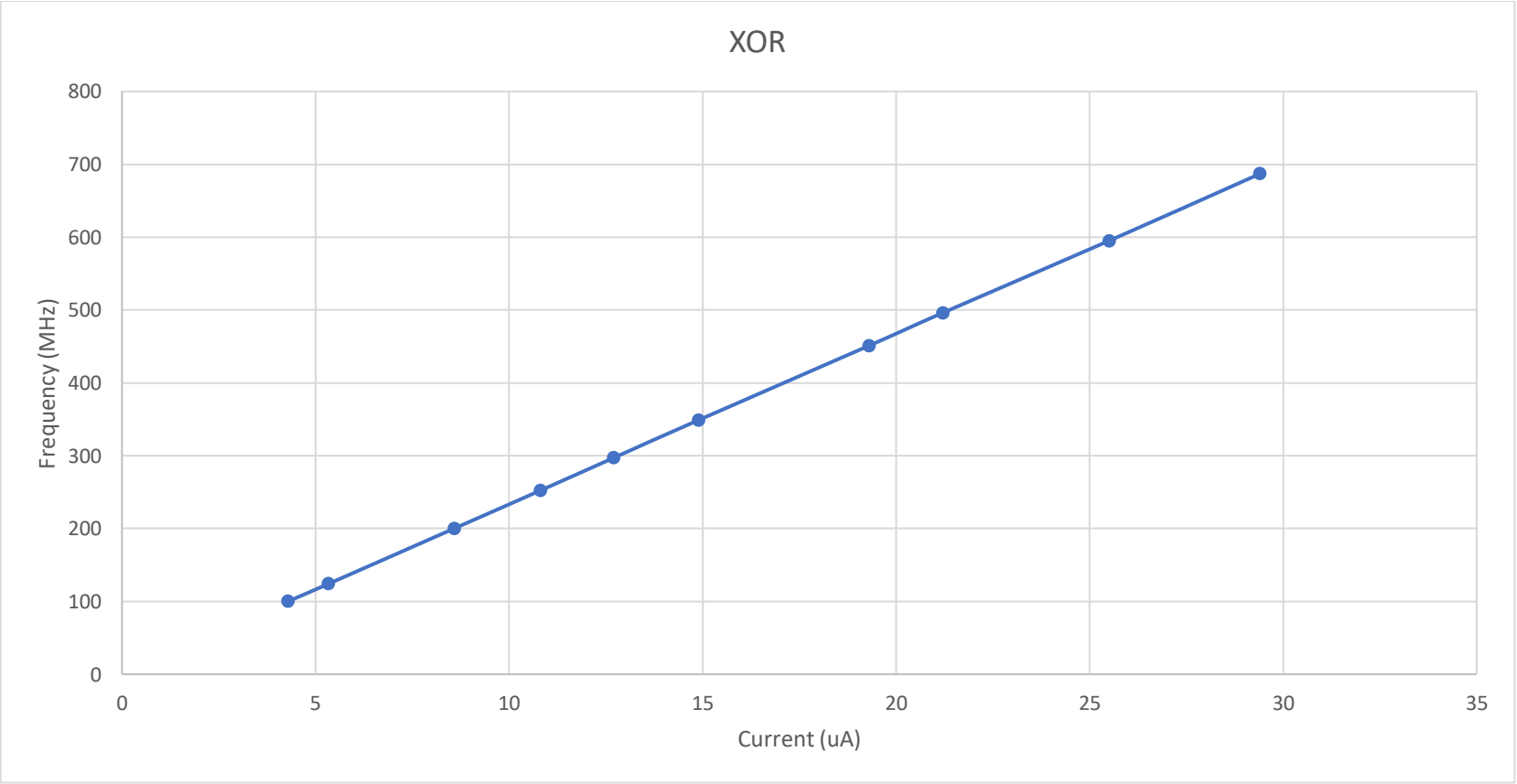
Delay Table for XOR:

XOR:				
Capacitance (fF)	Rising Delay (ps)	Falling Delay(p)	Difference in Delay	Error %
1	-43.6	-54.7	-11.1	20.29250457
4.7	-52.8	-64.5	-11.7	18.13953488
8.8	-59.7	-70.1	-10.4	14.83594864
15	-95.1	-104	-8.9	8.557692308
30	-136	-146	-10	6.849315068
47	-183	-194	-11	5.670103093
65	-232	-245	-13	5.306122449
88	-293	-309	-16	5.177993528
90	-298	-314	-16	5.095541401

Input Capacitance for XOR:

Current	Frequency	2*pi*F	Capacitance
4.29	100	628	0.00683121
5.33	124	778.72	0.006844565
8.58	200	1256	0.00683121
10.8	252	1582.56	0.006824386
12.7	297	1865.16	0.006809067
14.9	349	2191.72	0.006798314
19.3	451	2832.28	0.006814298

21.2	496	3114.88	0.006806041
25.5	595	3736.6	0.006824386
29.4	687	4314.36	0.006814452
		Avg Cap :	0.006819793



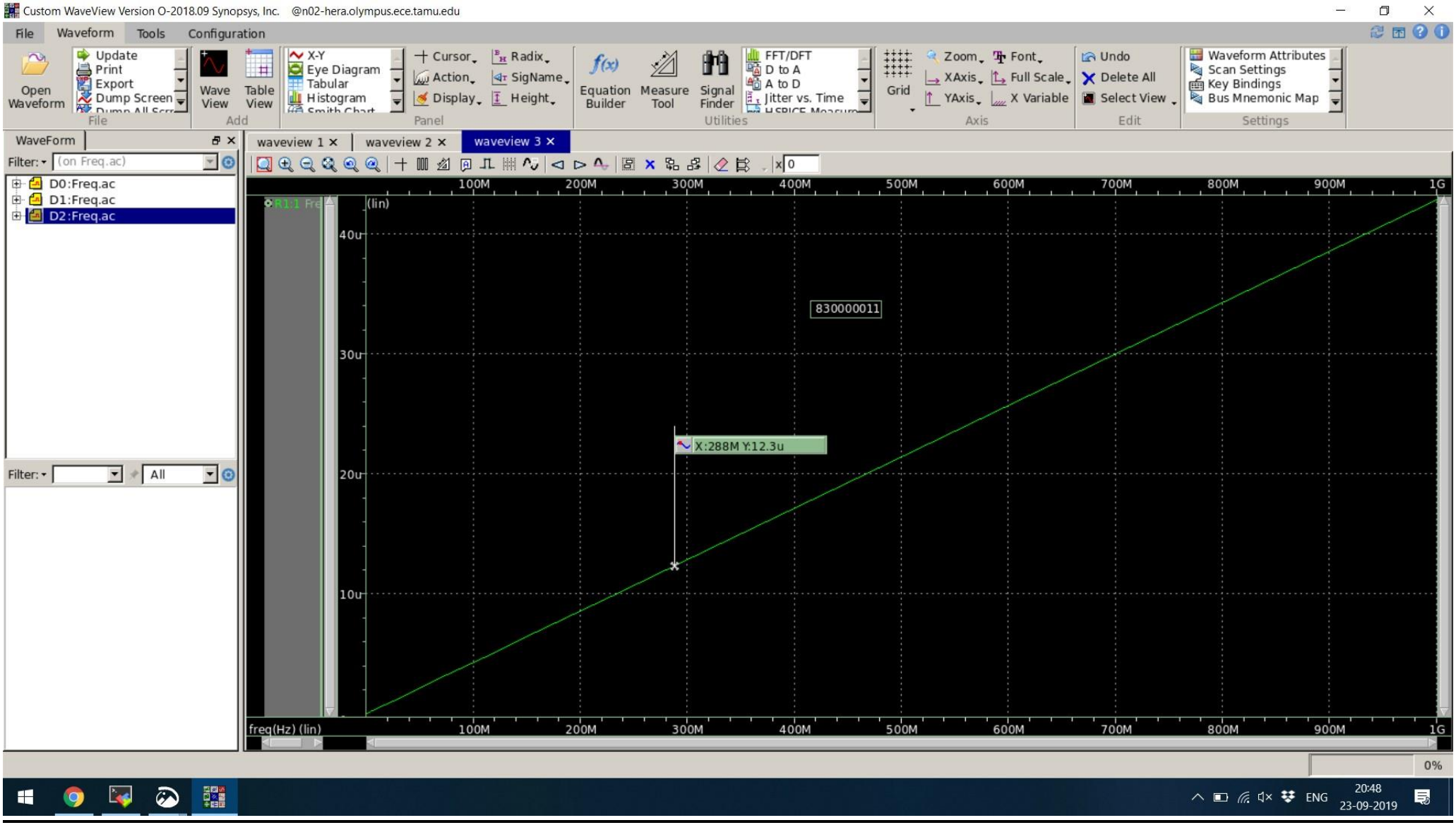


Figure 6 Plot of Frequency vs Current. Slope is proportional to the Input capacitance.

Cell18.spi for XOR:

```
//Spice netlist for an inverter
simulator lang=spectre

subckt IV1 (input1 notinA VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 notA input1 VDD VDD tsmc18P w=wp l=lp
           M7 notA input1 VSS VSS tsmc18N w=wn l=ln
ends IV1

subckt IV2 (input2 notinB VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
           M2 notB input2 VDD VDD tsmc18P w=wp l=lp
           M8 notB input2 VSS VSS tsmc18N w=wn l=ln
ends IV2

subckt XR (input1 input2 output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M3 x notinA VDD VDD tsmc18P w=wp l=lp
           M4 y input1 VDD VDD tsmc18P w=wp l=lp
           M5 output input2 x VDD tsmc18P w=wp l=lp
           M6 output notinB y VDD tsmc18P w=wp l=lp
        M9 output input1 u VSS tsmc18N w=wn l=ln
           M10 output notinA v VSS tsmc18N w=wn l=ln
           M11 u input2 VSS VSS tsmc18N w=wn l=ln
           M12 v notB VSS VSS tsmc18N w=wn l=ln
ends XR
```

Simulation file for XOR:

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "/home/grads/m/mana/ecen454/Lab1/model18.spi"
include "/home/grads/m/mana/ecen454/Lab1/xor18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XR_inA 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]
```

```
V2     (XR_inB 0) vsource dc = 1.8

X1 (IV_in IV_out vdd gnd) IV1 wp=0.9u lp=0.2u wn=0.3u ln=0.2u
X2 (IV_in IV_out vdd gnd) IV2 wp=0.9u lp=0.2u wn=0.3u ln=0.2u

X3 (XR_inA XR_inB XR_out vdd gnd) XR wp=1.8u lp=0.2u wn=0.9u ln=0.2u

R1 (XR_out 1) resistor r=1
C1 (1 0) capacitor c=90f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XR_inA XR_out
```

AC Simulation for XOR:

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "/home/grads/m/mana/ecen454/Lab1/model18.spi"
include "/home/grads/m/mana/ecen454/Lab1/xor18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8


acinput (XR_in 0) vsource dc=0 mag=1

V2     (XR_inB 0) vsource dc = 1.8


R1 (XR_in XR_inA) resistor r=0

X1 (IV1_in IV1_out vdd gnd) IV1 wp=0.9u lp=0.2u wn=0.3u ln=0.2u
X2 (IV2_in IV2_out vdd gnd) IV2 wp=0.9u lp=0.2u wn=0.3u ln=0.2u

X3 (XR_inA XR_inB XR_out vdd gnd) XR wp=1.8u lp=0.2u wn=0.9u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```