ECEN 714: Submission for LAB 1

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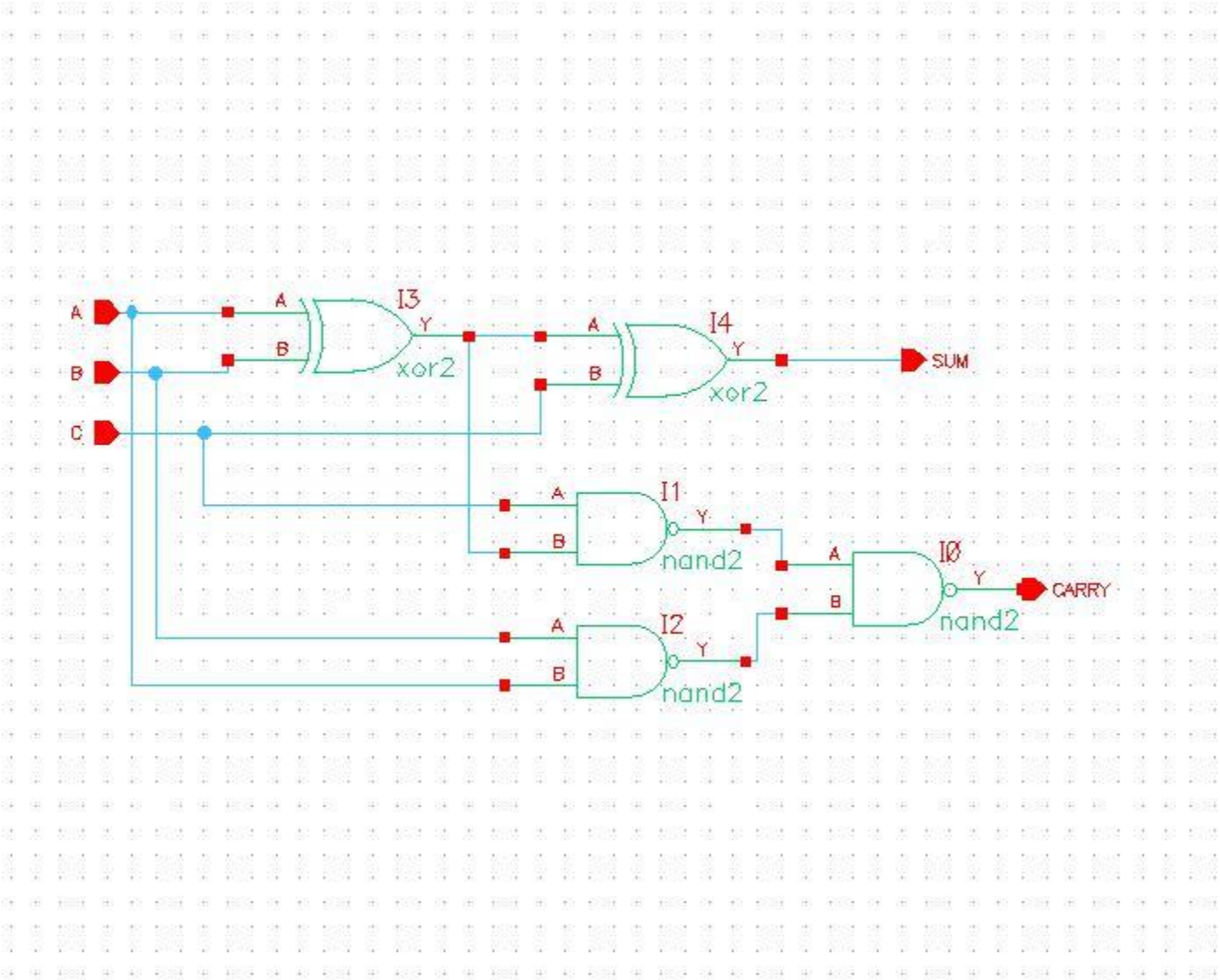
Contents (Schematic, Testbench, Simulation results and Symbols)

Full adder schematic:



Testbench for full adder:

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);


initial
begin

   A = 1'b0;
   B = 1'b0;
   C = 1'b0;

#50 A=1'b0; B=1'b0; C=1'b1;       //ABC=001
#50 A=1'b0; B=1'b1; C=1'b0;       //ABC=010
#50 A=1'b0; B=1'b1; C=1'b1;       //ABC=011
#50 A=1'b1; B=1'b0; C=1'b0;       //ABC=100
#50 A=1'b1; B=1'b0; C=1'b1;       //ABC=101
#50 A=1'b1; B=1'b1; C=1'b0;       //ABC=110
#50 A=1'b1; B=1'b1; C=1'b1;       //ABC=111
end
```

Simulation output for Full adder:

```
TOOL: ncxlmode    15.20-s077: Started on Sep 06, 2019 at 12:52:59 CDT
ncxlmode
      +delay_mode_path
      +typdelays
      -l
      simout.tmp
      /home/grads/m/mana/ecen454/Lab1/fulladder_run1/testfixture.template
      -f /home/grads/m/mana/ecen454/Lab1/fulladder_run1/verilog.inpfiles
```

```
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
            ihnl/cds0/netlist
      +nostdout
      +nocopyright
      +ncvlogargs+" -neverwarn -nostdout -nocopyright "
      +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -
timescale 1ns/1ns -nostdout -nocopyright"
      +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/grads/m/mana/ecen454/Lab1/fulladder_run1/.simTmpNCCmd "
      +mpssession+virtuoso187265
      +mpshost+n01-zeus.olympus.ece.tamu.edu

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Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 A=0, B=0, C=0, SUM=0, CARRY=0
                  50 A=0, B=0, C=1, SUM=1, CARRY=0
                 100 A=0, B=1, C=0, SUM=1, CARRY=0
                 150 A=0, B=1, C=1, SUM=0, CARRY=1
                 200 A=1, B=0, C=0, SUM=1, CARRY=0
                 250 A=1, B=0, C=1, SUM=0, CARRY=1
                 300 A=1, B=1, C=0, SUM=0, CARRY=1
                 350 A=1, B=1, C=1, SUM=1, CARRY=1
ncsim> ^C
ncsim> exit
TOOL: ncxlmode    15.20-s077: Exiting on Sep 06, 2019 at 12:57:12 CDT  (total: 00:04:13)
```
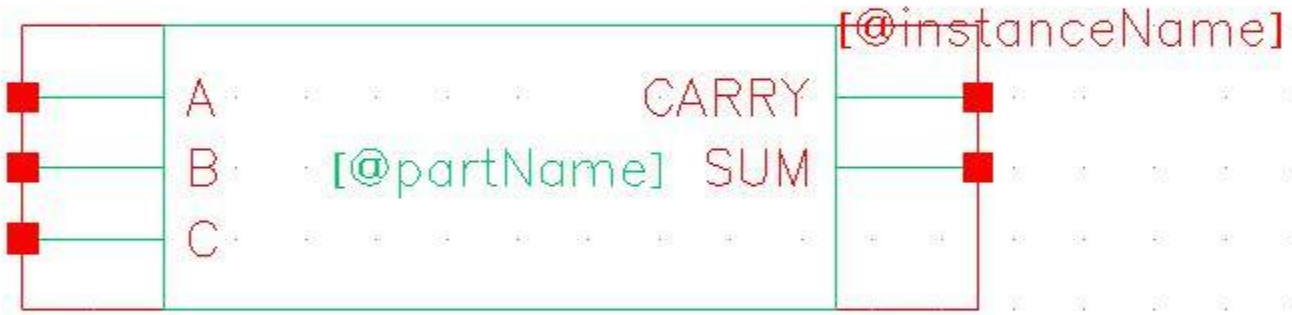
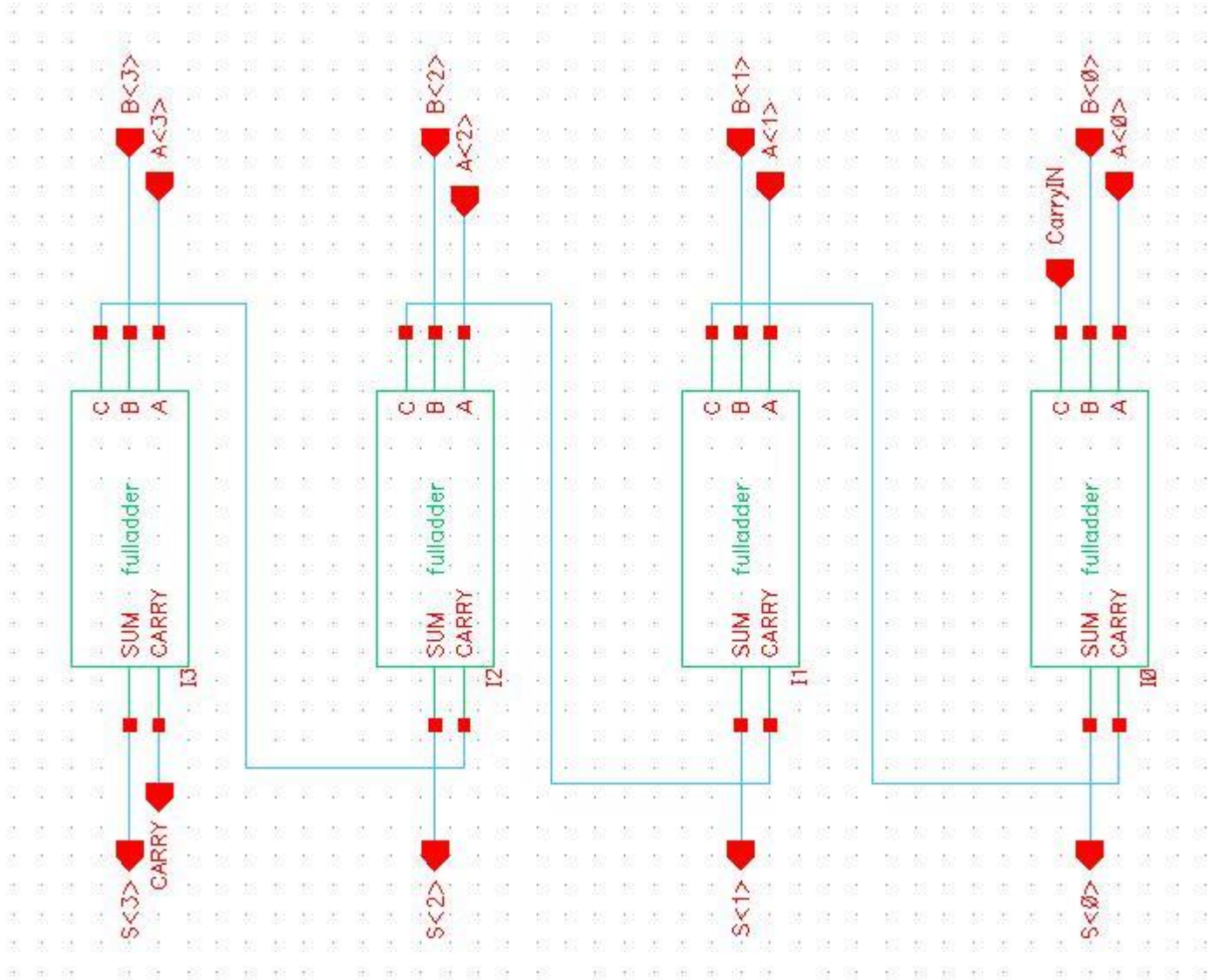

Symbol for Full adder:



4 Bit adder schematic:



Test bench for the 4 bit adder:

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
$monitor ($time," A[0:3]=%b, B[0:3]=%b,CarryIN=%b, S[0:3]=%b, CARRY=%b", A[0:3], B[0:3], CarryIN, S[0:3], CARRY);


initial
begin

   A[0:3]=0;
   B[0:3]=0;

   CarryIN=1'b0;

#50 A[0:3]=3'b1111; B[0:3]=3'b1111; CarryIN=0;          //A = 1111 B = 1111 CarryIN=0
#50 A[0:3]=3'b1010; B[0:3]=3'b1010; CarryIN=1;          //A = 1010 B = 1010 CarryIN=1
#50 A[0:3]=3'b0101; B[0:3]=3'b0101; CarryIN=1;          //A = 0101 B = 0101 CarryIN=1
end
```

Simulation output for 4 bit adder:

```
TOOL: ncxlmode    15.20-s077: Started on Sep 09, 2019 at 12:51:58 CDT
ncxlmode
      +delay_mode_path
      +typdelays
      -l
      simout.tmp
      /home/grads/m/mana/ecen454/Lab1/4BitAdder_run1/testfixture.template
      -f /home/grads/m/mana/ecen454/Lab1/4BitAdder_run1/verilog.inpfiles
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
            ihnl/cds0/netlist
            ihnl/cds1/netlist
      +nostdout
      +nocopyright
```

```
      +ncvlogargs+" -neverwarn -nostdout -nocopyright "
      +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -
timescale 1ns/1ns -nostdout -nocopyright"
      +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/grads/m/mana/ecen454/Lab1/4BitAdder_run1/.simTmpNCCmd "
      +mpssession+virtuoso27094
      +mpshost+n01-zeus.olympus.ece.tamu.edu

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Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 A[0:3]=0000, B[0:3]=0000,CarryIN=0, S[0:3]=0000, CARRY=0
                  50 A[0:3]=0111, B[0:3]=0111,CarryIN=0, S[0:3]=0011, CARRY=1
                 100 A[0:3]=0010, B[0:3]=0010,CarryIN=1, S[0:3]=1001, CARRY=0
                 150 A[0:3]=0101, B[0:3]=0101,CarryIN=1, S[0:3]=1010, CARRY=1
ncsim> ^C
ncsim> exit
TOOL: ncxlmode    15.20-s077: Exiting on Sep 09, 2019 at 12:54:18 CDT  (total: 00:02:20)
```
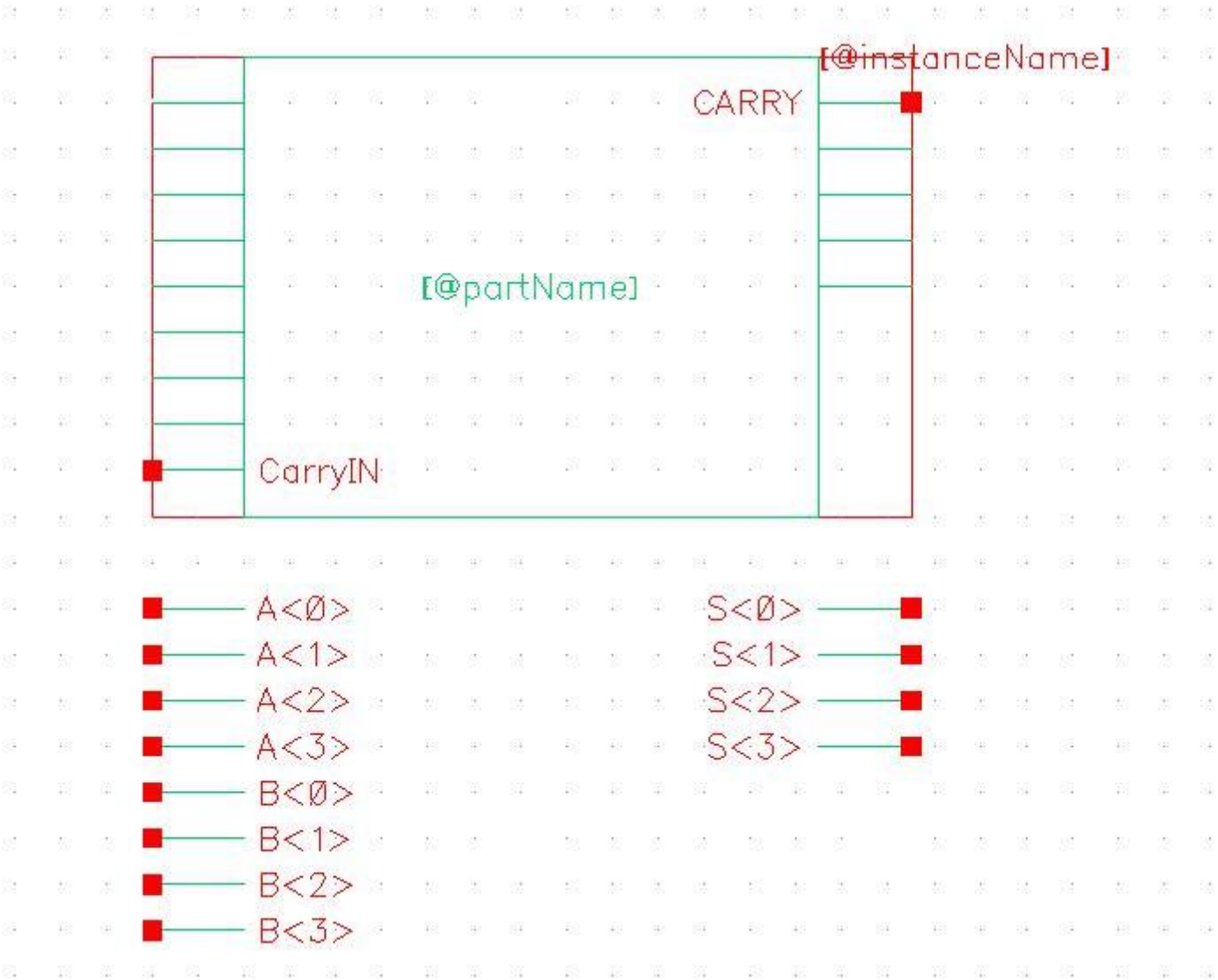
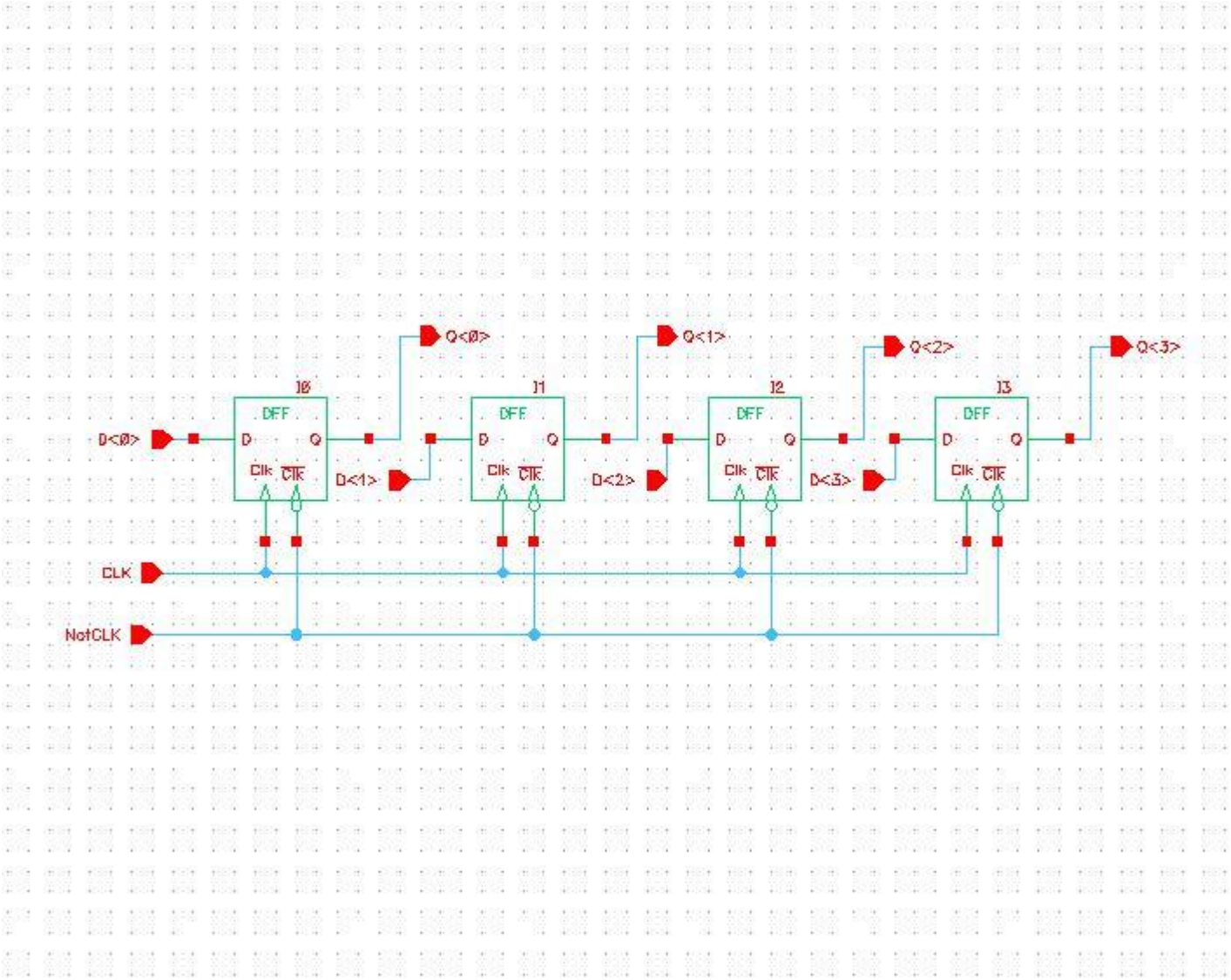

Symbol for 4 bit adder:



Schematic for 4 Bit Register:



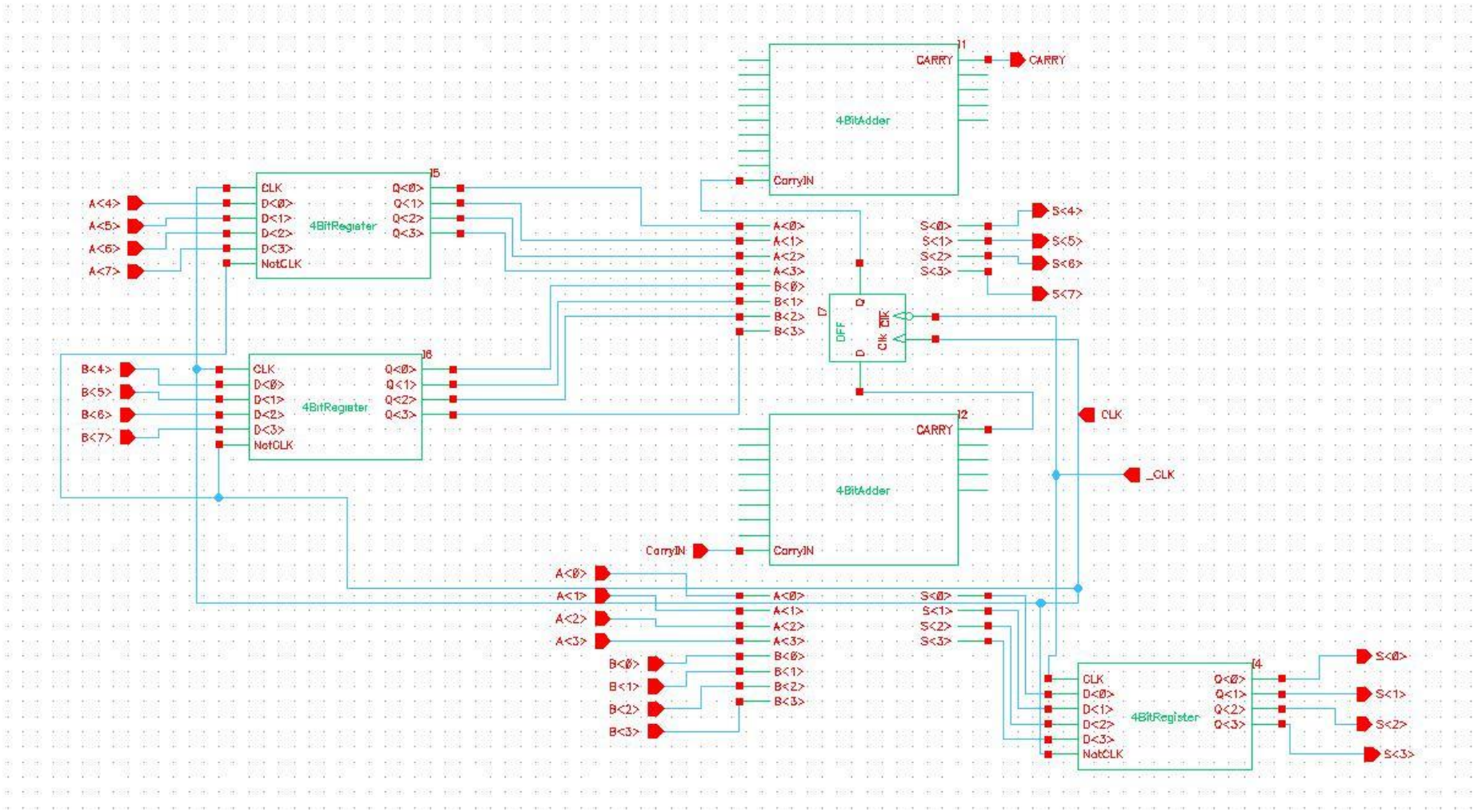
Test bench for the 4 bit register:

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.
initial begin
$monitor ($time," D[0:3]=%b, Q[0:3]=%b", D[0:3], Q[0:3]);
#500 $finish;
end

always begin
      CLK <= 1;
      NotCLK <= 0;
      #10
      CLK <= 0;
      NotCLK <= 1;
      #10;
end

initial begin
   //CLK = 1'b0;
   D[0] = 1'b0;
   D[1] = 1'b0;
   D[2] = 1'b0;
   D[3] = 1'b0;
   //NotCLK = 1'b0;
end


initial begin
 #40 @(posedge CLK) D[0:3]=4'b1111;
 #40 @(posedge CLK) D[0:3] = 4'b0101;

end
```

Simulation results for the 4 bit register:

```
TOOL: ncxlmode    15.20-s077: Started on Sep 09, 2019 at 17:28:05 CDT
ncxlmode
      +delay_mode_path
      +typdelays
      -l
      simout.tmp
      /home/grads/m/mana/ecen454/Lab1/4BitRegister_run1/testfixture.template
      -f /home/grads/m/mana/ecen454/Lab1/4BitRegister_run1/verilog.inpfiles
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/Dlatch/behavioral/verilog.v
            ihnl/cds0/netlist
            ihnl/cds1/netlist
      +nostdout
      +nocopyright
      +ncvlogargs+" -neverwarn -nostdout -nocopyright "
      +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -
timescale 1ns/1ns -nostdout -nocopyright"
      +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/grads/m/mana/ecen454/Lab1/4BitRegister_run1/.simTmpNCCmd "
      +mpssession+virtuoso133923
      +mpshost+n01-zeus.olympus.ece.tamu.edu

-------------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 D[0:3]=0000, Q[0:3]=xxxx
                  20 D[0:3]=0000, Q[0:3]=0000
                  40 D[0:3]=1111, Q[0:3]=1111
                  80 D[0:3]=0101, Q[0:3]=0101
Simulation complete via $finish(1) at time 500 NS + 0
./testfixture.verilog:9 #500 $finish;
ncsim> ^C
ncsim> exit
TOOL: ncxlmode    15.20-s077: Exiting on Sep 09, 2019 at 17:35:26 CDT  (total: 00:07:21)
```

8 Bit adder schematic:



TEST BENCH FOR THE PIPELINED 8BIT ADDER:

```
// Verilog stimulus file.
// Please do not create a module in this file.
```

```
// Default verilog stimulus.

initial begin
$monitor ($time," A[1:7]=%b, B[1:7]=%b, CarryIN=%b,  S[1:7]=%b, CARRY=%b", A[0:7], B[0:7], CarryIN, S[0:7], CARRY);

end

initial
begin
   A[0] = 1'b0;
   A[1] = 1'b0;
   A[2] = 1'b0;
   A[3] = 1'b0;
   A[4] = 1'b0;
   A[5] = 1'b0;
   A[6] = 1'b0;
   A[7] = 1'b0;
   B[0] = 1'b0;
   B[1] = 1'b0;
   B[2] = 1'b0;
   B[3] = 1'b0;
   B[4] = 1'b0;
   B[5] = 1'b0;
   B[6] = 1'b0;
   B[7] = 1'b0;
  // CLK = 1'b0;
   CarryIN = 1'b0;
   //_CLK = 1'b0;
end

always begin
      CLK <= 1;
      _CLK <= 0;
      #10
      CLK <= 0;
      _CLK <= 1;
      #10;
end


initial begin
//i.> 01111110 +11100111 + 0 (Carry In)
```

```
@(posedge CLK)#20 A[0:3]=4'b0111; B[0:3]=4'b1110; CarryIN=0;
@(posedge CLK)#20 A[4:7]=4'b1110; B[4:7]=4'b0111;
#20;

//ii.> 11111111 + 00000000 + 1 (Carry In)
@(posedge CLK)#20 A[0:3]=4'b1111; B[0:3]=4'b0000; CarryIN=1;
@(posedge CLK)#20 A[4:7]=4'b1111; B[4:7]=4'b0000;
#20;

//iii.> 10101010 + 01010101 + 0 (Carry In)
@(posedge CLK)#20 A[0:3]=4'b0101; B[0:3]=4'b1010; CarryIN=0;
@(posedge CLK)#20 A[4:7]=4'b0101; B[4:7]=4'b1010;
#20;

//iv.> 10101010 + 01010101 + 1 (Carry In)
@(posedge CLK)#20 A[0:3]=4'b0101; B[0:3]=4'b1010; CarryIN=1;
@(posedge CLK)#20 A[4:7]=4'b0101; B[4:7]=4'b1010;
#20;

//v.> 11001100 + 00110011 + 0 (Carry In)
@(posedge CLK)#20 A[0:3]=4'b0011; B[0:3]=4'b1100; CarryIN=0;
@(posedge CLK)#20 A[4:7]=4'b0011; B[4:7]=4'b1100;
#20;

//vi.> 11001100 + 00110011 + 1 (Carry In)
@(posedge CLK)#20 A[0:3]=4'b0011; B[0:3]=4'b1100; CarryIN=1;
@(posedge CLK)#20 A[4:7]=4'b0011; B[4:7]=4'b1100;
#20;

end
```

OUPUT OF SIMULATIONS FOR THE PIPELINED 8BIT ADDER:

```
TOOL: ncxlmode    15.20-s077: Started on Sep 09, 2019 at 19:48:45 CDT
ncxlmode
      +delay_mode_path
      +typdelays
      -l
      simout.tmp
      /home/grads/m/mana/ecen454/Lab1/8BitPipeAdder_run1/testfixture.template
      -f /home/grads/m/mana/ecen454/Lab1/8BitPipeAdder_run1/verilog.inpfiles
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
```

```
            /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/Dlatch/behavioral/verilog.v
            ihnl/cds0/netlist
            ihnl/cds1/netlist
            ihnl/cds2/netlist
            ihnl/cds3/netlist
            ihnl/cds4/netlist
      +nostdout
      +nocopyright
      +ncvlogargs+" -neverwarn -nostdout -nocopyright "
      +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -
timescale 1ns/1ns -nostdout -nocopyright"
      +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/grads/m/mana/ecen454/Lab1/8BitPipeAdder_run1/.simTmpNCCmd "
      +mpssession+virtuoso191263
      +mpshost+n01-zeus.olympus.ece.tamu.edu

-------------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 A[1:7]=00000000, B[1:7]=00000000, CarryIN=0,  S[1:7]=xxxxxxxx, CARRY=x
                  10 A[1:7]=00000000, B[1:7]=00000000, CarryIN=0,  S[1:7]=0000xxxx, CARRY=x
                  20 A[1:7]=01110000, B[1:7]=11100000, CarryIN=0,  S[1:7]=0000xxxx, CARRY=x
                  30 A[1:7]=01110000, B[1:7]=11100000, CarryIN=0,  S[1:7]=10101000, CARRY=0
                  40 A[1:7]=01111110, B[1:7]=11100111, CarryIN=0,  S[1:7]=10101000, CARRY=0
                  70 A[1:7]=01111110, B[1:7]=11100111, CarryIN=0,  S[1:7]=10100110, CARRY=1
                  80 A[1:7]=11111110, B[1:7]=00000111, CarryIN=1,  S[1:7]=10100110, CARRY=1
                  90 A[1:7]=11111110, B[1:7]=00000111, CarryIN=1,  S[1:7]=00000110, CARRY=1
                 100 A[1:7]=11111111, B[1:7]=00000000, CarryIN=1,  S[1:7]=00000110, CARRY=1
                 130 A[1:7]=11111111, B[1:7]=00000000, CarryIN=1,  S[1:7]=00000000, CARRY=1
                 140 A[1:7]=01011111, B[1:7]=10100000, CarryIN=0,  S[1:7]=00001111, CARRY=0
                 150 A[1:7]=01011111, B[1:7]=10100000, CarryIN=0,  S[1:7]=11111111, CARRY=0
                 160 A[1:7]=01010101, B[1:7]=10101010, CarryIN=0,  S[1:7]=11111111, CARRY=0
                 200 A[1:7]=01010101, B[1:7]=10101010, CarryIN=1,  S[1:7]=11110000, CARRY=1
                 210 A[1:7]=01010101, B[1:7]=10101010, CarryIN=1,  S[1:7]=00000000, CARRY=1
                 260 A[1:7]=00110101, B[1:7]=11001010, CarryIN=0,  S[1:7]=00001111, CARRY=0
                 270 A[1:7]=00110101, B[1:7]=11001010, CarryIN=0,  S[1:7]=11111111, CARRY=0
                 280 A[1:7]=00110011, B[1:7]=11001100, CarryIN=0,  S[1:7]=11111111, CARRY=0
                 320 A[1:7]=00110011, B[1:7]=11001100, CarryIN=1,  S[1:7]=11110000, CARRY=1
```

```
                330 A[1:7]=00110011, B[1:7]=11001100, CarryIN=1,  S[1:7]=00000000, CARRY=1
Simulation interrupted at 88334850 NS + 0
ncsim> ^C
ncsim> exit
TOOL: ncxlmode    15.20-s077: Exiting on Sep 09, 2019 at 19:50:19 CDT  (total: 00:01:34)
```

8 Bit adder symbol: