ECEN 714: Submission for LAB 7

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Contents (Schematic, Layout, DRC and LVS for the 6-bit Pipelined Adder and H-clock tree)

Schematic:

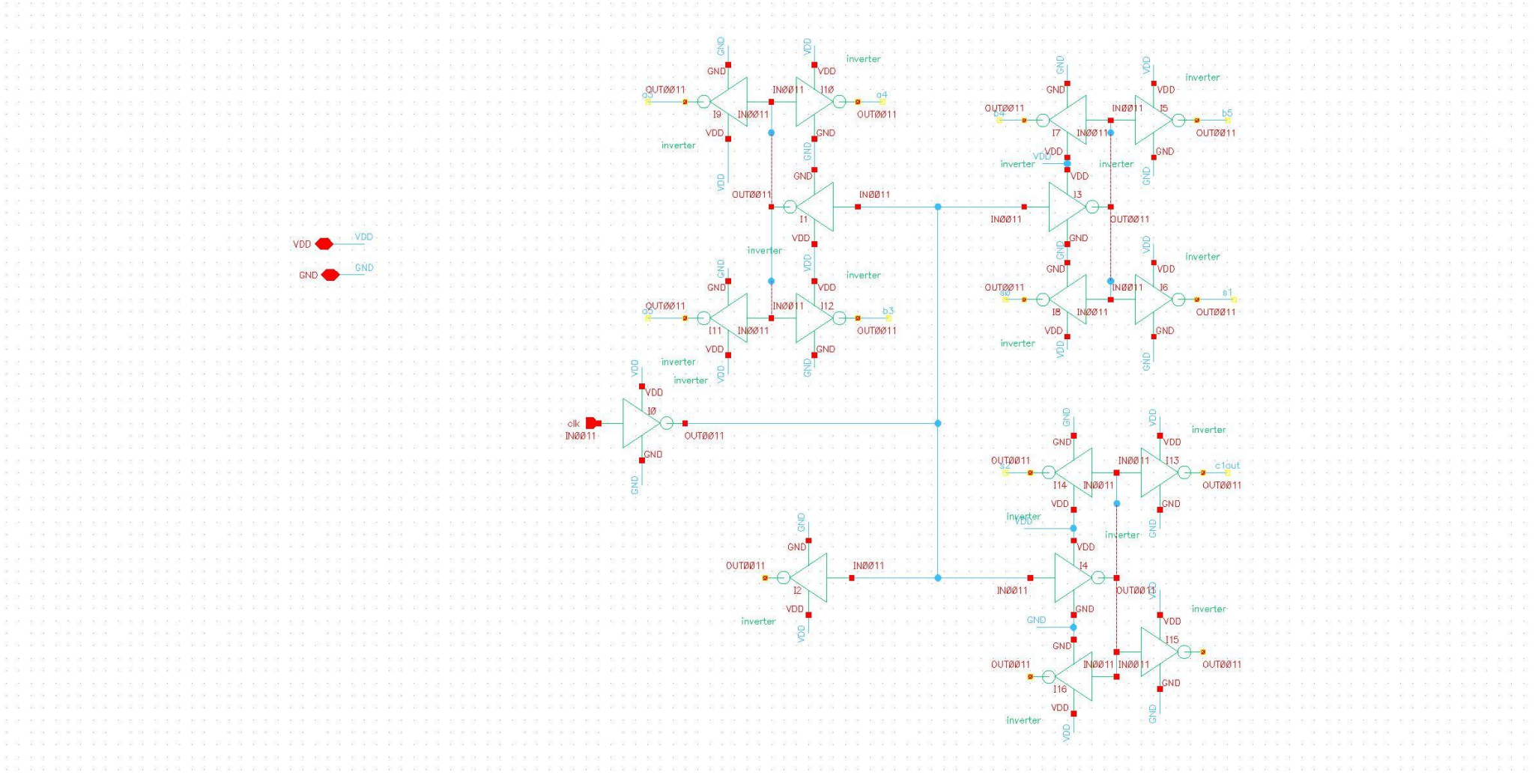


Figure 1: Schematic for the H-tree clock distribution network.

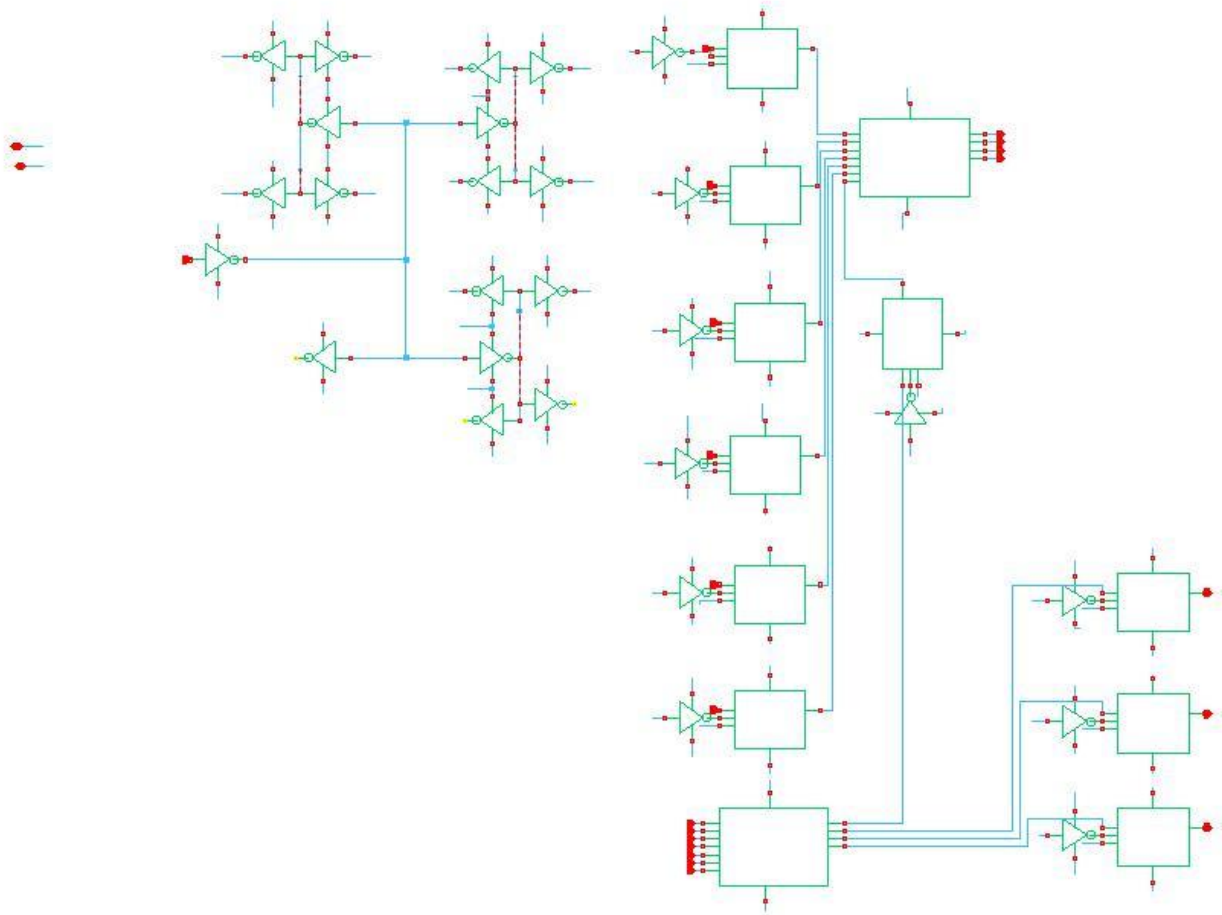


Figure 2: Schematic of the 6-bit Pipelined adder

Layout

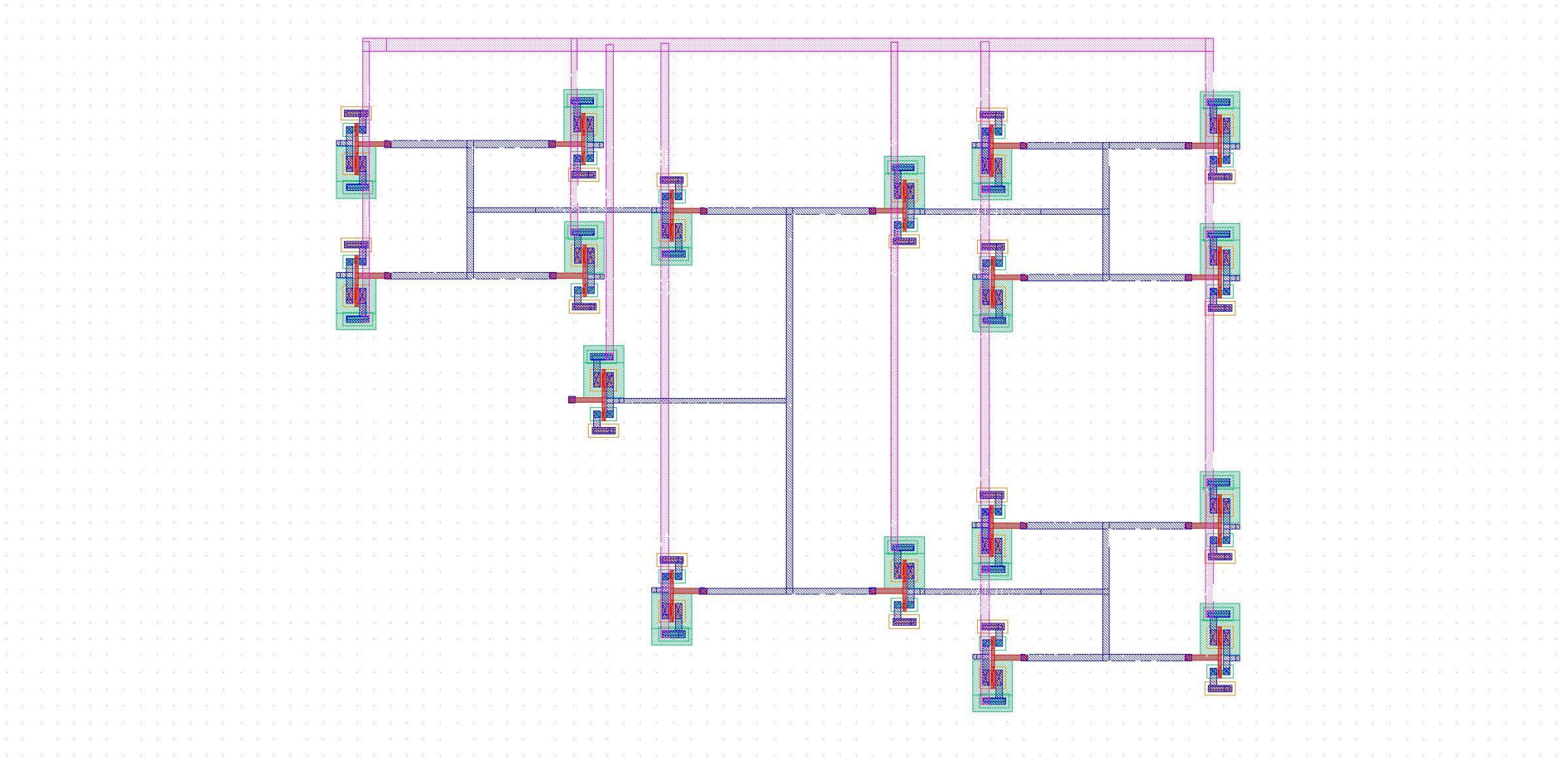


Figure 3: Layout for the H-tree clock distribution network

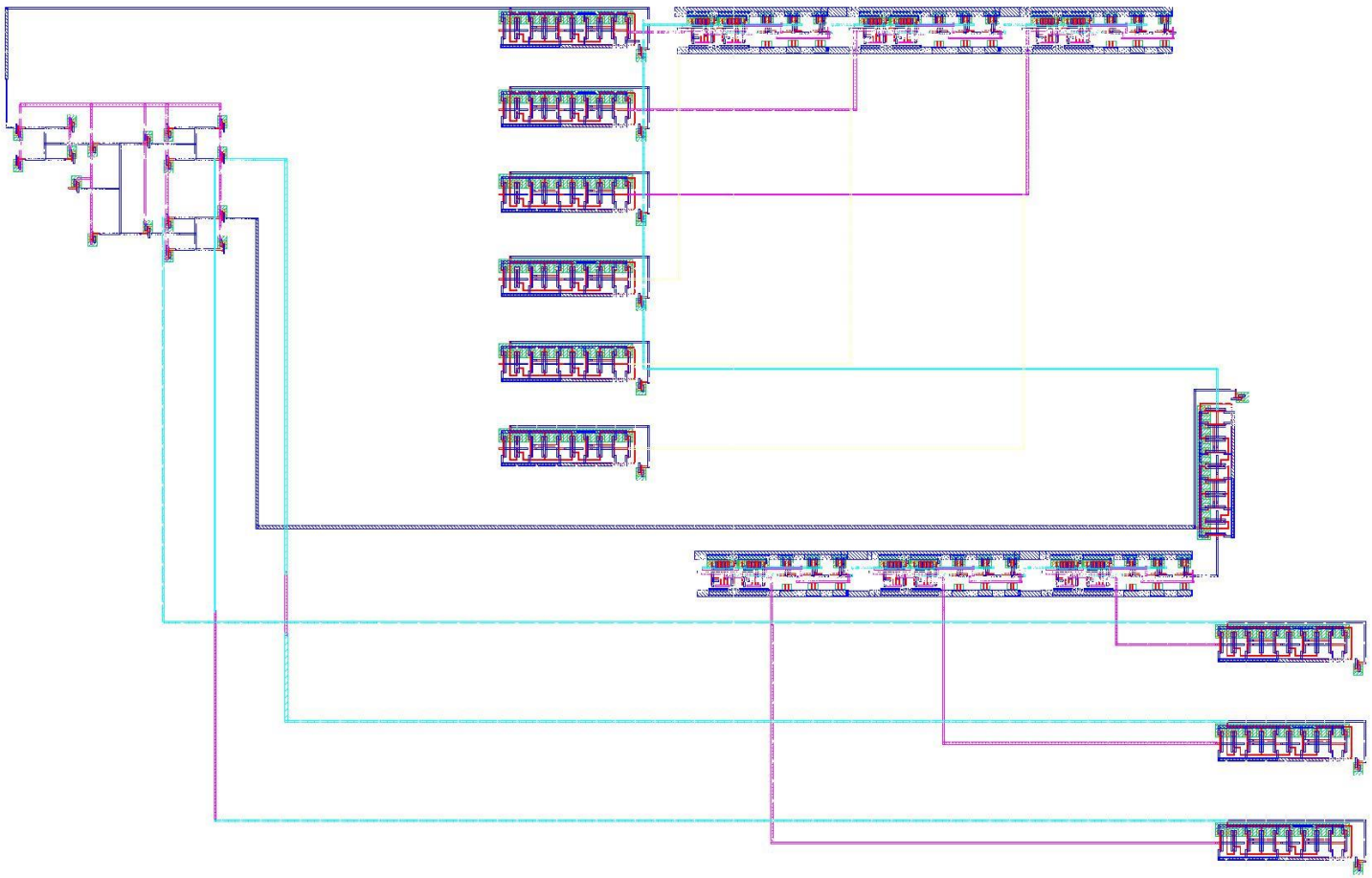
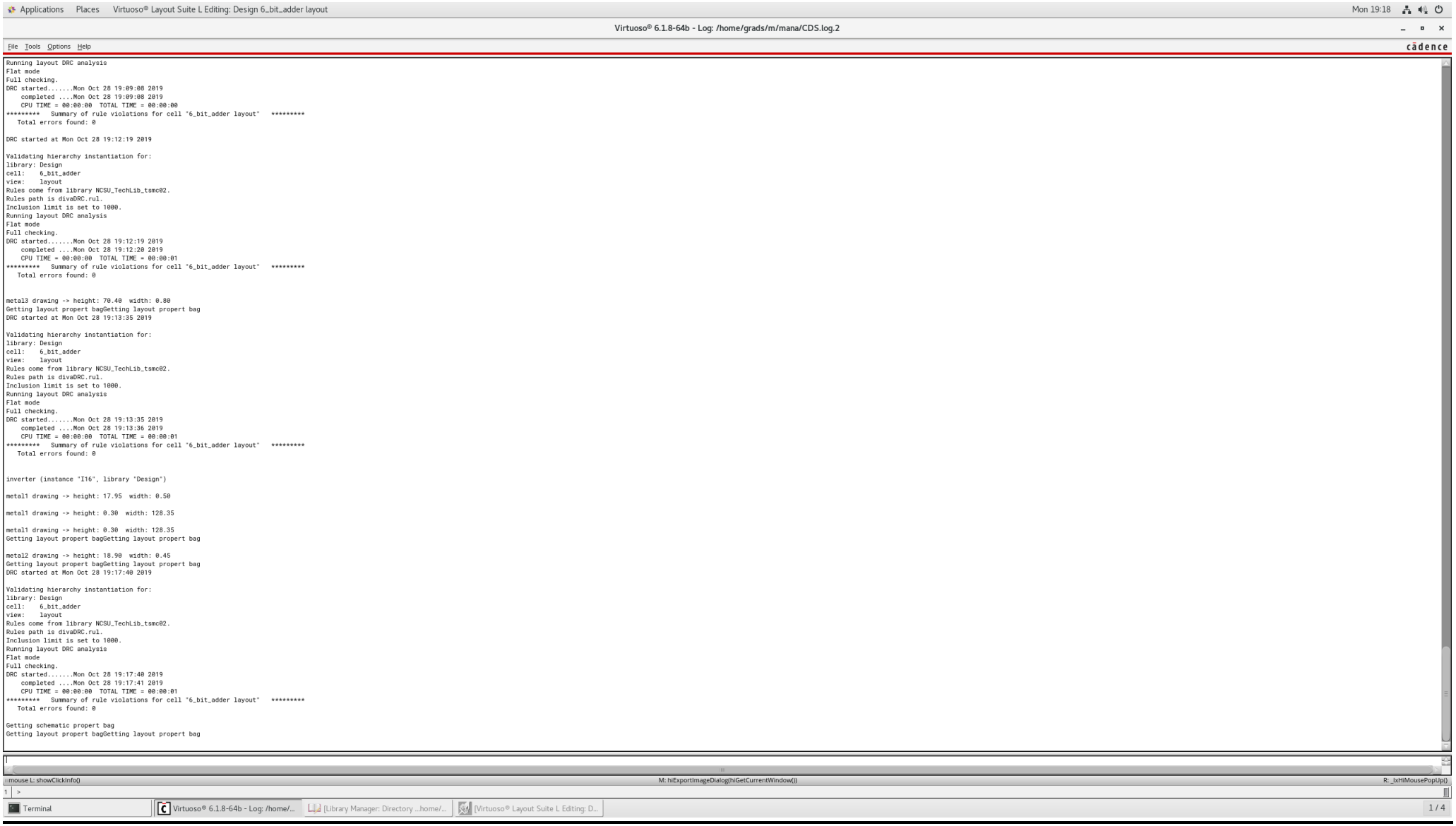


Figure 4: Layout for the 6-bit Pipelined Adder

DRC:


Applications Places Virtuoso® Layout Suite L Editing: Design 6_bit_adder layout
Mon 19:18
Virtuoso® 6.1.8-64b - Log: /home/grads/m/mana/CDS.log.2
File Tools Options Help
cadence
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Oct 28 19:09:08 2019
completed ....Mon Oct 28 19:09:08 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
********* Summary of rule violations for cell "6_bit_adder layout" *********
Total errors found: 0
DRC started at Mon Oct 28 19:12:19 2019
Validating hierarchy instantiation for:
library: Design
cell: 6_bit_adder
view: layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Oct 28 19:12:19 2019
completed ....Mon Oct 28 19:12:20 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
********* Summary of rule violations for cell "6_bit_adder layout" *********
Total errors found: 0
metal3 drawing -> height: 70.40 width: 0.80
Getting layout propert bagGetting layout propert bag
DRC started at Mon Oct 28 19:13:35 2019
Validating hierarchy instantiation for:
library: Design
cell: 6_bit_adder
view: layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Oct 28 19:13:35 2019
completed ....Mon Oct 28 19:13:36 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
********* Summary of rule violations for cell "6_bit_adder layout" *********
Total errors found: 0
inverter (instance "I16", library "Design")
metal1 drawing -> height: 17.95 width: 0.50
metal1 drawing -> height: 0.30 width: 128.35
metal1 drawing -> height: 0.30 width: 128.35
Getting layout propert bagGetting layout propert bag
metal2 drawing -> height: 18.90 width: 0.45
Getting layout propert bagGetting layout propert bag
DRC started at Mon Oct 28 19:17:40 2019
Validating hierarchy instantiation for:
library: Design
cell: 6_bit_adder
view: layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Oct 28 19:17:40 2019
completed ....Mon Oct 28 19:17:41 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
********* Summary of rule violations for cell "6_bit_adder layout" *********
Total errors found: 0
Getting schematic propert bag
Getting layout propert bagGetting layout propert bag
mouse L: showClickInfo()
M: hiExportImageDialog(hiGetCurrentWindow())
R: _lxHiMousePopUp()
Terminal
Virtuoso® 6.1.8-64b - Log: /home/...
[Library Manager: Directory ...home/...
[Virtuoso® Layout Suite L Editing: D...
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LVS report for only the H-tree:

```
@(#)$CDS: LVS version 6.1.8-64b 10/01/2018 19:50 (ip-172-18-22-57) $
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t
/home/grads/m/mana/ecen454/Lab1/LVS/layout /home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
       count
        20              nets
        3               terminals
        17              pmos
        17              nmos

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
       count
        20              nets
        3               terminals
        17              pmos
        17              nmos


    Terminal correspondence points
    N17       N8        GND
    N19       N3        VDD
    N18       N0        clk

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

15 net-list ambiguities were resolved by random selection.

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
```

```
        size errors             0       0
        pruned                  0       0
        active                  34      34
        total                   34      34

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  20      20
        total                   20      20

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   3       3


Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:
```

```
termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```