ECEN 714: Submission for LAB 5

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Contents (Simulation for 3-bit adder with Schematic and Layout)

3-bit Adder:

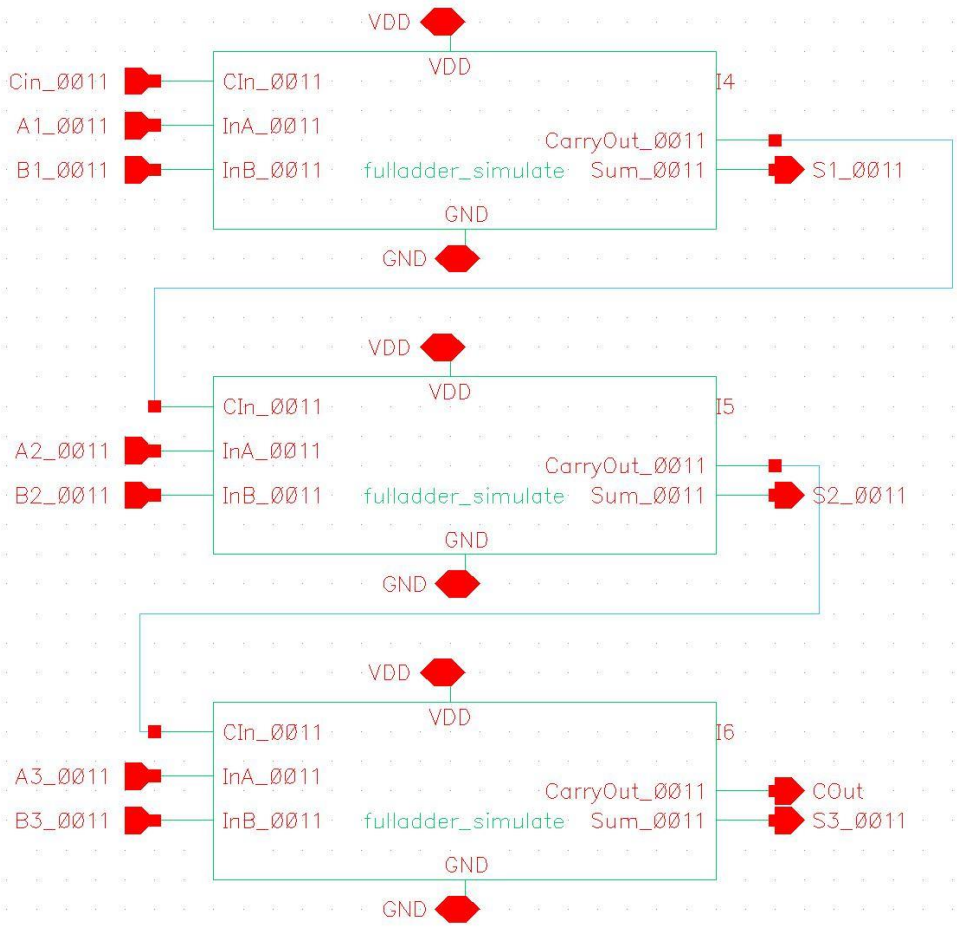

Figure 1: 3 bit adder Schematic

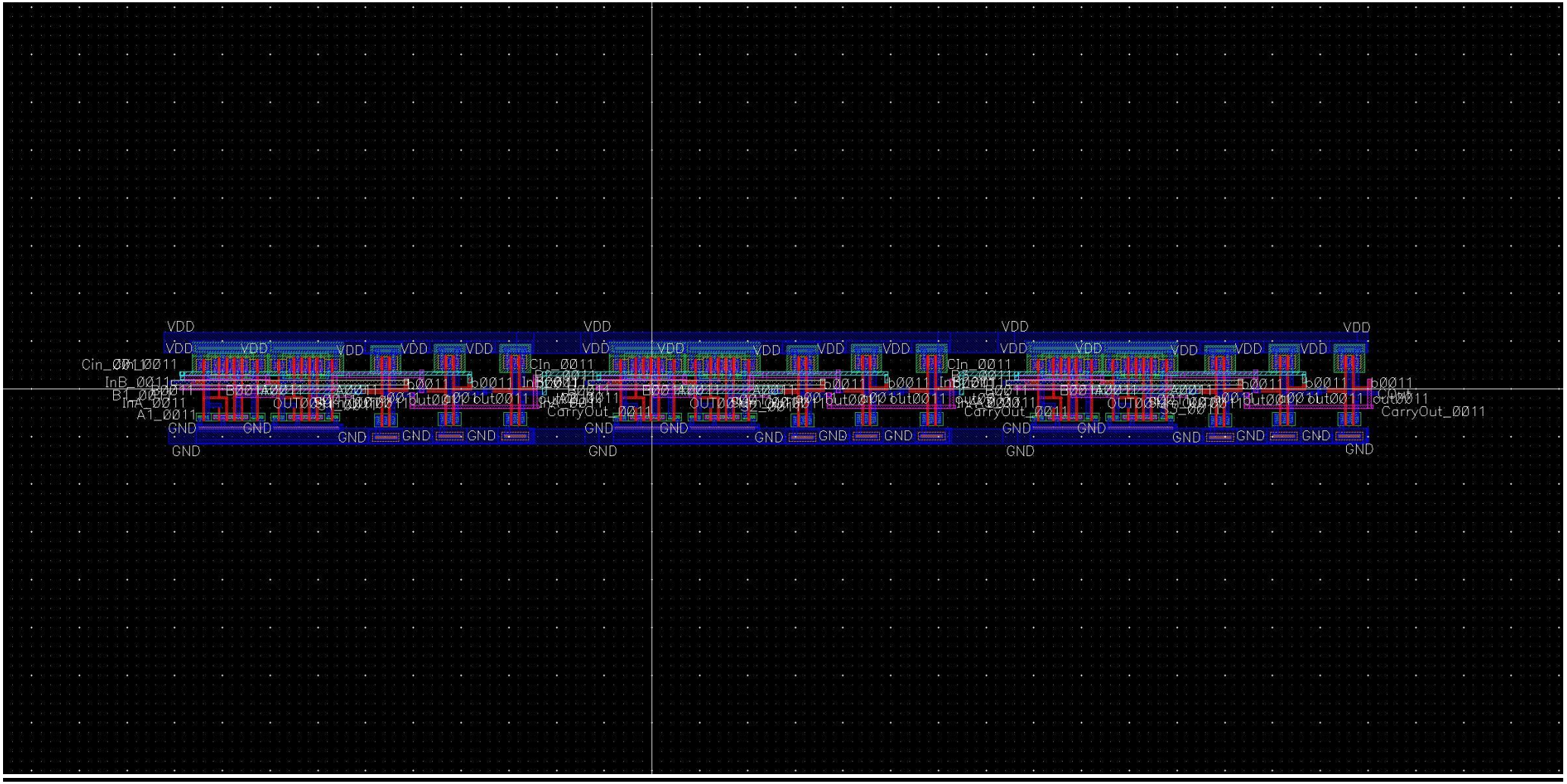

Figure 2: 3 bit adder Layout

DRC Results:

```
DRC started at Mon Oct 14 17:49:06 2019

Validating hierarchy instantiation for:
library: Design
cell:    3_bit_adder
view:    layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Parsing drcExtractRules of "/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_TechLib_tsmc02/divaDRC.rul"...
Optimizing rules...
removing unused task: nwellResEdge = geomGetEdge(nwellRes coincident nwell)
removing unused task: polyResEdge = geomGetEdge(polyRes coincident poly)
removing unused task: sGateWidthCheckEdge = geomGetEdge(sGateWidthCheck)
removing unused task: metalcapEdge = geomGetEdge(metalcap)
removing unused task: padEdge = geomGetEdge(pad)
removing unused task: ccEdge = geomGetEdge(cc)
removing unused task: gselectEdge = geomGetEdge(gselect)
removing unused task: gwellEdge = geomGetEdge(gwell)
removing unused task: nwellRes = geomButting(geomAnd(res_id nwell) nBulk (keep == 2))
removing unused task: polyRes = geomButting(geomAndNot(geomAnd(res_id poly) polySRes) fieldPoly (keep == 2))
removing unused task: sGateWidthCheck = geomSize(geomSize(geomAnd(Gate sblock) -2.9) 2.9)
removing unused task: NwPdiode = geomAnd(dio_id geomOutside(nwell pNotOhmic))
removing unused task: PNdiode = geomAnd(dio_id geomOutside(pNotOhmic poly))
removing unused task: NPdiode = geomAnd(dio_id geomOutside(nNotOhmic poly))
removing unused task: m6m5Cap = geomAnd(geomAnd(metal5 metal6) cap_id)
removing unused task: m5m4Cap = geomAnd(geomAnd(metal4 metal5) cap_id)
removing unused task: m4m3Cap = geomAnd(geomAnd(metal3 metal4) cap_id)
removing unused task: m3m2Cap = geomAnd(geomAnd(metal2 metal3) cap_id)
removing unused task: m2m1Cap = geomAnd(geomAnd(metal1 metal2) cap_id)
removing unused task: m1sCap = geomAnd(geomAndNot(metal1 poly) cap_id)
removing unused task: m1pCap = geomAnd(geomAnd(poly metal1) cap_id)
removing unused task: pChannelTran = geomAndNot(pChannelTran hvpChannelTran)
removing unused task: hvpChannelTran = geomAnd(pChannelTran tactive)
removing unused task: nChannelTran = geomAndNot(nChannelTran hvnChannelTran)
removing unused task: hvnChannelTran = geomAnd(nChannelTran tactive)
removing unused task: pChannelCap = geomButting(pChannel pDiff (keep == 1))
removing unused task: nChannelCap = geomButting(nChannel nDiff (keep == 1))
removing unused task: pChannelTran = geomButting(pChannel pDiff (keep == 2))
removing unused task: nChannelTran = geomButting(nChannel nDiff (keep == 2))
removing unused task: Space = geomNot(geomOr(active poly))
removing unused task: pChannel = geomAnd(pNotOhmic poly)
removing unused task: nChannel = geomAnd(nNotOhmic poly)
removing unused task: dio_id = geomOr("dio_id")
removing unused task: cap_id = geomOr("cap_id")
removing unused task: nolpe = geomOr("nolpe")
removing unused task: bkgnd = geomBkgnd()
warn:   Duplicate check "(SCMOS Rule 20.9) sblock enclosure of poly resistor: 0.20 um" is being ignored.
warn:   Duplicate check "(SCMOS Rule 26.2) metal5 width: 0.30 um" is being ignored.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Mon Oct 14 17:49:06 2019
    completed ....Mon Oct 14 17:49:07 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "3_bit_adder layout"   *********
   Total errors found: 0
```

mouse L: showClickInfo()

1 >

LVS Results:

```
@(#)$CDS: LVS version 6.1.8-64b 10/01/2018 19:50 (ip-172-18-22-57) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t
/home/grads/m/mana/ecen454/Lab1/LVS/layout /home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
       count
        69              nets
        13              terminals
        54              pmos
        54              nmos

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
       count
        69              nets
        13              terminals
        54              pmos
        54              nmos


    Terminal correspondence points
    N58       N13       A1_0011
    N62       N9        A2_0011
    N64       N5        A3_0011
    N56       N14       B1_0011
    N60       N2        B2_0011
    N63       N4        B3_0011
    N65       N11       COut
    N67       N0        Cin_0011
    N59       N6        GND
    N68       N10       S1_0011
    N57       N8        S2_0011
    N61       N7        S3_0011
    N66       N12       VDD
```

```
Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  108     108
        total                   108     108

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  69      69
        total                   69      69

                               terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   13      13


Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:
```

audit.out:

Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

3 Bit Adder Delays

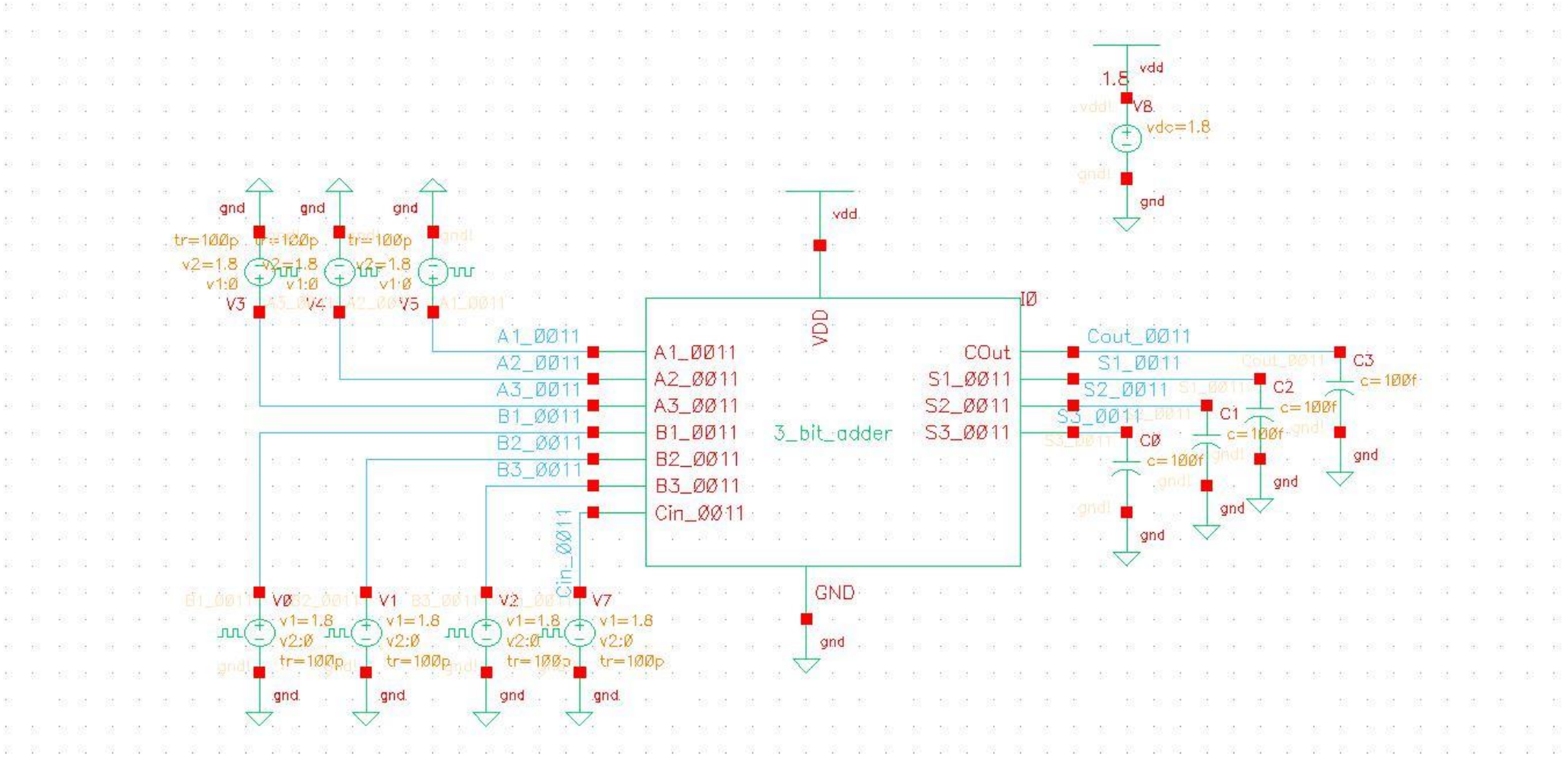

Figure 3: Post Layout Simulation setup

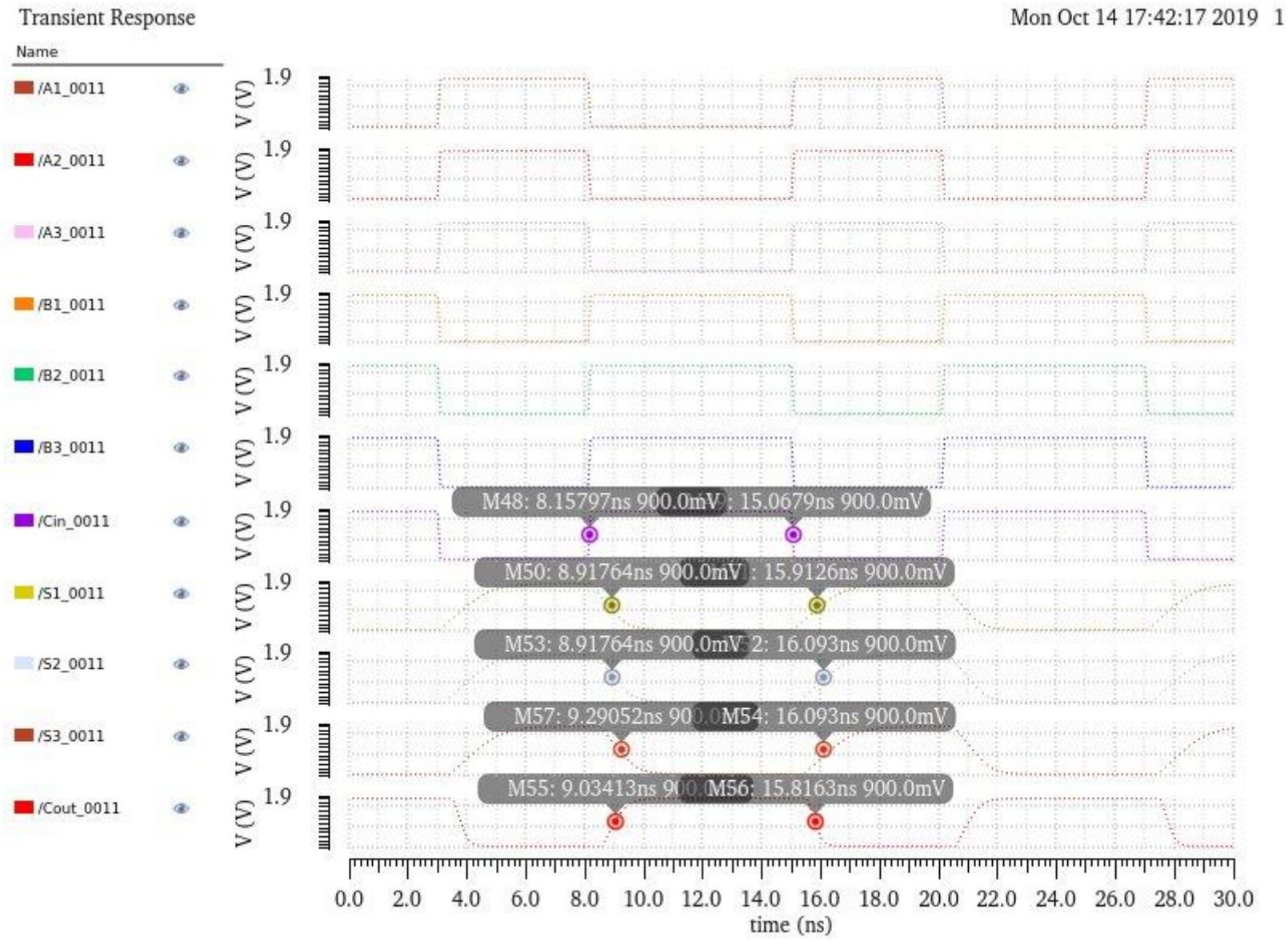

Figure 4: Input Vector 1 delays

Vector 1 *A=000; B=111; Cin= 1*	**Cin**	**s1**	**s2**	**s3**	**Cout**

	8.1597	8.91764	8.91764	9.29052	9.03413
	15.0679	15.9126	16.093	16.093	15.816
Delay	**s1**	**s2**	**s3**	**Cout**	
Rising	0.75794	0.75794	1.13082	0.7481	
Falling	0.8447	1.0251	1.0251	0.87443	

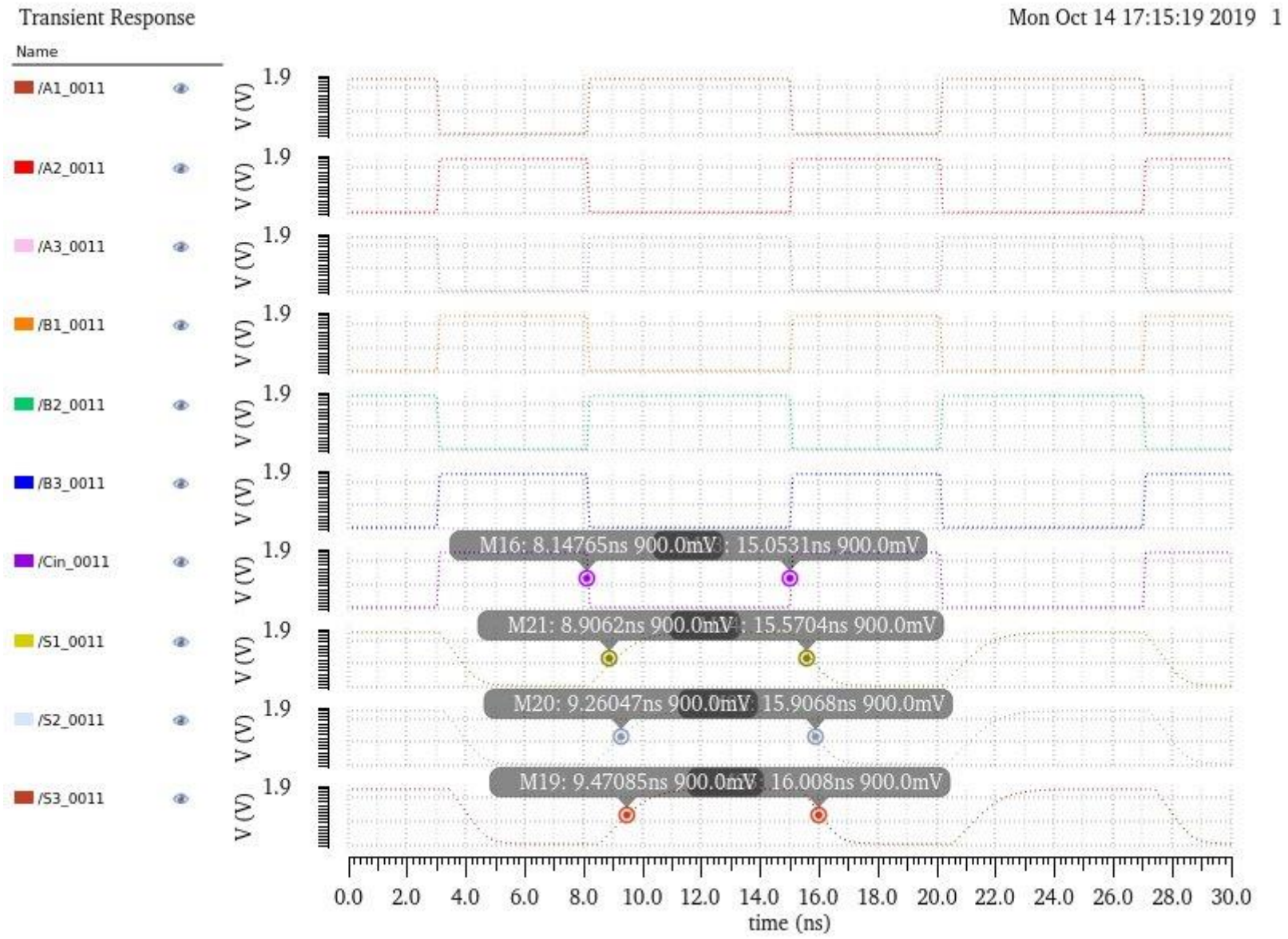

Figure 5: Delay for input vector 2

Vector 2 *A=101; B=010; Cin=0*	**Cin**	**s1**	**s2**	**s3**	**Cout**
	8.14765	8.9062	9.26074	9.47085	8.99078
	15.0565	15.5704	15.9068	16.008	15.9326
Delay	**s1**	**s2**	**s3**	**cout**	
Rising	0.75855	1.11309	1.3232	0.8761	
Falling	0.5139	0.8503	0.9515	0.84313	

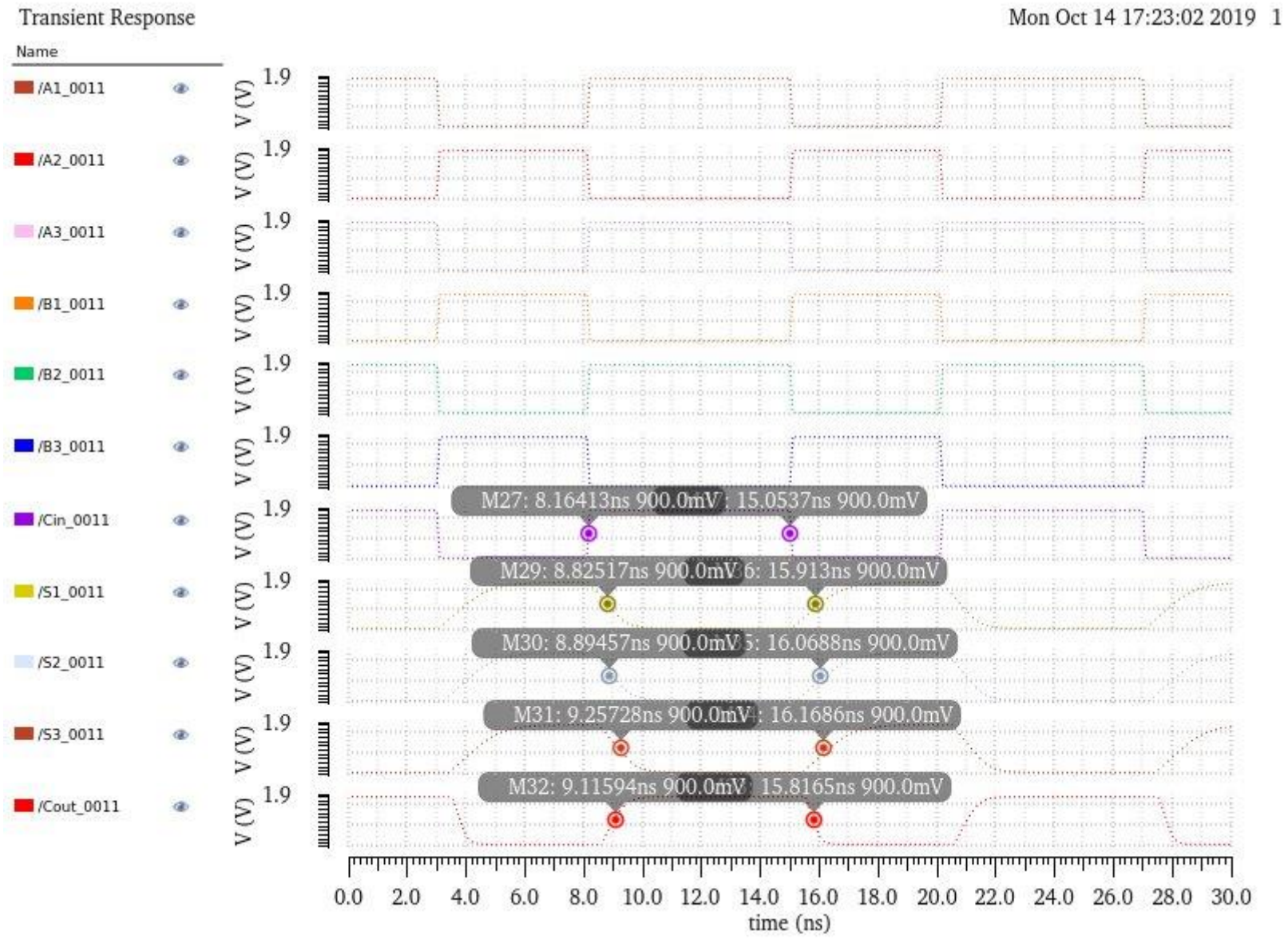

Figure 6: Input Vector 3 delays

Vector 3 *A=101; B=010; Cin=1*	**Cin**	**s1**	**s2**	**s3**	**Cout**
	8.16413	8.82517	8.89457	9.25728	9.11594
	15.0537	15.913	16.0688	16.1686	15.8164
Delay	**s1**	**s2**	**s3**	**cout**	
Rising	0.8593	1.0151	1.1149	0.95181	
Falling	0.66104	0.73044	1.09315	0.7627	

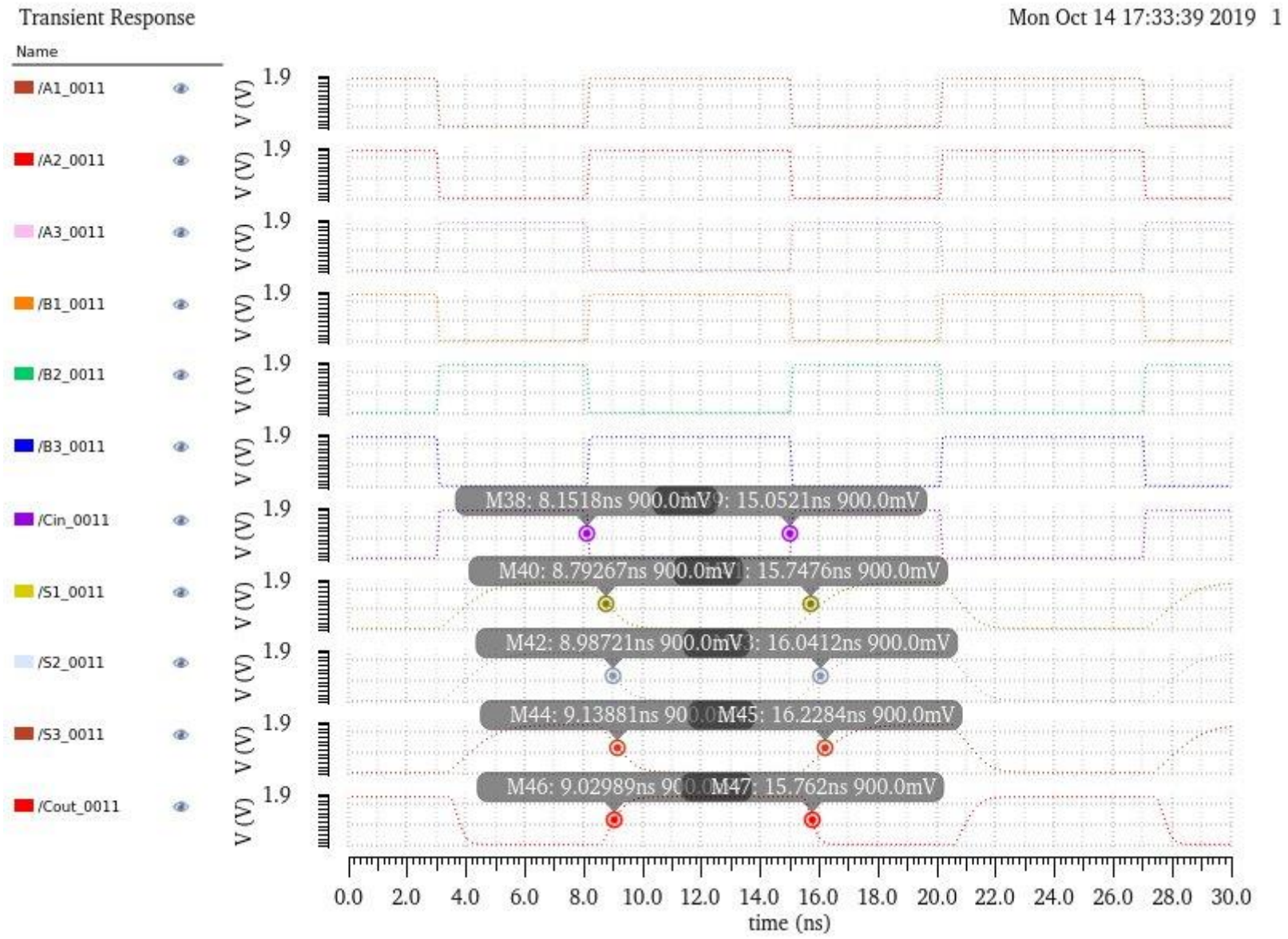

Figure 7: Input vector 4 delays

Vector 4 *A=110; B=101; Cin=0*	**Cin**	**s1**	**s2**	**s3**	**Cout**
	8.1518	8.79267	8.98721	9.13881	9.02989
	15.0521	15.7476	16.0412	16.2284	15.762
Delay	**s1**	**s2**	**s3**	**cout**	
Rising	0.64087	0.83541	0.98701	0.7099	
Falling	0.6955	0.9891	1.1763	0.87809	

Power Calculations:

Input vector 1: (*A=000; B=111; Cin= 1)*

I	V	P
-9.55E-05	1.8	-0.00017

Input vector 2: (*A=101; B=010; Cin=0)*

I	V	P
-8.56E-05	1.8	-0.00015

Input vector 3: (*A=101; B=010; Cin=1)*

I	V	P
-9.55E-05	1.8	-0.00017

Input vector 4: (*A=110; B=101; Cin=0)*

I	V	P
-9.58E-05	1.8	-1.72E-04