ECEN 714: Submission for LAB 3

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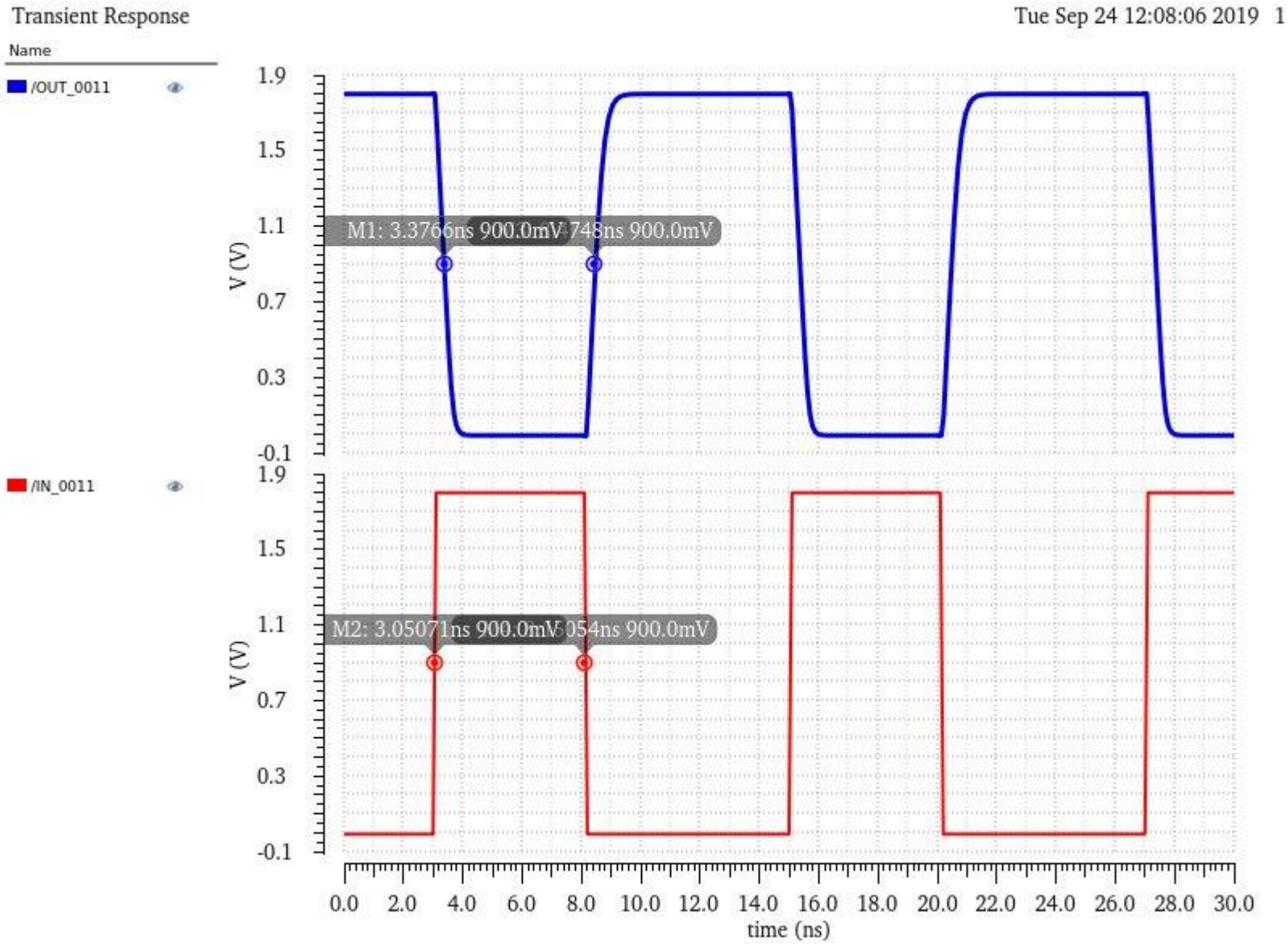
Contents (Simulation for Inverter, NAND, XOR and Schematic, Layout and Simulation of 1 bit adder)

Inverter Simulation:

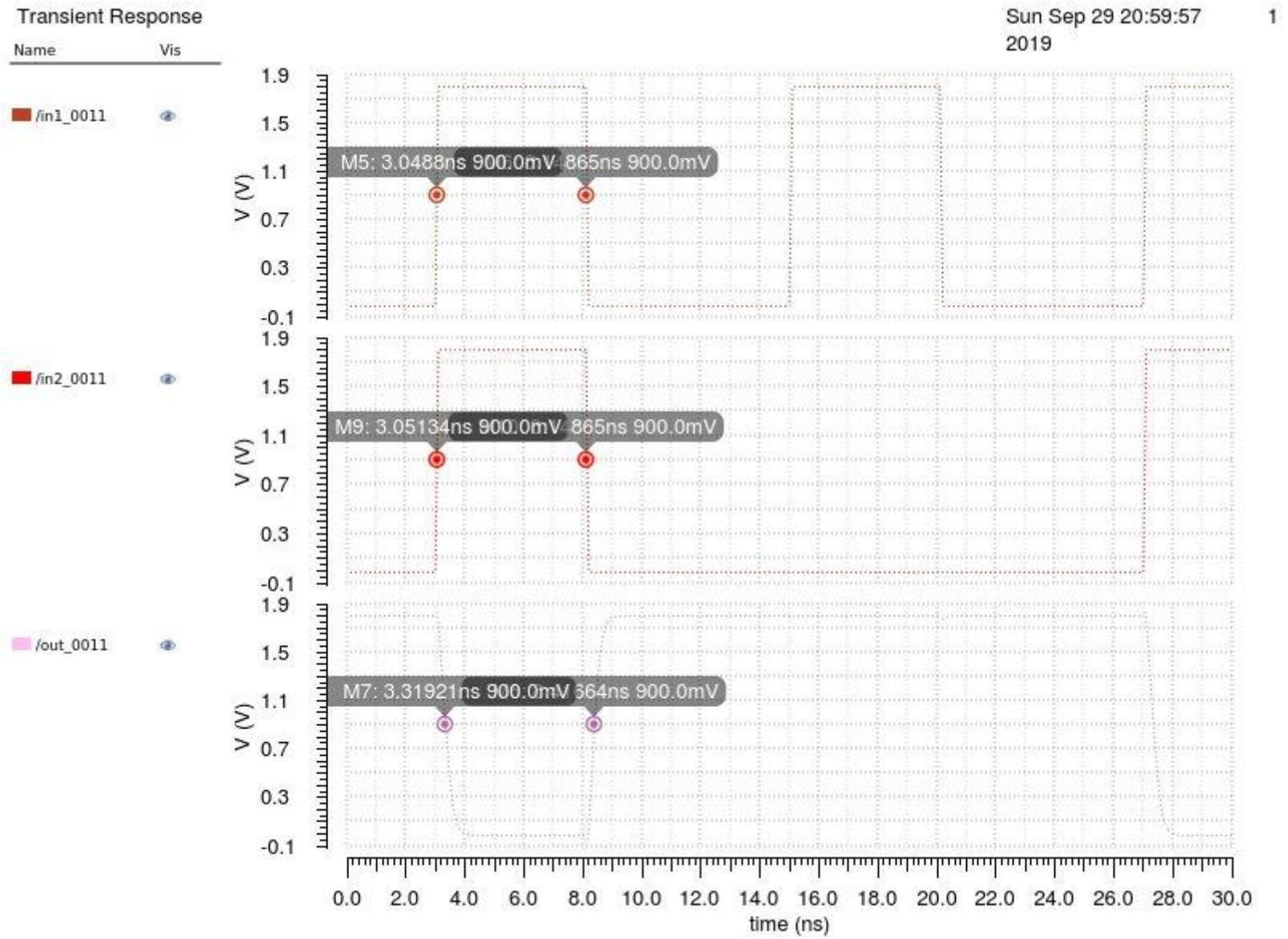


Delay Table for the Inverter:

	Delay		
	In	Out	Diff
Falling	3.376	3.057	0.319
Rising	8.478	8.15054	0.327
		%error	2.44

Inverter:	Power Consumption
Current DC:	0.789
Power DC:	1.42
Pulse Input:	Power Consumption
Current Pulse:	-2.253E-07
Power pulse:	-4.056E-07

NAND Delays:

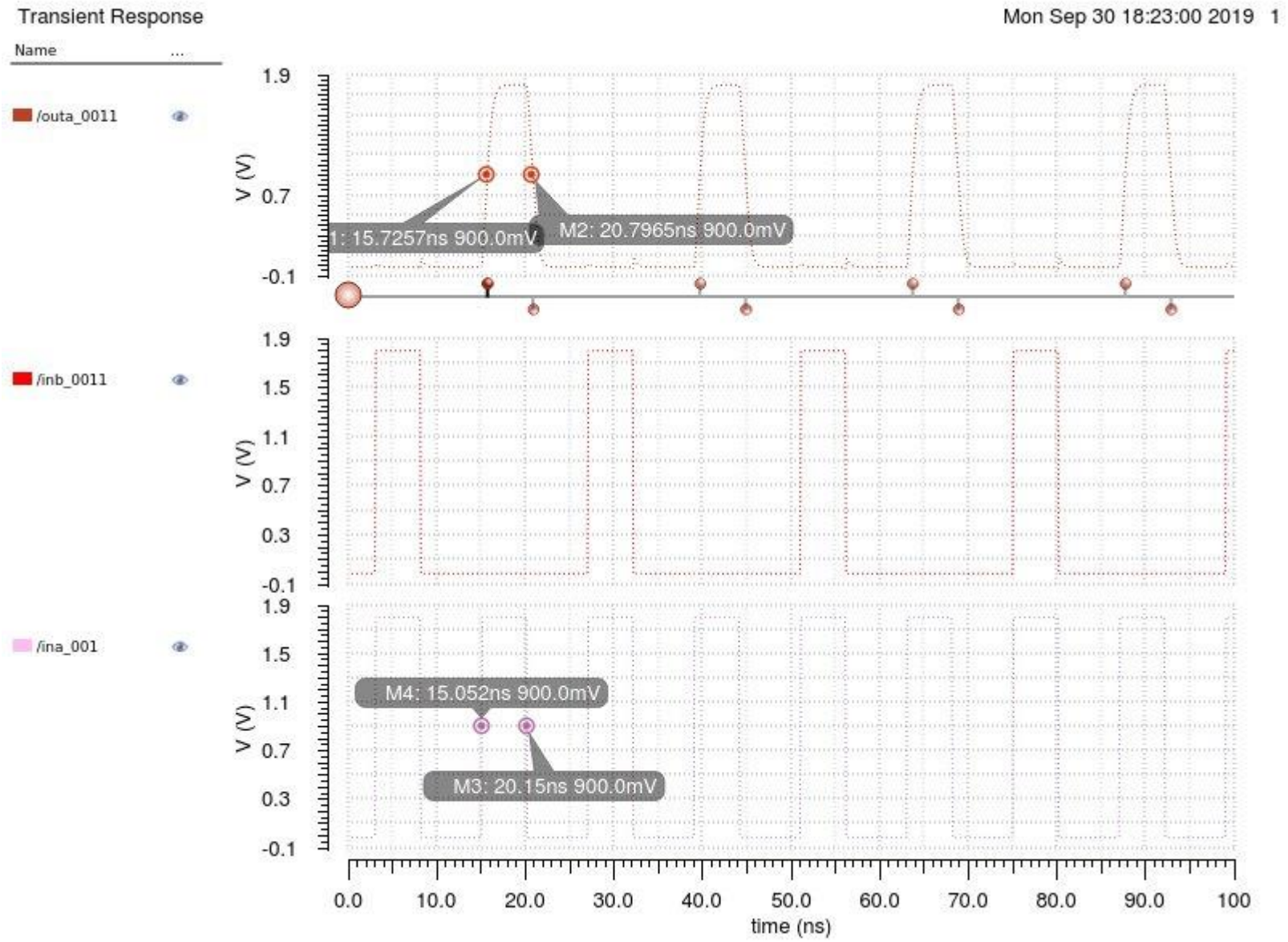

Transient Response
Sun Sep 29 20:59:57 2019
1
Name
Vis
/in1_0011
/in2_0011
/out_0011
M5: 3.0488ns 900.0mV 865ns 900.0mV
M9: 3.05134ns 900.0mV 865ns 900.0mV
M7: 3.31921ns 900.0mV 364ns 900.0mV
V (V)
1.9
1.5
1.1
0.7
0.3
-0.1
0.0 2.0 4.0 6.0 8.0 10.0 12.0 14.0 16.0 18.0 20.0 22.0 24.0 26.0 28.0 30.0
time (ns)

Delay Table for NAND:

	In1	out	diff
Falling	8.14865	8.41664	0.26799
Rising	3.0488	3.31921	0.27041
		%error	0.894937
	in2	out	diff
Falling	8.14865	8.41664	0.26799
Rising	3.05134	3.31921	0.26787
		%error	0.044778

Nand	
Current DC:	-6.71E-06
Power DC:	-1.20744E-05
In1 Pulse	-4.04E-07
Power1 pulse:	-3.18835E-07
In2 Pulse	-3.50E-07
Power2 pulse:	-1.69147E-07

XOR Delays:


Transient Response
Mon Sep 30 18:23:00 2019 1
Name
/outa_0011
/inb_0011
/ina_001
V (V)
1.9
0.7
-0.1
1.5
1.1
0.3
M1: 15.7257ns 900.0mV
M2: 20.7965ns 900.0mV
M4: 15.052ns 900.0mV
M3: 20.15ns 900.0mV
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
time (ns)

	In1	out	diff
Falling	20.151	20.7965	0.6455
Rising	15.0501	15.7257	0.6756
		%error	4.663052
	In1	out	diff
Falling	20.1483	20.9686	0.8203
Rising	15.0538	15.793	0.7392
		%error	10.97132

XOR	
Current DC:	-1.00E-05
Power DC:	-0.000018050
InA	
Current avg	-1.32E-07
Voltage avg	7.52E-01
power avg	-9.92E-08
InB	
Current Avg	-1.45E-07
Voltage avg	3.84E-01
power avg	-5.58E-08

Full Adder:

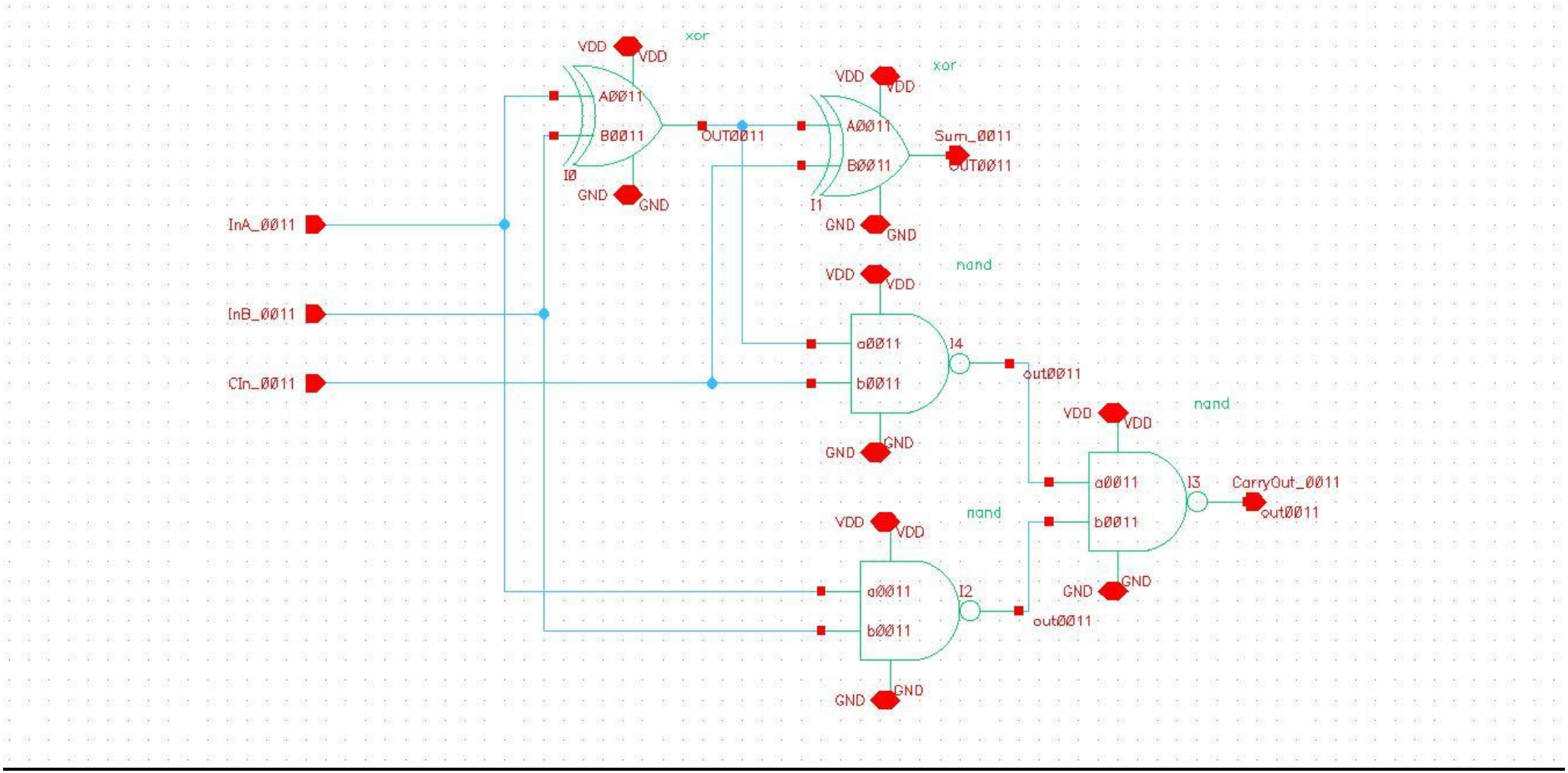


Figure 1Full adder Schematic

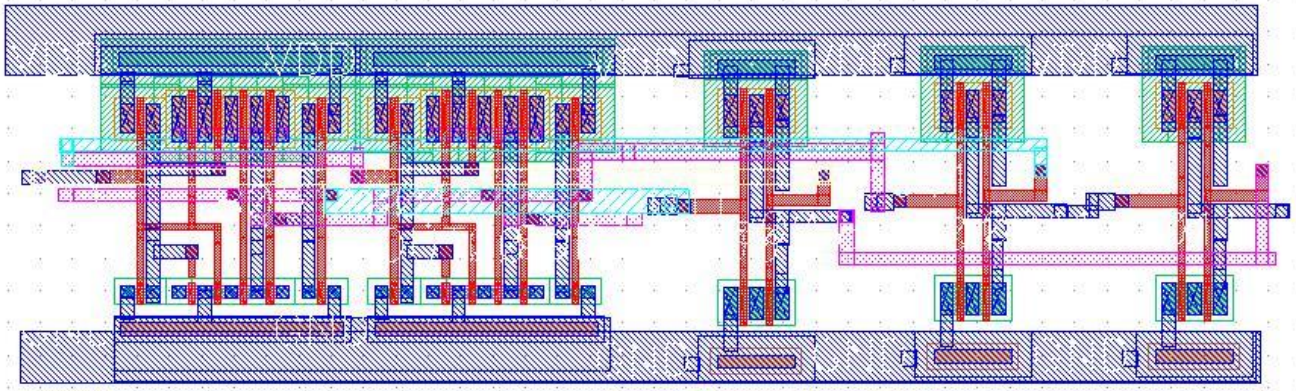
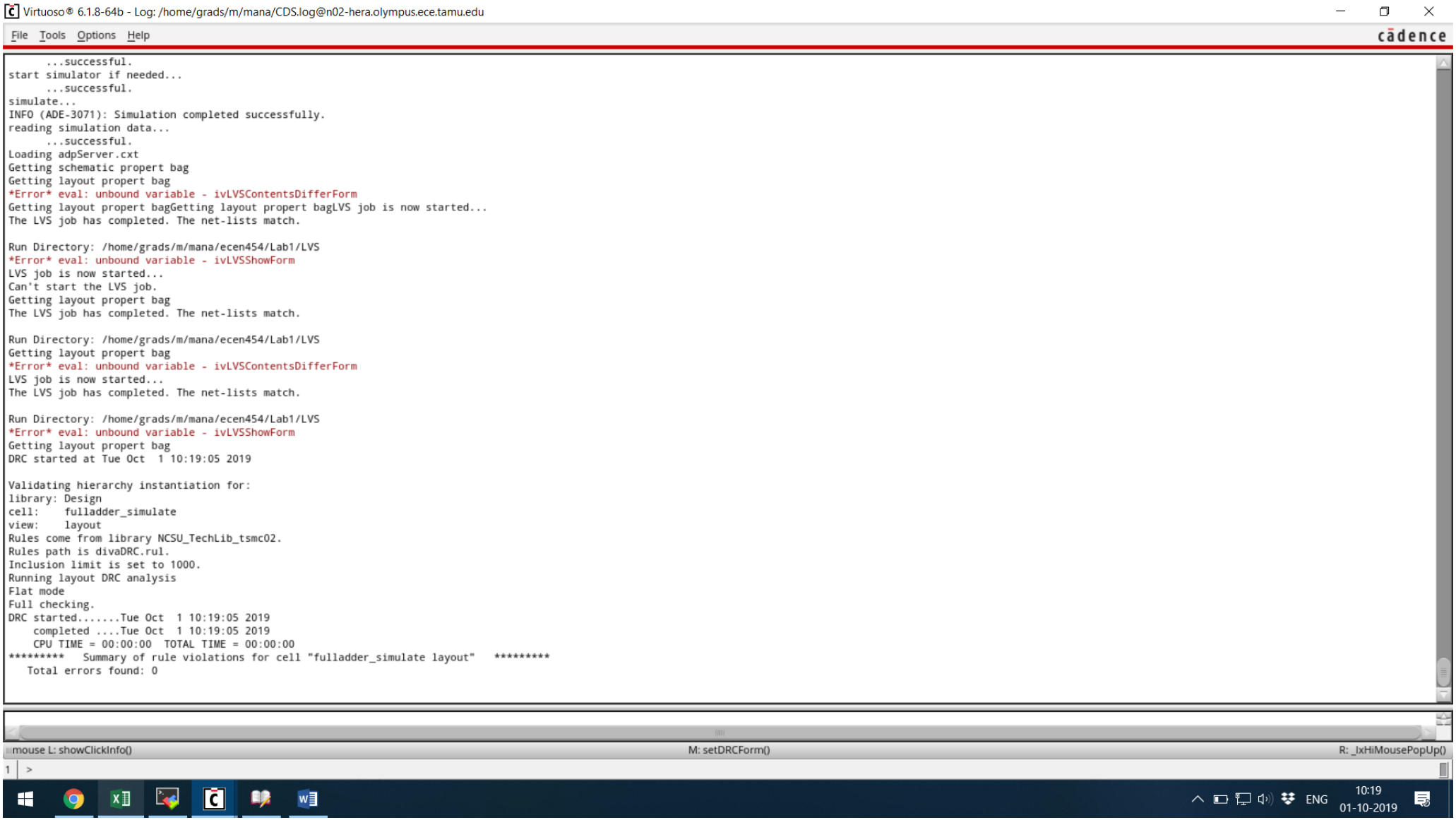


Figure 2Full adder Layout

DRC Results:


Virtuoso® 6.1.8-64b - Log: /home/grads/m/mana/CDS.log@n02-hera.olympus.ece.tamu.edu
File Tools Options Help
cadence
...successful.
start simulator if needed...
...successful.
simulate...
INFO (ADE-3071): Simulation completed successfully.
reading simulation data...
...successful.
Loading adpServer.cxt
Getting schematic propert bag
Getting layout propert bag
Error eval: unbound variable - ivLVSContentsDifferForm
Getting layout propert bagGetting layout propert bagLVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/grads/m/mana/ecen454/Lab1/LVS
Error eval: unbound variable - ivLVSShowForm
LVS job is now started...
Can't start the LVS job.
Getting layout propert bag
The LVS job has completed. The net-lists match.
Run Directory: /home/grads/m/mana/ecen454/Lab1/LVS
Getting layout propert bag
Error eval: unbound variable - ivLVSContentsDifferForm
LVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/grads/m/mana/ecen454/Lab1/LVS
Error eval: unbound variable - ivLVSShowForm
Getting layout propert bag
DRC started at Tue Oct 1 10:19:05 2019
Validating hierarchy instantiation for:
library: Design
cell: fulladder_simulate
view: layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Tue Oct 1 10:19:05 2019
completed ....Tue Oct 1 10:19:05 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
********* Summary of rule violations for cell "fulladder_simulate layout" *********
Total errors found: 0
mouse L: showClickInfo()
M: setDRCForm()
R: _lxHiMousePopUp()
1 >
ENG
10:19
01-10-2019

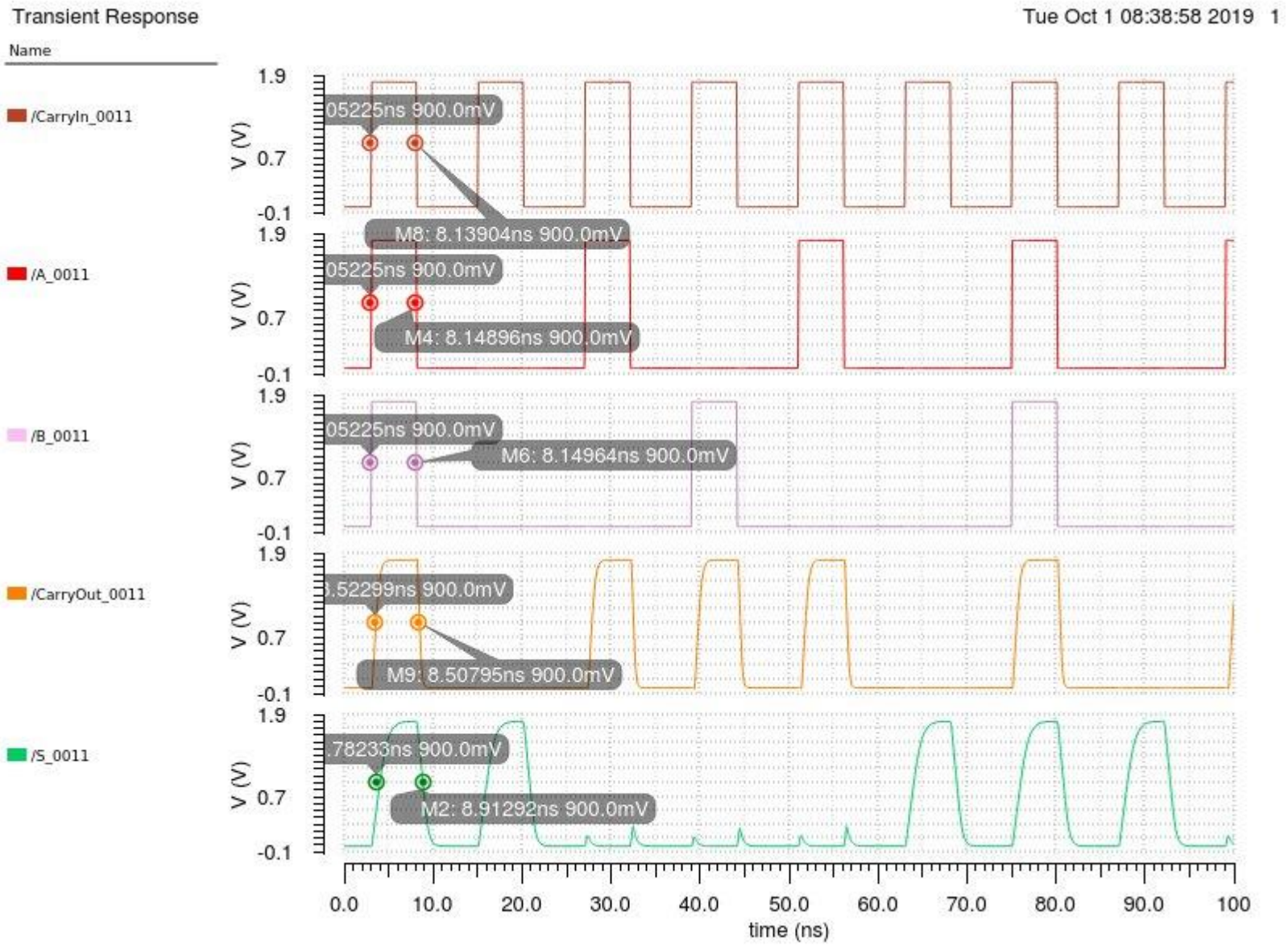
LVS Results:

```
@(#)$CDS: LVS version 6.1.8-64b 07/16/2019 19:56 (sjfhw317) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t
/home/grads/m/mana/ecen454/Lab1/LVS/layout /home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
       count
        25              nets
        7               terminals
        18              pmos
        18              nmos

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
       count
        25              nets
        7               terminals
        18              pmos
        18              nmos


    Terminal correspondence points
    N23       N2        CIn_0011
    N20       N3        CarryOut_0011
    N18       N0        GND
    N21       N8        InA_0011
    N24       N7        InB_0011
    N19       N5        Sum_0011
    N22       N9        VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
```

```
                              instances
        un-matched            0       0
        rewired               0       0
        size errors           0       0
        pruned                0       0
        active                36      36
        total                 36      36

                                nets
        un-matched            0       0
        merged                0       0
        pruned                0       0
        active                25      25
        total                 25      25

                              terminals
        un-matched            0       0
        matched but
        different type        0       0
        total                 7       7


Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout

devbad.out:
```

```
netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Full Adder Delays:



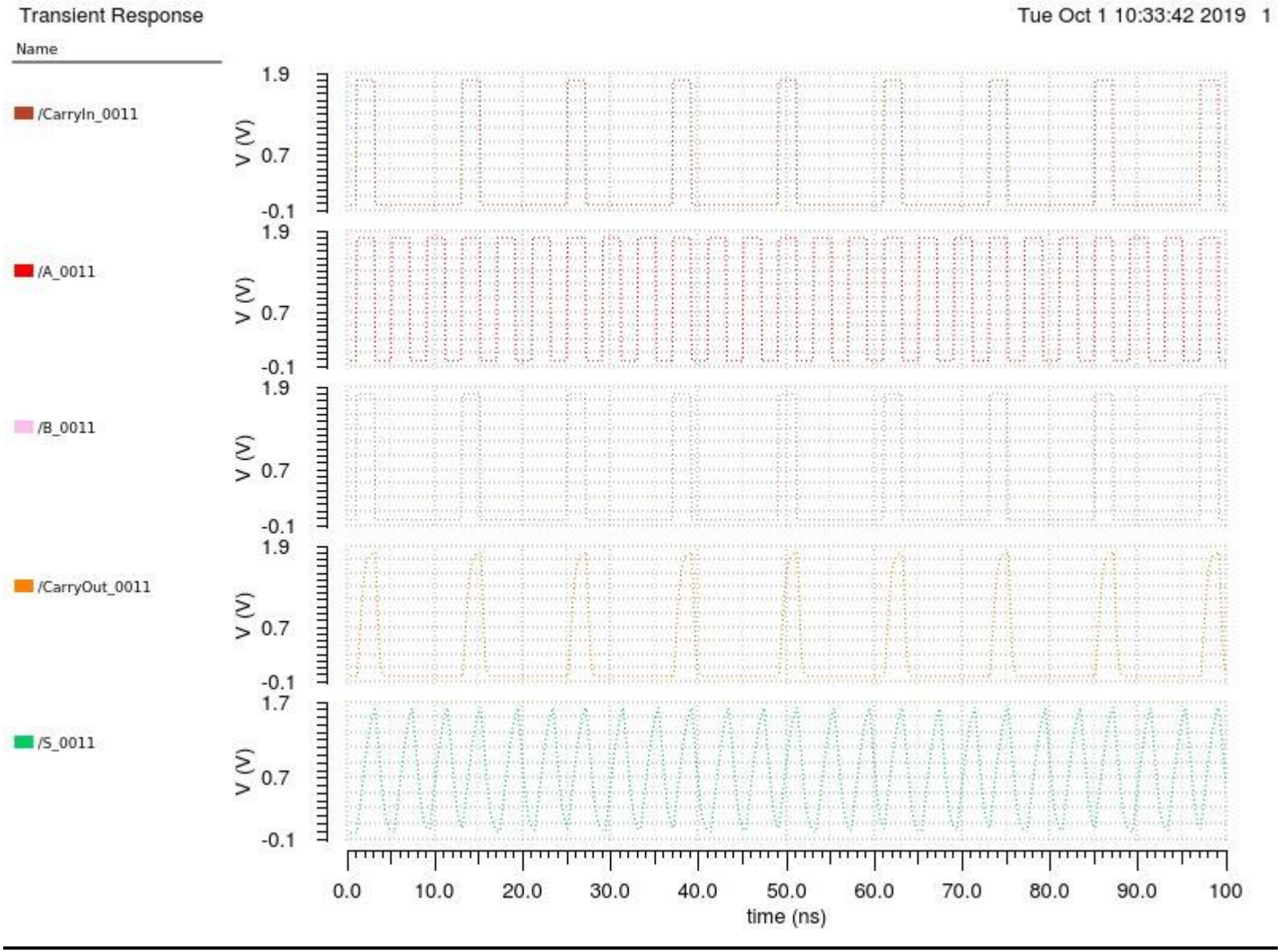
	In1	out	diff
Falling	8.14896	8.91292	0.76396
Rising	3.05225	3.78233	0.73008
		%error	4.640587
	In2	out	diff
Falling	8.14896	8.91292	0.76396
Rising	3.05225	3.78233	0.73008
		%error	4.640587
	CarryIn	Out	diff
Falling	8.13904	8.91292	0.77388
Rising	3.05225	3.78233	0.73008
		%error	5.999343

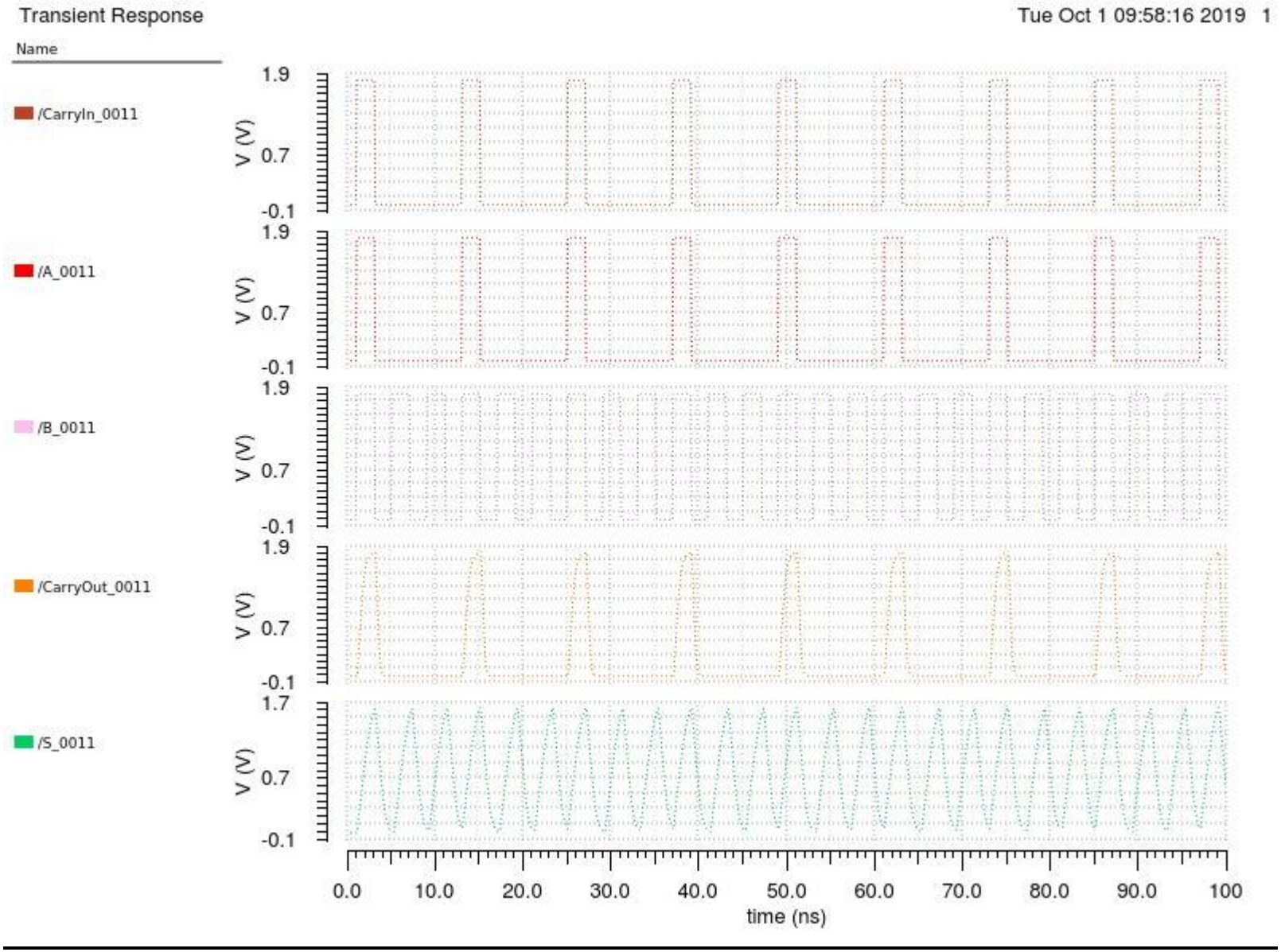
Full Adder	
DC Current:	-2.83E-05
DC Power:	-5.09E-05
InA	
Current:	-2.53E-07
Power:	-9.71E-08
InB	

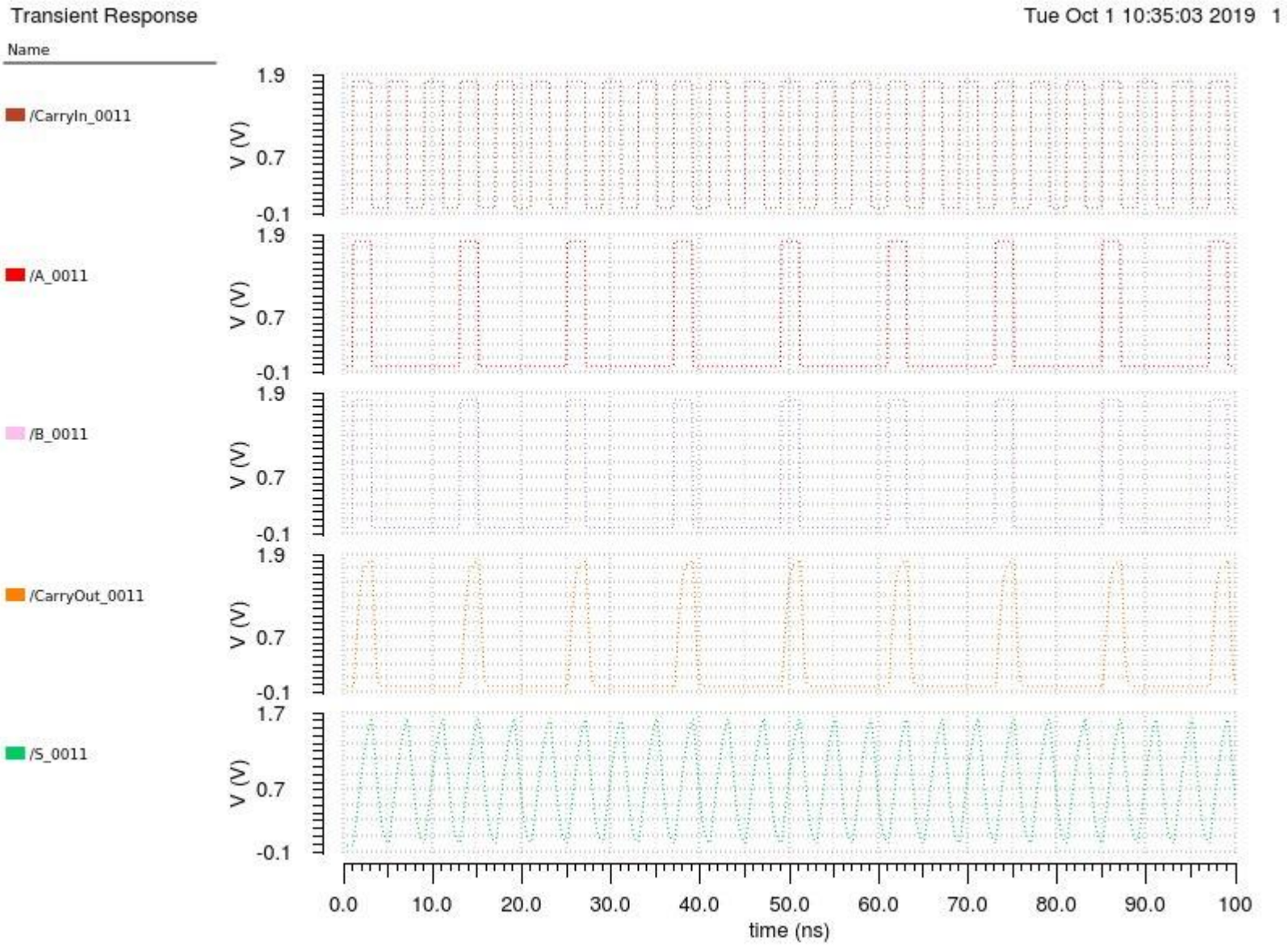
Current:	-2.12E-07
Power:	-5.82E-08
Carry In	
Current:	3.89E-08
Power:	2.92E-08

Maximum Frequency of fulladder operation:

Max Frequency	
InA	0.25Ghz
InB	0.25Ghz
CarryIn	0.25Ghz
Full Adder	0.25Ghz


Transient Response
Tue Oct 1 10:33:42 2019 1
Name
/CarryIn_0011
/A_0011
/B_0011
/CarryOut_0011
/S_0011
V (V)
1.9
0.7
-0.1
1.7
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
time (ns)


Transient Response
Tue Oct 1 09:58:16 2019 1
Name
/CarryIn_0011
/A_0011
/B_0011
/CarryOut_0011
/S_0011
1.9
0.7
-0.1
1.7
V (V)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
time (ns)


Transient Response
Tue Oct 1 10:35:03 2019 1
Name
/CarryIn_0011
/A_0011
/B_0011
/CarryOut_0011
/S_0011
1.9
0.7
-0.1
V (V)
1.7
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
time (ns)