

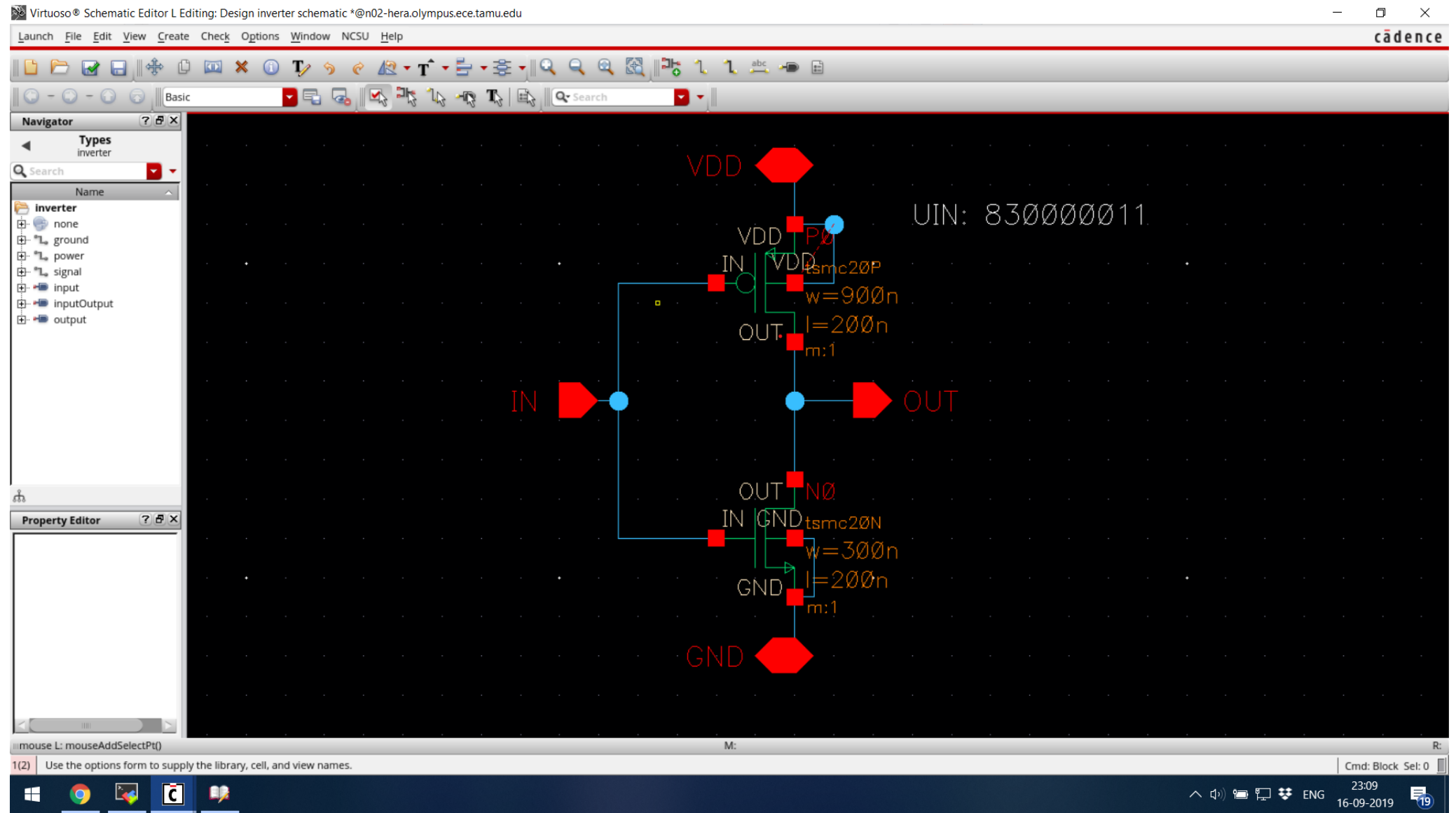
ECEN 714: Submission for LAB 2

Manav Gurumoorthy
830000011

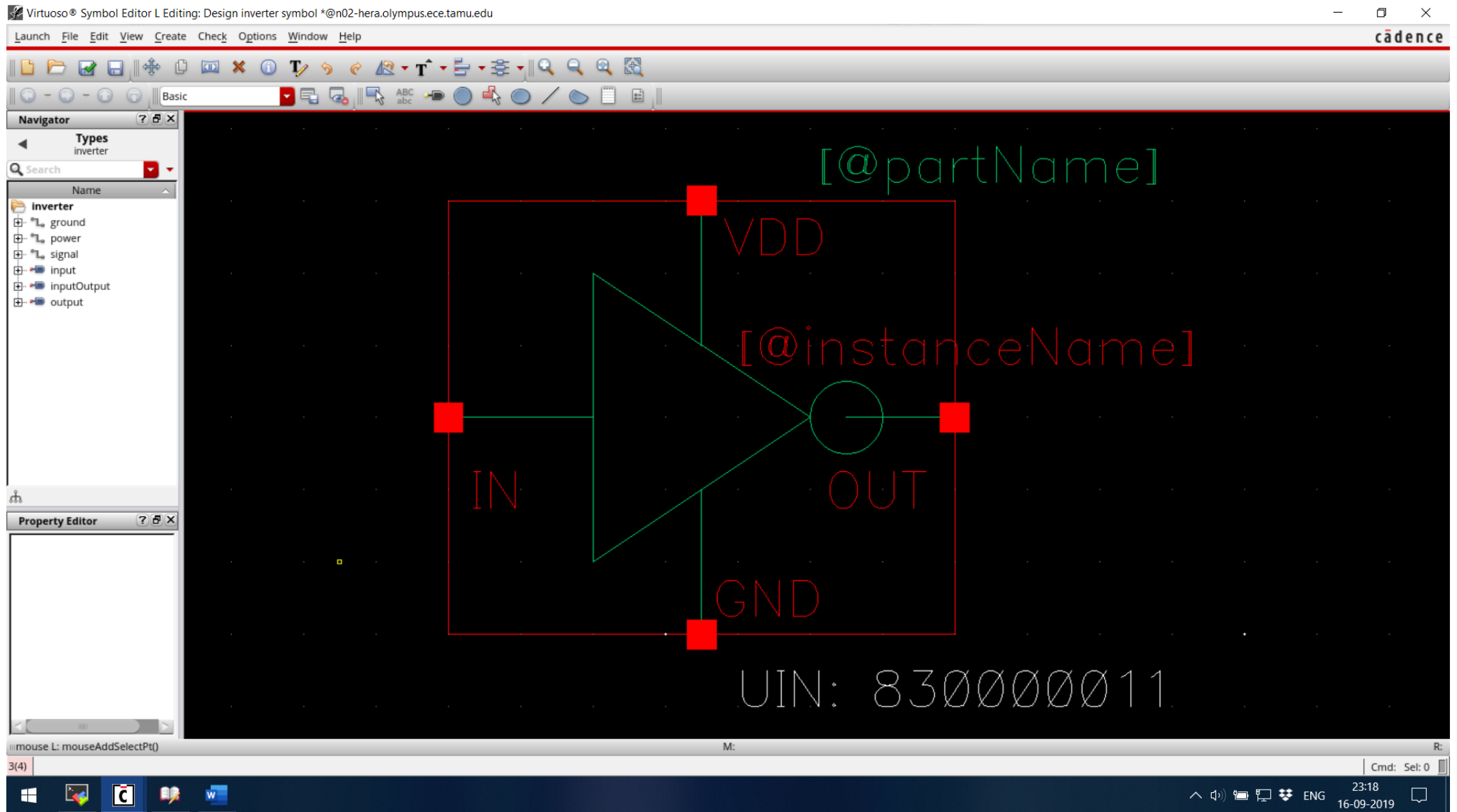
Contents (Schematic, Symbol, Layout, DRC and LVS)

1. Inverter
2. Nand
3. XOR

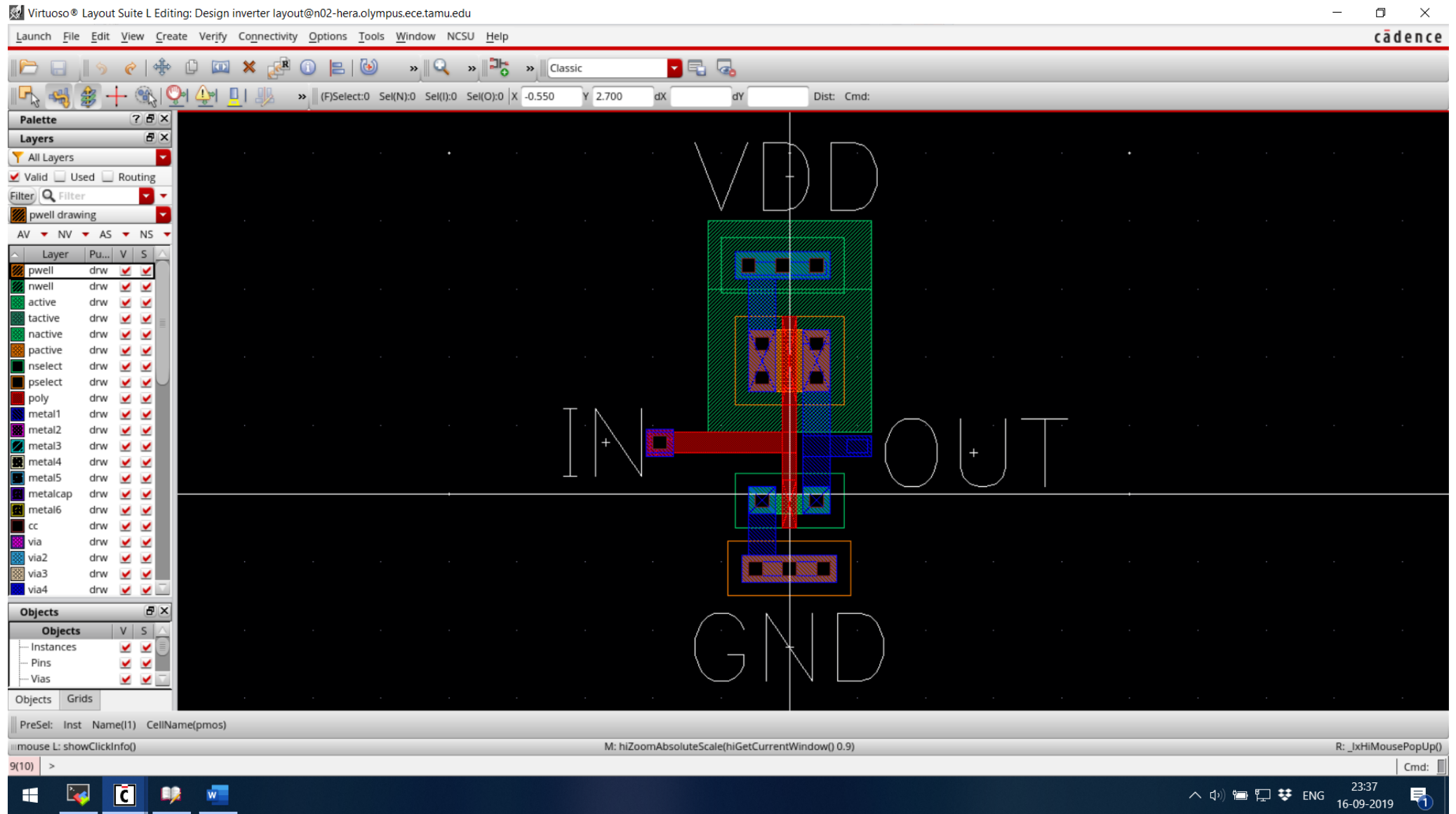
Inverter schematic:



Symbol for Inverter:



Layout for Inverter:



DRC Results for Inverter:

Virtuoso® 6.1.8-64b - Log: /home/grads/m/mana/CDS.log@n02-hera.olympus.ece.tamu.edu

FileToolsOptionsHelp

cadence

```
Optimizing rules...
removing unused task: nwellResEdge = geomGetEdge(nwellRes coincident nwell)
removing unused task: polyResEdge = geomGetEdge(polyRes coincident poly)
removing unused task: sGateWidthCheckEdge = geomGetEdge(sGateWidthCheck)
removing unused task: metalCapEdge = geomGetEdge(metalcap)
removing unused task: padEdge = geomGetEdge(pad)
removing unused task: ccEdge = geomGetEdge(cc)
removing unused task: gselectEdge = geomGetEdge(gselect)
removing unused task: gwellEdge = geomGetEdge(gwell)
removing unused task: nwellRes = geomButting(geomAnd(res_id nwell) nBulk (keep == 2))
removing unused task: polyRes = geomButting(geomAndNot(geomAnd(res_id poly) polySRes) fieldPoly (keep == 2))
removing unused task: sGateWidthCheck = geomSize(geomSize(geomAnd(Gate sblock) -2.9) 2.9)
removing unused task: NwPdiod = geomAnd(dio_id geomOutside(nwell pNotOhmic))
removing unused task: PNdiode = geomAnd(dio_id geomOutside(pNotOhmic poly))
removing unused task: NPdiode = geomAnd(dio_id geomOutside(nNotOhmic poly))
removing unused task: m6m5Cap = geomAnd(geomAnd(metal5 metal6) cap_id)
removing unused task: m5m4Cap = geomAnd(geomAnd(metal4 metal5) cap_id)
removing unused task: m4m3Cap = geomAnd(geomAnd(metal3 metal4) cap_id)
removing unused task: m3m2Cap = geomAnd(geomAnd(metal2 metal3) cap_id)
removing unused task: m2m1Cap = geomAnd(geomAnd(metal1 metal2) cap_id)
removing unused task: m1sCap = geomAnd(geomAndNot(metal1 poly) cap_id)
removing unused task: m1pCap = geomAnd(geomAnd(poly metal1) cap_id)
removing unused task: pChannelTran = geomAndNot(pChannelTran hvpChannelTran)
removing unused task: hvpChannelTran = geomAnd(pChannelTran tactive)
removing unused task: nChannelTran = geomAndNot(nChannelTran hvnChannelTran)
removing unused task: hvnChannelTran = geomAnd(nChannelTran tactive)
removing unused task: pChannelCap = geomButting(pChannel pDiff (keep == 1))
removing unused task: nChannelCap = geomButting(nChannel nDiff (keep == 1))
removing unused task: pChannelTran = geomButting(pChannel pDiff (keep == 2))
removing unused task: nChannelTran = geomButting(nChannel nDiff (keep == 2))
removing unused task: Space = geomNot(geomOr(active poly))
removing unused task: pChannel = geomAnd(pNotOhmic poly)
removing unused task: nChannel = geomAnd(nNotOhmic poly)
removing unused task: dio_id = geomOr("dio_id")
removing unused task: cap_id = geomOr("cap_id")
removing unused task: nolpe = geomOr("nolpe")
removing unused task: bkgnd = geomBkgnd()
warn: Duplicate check "(SCM05 Rule 20.9) sblock enclosure of poly resistor: 0.20 um" is being ignored.
warn: Duplicate check "(SCM05 Rule 26.2) metal5 width: 0.30 um" is being ignored.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Sep 16 23:22:39 2019
completed ....Mon Sep 16 23:22:39 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "inverter layout" *****
Total errors found: 0
```

mouse L: showClickInfo()M: setDRCForm()R: _lxHiMousePopUp()

1 >

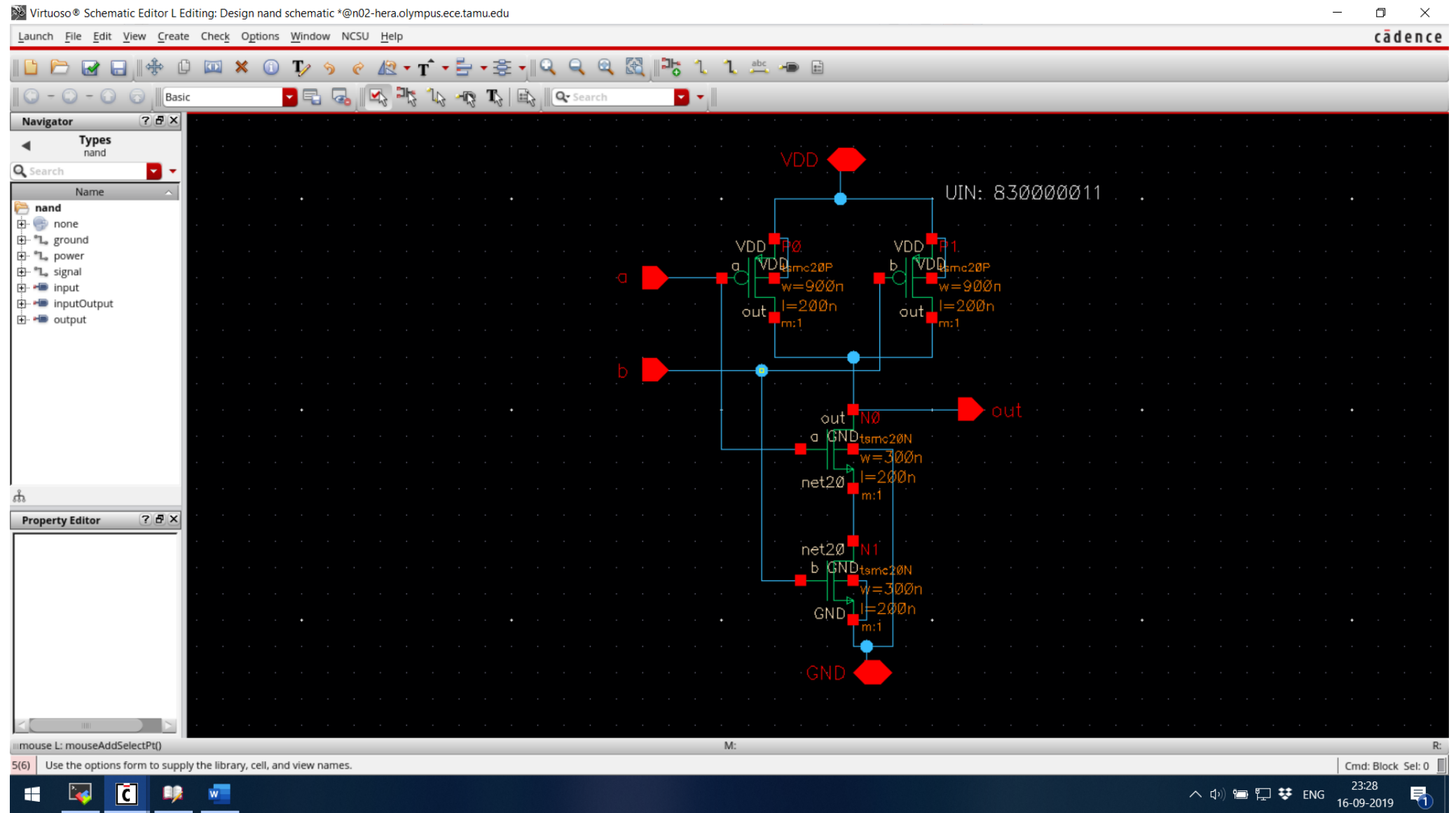
23:23
16-09-2019

LVS Results for the Inverter :

```
@(#) $CDS: LVS version 6.1.8-64b 10/01/2018 19:50 (ip-172-18-22-57) $
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t /home/grads/m/mana/ecen454/Lab1/LVS/layout
/home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
  Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
    count
      4          nets
      4          terminals
      1          pmos
      1          nmos
  Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
    count
      4          nets
      4          terminals
      1          pmos
      1          nmos
  Terminal correspondence points
    N0          N3          GND
    N2          N0          IN
    N1          N2          OUT
    N3          N1          VDD
Devices in the netlist but not in the rules:
  pcapacitor
Devices in the rules but not in the netlist:
  cap nfet pfet nmos4 pmos4
The net-lists match.
                                layout schematic
                                instances
un-matched                    0          0
rewired                        0          0
size errors                    0          0
pruned                         0          0
active                         2          2
total                          2          2
                                nets
un-matched                     0          0
merged                         0          0
pruned                         0          0
active                         4          4
total                          4          4
                                terminals
un-matched                     0          0
matched but
different type                 0          0
total                          4          4
Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
```

```
prunedev.out:
audit.out:
Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

NAND Schematic:



Symbol for NAND:

Virtuoso® Symbol Editor L Editing: Design nand symbol *@n02-hera.olympus.ece.tamu.edu

Launch File Edit View Create Check Options Window Help

Basic

Navigator

Types
nand

Search

Name

- nand
- ground
- power
- signal
- input
- inputOutput
- output

Property Editor

6(7) Click on text to edit or press ESC to cancel.

M: schShiftCmdOption()

R: schShiftCmdOption()

Cmd: Text Sel: 0

23:31
16-09-2019

ENG

cadence

[@partName]

VDD

a

b

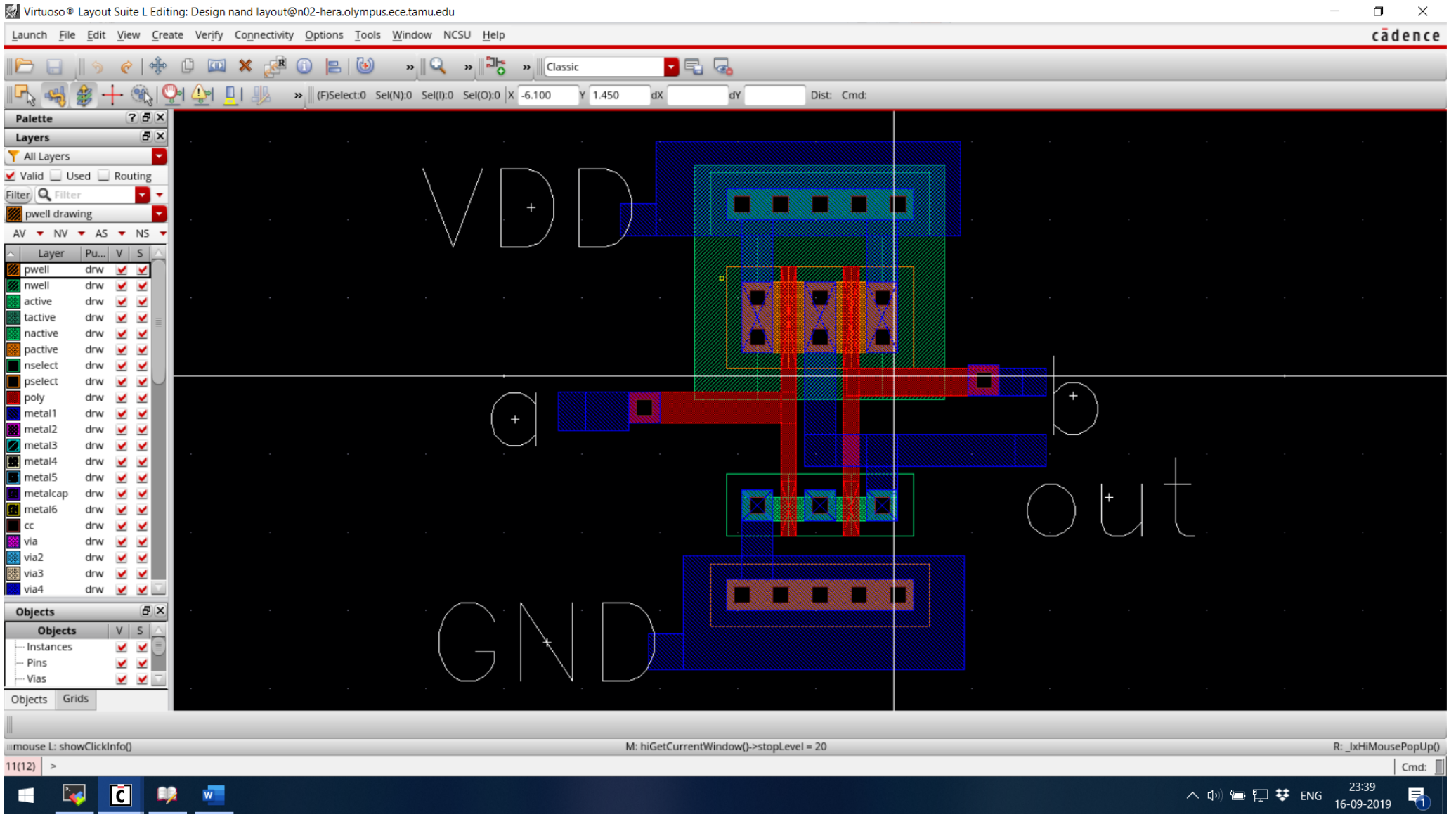
[@instanceName]

out

GND

UIN: 830000011

Layout for NAND:



DRC Results for NAND:

Virtuoso® 6.1.8-64b - Log: /home/grads/m/mana/CDS.log@n02-hera.olympus.ece.tamu.edu

File Tools Options Help

cadence

```
*WARNING* (SCH-4008): No cell name(s) given in the Create Block form. Update the Cells field to create one or more cell names.  
*WARNING* (SCH-4008): No cell name(s) given in the Create Block form. Update the Cells field to create one or more cell names.
```

```
Getting schematic proper bag  
Getting schematic proper bag  
Getting schematic proper bag  
Getting layout proper bag  
Getting layout proper bag  
Getting layout proper bag  
Getting layout proper bag  
Getting schematic proper bag  
Getting schematic proper bag  
Getting layout proper bag
```

DRC started at Mon Sep 16 23:40:51 2019

```
Validating hierarchy instantiation for:  
library: Design  
cell: nand  
view: layout
```

Rules come from library NCSU_TechLib_tsmc02.

Rules path is divaDRC.rul.

Inclusion limit is set to 1000.

Running layout DRC analysis

Flat mode

Full checking.

DRC started.....Mon Sep 16 23:40:51 2019

completedMon Sep 16 23:40:52 2019

CPU TIME = 00:00:00 TOTAL TIME = 00:00:01

```
***** Summary of rule violations for cell "nand layout" *****
```

Total errors found: 0

DRC started at Mon Sep 16 23:41:14 2019

```
Validating hierarchy instantiation for:  
library: Design  
cell: nand  
view: layout
```

Rules come from library NCSU_TechLib_tsmc02.

Rules path is divaDRC.rul.

Inclusion limit is set to 1000.

Running layout DRC analysis

Flat mode

Full checking.

DRC started.....Mon Sep 16 23:41:14 2019

completedMon Sep 16 23:41:14 2019

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

```
***** Summary of rule violations for cell "nand layout" *****
```

Total errors found: 0

mouse L: showClickInfo()

M: setDRCForm()

R: _IxDiMousePopUp()

1 >



23:41
16-09-2019

LVS for NAND:

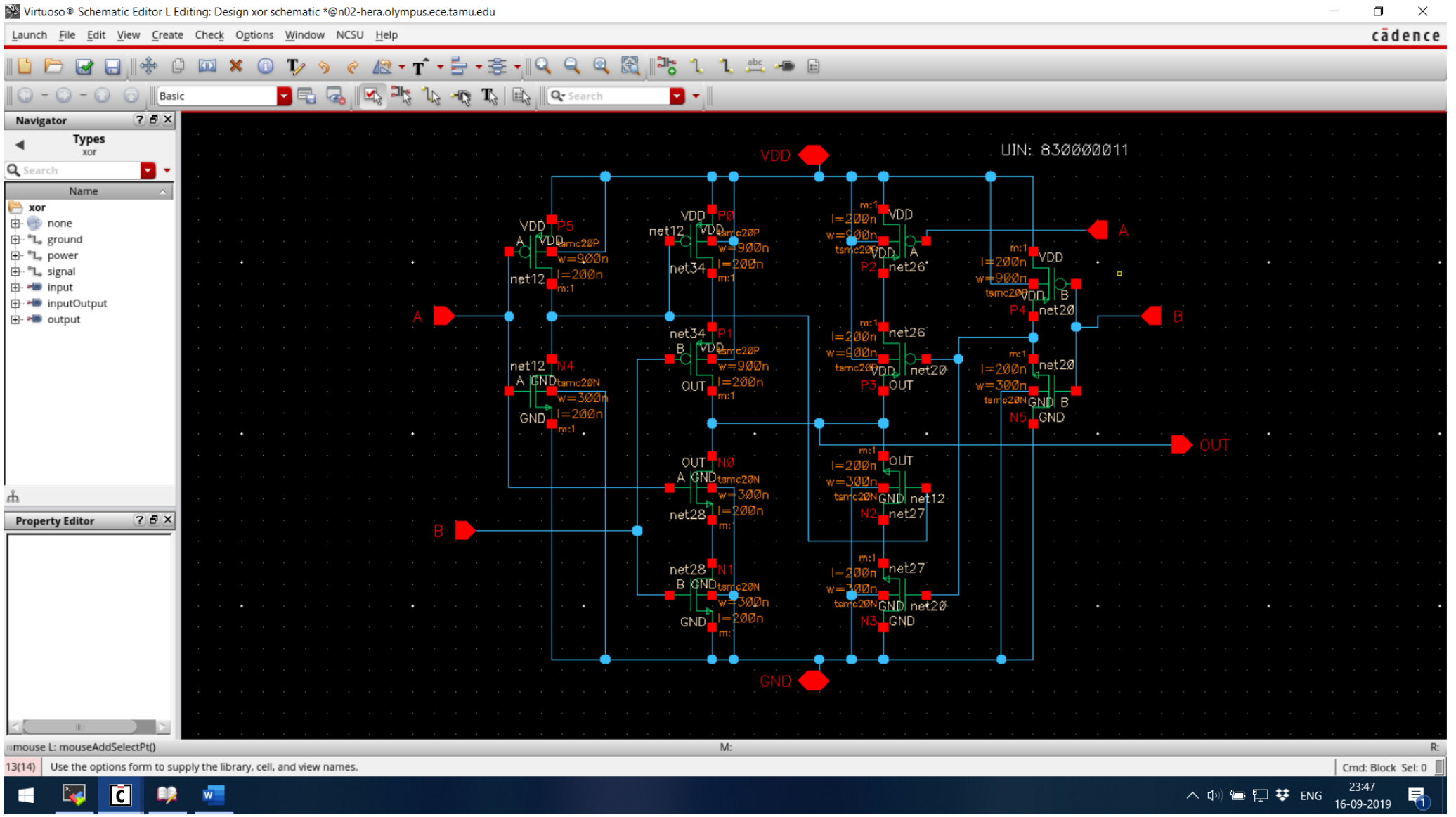
```
@(#)SCDS: LVS version 6.1.8-64b 10/01/2018 19:50 (ip-172-18-22-57) $
Command line: /opt/coe/cadence/IC618/tools.lnx86/dflI/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t /home/grads/m/mana/ecen454/Lab1/LVS/layout
/home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
  Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
    count
      6          nets
      5          terminals
      2          pmos
      2          nmos
  Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
    count
      6          nets
      5          terminals
      2          pmos
      2          nmos
  Terminal correspondence points
  N3      N3      GND
  N5      N5      VDD
  N2      N2      a
  N1      N1      b
  N4      N4      out
Devices in the netlist but not in the rules:
  pcapacitor
Devices in the rules but not in the netlist:
  cap nfet pfet nmos4 pmos4
The net-lists match.

              layout schematic
              instances
un-matched    0      0
rewired       0      0
size errors   0      0
pruned        0      0
active        4      4
total         4      4
              nets
un-matched    0      0
merged        0      0
pruned        0      0
active        6      6
total         6      6
              terminals
un-matched    0      0
matched but
different type 0      0
total         5      5

Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
```

```
prunenet.out:
prunedev.out:
audit.out:
Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Schematic for XOR:



Symbol for XOR:

Virtuoso® Symbol Editor L Editing: Design xor symbol *@n02-hera.olympus.ece.tamu.edu

Launch File Edit View Create Check Options Window Help

Basic

Navigator

Types
xor

Search

Name

- xor
- ground
- power
- signal
- input
- inputOutput
- output

Property Editor

14(15)

14(15)

mouse L: mouseAddSelectPt()

M:

R:

Cmd: Sel: 0

23:48
16-09-2019

ENG

cadence

[@partName]

VDD

A

B

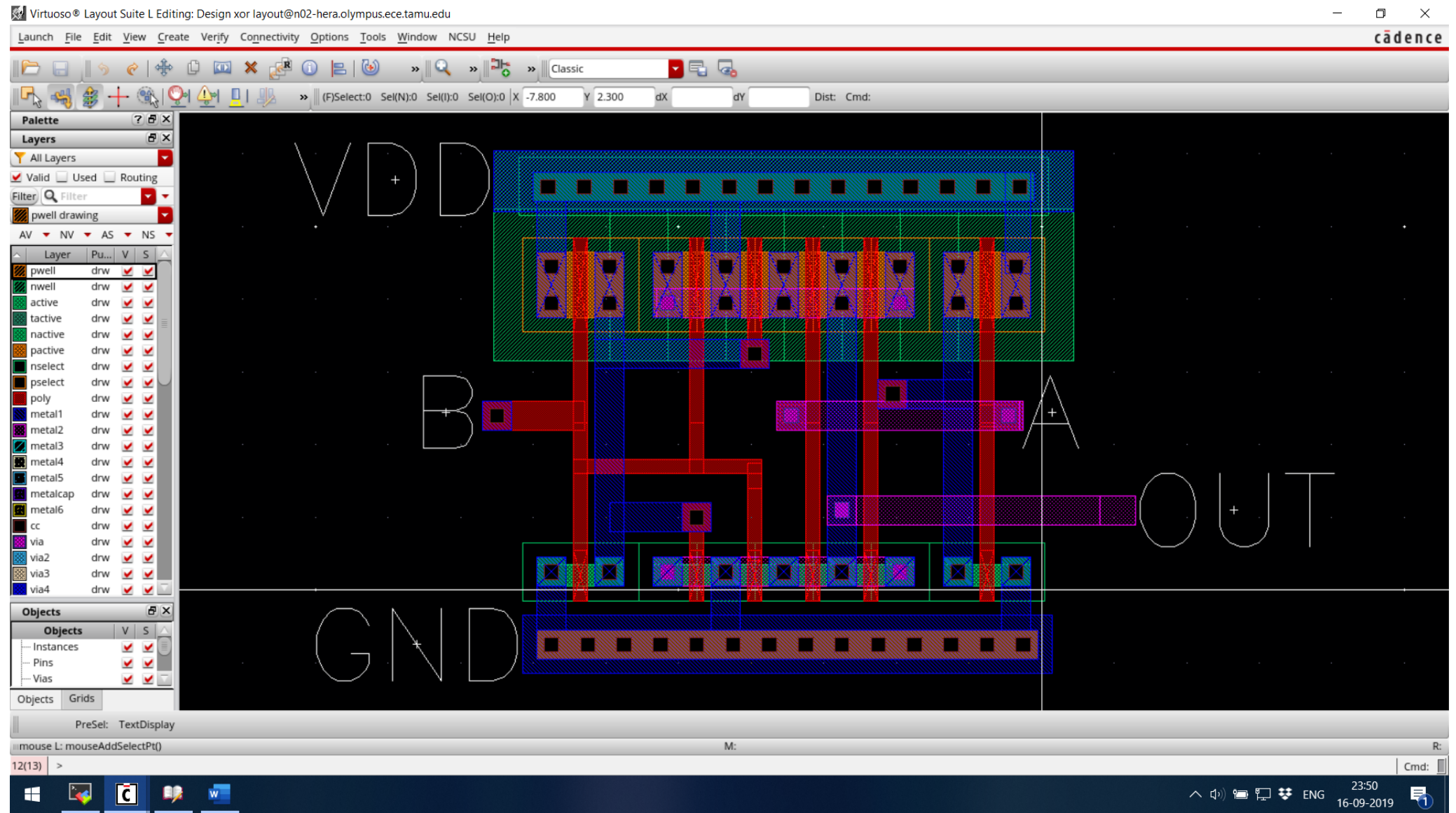
OUT

[@instanceName]

GND

UIN: 830000011

Layout for XOR:



DRC Results for XOR:

Virtuoso® 6.1.8-64b - Log: /home/grads/m/mana/CDS.log@n02-hera.olympus.ece.tamu.edu

File Tools Options Help

cadence

```
Flat mode
Full checking.
DRC started.....Mon Sep 16 23:40:51 2019
  completed ....Mon Sep 16 23:40:52 2019
  CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "nand layout" *****
  Total errors found: 0

DRC started at Mon Sep 16 23:41:14 2019

Validating hierarchy instantiation for:
library: Design
cell:    nand
view:    layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Sep 16 23:41:14 2019
  completed ....Mon Sep 16 23:41:14 2019
  CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "nand layout" *****
  Total errors found: 0

Getting layout propert bag
Getting layout propert bag
Getting schematic propert bag
Getting schematic propert bag
DRC started at Mon Sep 16 23:51:58 2019

Validating hierarchy instantiation for:
library: Design
cell:    xor
view:    layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Sep 16 23:51:58 2019
  completed ....Mon Sep 16 23:51:58 2019
  CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "xor layout" *****
  Total errors found: 0
```

mouse L: showClickInfo()

M: setDRCForm()

R: _lxHiMousePopUp()

1 >



LVS for XOR:

```
@(#)SCDS: LVS version 6.1.8-64b 10/01/2018 19:50 (ip-172-18-22-57) $
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t /home/grads/m/mana/ecen454/Lab1/LVS/layout
/home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
  Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
    count
    11          nets
    5          terminals
    6          pmos
    6          nmos
  Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
    count
    11          nets
    5          terminals
    6          pmos
    6          nmos
  Terminal correspondence points
  N9      N2      A
  N8      N5      B
  N6      N9      GND
  N7      N6      OUT
  N10     N4      VDD
Devices in the netlist but not in the rules:
  pcapacitor
Devices in the rules but not in the netlist:
  cap nfet pfet nmos4 pmos4
The net-lists match.

              layout  schematic
              instances
un-matched    0      0
rewired       0      0
size errors   0      0
pruned        0      0
active        12     12
total         12     12
              nets
un-matched    0      0
merged        0      0
pruned        0      0
active        11     11
total         11     11
              terminals
un-matched    0      0
matched but
different type 0      0
total         5      5

Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
```

```
prunenet.out:
prunedev.out:
audit.out:
Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```