

ECEN 714: Submission for LAB 6

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Contents (Cruise control and test bench file)

Cruise Control (Verilog)

```
module cruise_control(input clk, input reset, input throttle,
input set_0011, input accel, input coast, input cancel, input resume,
input brake,output [7:0] speed, output [7:0] cruisespeed,
output cruisecontrol);
reg [7:0] speed;
reg [7:0] cruisespeed;
reg cruisecontrol;
reg [2:0]state, nextstate;
parameter init= 3'b000, acc = 3'b001, dec = 3'b010, cruise = 3'b011,
brake_s = 3'b100, cancel_s = 3'b101, resume_s = 3'b110, cruise_s = 3'b111;

always @(posedge clk)
begin
    if (reset == 1)
        state = init;
    else
        state = nextstate;
case(state)
    init : begin
        nextstate = init;
        speed = 8'b000000000;
        cruisespeed = 8'b00000000;
        cruisecontrol = 1'b0;
        if (throttle)nextstate = acc;
    end

    acc : begin
        if(throttle)begin
            speed = speed + 2'b10;
            nextstate =acc;
        end
        if (set_0011 && speed > 8'b00101000)begin
            cruisespeed = speed;
            cruisecontrol = 1'b1;
            nextstate = cruise;
        end
    end
    else if(throttle == 0)
        nextstate = dec;
    end

    dec : begin
```

```

if(throttle == 0) begin
    nextstate = dec;
    speed = speed -1'b1;
end
if (set_0011 && speed> 8'b00101000) begin
    cruisespeed = speed;
    cruisecontrol = 1'b1;
    nextstate = cruise;
end
else if( throttle == 1)
    nextstate = acc;
end

cruise: begin
    if(throttle)
        speed = speed + 2'b10;
    if(accel) begin
        cruisespeed = cruisespeed + 8'b00000001;
        nextstate = cruise_s;
    end
    if (coast && cruisespeed>8'b00101000) begin
        cruisespeed = cruisespeed - 8'b00000001;
        nextstate = cruise_s;
    end
    if (cancel) begin
        nextstate = acc;
        cruisecontrol = 1'b0;
    end
    if (brake)begin
        speed = speed -2'b10;
        cruisecontrol = 1'b0;
        nextstate = brake_s;
    end
end

brake_s:begin
    speed = speed - 2'b10;
    nextstate = brake_s;
    if (resume && speed!= 8'b00000000)begin
        nextstate = resume_s;
        cruisecontrol = 1'b1;
    end
end
end

```

```

        cruise_s: begin
            if (accel)begin
                cruisespeed = cruisespeed + 1;
                nextstate = cruise;
            end
            else begin
                if (coast && cruisespeed> 8'b00101000)begin
                    cruisespeed = cruisespeed - 1;
                end
                nextstate = cruise;
            end
        end

        resume_s: begin
            if(speed < cruisespeed)
                speed = speed +1;
            else
                nextstate = cruise;
            end
        end

        default: nextstate = init;
    endcase
end
endmodule

```

Testbench

```

module testbench();
    reg clk, reset, throttle, set_0011, accel, coast, cancel,
    resume, brake;

    cruise_control dut( clk, reset, throttle, set_0011, accel, coast, cancel,
    resume, brake, speed, cruisespeed, cruisecontrol );

    initial begin
        clk =1;
        reset =0;
        throttle =0; set_0011 = 0; accel= 0; coast =0; cancel = 0; resume = 0; brake =0;

        #10 reset =1;
        #10 reset =0;
    end
endmodule

```

```
#20 throttle = 1;
#180 set_0011 = 1;
#10 set_0011 = 0;
#10 throttle = 0;
#170 throttle = 1;
#190 set_0011 = 1;
#10 set_0011 = 0;
#30 throttle = 0;
#150 brake = 1;
#160 brake = 0;
#100 resume = 1;
#10 resume = 0;
#200 accel=1;
#10 accel =0;
#10 accel =1;
#10 accel =0;
#10 accel =1;
#10 accel =0;
#10 accel =1;
#10 accel =0;
#10 accel =1;
#10 accel =0;
#60 coast=1;
#10 coast =0;
#10 coast =1;
#10 coast =0;
#10 coast =1;
#10 coast =0;
#10 coast =1;
#10 coast =0;
#10 coast =1;
#10 coast =0;
#60 cancel =1;
#620 $finish;
end

always begin
    # 5 clk =~clk;
end

endmodule
```

Screenshot of the timing waveform:

