

ECEN 714: Submission for LAB 10

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Contents (Logical Effort Calculations and optimization, Comparisons between old design and the optimized design.)

Transistor Level diagram of the 3-Bit Adder with Critical Path

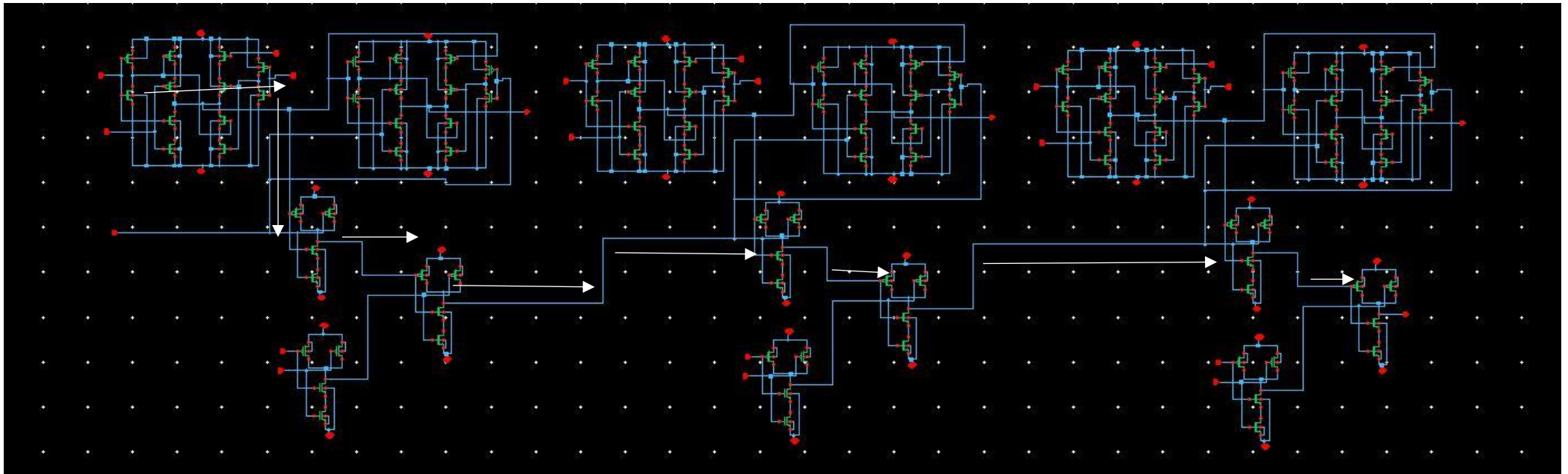


Figure 1: The White arrows show the critical path

Logic Effort Calculation(G):

$$G = \text{Path Logical Effort} = \prod g_i$$

$$g_{\text{XOR}} = \frac{C_{\text{in}}}{C_{\text{in of equivalent inverter}}} = \frac{2Wp+2Wn}{\frac{Wp}{2} + \frac{Wn}{2}} = 4$$

$$g_{\text{NAND}} = \frac{C_{\text{in}}}{C_{\text{in of equivalent inverter}}} = \frac{Wp+Wn}{Wp + \frac{Wn}{2}} = \frac{900+450}{900+450/2} = 1.2$$

$$G = 11.94$$

Branch Effort Calculation(B)

$$B = \prod b = \prod \frac{(C_{\text{on-path}} + C_{\text{off-path}})}{(C_{\text{on-path}})} = 30.52$$

$$b_1 = 3.125; b_2 = 1; b_3 = 3.125; b_4 = 1; b_5 = 3.125; b_6 = 1; b_7 = 1$$

Electrical Effort Calculation (H)

$$H = \frac{30fF}{C_{\text{xor}}} = \frac{30fF}{6.8fF} = 4.41$$

Path Effort Calculation (F)

$$F = GBH = 11.94 * 30.52 * 4.41 = 1607.04$$

$$f_{\sim} = F^{1/7} = 2.87$$

Resizing of Transistors

Resizing begins at output and moves towards the input. Hence starting at gate 7.

$$C_{\text{in7}} = g_{\text{NAND}} * \frac{30fF}{f_{\sim}} = 1.2 * \frac{30fF}{2.87} = 12.54fF$$

As this capacitance is not up to the specification this transistor needs to be resized.

$$W_{\text{new}_n} = \frac{12.54fF}{C_{\text{gate}}} * W_n = \frac{12.54fF}{3.2fF} * 450nm = 1763nm$$

$$W_{\text{new}_p} = \frac{12.54fF}{C_{\text{gate}}} * W_p = \frac{12.54fF}{3.2fF} * 900nm = 3526nm$$

For gate 6;

$$C_{in6} = g_{NAND} * \frac{12.54fF}{f_{\sim}} = 1.2 * \frac{12.54fF}{2.87} = 5.24fF$$

As this is still not upto specification we need to resize once again.

$$W_{new_n} = \frac{5.24fF}{C_{gate}} * W_n = \frac{5.24fF}{3.2fF} * 450nm = 736nm$$

$$W_{new_p} = \frac{5.24fF}{C_{gate}} * W_p = \frac{5.24fF}{3.2fF} * 900nm = 1473.75nm$$

For gate 5;

$$C_{in5} = g_{NAND} * \frac{5.24fF}{f_{\sim}} = 1.2 * \frac{5.24fF}{2.87} = 2.19fF$$

As the capacitance is within specification we stop the resizing of transistors.

Delay Comparision

Old Values:

<u>Vector 1</u> <i>A=000; B=111; Cin= 1</i>	<u>Cin</u>	<u>s1</u>	<u>s2</u>	<u>s3</u>	<u>Cout</u>
	8.1597	8.91764	8.91764	9.29052	9.03413
	15.0679	15.9126	16.093	16.093	15.786
Delay	<u>s1</u>	<u>s2</u>	<u>s3</u>	<u>Cout</u>	
Rising	0.75794	0.75794	1.13082	0.7181	
Falling	0.8447	1.0251	1.0251	0.87443	

Vector 1	Cin	s1	s2	s3	Cout
	8.15416	8.799	9.0774	9.228	8.84044
	15.0396	15.7337	16.01	16.215	15.8043
Delay	s1	s2	s3	cout	
rising	0.64484	0.92324	1.07384	0.7647	
falling	0.6941	0.9704	1.1754	0.68628	

New Values:

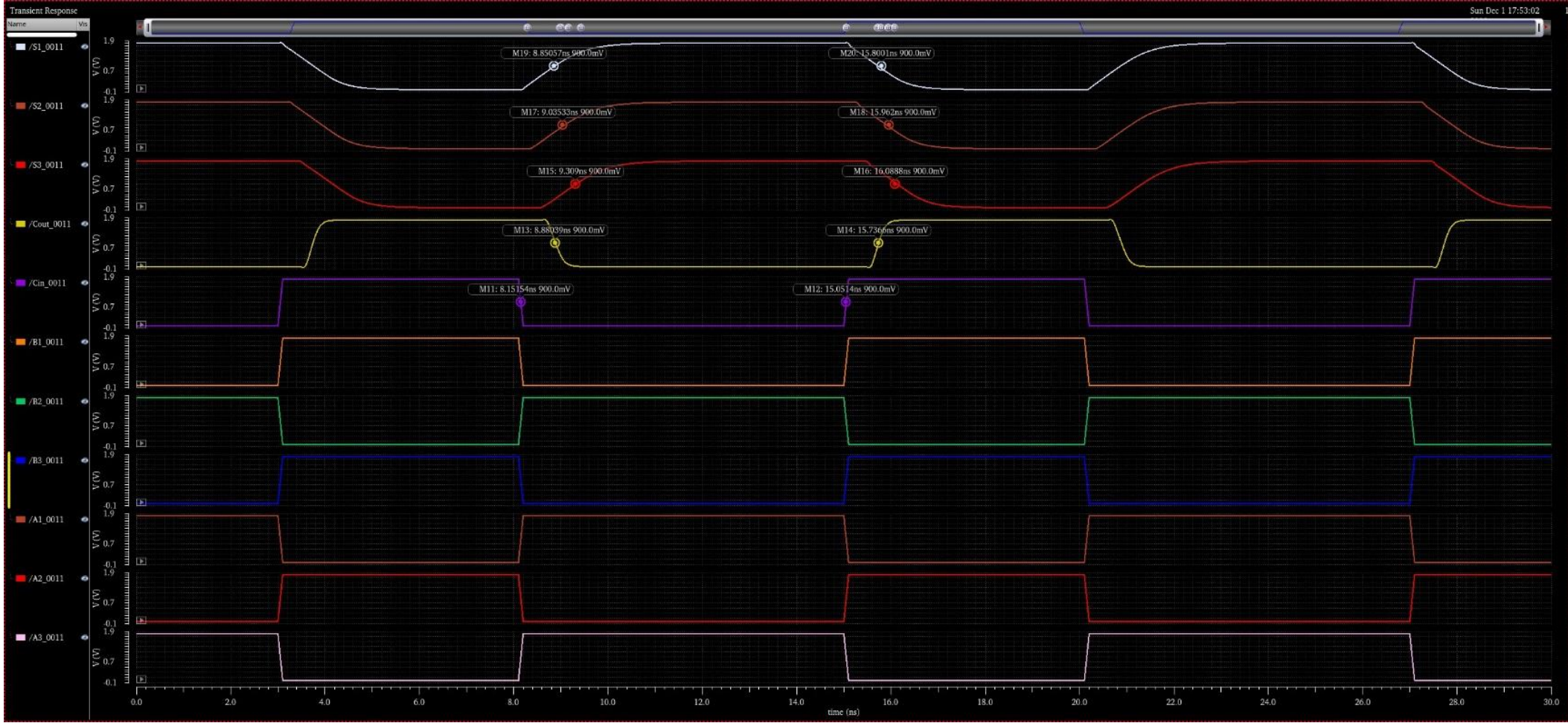


Old Values:

<u>Vector 2</u>	<u>Cin</u>	<u>s1</u>	<u>s2</u>	<u>s3</u>	<u>Cout</u>
<i>A=101; B=010; Cin=0</i>					
	8.14765	8.9062	9.26074	9.47085	8.99078
	15.0565	15.8704	15.9068	16.008	15.9326
<u>Delay</u>	<u>s1</u>	<u>s2</u>	<u>s3</u>	<u>cout</u>	
Rising	0.75855	1.11309	1.3232	0.8761	
Falling	0.8139	0.8503	0.9515	0.84313	

New Values:

Vector 2	Cin	s1	s2	s3	Cout
	8.15154	8.85057	9.03533	9.309	8.88039
	15.0514	15.8001	15.962	16.088	15.7366
Delay	s1	s2	s3	cout	
rising	0.69903	0.88379	1.15746	0.6852	
falling	0.7487	0.9106	1.0366	0.72885	



Old Values:

<u>Vector 3</u>	<u>Cin</u>	<u>s1</u>	<u>s2</u>	<u>s3</u>	<u>Cout</u>
<i>A=101; B=010; Cin=1</i>					
	8.16413	8.82517	8.89457	9.25728	9.11594
	15.0537	15.913	16.0688	16.1686	15.8164
<u>Delay</u>	<u>s1</u>	<u>s2</u>	<u>s3</u>	<u>cout</u>	
Rising	0.8593	1.0151	1.1149	0.95181	
Falling	0.66104	0.73044	1.09315	0.7627	

New Values:

Vector 3	Cin	s1	s2	s3	Cout
	8.1444	8.91002	9.02787	9.2835	8.832
	15.0537	15.8169	15.8931	16.0633	15.7812
Delay	s1	s2	s3	cout	
rising	0.7632	0.8394	1.0096	0.6876	
falling	0.76562	0.88347	1.1391	0.7275	

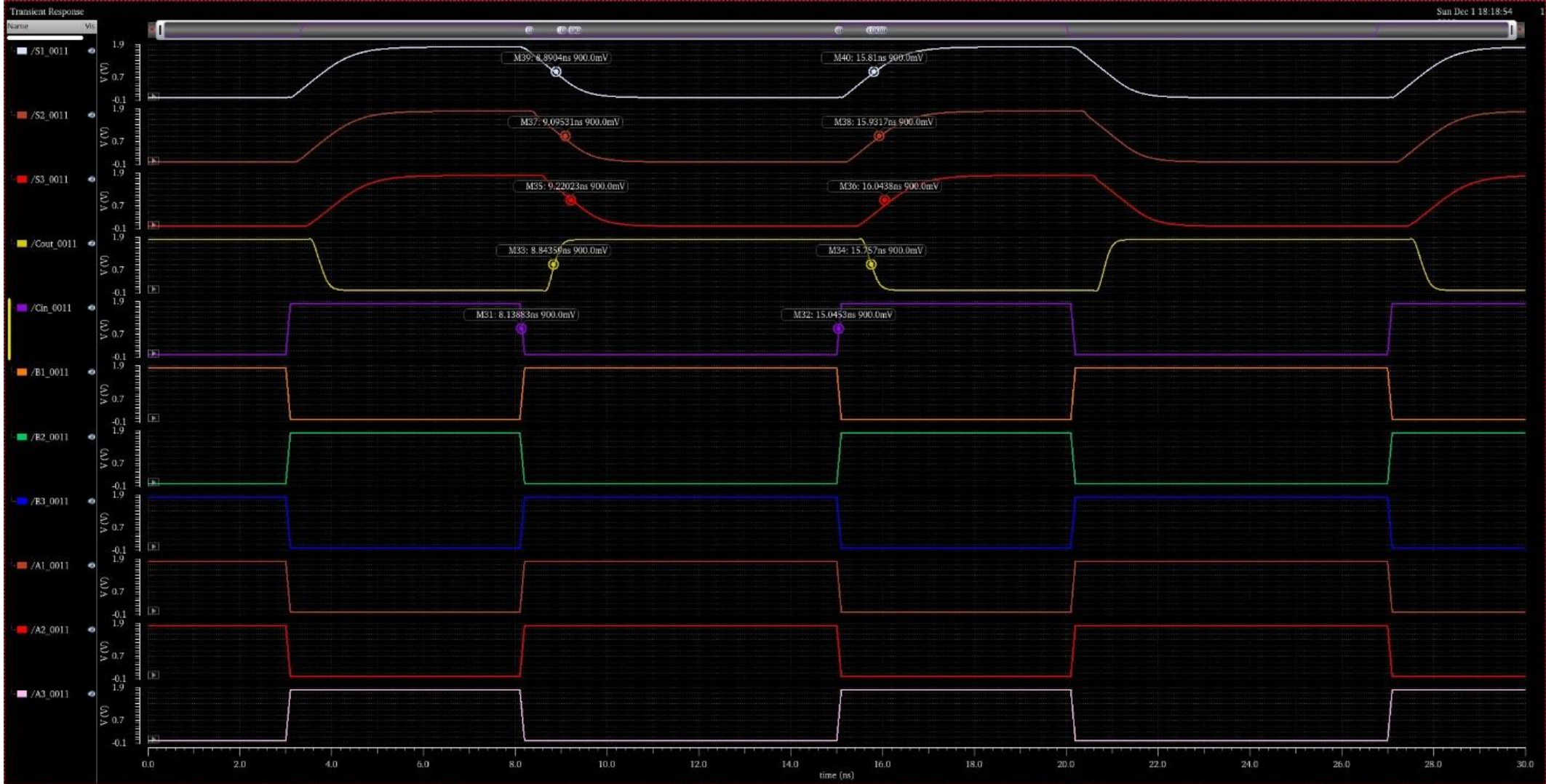


Old Values:

Vector 4	Cin	s1	s2	s3	Cout
<i>A=110; B=101; Cin=0</i>					
	8.1518	8.79267	8.98721	9.13881	9.02989
	15.0521	15.7476	16.0412	16.2284	15.792
Delay	s1	s2	s3	cout	
Rising	0.64087	0.83541	0.98701	0.7399	
Falling	0.6955	0.9891	1.1763	0.87809	

New Values:

Vector 4	Cin	s1	s2	s3	Cout
	8.1368	8.8904	9.09531	9.22023	8.84359
	15.0432	15.81	15.9317	16.0438	15.757
Delay	s1	s2	s3	cout	
rising	0.7536	0.95851	1.08343	0.7138	
falling	0.7668	0.8885	1.0006	0.70679	



Power Comparision

	Old Power	New Power
Vector 1	-0.000176	-0.000184
Vector 2	-0.000150	-0.000163
Vector 3	-0.000173	-0.000192
Vector 4	-0.000172	-0.000186

Area Comparision

Area of the old design : $15.78 \mu\text{m}^2$

Area of the new design: $17.94 \mu\text{m}^2$