ECEN 714: Submission for LAB 7b

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Contents (Schematic, Layout, DRC and LVS for the 6-bit Pipelined Adder and H-clock tree and Post Layout Simulation)

Schematic:

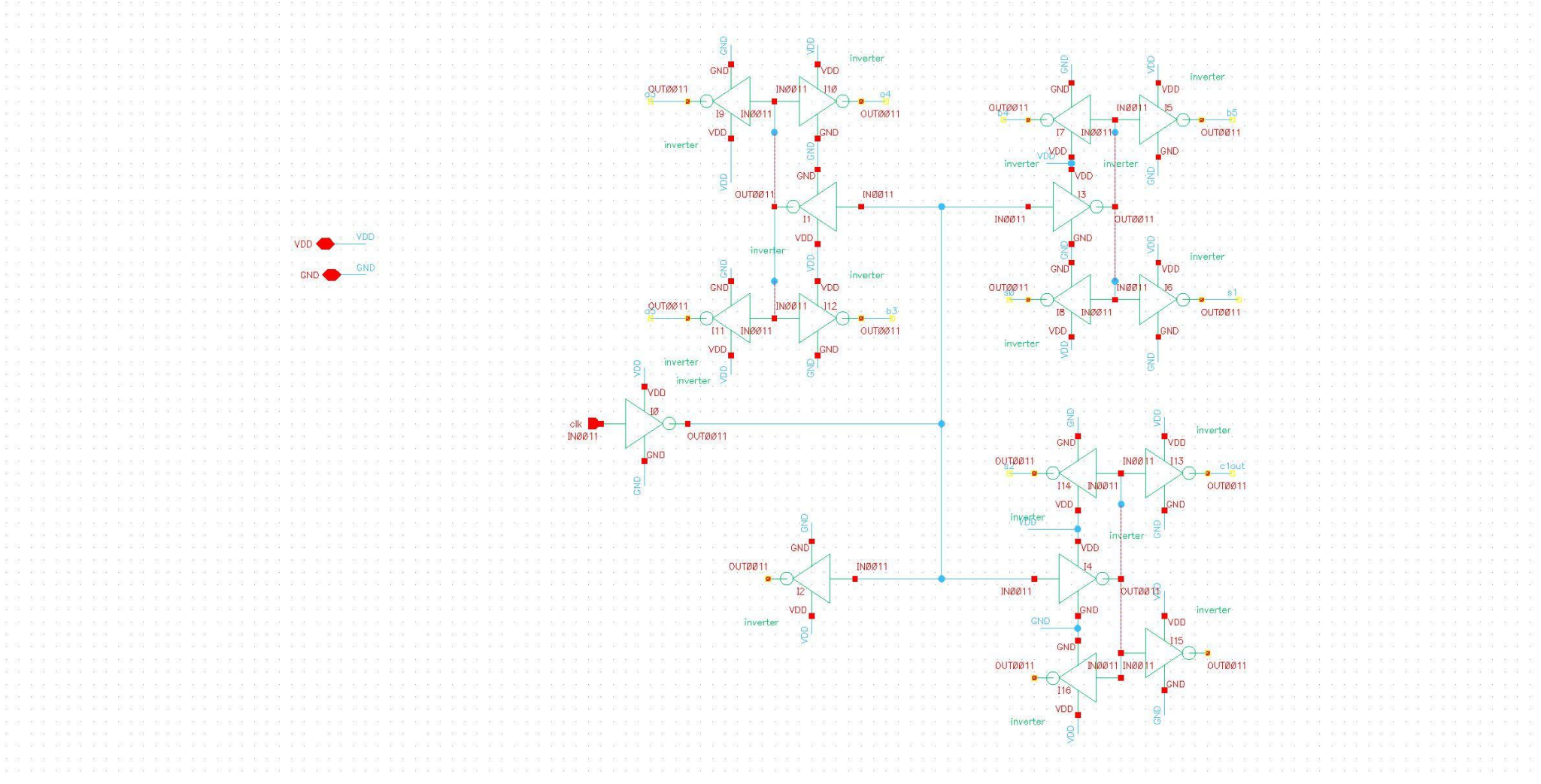


Figure 1: Schematic for the H-tree clock distribution network.

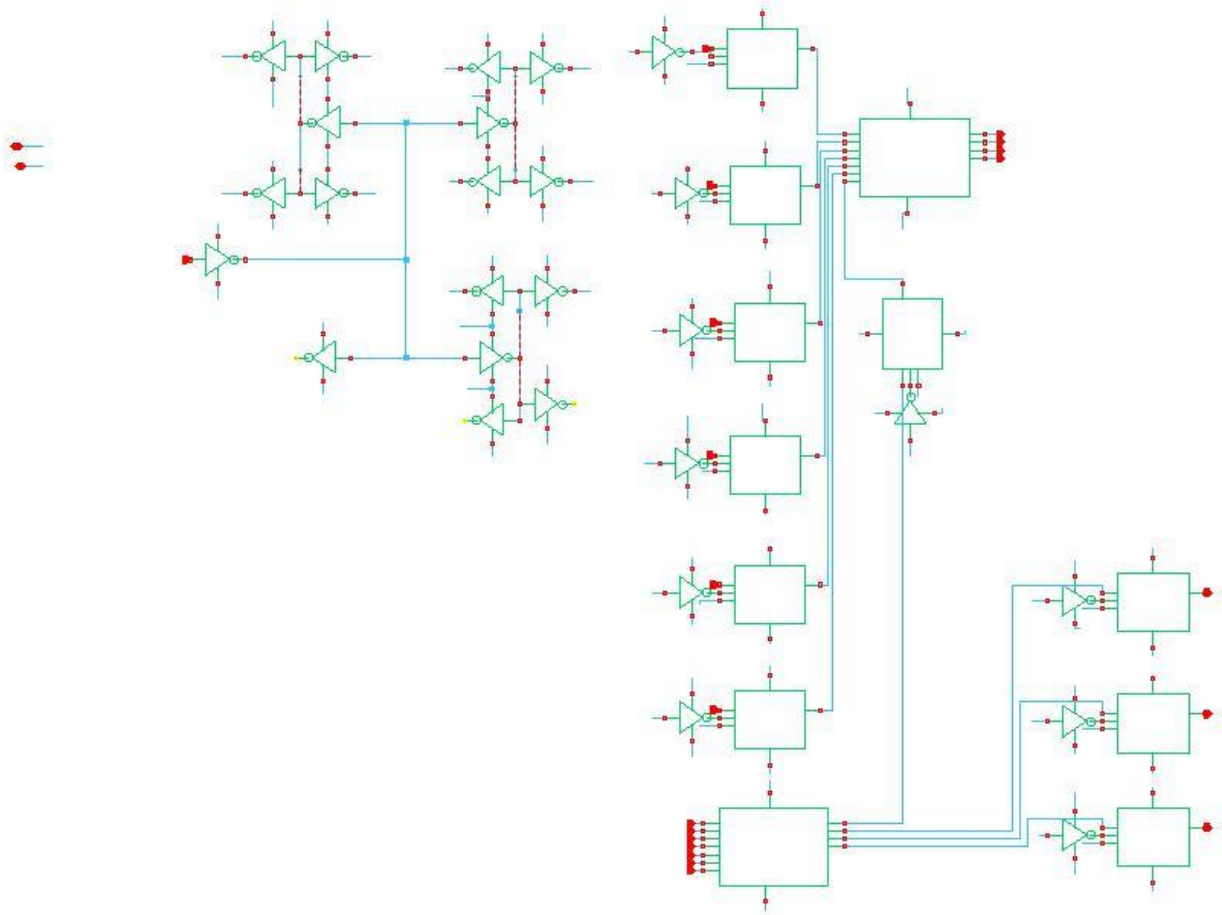


Figure 2: Schematic of the 6-bit Pipelined adder

Layout

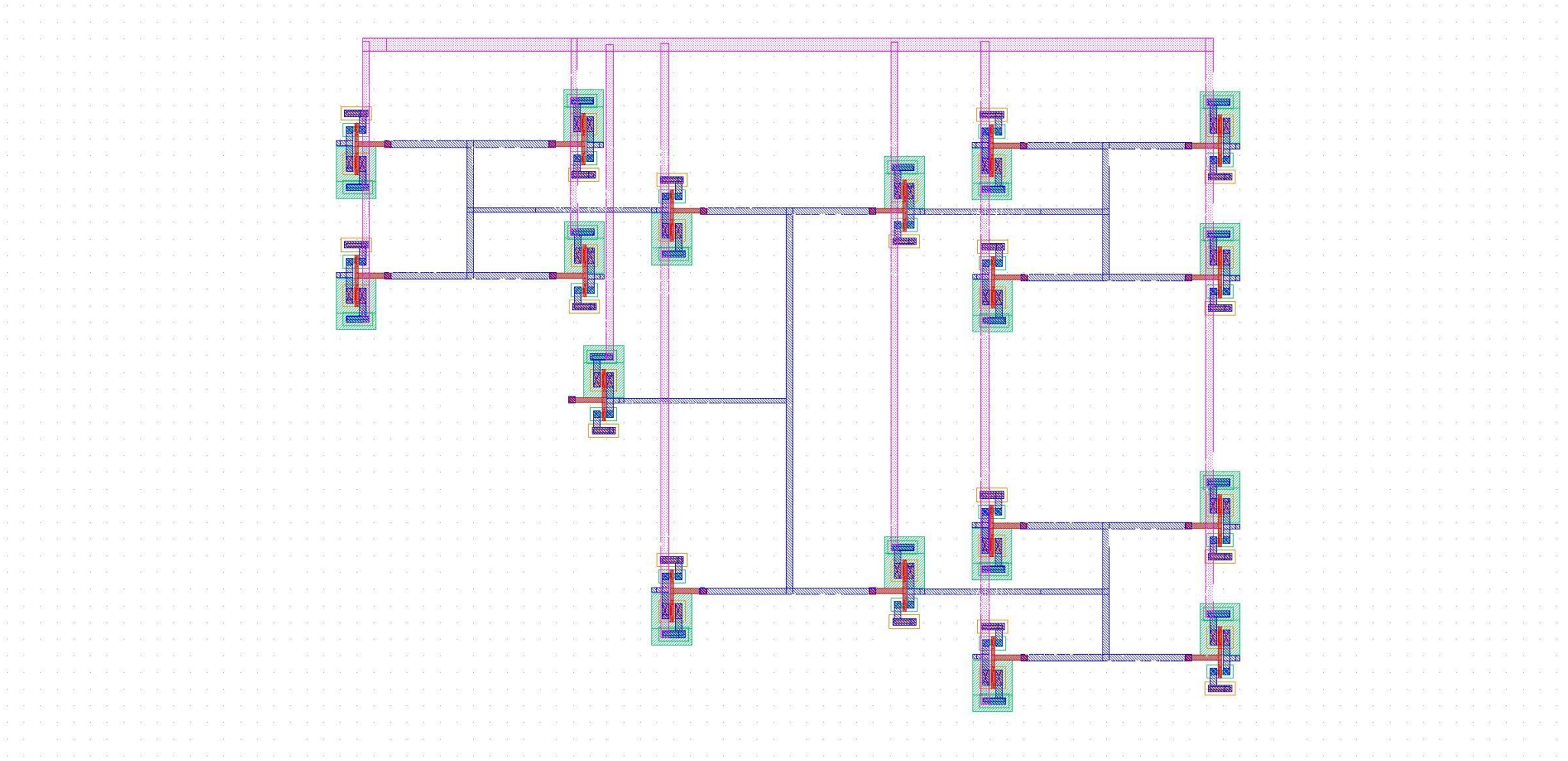


Figure 3: Layout for the H-tree clock distribution network

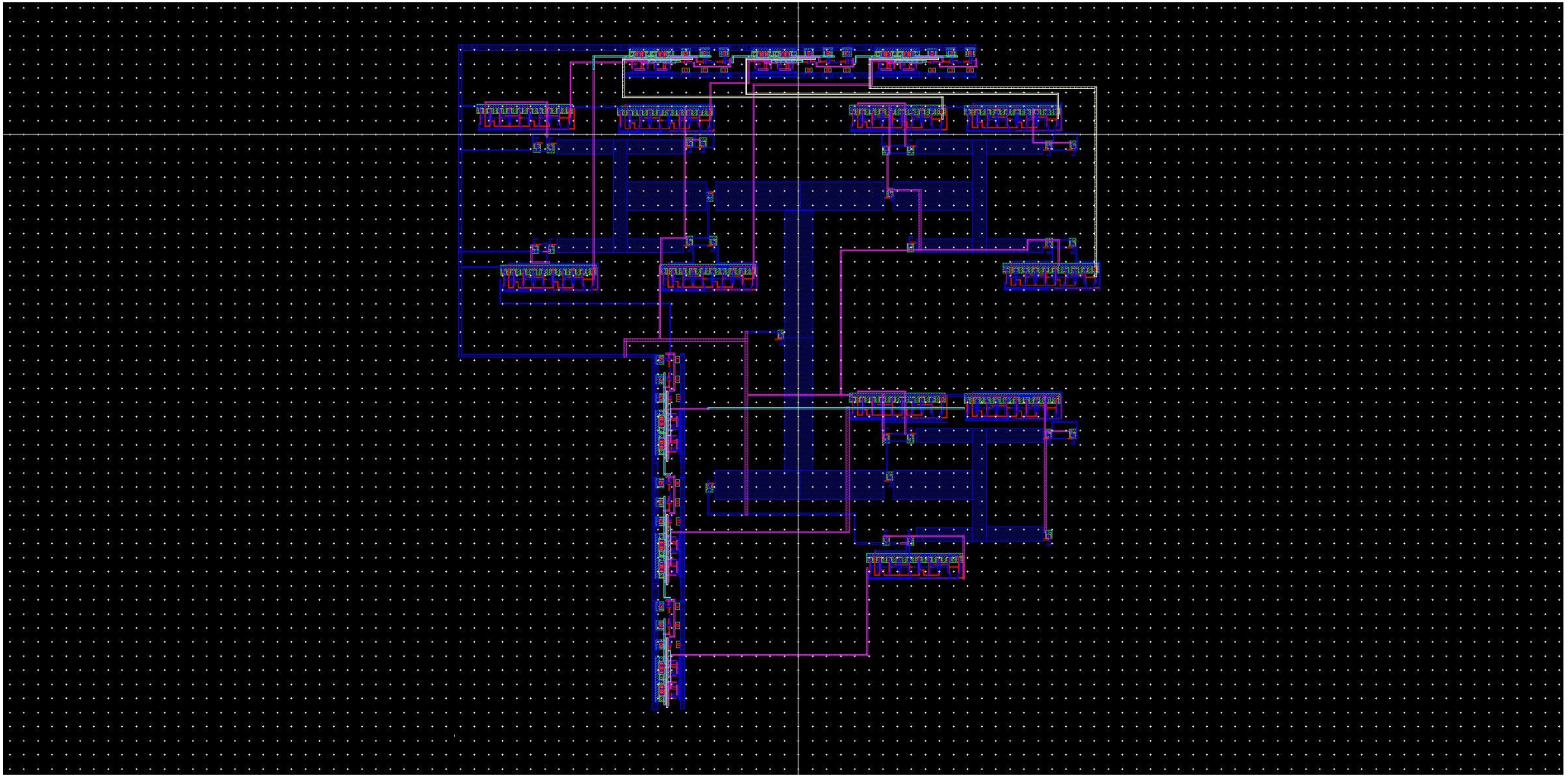


Figure 4: Layout for the 6-bit Pipelined Adder

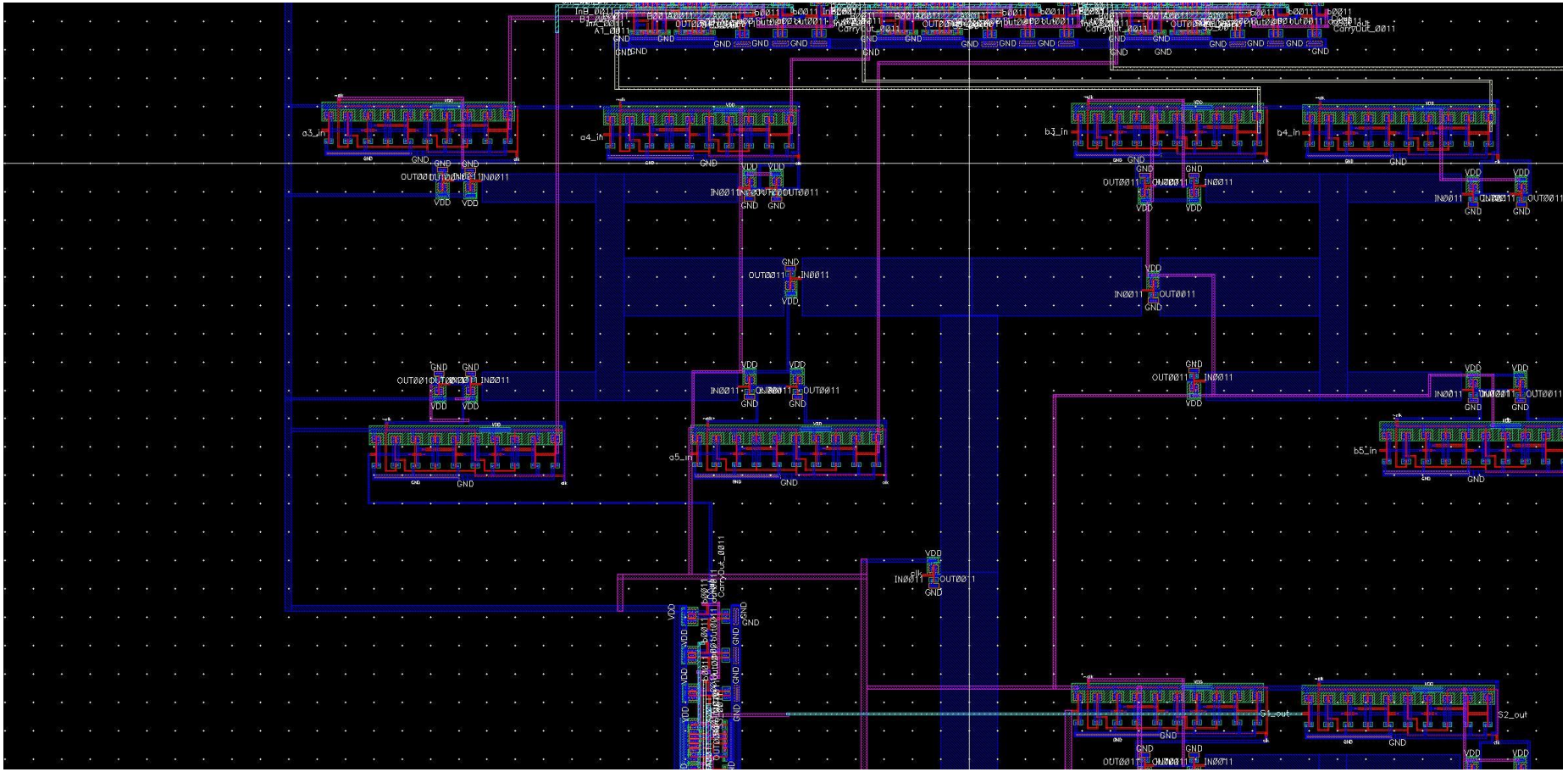


Figure 5. Same layout (To show UIN)

Total Area of the Layout

Length	245
Breadth	233.65
Total Area	57244.25

DRC:

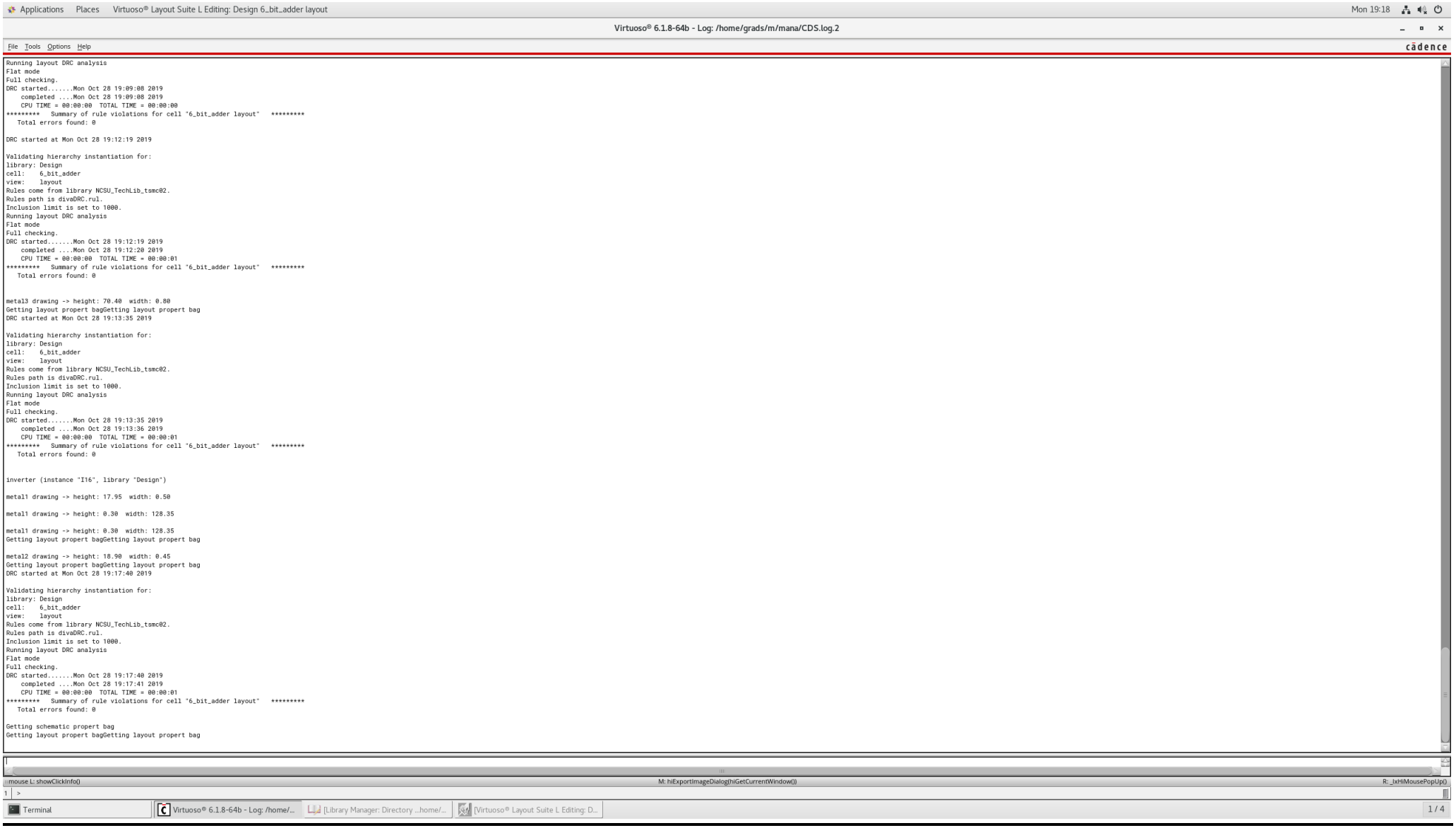


Figure 6. DRC results

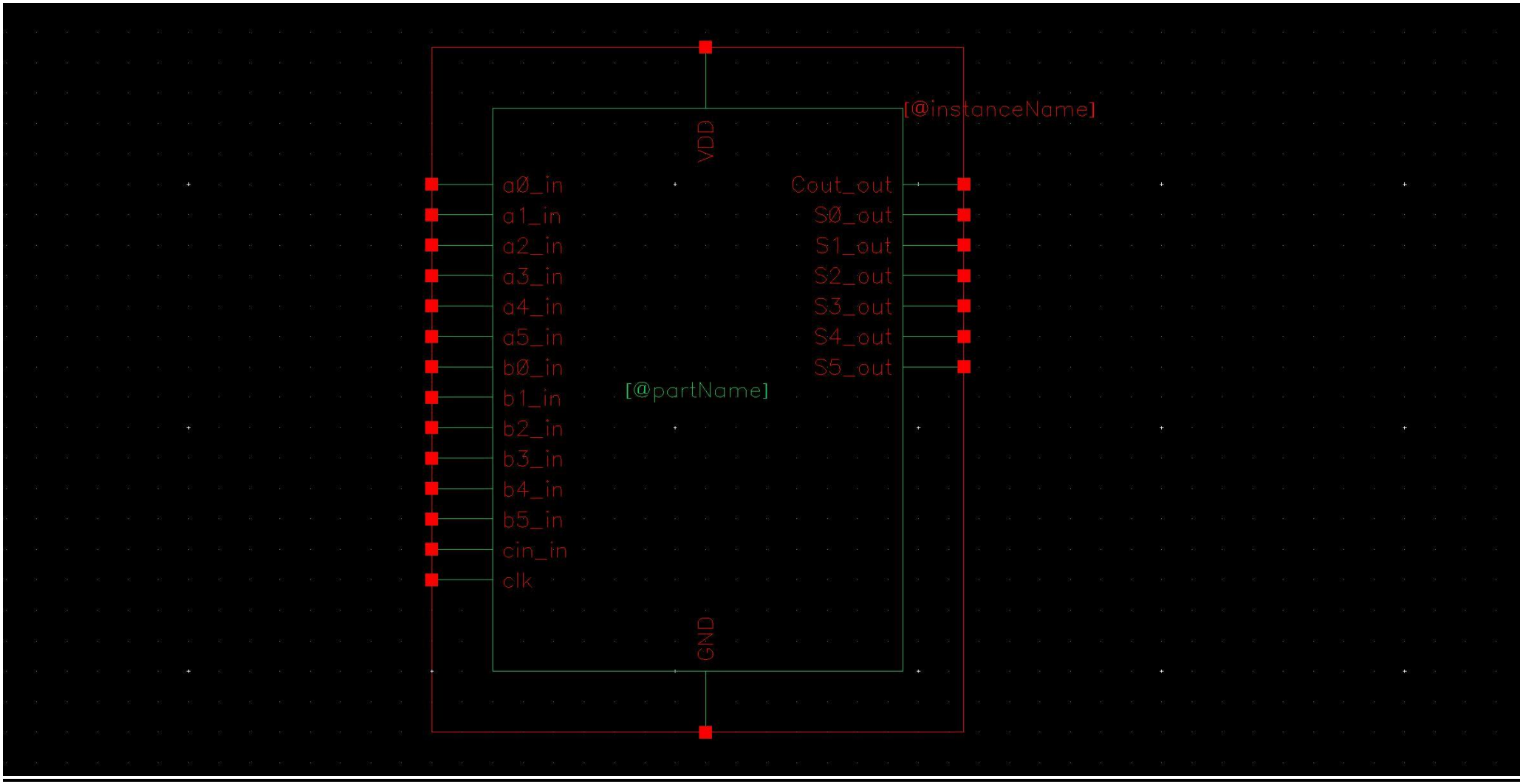
LVS report:

```
@(#)$CDS: LVS version 6.1.8-64b 10/01/2018 19:50 (ip-172-18-22-57) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/m/mana/ecen454/Lab1/LVS -l -s -t
/home/grads/m/mana/ecen454/Lab1/LVS/layout /home/grads/m/mana/ecen454/Lab1/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/layout/netlist
       count
        243             nets
        23              terminals
        235             pmos
        235             nmos

    Net-list summary for /home/grads/m/mana/ecen454/Lab1/LVS/schematic/netlist
       count
        243             nets
        23              terminals
        235             pmos
        235             nmos


    Terminal correspondence points
    N231      N58       Cout_out
    N225      N42       GND
    N236      N53       S0_out
    N242      N50       S1_out
    N223      N52       S2_out
    N229      N0        S3_out
    N235      N46       S4_out
    N241      N56       S5_out
    N240      N31       VDD
    N233      N55       a0_in
    N224      N45       a1_in
    N237      N13       a2_in
    N226      N60       a3_in
    N238      N39       a4_in
    N227      N47       a5_in
    N239      N57       b0_in
```

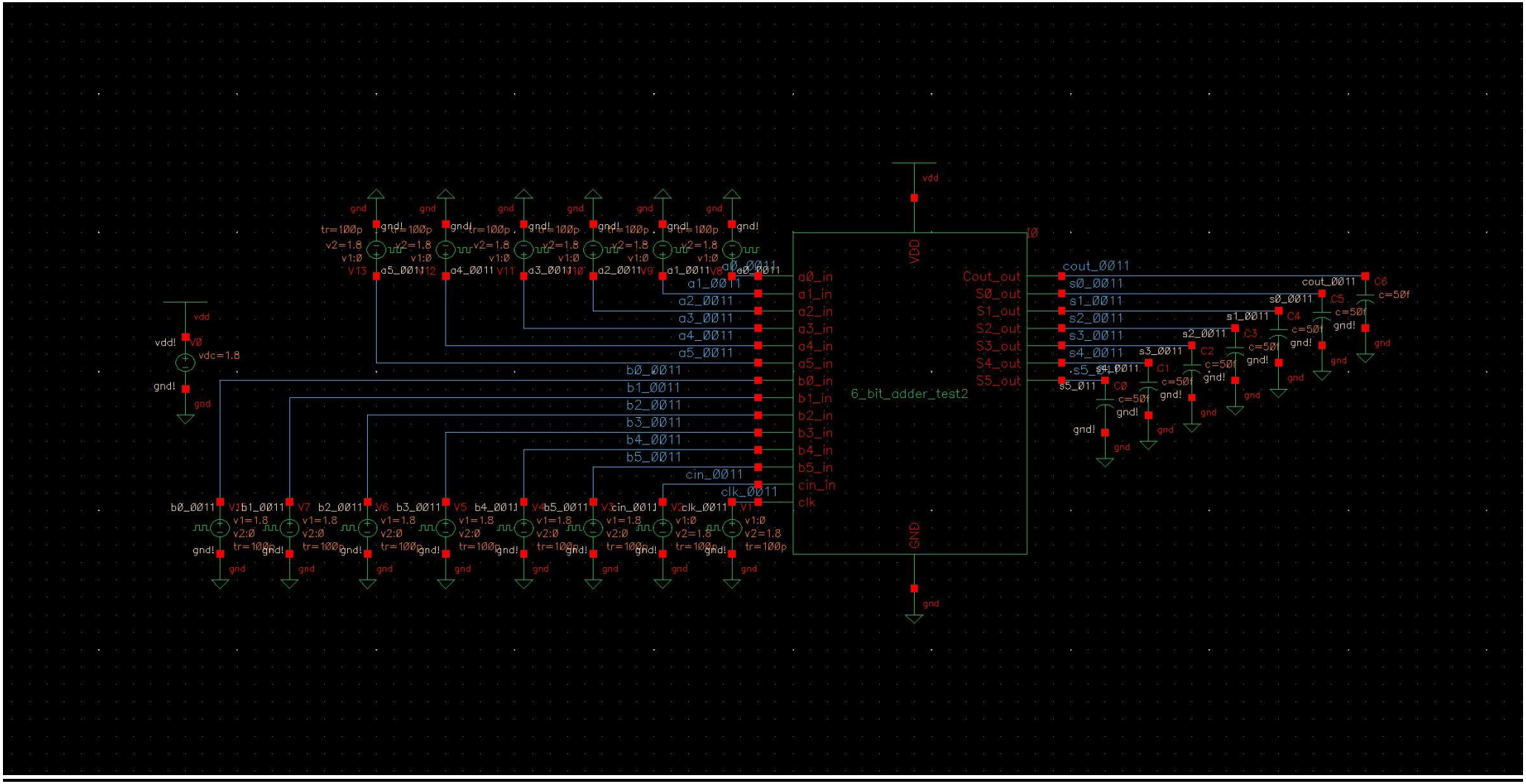
```
    N228      N48       b1_in
    N220      N54       b2_in
    N232      N41       b3_in
    N222      N51       b4_in
    N234      N43       b5_in
    N221      N7        cin_in
    N230      N26       clk

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  470     470
        total                   470     470

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  243     243
        total                   243     243

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   23      23


Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/schematic

devbad.out:

netbad.out:
```

```
mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/m/mana/ecen454/Lab1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

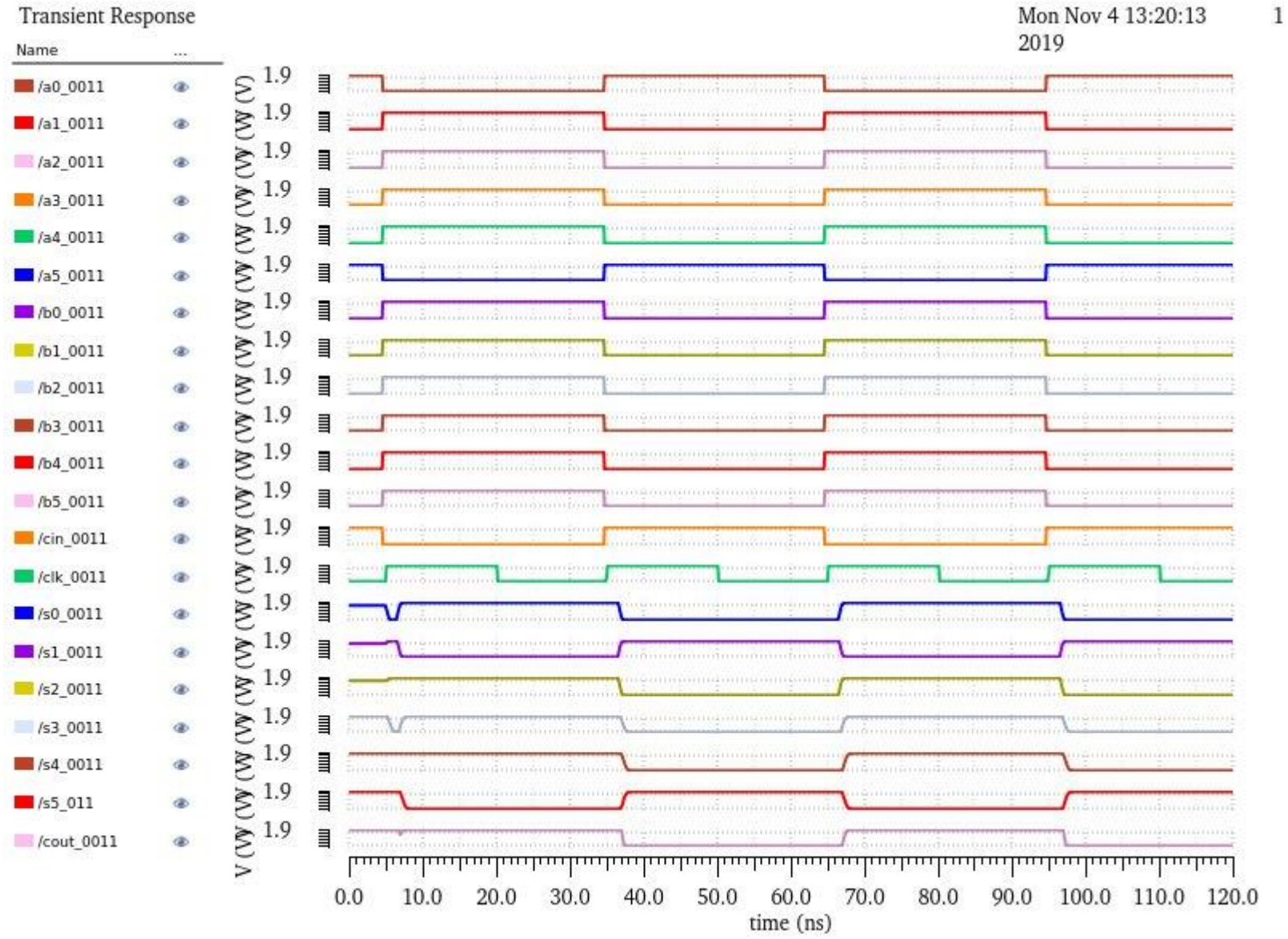
6-bit Adder Layout:



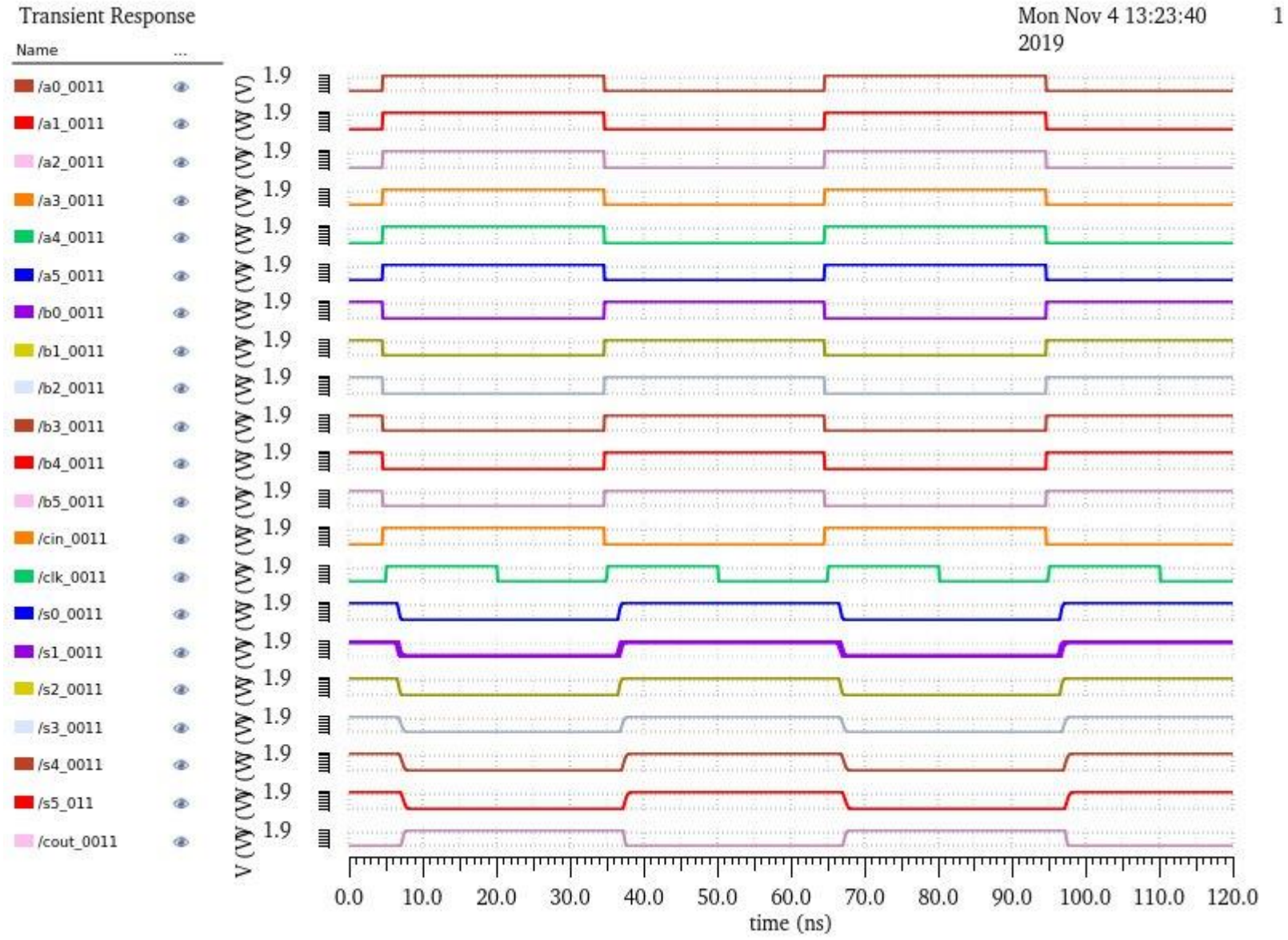
Post Layout Simulation:



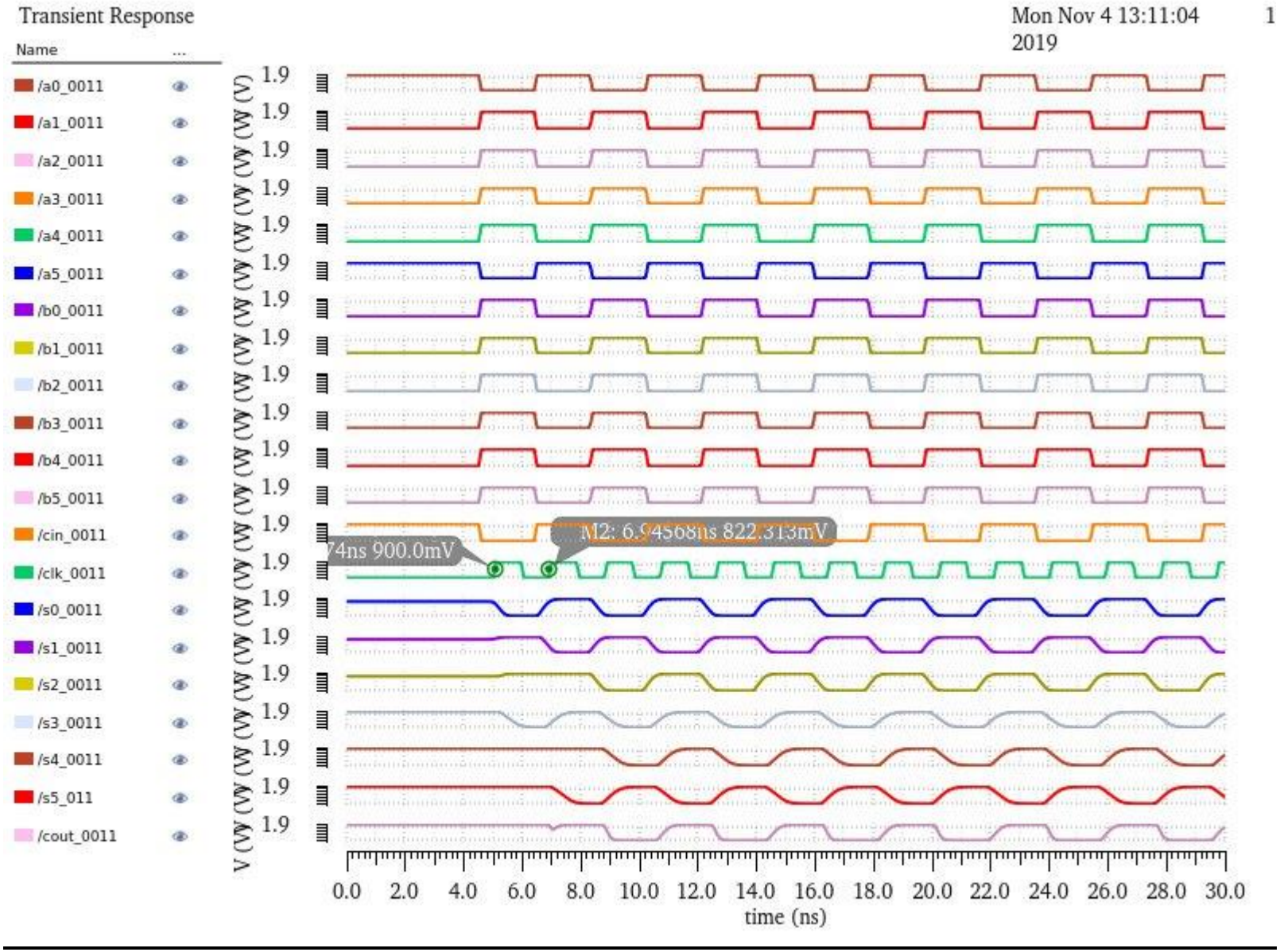
Input Vector 1: (30ns clock period)



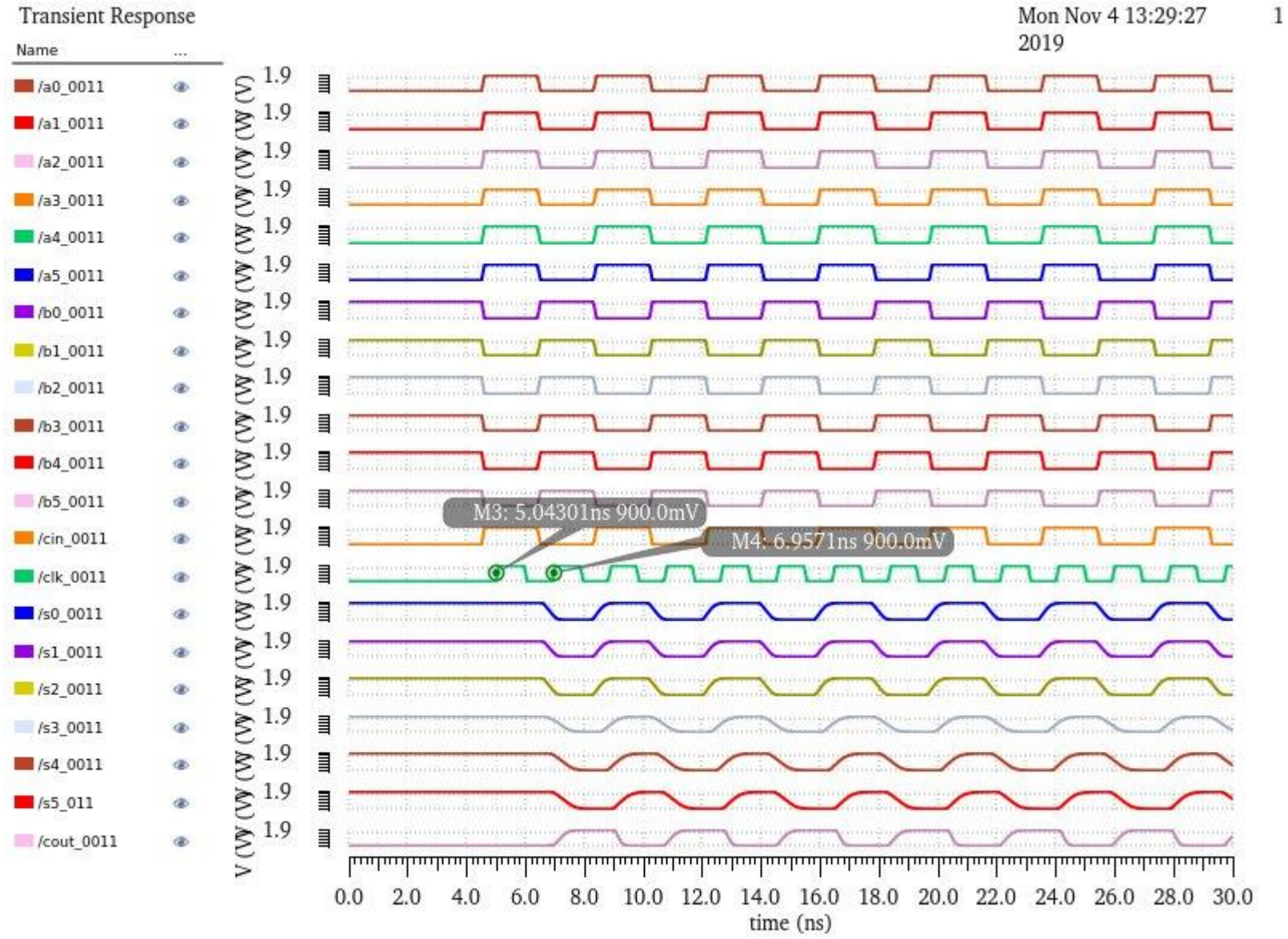
Input Vector 2: (30ns clock period)



Input Vector 1: (Highest Performance)



Input Vector 2: (Highest Performance)



Calculations:

Input Vector 1	011110+ 111111+ 0
Max Period	1.9ns
Delay	5ns
Current	-1.38E-03
Voltage	1.8
Power	-0.0024858

Input Vector 2	0000000+111111+1
Max Period	1.9ns
Delay	5ns
Current	-1.41E-03
Voltage	1.8
Power	-0.0025452