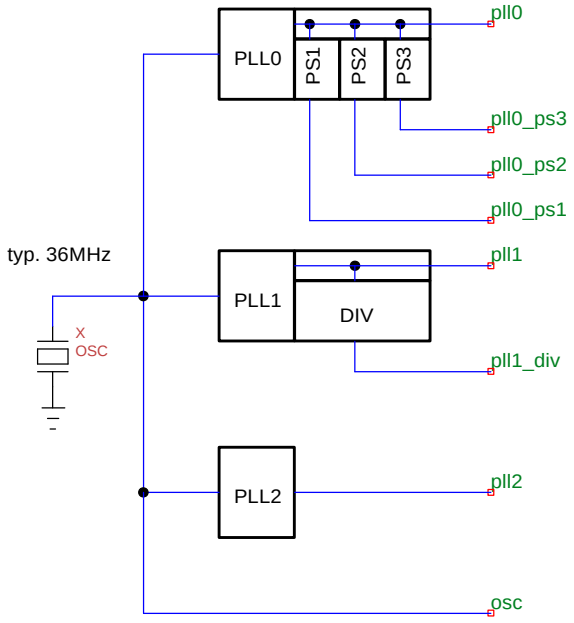
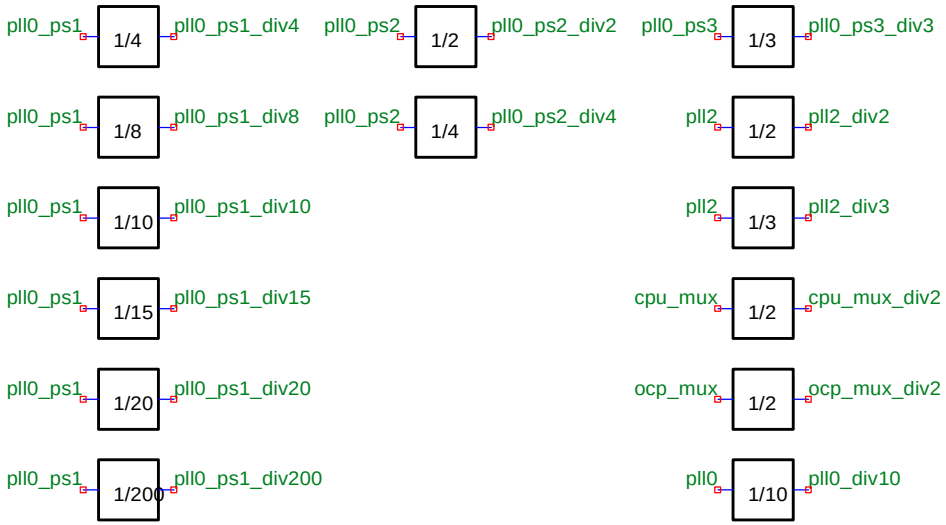
[0] CLOCK GENERATION

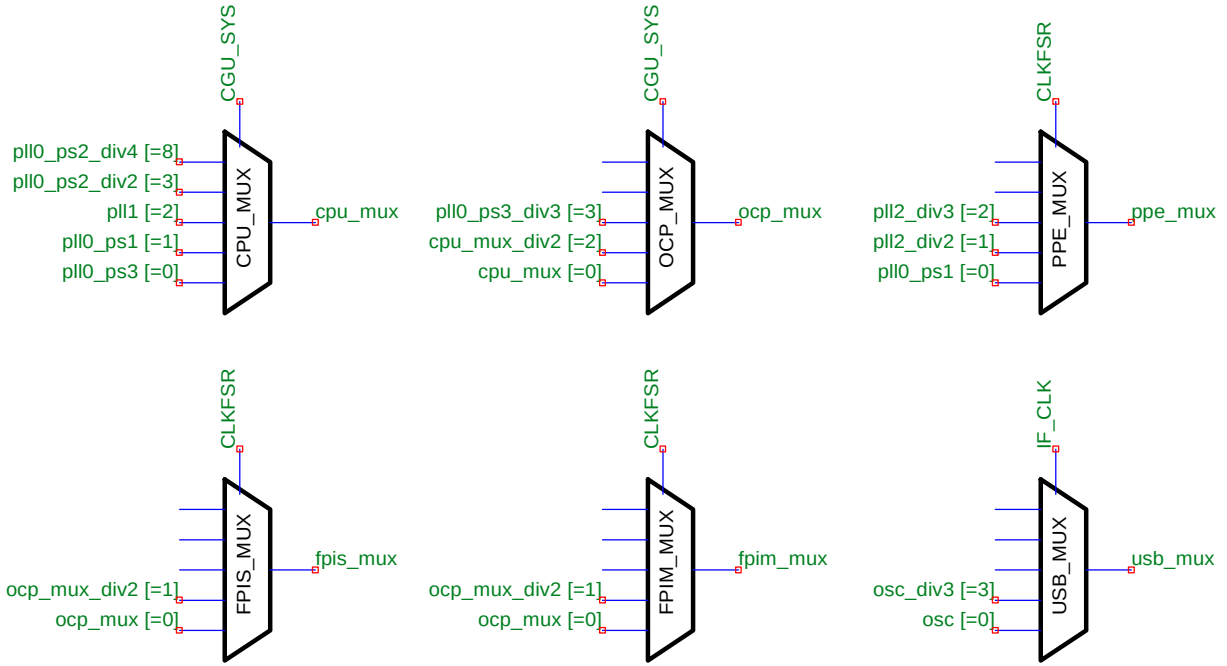


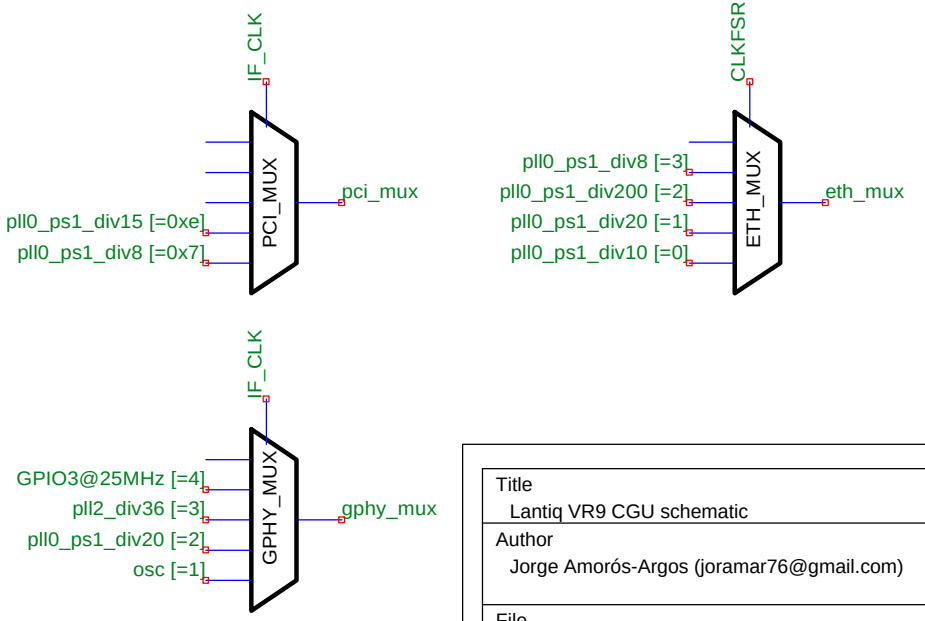
Note: pll0_ps1, ps2 _ps3 are in fact dividers of respective factors 1/2, 2/3 and 6/10

[1] CLOCK DIVIDERS



[2] CLOCK MUXERS (REGISTER DRIVEN)





Title: Lantiq VR9 CGU schematic		
Author: Jorge Amorós-Argos (joramar76@gmail.com)		
File: \Users\Tooney\D ... VR9_CGU_v0_20200503.dsn		Document
Revision: 1.0	Date: 3rdt May 2020	Sheets: 1 of 2

[3] PMU (CLOCK GATING)

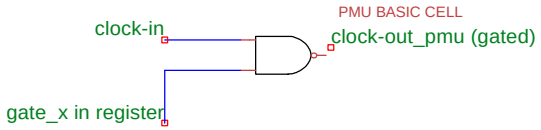
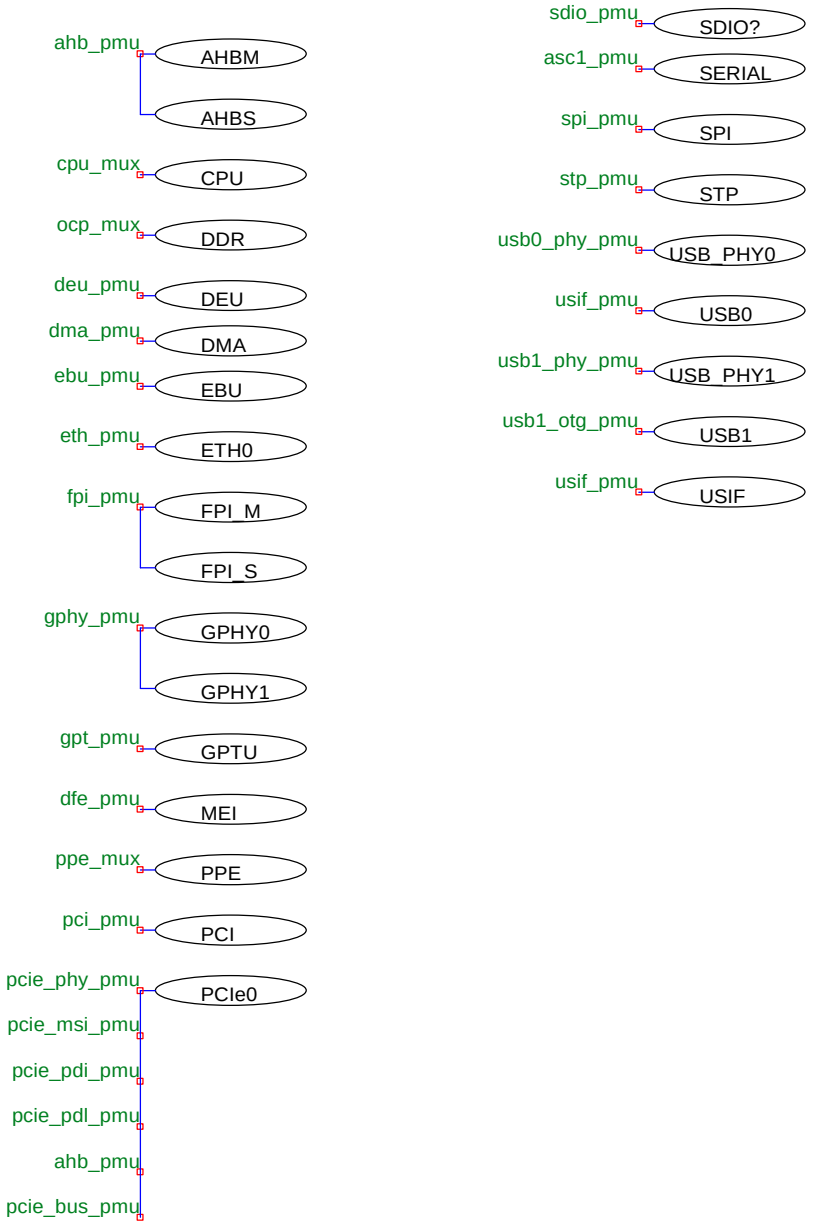


TABLE of relationships:

PMU clk	Parent clk	PMU Module
usb0_phy_pmu	usb_mux	0
pci_pmu	pci_mux	0
ocp_mux	dma_pmu	0
usb0_otg_pmu	usb_mux	0
usif_pmu	pll0_div10	0
spi_pmu	fpim_mux	0
dfe_pmu	?	0
ebu_pmu	pci_mux	0
gpt_pmu	fpim_mux	0
stp_pmu	fpim_mux	0
fpim_pmu	fpim_mux	0
ahb_pmu	ocp_mux	0
sdio_pmu	?	0
asc1_pmu	ocp_mux	0
deu_pmu	?	0
eth0_pmu	eth_mux	0
usb1_phy_pmu	usb_mux	0
usb1_otg_pmu	usb_mux	0
gphy_pmu	gphy_mux	0
pcie_bus_pmu	?	0
pcie_phy_pmu	?	1
pcie_ctl_pmu	?	1
pcie_pdi_pmu	?	1
pcie_msi_pmu	?	1

[4] CLOCK CONSUMERS



DISCLAIMER: The information shown in this document is provided "as-is", based on the study of the available source code by Lantiq/Infineon

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