

PART- 1

Introduction to IC Technology : SSI, MSI, LSI, VLSI Integrated Circuits, Crystal Growth and Wafer Preparation : Electronic Grade Silicon, Czochralski Crystal Growth.

CONCEPT OUTLINE

- EGS, a polycrystalline material of high purity, is the raw material for the preparation of single-crystal silicon.
- Czochralski growth is the process used to grow most of the crystals from which silicon wafers are produced.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 1.1. Define the term : **SSI, MSI, LSI, VLSI and ULSI.**

Answer

Depending upon the number of active devices per chip, there are different levels of integration :

i. SSI :

When the active devices per chip are less than 100, then it is referred as small scale integration (SSI). Most of the SSI chips use integrated resistors, diodes and bipolar transistors.

ii. MSI :

When the count of active devices per chip is between 100 and 1000, then it is referred as medium scale integration (MSI). In most of the MSI chips, BJTs and enhancement mode MOSFETs are integrated.

iii. LSI :

In large scale integration (LSI), the number of active devices per chip ranges between 1000 and 100,000. In general, LSI chips use MOS transistors; as it requires less number of steps for integration. Thus more number of components can be produced on the chip with MOS transistors than with the bipolar transistors.

iv. VLSI :

When the active devices per chip are over hundreds of thousands, then it is referred as very large scale integration (VLSI). Almost all modern chips employ VLSI technique.

v. ULSI:

Recently a new level of integration has been introduced which is known as ultra large scale integration (ULSI). In ULSI technique, more than one million active devices are integrated on a single chip. Pentium microprocessors use ULSI technology.

Table 1.1.1.

S. No.	Level of integration devices per chip	Number of active
1.	Small scale integration (SSI)	less than 100
2.	Medium scale integration (MSI)	100 - 10000
3.	Large scale integration (LSI)	1000 - 100000
4.	Very large scale integration (VLSI)	Over 100000
5.	Ultra large scale integration (ULSI)	Over 1 million

Que 1.2. Explain electronic grade silicon with neat diagram.

Answer

1. Electronic-Grade Silicon (EGS), a polycrystalline material of high purity is the raw material for the preparation of single-crystal silicon.
2. EGS is undoubtedly one of the purest materials available. The major impurities are boron, carbon, and residual donors.
3. To obtain EGS requires a multistep process. First, Metallurgical-Grade Silicon (MGS) is produced in a submerged-electrode arc furnace, as shown in Fig. 1.2.1.

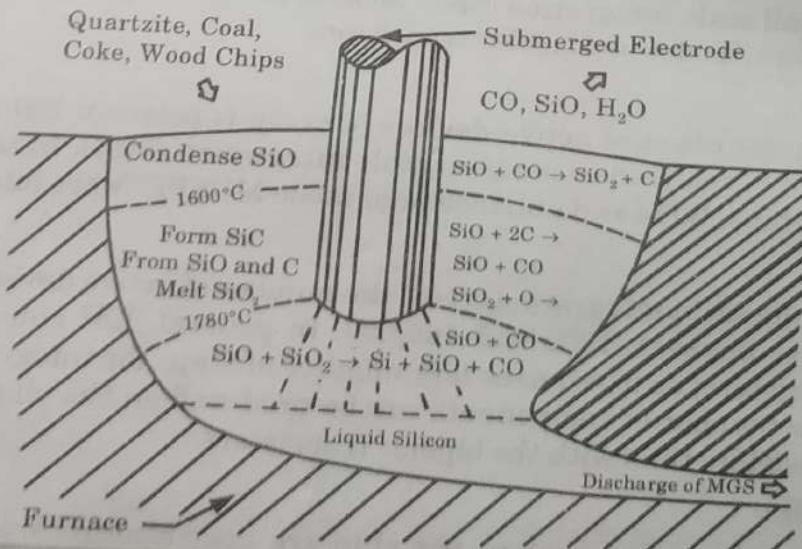
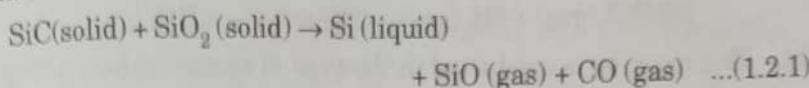


Fig. 1.2.1. Schematic of a submerged-electrode arc furnace for the production of metallurgical-grade silicon.

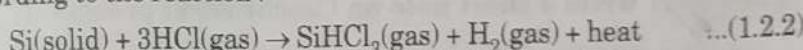
4. The furnace is charged with quartzite, a relatively pure form of sand (SiO_2), and carbon in the form of coal, coke, and wood chips. In the furnace a number of reactions take place, the overall reaction being



5. The process is power intensive, requiring 13 kWh/kg, and MGS is drawn off and solidified at a purity of 98 %.

6. The MGS used in the making of metal alloys is not sufficiently pure to use in the manufacture of solid-state devices.

7. The next process step is to pulverize the silicon mechanically and react it with anhydrous hydrogen chloride to form trichlorosilane (SiHCl_3), according to the reaction :



8. The reaction takes place in a fluidized bed at a nominal temperature of 300°C using a catalyst. Here silicon tetrachloride and the chlorides of impurities are formed.

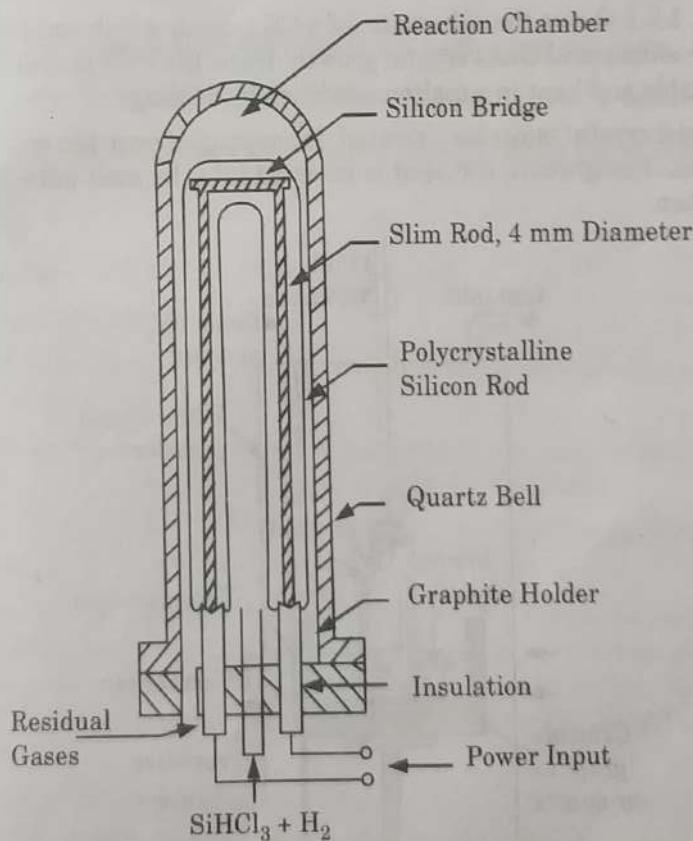


Fig. 1.2.2. Schematic of a CVD reactor used for EGS production.

9. At this point the purification process occurs. Trichlorosilane is a liquid at room temperature, as are many of the unwanted chlorides. Purification is therefore done by fractional distillation.

10. EGS is prepared from the purified SiHCl_3 in a chemical vapor deposition (CVD) process similar to the epitaxial CVD process. The chemical reaction is a hydrogen reduction of trichlorosilane.
- $$2\text{SiHCl}_3(\text{gas}) + 2\text{H}_2(\text{gas}) \rightarrow 2\text{Si}(\text{solid}) + 6\text{HCl}(\text{gas}) \quad \dots(1.2.3)$$
11. This reaction is conducted in the type of system shown in Fig. 1.2.2. A resistance-heated rod of silicon, called a "slim rod" serves as the nucleation point for the deposition of silicon.
12. A complete process cycle takes many hours and results in rods of EGS, which are polycrystalline in structure, up to 0.2 m in diameter and several meters in length.
13. EGS can be cut from these rods as single chunks or crushed into nuggets.

Que 1.3 Write a short note on Czochraslski process.

AKTU 2015-16, Marks 05

Answer

- Fig. 1.3.1 shows the schematic of a CZ system which can be used for both silicon and GaAs crystal growth. Here, the melt is contained in a crucible and kept in a molten condition by heating.
- A seed crystal, suitably oriented, is suspended over the crucible in a chuck. For growth, the seed is inserted into the melt until its end is molten.

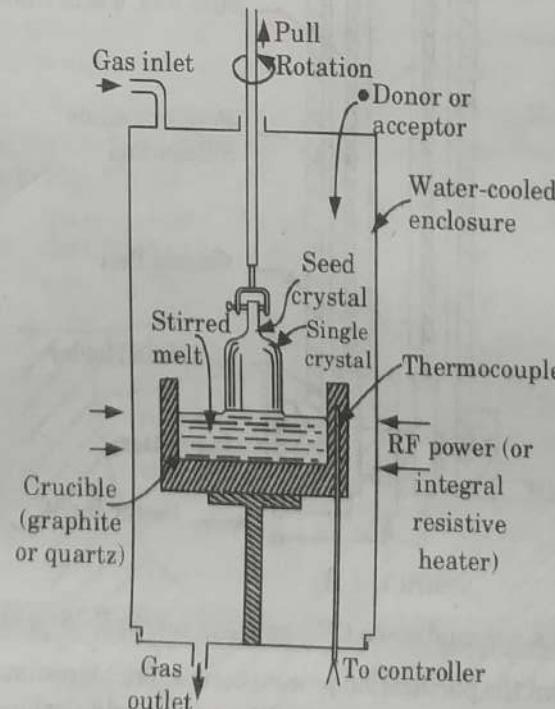


Fig. 1.3.1. Czochralski crystal-growing apparatus.

3. It is now slowly withdrawn, resulting in a single crystal which grows by progressive freezing at the liquid-solid interface. A pull rate of about 50-100 mm/hr is typical for both silicon and GaAs.
4. Provisions are also made to rotate the crystal, and sometimes the crucible as well, during the pulling operation.
5. A series of annular heat shields are provided between the growth region and the walls of the reactor, in order to control radial thermal gradients during the solidification process.
6. For silicon the entire assembly is enclosed within an envelope which is water-cooled and flushed with an inert gas.
7. With GaAs, on the other hand, it is important to prevent decomposition of the melt during crystal growth by maintaining an overpressure of about 1.0 atm of arsenic.
8. It is necessary that the latent heat of fusion be removed from the crystal-melt system during the growth process. This heat is lost by radiation from the crystal surface and by thermal conduction along the crystal axis.

Que 1.4 ~~Describe CZ process in detail with neat diagram. What is the pull rate in CZ technique ? How the pull rate is controlled during the CZ crystal growth process ?~~ **AKTU 2017-18, Marks 10**

Answer

- A. **CZ process :** Refer Q. 1.3, Page 1-5F, Unit-1.
- B. **Pull rate in CZ technique :**
 1. The pull rate influences the incorporation of impurities into the crystal and is a factor in defect generation.
 2. Generally, when the temperature gradient in the melt is small, the heat transferred to the crystal is the latent heat of fusion.
 3. As a result, the pull rate generally varies inversely with the diameter as shown in Fig. 1.4.1.
 4. Pull rate affects the defect properties of CZ crystals in the following way. The condensation of thermal point defects (*i.e.*, vacancies and silicon self-interstitials) into small dislocation loops (termed microdefects) occurs as the crystal cools from the solidification temperature.
 5. The number of defects depends on the cooling rate, which is a function of pull rate and diameter, at temperatures above 950 °C.
 6. A pull rate of 2 mm/min eliminates defect formation by quenching the point defects in the lattice before they can agglomerate.
 7. We observe from Fig. 1.4.1 that large diameters preclude this pull rate for crystal diameters above 75 mm.

8. Large defects such as edge dislocations are not influenced by the point defect condensation process.
9. A related phenomenon is the remelting of the crystal that occurs because of temperature instabilities in the melt caused by thermal convection.
10. This condition can also be suppressed by attaining a pull rate of 2.7 mm/min, which is half the maximum attainable pull rate.

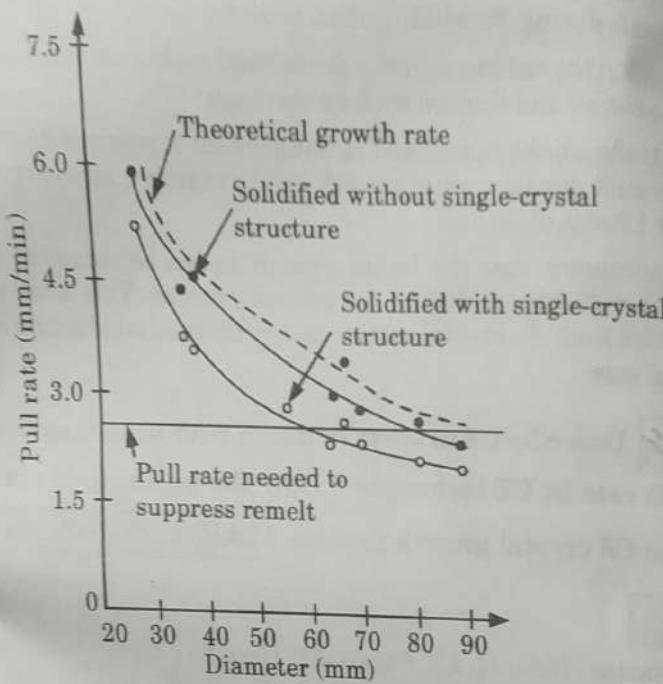


Fig. 1.4.1.

Que 1.5 A silicon ingot with 0.5×10^{16} boron atoms/cm³ is to be grown by CZ method. What should be the concentration of boron in the melt to obtain the required doping concentration? The segregation coefficient of the boron is 0.8. AKTU 2017-18, Marks 10

Answer

Given : $C_S = 0.5 \times 10^{16}$ B atoms/cm³, $k_0 = 0.8$ for boron

To Find : Concentration of boron.

1. The concentration of dopant in the solid phase of silicon is given by,

$$C_S = k_0 C_0 \left(1 - \frac{M}{M_0}\right)^{k_0 - 1}$$

2. Assume $M_0 = 2 M_{\text{ingot}}$

3. We want a concentration of $C_S = 0.5 \times 10^{16}$ atoms of B/cm³ halfway through the final grown ingot,

i.e., when $\frac{M}{M_0} = \frac{1}{4}$

4. The initial concentration of B atoms in the melt should be,

$$C_0 = \frac{C_S}{k_0 \left(1 - \frac{M}{M_0}\right)^{k_0-1}}$$

$$C_0 = \frac{0.5 \times 10^{16}}{0.8(1 - 0.25)^{0.8-1}} \text{ cm}^{-3}$$

$$= 5.90 \times 10^{15} \text{ B atoms/cm}^3.$$

Que 1.6. Explain crystal structure with its types.

Answer

Crystal structure :

1. The crystal structure is formed by associating every lattice point with an assembly of atoms or molecules or ions, which are identical in composition, arrangement and orientation.

2. Following are the different types of crystal structures :

i. **Body Centred Cubic Structure (BCC) :**

1. BCC structure has atoms at its each corner and one atom in its centre.
 \therefore Total atoms in BCC = $1/8 \times 8 + 1 = 2$ atoms
2. The coordination number of BCC arrangement is 8 and packing factor is 0.68.
3. The BCC structure can be generally seen in Lithium, Potassium, Sodium etc.

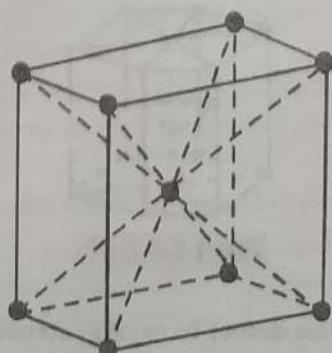


Fig. 1.6.1. BCC.

ii. Face Centred Cubic Structure (FCC) :

1. It consists of atoms at its each corner and one atom at centre of each face.
 \therefore Total atoms in FCC unit cell = $1/8 \times 8 + 1/2 \times 6 = 1 + 3 = 4$ atoms
2. The coordination number is 12 and packing factor is 0.74 for FCC arrangement.
3. The FCC structure can be generally seen in Copper, Gold, Silver and Lead etc.

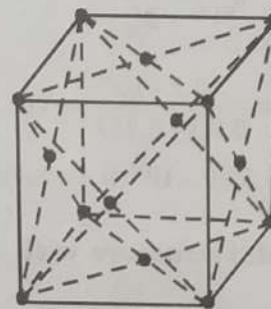


Fig. 1.6.2. FCC.

iii. Hexagonal Close-Packed Structure (HCP) :

1. The unit cell is like a hexagonal prism in HCP.
2. There are twelve corners and each corner have an atom and one atom at the centre of each of the two hexagonal faces and three atoms in the body of the cell. In total, seventeen atoms take part in formation of a HCP unit cell.

$$\therefore \text{Total atoms in HCP} = 12 \times \frac{1}{6} + 3 + 2 \times \frac{1}{2} = 6 \text{ atoms}$$

3. This is identical to FCC, having coordination number 12 and packing factor 0.74.
4. This HCP structure is generally seen in Zinc, Magnesium and Beryllium etc.

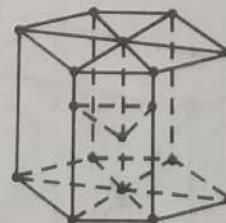


Fig. 1.6.3. HCP.

Que 1.7.

Classify the defect in crystal structure.

Answer**Classifications of defects :****i. Point defects :**

- Point defects take several forms as shown in Fig. 1.7.1 Any non-silicon atom incorporated into the lattice at either a substitutional (*i.e.*, replacing a host silicon atom) or interstitial (*i.e.*, between silicon atoms) site is considered a point defect.
- This is true whether the atom is an intentional dopant or unintentional impurity. Missing atoms create a vacancy in the lattice called a "Schottky defect" which is also considered a point defect.
- A silicon atom in an interstitial lattice site with an associated vacancy is called a "Frenkel defect."
- Vacancies and interstitials have equilibrium concentrations that depend on temperature.

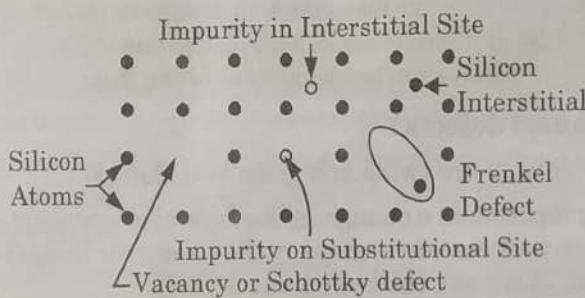


Fig. 1.7.1. The location and types of point defects in a simple lattice.

- Point defects are important in the kinetics of diffusion and oxidation. The diffusion of many impurities depends on the vacancy concentration, as does the oxidation rate of silicon.
- Vacancies and interstitials are also associated with defect formation in processing.

ii. Dislocations :

- Dislocations form the second class of defects. Two general categories of dislocations are screw and line (edge), the terms being aptly descriptive of their shape.
- Fig. 1.7.2 is a schematic representation of a line dislocation in a cubic lattice; it can be seen as an extra plane of atoms AB inserted into the lattice.
- The line of dislocation would be perpendicular to the plane of the page.
- Dislocations in a lattice are dynamic defects; that is, they can move under applied stress, disassociate into two or more dislocations, or combine with other dislocations.
- A vector notation developed by Burgers characterizes dislocations in the crystal as to their length and direction. The vector notation is also used to describe dislocation interactions.

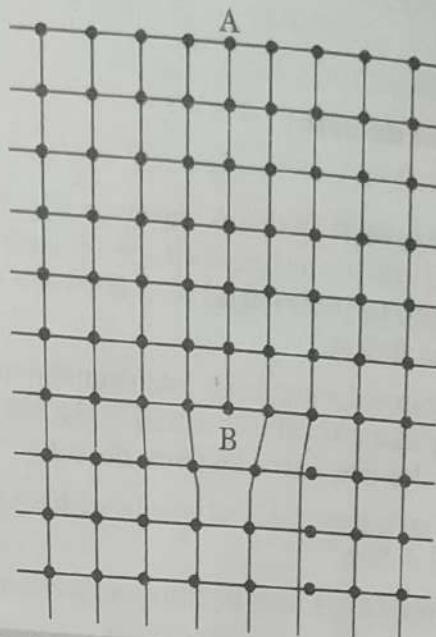


Fig. 1.7.2. An edge dislocation in a cubic lattice created by an extra plane of atoms. The line of the dislocation perpendicular to the page.

iii. Area (planar) defects :

1. Two area defects are twins and grain boundaries.
2. Twinning represents a change in the crystal orientation across a twin plane, such that certain symmetry (like a mirror image) exists across that plane. In silicon, the twin plane is {111}.
3. A grain boundary represents a transition between crystals having no particular orientation relationship to one another.
4. Grain boundaries are more disordered than twins and separate grains of single crystals in polycrystalline silicon.
5. Area defects, such as twins or grain boundaries, represent a large area discontinuity in the lattice.
6. The crystal on either side of the discontinuity may be otherwise perfect. The defects appear during crystal growth, but crystals having such defects are not considered usable for IC manufacture and are discarded.

iv. Volume defects :

1. Volume or three-dimensional defects form when a cluster of point defects join to form a three-dimensional void or a pore. Conversely a cluster of impurity atoms may join to form a three-dimensional precipitate.
2. The size of a volume defect may range from a few nanometers to centimeters or sometimes larger.
3. Such defects have a tremendous effect or influence on the behaviour and performance of the material.

Que 1.8. Discuss the crystal hardening techniques.

Answer

The generation of thermally induced glide dislocations can be reduced if the crystal is strengthened, so as to increase its critical resolved shear stress.

1. In silicon growth, for example, this occurs to some extent by the incorporation of oxygen due to the corrosive action of the SiO_2 crucible walls.
2. In GaAs, the intentional doping with group III and V impurities has been used for this purpose.
3. The mechanism of solution hardening is not fully understood at the present time.
4. It has been proposed that it is caused by the strain field created by the lattice misfit due to the impurity, which inhibits the propagation of dislocations, once they are formed.
5. The energy of movement of dislocations is much lower than their energy of formation, which may account for the effectiveness of this technique.
6. Isoelectronic doping is not used commercially for a number of reasons.
7. First, although the material is almost dislocation-free, it is extremely brittle so that it is hard to manufacture into slices, and tends to fracture during device fabrications.
8. Next, the addition of indium to the GaAs increases its lattice parameter, so that any subsequent growth on its surface occurs under conditions of lattice mismatch.
9. Finally, it was shown that double annealing of GaAs provided crystals which met the requirements for threshold voltage uniformity of field effect transistor device across a slice without a need for solid solution hardening.

Que 1.9. How the evaluation of crystals can be done ?**Answer**

1. Routine evaluation of crystals involves testing their resistivity, evaluating their crystal perfection, and examining their mechanical properties, such as size and mass.
2. Other less routine evaluations include measuring the crystals oxygen, carbon, and heavy metal content.
3. The evaluations of heavy metal content are made by minority carrier measurements or neutron activation analysis.
4. After growth, the crystal is usually weighed, then inspected visually.
5. Gross crystalline imperfections such as twinning are visible easily.

6. Sections of the ingot containing such defects are cut from the boule, i.e., are sections of the boule that are irregularly shaped.

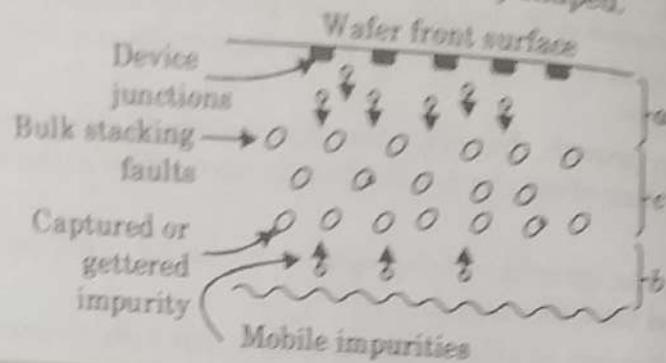


Fig. 1.9.1. Schematic of a denuded zone in a wafer cross section and gettering sites. *a* and *b* are zones denuded of defects, and *c* represents the region of intrinsic gettering.

7. Next the butt end of the ingot, or a slice cut from that position, is preferentially etched to reveal defects such as dislocations.
8. A common etchant is Sirtl's etch, which is a one-one mixture of HF acid and five-molar chromic acid.
9. This same etch can be used on polish and processed wafers to delineate other types of micro defects or impurity precipitates.
10. Cracks can be detected by a method that uses ultrasonic waves.

PART-2

Silicon Shaping, Processing Considerations, Wafer Cleaning Technology-Basic Concepts, Wet Cleaning, Dry Cleaning.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.10 Discuss different shaping operations involved in preparing wafers with diagram.

AKTU 2016-17, Marks 7.5

Answer

The shaping operations consist of two steps :

- i. **The seed and tang ends of the ingot are removed :**
1. The first step in the wafer preparation is to remove the tapered crystal ends, i.e., seed and tang ends from the boule. This process is known as end cropping.

2. The portion of the ingot that fails the resistivity and perfection evaluation should also be cut away.
 - ii. The surface of the ingot is ground to get a uniform diameter across the length of the ingot :
 1. In this step, we have to define the diameter of the material.
 2. The required diameter is achieved by surface grinding, which is a mechanical operation.
 3. Silicon ingots are grown slightly oversized because the automatic diameter control in crystal growth cannot maintain the needed diameter tolerance and crystal cannot be grown perfectly round.
 4. After diameter grinding, one or more flats are ground along the length of the ingot as shown in Fig. 1.10.1.

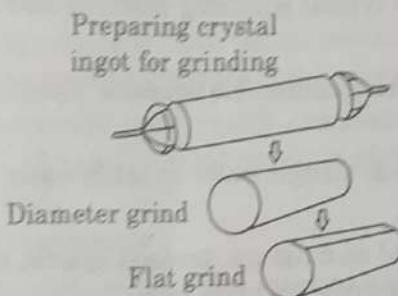


Fig. 1.10.1. Flat grind along the length of the ignot.

5. The larger flat is known as primary flat, which is used as a mechanical locator in automated processing equipment to position the wafer.
 6. It also serves to orient the IC device relative to the crystal.
 7. The smallest flat is called secondary flat and used to identify the orientation and type of the material as shown in Fig. 1.10.2.

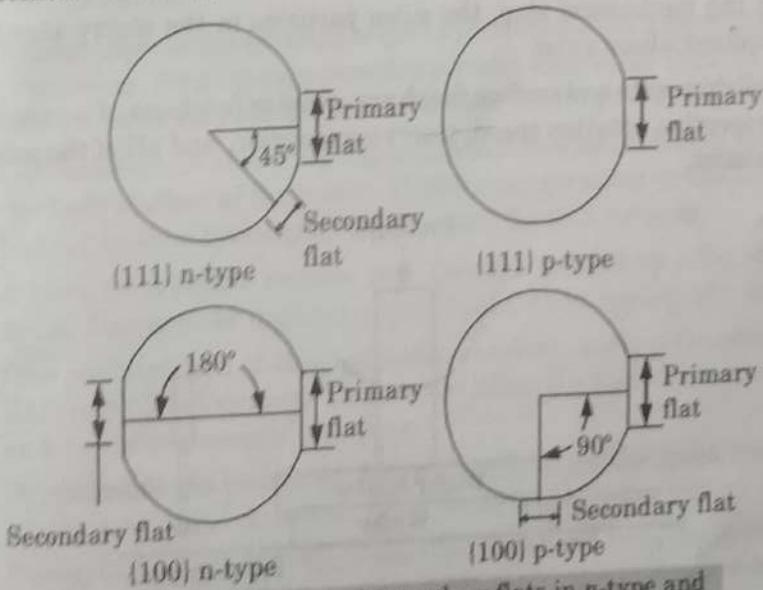


Fig. 1.10.2. Primary and secondary flats in *n*-type and *p*-type Si wafer at different orientations.

Que 1.11 Explain electronic grade silicon with neat diagram.
Explain the polishing process of silicon in detail.

AKTU 2016-17, Marks 10

Answer

- A. **Electronic grade silicon :** Refer Q. 1.2, Page 1-3F, Unit-1.
- B. **Polishing process of silicon :**
1. Polishing is the final step. Its purpose is to provide a smooth, specular surface on which device features can be photo engraved.
 2. Fig. 1.11.1 shows a typical polishing machine and a schematic of the process.
 3. The process requires considerable operator attention for loading and unloading.
 4. It can be conducted as a single wafer or batch-wafer process depending on the equipment.
 5. Wafers are mounted on a fixture, pressed against the pad under high pressure, and rotated relative to the pad.
 6. A mixture of polishing slurry and water, dripped onto the pad, does the polishing.
 7. The porosity of the pad is a factor in carrying slurry to the wafer for polishing.
 8. The slurry is a colloidal suspension of the SiO_2 particles in an aqueous solution of sodium hydroxide.
 9. In the mechanical step, the silica particles in the slurry abrade the oxidized silicon away.
 10. Polishing rate and surface finish are complex functions of pressure, pad properties, rotation speed, slurry composition, and pH of the polishing solution.

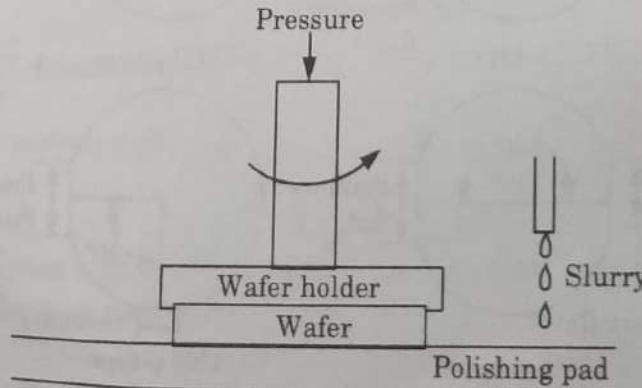


Fig. 1.11.1. Schematic of polishing process.

Que 1.12. Discuss the processing considerations of silicon wafers.

Answer

In the IC processing of silicon wafers, it is usually necessary to maintain the purity and perfection of the material and it is done by three methods :

i. **Chemical cleaning :**

1. Silicon wafers are usually cleaned chemically to remove organic films, heavy metals, and particulates.
2. The ammonium hydroxide and sulfuric acid based mixtures will also remove organic contaminants.
3. These cleaning solutions leave the surface of a wafer in a hydrophilic state due to the oxidizing nature of the peroxide.
4. Since the chemically grown oxide can contain impurities from the chemicals, it is usually removed by a short immersion in dilute hydrofluoric acid.

ii. **Gettering Treatments :**

1. Many VLSI circuits require low junction leakage currents. Narrow-base bipolar transistors are sensitive to conductive impurity precipitates, which act like shorts between emitter and collector.
2. These elements are located at interstitial or substitution lattice sites and are generation-recombination centres for carriers.
3. Gettering is a general term taken to mean a process that removes harmful impurities or defects from the regions in wafer where devices are fabricated.
4. Among these techniques are ways to pretreat silicon wafers prior to IC processing. Pregettering provides a wafer with sinks that can absorb impurities as they are introduced during device processing.
5. One technique of removing impurities involves intentionally damaging the back surface of the wafer. Mechanical abrasion methods such as lapping or sand blasting have been used for this purpose.
6. A more controllable process uses damage created by a focused heat beam. This process requires a threshold energy density of 5 J/cm^2 .
7. One configuration of this technique involves using a Q-pulsed, Nd : YAG laser. The laser beam is rastered along the back surface to create an array of micromachined spots.
8. Depending on the energy density and proximity of the spots, the silicon lattice is damaged and/or strained by the high-energy pulse.
9. During thermal processing, dislocations emanate from the spots. If the stresses placed on the wafer during furnace processing are low, the dislocations remain localized on the back surface.

10. The dislocations represent favourable trapping sites for fast-diffusing species. When trapped on the rear surface, these impurities are harmless.

iii. Thermal stress :

1. Wafers are typically processed in furnaces using racks with a high wafer diameter to spacing ratio.
2. When the wafer is removed from a high temperature furnace, the wafer edges cool rapidly by radiation to the surroundings, but the wafer centers remain relatively hot.
3. The resultant temperature gradient creates a thermal stress S that can be estimated as

$$S = aE\Delta T$$

where,

a = Coefficient of thermal expansion.

E = Young's modulus.

ΔT = Temperature difference across the wafer.

4. Stresses are usually kept to acceptable level by withdrawing wafers from the furnace slowly to minimize the temperature gradient or by lowering the furnace temperature to the point where the yield strength at the removal temperature exceeds the stresses imposed.
5. Oxygen precipitates can reduce the yield strength up to five fold.

Que 1.13 Why is cleaning of silicon wafer necessary before any processing steps ? Explain the crystal structure.

AKTU 2016-17, Marks 10

Answer

A. Reason :

1. The silicon surface must be prevented against contaminants during diffusion, which may interfere seriously with the uniformity of the diffusion profile.
2. The crystal defects may produce localized impurity concentration. This results in the degradation of junction characteristics.
3. Hence, the silicon crystals must be made highly perfect.

B. Crystal structure : Refer Q. 1.6, Page 1-8F, Unit-1.

Que 1.14 What is the objective of wafer cleaning ? Explain any one method of wafer cleaning.

Answer

- A. Objective of wafer cleaning :** The objective of wafer cleaning is the removal of particle and chemical impurities from the semiconductor surface without damaging or deleteriously altering the substrate surface.
- B. RCA :**
1. One highly successful approach to cleaning silicon, known as "RCA clean," is to use two solutions in sequence.
 2. The first of these consists of 1 : 1 : 5 to 1 : 2 : 7 volumes of NH_4OH : H_2O_2 : H_2O .
 3. Here, the H_2O_2 functions to oxidize all remaining organic contaminants on the surface, which are present because of incomplete removal of photoresist, and also because of airborne materials and physical handling.
 4. The NH_4OH is effective in removing heavy metals such as cadmium, cobalt, copper, iron, mercury, nickel, and silver by forming amino complexes with them.
 5. Next, a solution consisting of HCl : H_2O_2 : H_2O in a 1 : 1 : 6 to 1 : 2 : 8 volume ratio is used to remove aluminum, magnesium, and the light alkali ions, and to prevent displacement replating from the solution.
 6. Each of these steps is carried out for 10-20 min at 75-85°C, under conditions of rapid agitation. Nitrogen gas bubbling through the etchants is often used for this purpose.
 7. Finally, wafers are blown dry and stored in a clean environment until further processing.
 8. Results with this cleaning technique make it quite suitable for bipolar as well as MOS microcircuits, so that it is in wide use in industry at the present time.

Que 1.15. Write a short note on dry cleaning method.**Answer**

1. A major disadvantage of all wet cleaning systems is the use of large amounts of hazardous/toxic liquids.
2. Increasingly, interest has focused on the use of "dry" cleaning processes, with their inherent advantage of greatly reduced chemical usage.
3. An additional advantage is that they can be readily integrated into automated manufacturing tools.
4. A number of different chemicals can be used in dry cleaning processes. Anhydrous HF, as well as HF/ H_2O vapor, has been used for oxide removal.

5. Anhydrous NH_4OH , NF_3 , and HCl gases, followed by a rinse in de-ionized water, have also been used for removing heavy metal and alkali ions.
6. Oxygen, irradiated with ultraviolet light to produce ozone and atomic oxygen, is useful for removing organic photoresist residues, and is often used for cleaning the surface of GaAs.
7. Ozone has also been used in conjunction with $\text{HF}/\text{H}_2\text{O}$ vapor for light etching the surface of silicon slices.
8. Finally, plasma discharges have also been used for cleaning purposes.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Write a short note on Czochralski process.

Ans. Refer Q. 1.3.

Q. 2. Describe CZ process in detail with neat diagram. What is the pull rate in CZ technique ? How the pull rate is controlled during the CZ crystal growth process ?

Ans. Refer Q. 1.4.

Q. 3. A silicon ingot with 0.5×10^{16} boron atoms/cm³ is to be grown by CZ method. What should be the concentration of boron in the melt to obtain the required doping concentration? The segregation coefficient of the boron is 0.8.

Ans. Refer Q. 1.5.

Q. 4. Discuss different shaping operations involved in preparing wafers with diagram.

Ans. Refer Q. 1.10.

Q. 5. Explain electronic grade silicon with neat diagram. Explain the polishing process of silicon in detail.

Ans. Refer Q. 1.11.

Q. 6. Discuss the processing considerations of silicon wafers.

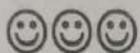
Ans. Refer Q. 1.12.

Q. 7. Why is cleaning of silicon wafer necessary before any processing steps ? Explain the crystal structure.

Ans. Refer Q. 1.13.

Q. 8. What is the objective of wafer cleaning ? Explain any one method of wafer cleaning.

Ans. Refer Q. 1.14.



2

UNIT

Epitaxy and Oxidation

CONTENTS

Part-1 : Epitaxy : Vapor-Phase Epitaxy, 2-2F to 1-10F
Molecular Beam Epitaxy,
Silicon on Insulators,
Epitaxial Evaluation

Part-2 : Oxidation : Growth Kinetics, 2-11F to 2-20F
Thin Oxides, Oxidation
Techniques and Systems,
Oxides Properties

PART- 1

*Epitaxy : Vapor-Phase Epitaxy, Molecular Beam Epitaxy,
Silicon on Insulators, Epitaxial Evaluation.*

CONCEPT OUTLINE

- Epitaxy offers doping profiles and material properties.
- Silicon on Insulator (SOI) is a recent non epitaxial approach to providing single-crystal silicon.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 2.1. What is epitaxial growth ? What are the advantages of epitaxial process over diffusion and Czochralski process ?

AKTU 2015-16, Marks 05

Answer

A. Epitaxial growth : Epitaxial growth is the process used to grow a thin crystalline layer on a crystalline surface (substrate). The substrate wafer acts as seed crystal. In this process, crystal is grown below melting point, which uses an evaporation method.

B. Advantage of epitaxial process over diffusion process :

1. Epitaxial process offers device engineers a means to control the doping profiles which is not attainable through diffusion process.
2. The physical and chemical properties of the wafer can be made different using epitaxial process.

C. Advantage of epitaxial process over Czochralski process :

1. Unlike the Czochralski process, crystalline thin films can be grown below the melting point using epitaxial process.

Que 2.2. Discuss Vapor-Phase Epitaxy (VPE).

Answer

1. In vapor-phase epitaxy (VPE), which is a subset of chemical vapor deposition (CVD), transport of the element(s) occurs in the form of volatile species which flow toward the substrate.

2. As indicated earlier, those species may be adsorbed (or chemisorbed) at the substrate surface where they react to form the element(s) of which the layer is composed; alternatively, one or more species may thermally convert to this form before being adsorbed on the surface.
3. The surface temperature is high, and the species are free to move by surface diffusion, until eventual incorporation, at kink sites, into the growth layer.
4. This process continues as the epitaxial film builds up.

Que 2.3. Explain basic transport process in VPE.

Answer

1. Let us consider the Reynolds number R_e , a dimensionless parameter that characterizes the type of fluid flow in the reactor,

$$R_e = \frac{D_r v \rho}{\mu}$$

where,

D_r = Diameter of reaction tube

v = Gas velocity

ρ = Gas density

μ = Gas viscosity

2. The carrier gas is usually hydrogen. A boundary layer of reduced gas velocity will form above the susceptor and at walls of the reaction chamber. The thickness of the boundary layer y is defined as

$$y = \left[\frac{D_r x}{R_e} \right]^{1/2}$$

where x is distance along the reaction chamber.

3. The fluxes of species going to and coming from the wafer surface are complex functions of several variables, including temperature, system pressure, reactant concentration and layer thickness. The flux is defined as

$$J = \frac{D dn}{dy}$$

and approximated as

$$J = \frac{D(n_g - n_s)}{y}$$

where n_g and n_s are the gas stream and surface reactant concentrations.

- D = Gas-phase diffusivity which is function of temperature and pressure.

y = Boundary layer thickness.

J = Reactant flux of molecules per unit area per unit time.

4. Under steady state conditions, the flux of reactant across the boundary layer is equated by a chemical reaction at the silicon surface where the film is growing.
5. In approximate terms

$$J = k_s n_s$$

where

k_s = chemical reaction rate constant representing the surface reaction.

$$n_s = \frac{n_g}{1 + \frac{k_s y}{D}}$$

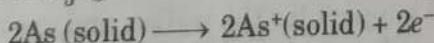
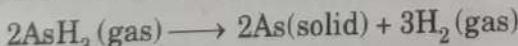
6. The quantity D/y is often called the gas-phase mass-transfer coefficient h_g .

Que 2.4. Describe dopant profile in brief.

AKTU 2015-16, Marks 05

Answer

1. Incorporating dopant atoms into the epitaxial layer involves the same considerations as the growth process requires.
2. Hydrides of the impurity atoms are used as the source of dopant.
3. Thermodynamic calculation indicates the hydrides are relatively stable because of large volume of hydrogen present in the reaction.
4. Arsine is being absorbed on the surface, decomposed, and being incorporated into the growing layer.



5. Interactions take place between the doping process and growth process.
6. In the case of boron and arsenic the formation of chlorides of these species is a competing reaction.
7. The growth rate of film influences the amount of dopant incorporated in the silicon.
8. At low growth rates equilibrium is established between the solid and the gas phases, which is not achieved at higher growth rates.
9. Dopant is released from the substrate through solid-state diffusion and evaporation.
10. This dopant is reincorporated into the growing layer either by diffusion through the gas phase or at interface.

Que 2.5. Explain auto doping process.**Answer**

1. It is manifested as an enhanced transition region between the layer and the substrate.
 2. The shape of doping profile, close to the substrate, is dominated by solid-state diffusion from the substrate and is a complementary error function if
- $$v < 2(D/t)^{1/2}$$
- v = Growth velocity
 D = Substrate dopant diffusion constant
 t = Deposition time
3. Auto doping is a time-dependent phenomenon. The dopant evaporating from the wafer surface is supplied from the wafer interior by solid-state diffusion.
 4. Thus, the flux of dopant from an exposed surface is not constant, but decreases with time.
 5. Once the auto doping is diminished, the intentional doping predominates, and the profile becomes flat.
 6. The extent of the auto doping tail is a function of the substrate dopant species and reaction parameters such as temperature and growth rate.
 7. Auto doping limits the minimum layer thickness that can be grown with controlled doping as well as the minimum doping level.

Que 2.6. What are susceptors? How it is used in epitaxial layers?**Answer**

1. Susceptors in epitaxial reactors are the analogs of crucibles in the crystal growing process.
2. They provide mechanical support for the wafers and are the source of thermal energy for the reaction in induction-heated reactors.
3. The geometric shape or configuration of the susceptor usually provides the name for reactor. Like crucibles the susceptor must be mechanically strong and non-contaminating to the process.
4. The susceptor must not react with the process reactants and by products.
5. Induction-heated reactors require a material that will couple to the RF field.
6. The preferred material is graphite, but graphite susceptors require a coating because they are relatively impure and soft.
7. A carbon blank is shaped to the required dimensions before the coating is applied.

8. Energy for the reaction has been supplied by heating the susceptor inductively.
 9. The energy is then transported to the wafer by conduction and radiation.
 10. Motor-generator sets at 10 kHz or self-excited RF oscillators at 500 kHz are used for heating.
 11. A water-cooled coil is placed close to the susceptor so coupling can occur.
 12. The coil can be inside or outside the reaction chamber depending on the design of the reactor.
 13. Radiant heating, a newer way of supplying energy to the reaction chamber, provides more uniform heating than inductive heating provides.
 14. The energy is supplied by banks of quartz halogen lamps.
 15. In most cases, process control involves maintaining gas flows and temperatures at the desired values.
 16. In modern equipment, the process cycle is generally microprocessor controlled, and the operator has only to bring wafers to the reactor and take the finished wafers away.
 17. Three basic reactor configurations are shown in Fig. 2.6.1.

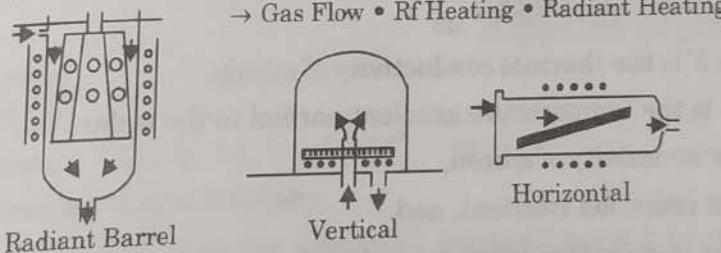


Fig. 2.6.1. Schematic of three common reactors.

There are :

- i. **Horizontal** : Horizontal reactors offer low cost construction.
 - ii. **Vertical or Pancake** : Pancake reactors are capable of very uniform deposition, but suffer from mechanical complexity.
 - iii. **Barrel** : Radiated-heated barrel reactors are also capable of uniform deposition, but are not suited for extended operation.

Que 2.7. Discuss about the epitaxial defects.

Answer

- Answer**

 1. Defects arising from the substrate wafer can be related to the bulk properties of the wafer or its surface finish.
 2. Impurity precipitates are one kind of surface defect that nucleate on an epitaxial stacking fault.
 3. Process related defects include slip. Dislocations accompany the formation of slip and of impurity precipitates from contamination.

4. These precipitates have been shown to degrade the quality of thin oxide layers used in MOSFET gates.
5. Fig. 2.7.1 is an example of an existing line dislocation continuing into epitaxial layer.

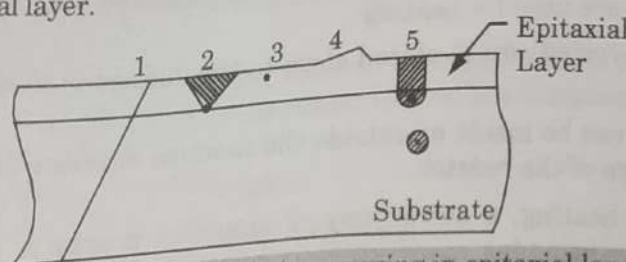


Fig. 2.7.1. Common defects occurring in epitaxial layers.

6. A temperature gradient exists normal to the substrate in an RF-heated reactor.
7. Slip due to this gradient (during epitaxy) is produced in the following manner.
8. Heat flow from the susceptor through the wafer equals subsequent radiation from the front surface and is given approximately by

$$\varepsilon k T^4 = \frac{KdT}{dx}$$

where K is the thermal conductivity of silicon,

dT/dx is the temperature gradient normal to the wafer,

ε is the emissivity of silicon,

k is the radiation constant, and

T is the nominal (or average) wafer temperature.

9. A front-to-rear temperature difference of only a few degrees causes a differential expansion of the wafer.
10. In effect, the wafer curls up on the susceptor. When the wafer edge loses contact with the susceptor, the edge temperature drops, causing still further bowing.
11. This radial temperature gradient results in sufficient stress to create dislocations in the wafer.
12. The inverted heat flow of the radiant-heated reactor minimizes this problem.
13. Misfit dislocations, caused by lattice mismatch when the substrate is highly doped, constitute another class of defects.
14. The resultant strain between the layer and substrate is relieved by the formation of dislocations.

Que 2.8. Write short notes on chemical vapor deposition (CVD).

Answer

1. The chemical vapour deposition (CVD) of single crystal silicon is usually performed in a reactor consisting of, in elemental form, a quartz reaction chamber into which a susceptor is placed.
2. The susceptor provides physical support for the substance wafer and provides more uniform thermal environment.
3. Deposition occurs at a high temperature at which several chemical reactions take place when process gases flow into the chamber.

Que 2.9. Explain molecular beam epitaxy in detail. What are its advantages over VPE ?

AKTU 2015-16, Marks 10

OR

Explain the principle of molecular beam epitaxy.

AKTU 2016-17, Marks 7.5

OR

What is Epitaxy ? Discuss Molecular Beam Epitaxy technique in brief. What are the advantages of MBE over VPE ?

AKTU 2017-18, Marks 10

Answer

A. Epitaxy : Refer Q. 2.1, Page 2-2F, Unit-2.

B. Molecular Beam Epitaxy :

1. Fig. 2.9.1 shows a simple schematic illustrating the basic principle of MBE.

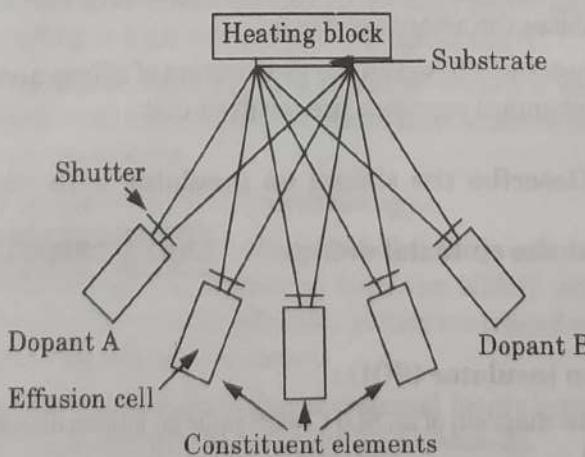


Fig. 2.9.1. Basic principle of MBE.

2. Molecular beam epitaxy (MBE) involves the direct physical transport of the material to be grown, or its components, to a heated substrate.

3. In essence, therefore, it is similar to vacuum evaporation, and growth is achieved by directing atomic or molecular beams in a well-controlled ultra-high-vacuum system.
 4. Both silicon and GaAs can be grown by MBE.
 5. Gallium and arsenic are used as source materials for GaAs. Additionally, aluminum is used for the growth of AlGaAs layers.
 6. Elemental silicon and germanium are used in growth of silicon and Si_xGe alloys.
 7. The beams of material to be transported are usually generated by thermal evaporation from crucibles known as effusion cells, which are shuttered in order to initiate and terminate the flux of the evaporant species.
 8. A series of effusion cells, each with a separate shutter, are set up so that their flux is directed to the substrate.
 9. In the case of silicon MBE, however, electron beam heating is commonly used to produce a significant flux of source material, and thermal evaporation is used for germanium.
 10. The substrate on which the wafer is mounted usually consists of a heated molybdenum block, which can be rotated during growth at a few rpm, for increased layer uniformity.
 11. Sample mounting is done by means of indium or gallium on its back face or by means of mechanical fasteners.
- C. Advantages of MBE over VPE :**
1. MBE is low temperature process which is advantageous for VLSI
 2. While preparing thin layers using MBE process, autodoping and autodiffusion both are minimized.
 3. The MBE process can be used for generating complicated doping profiles as it regulates the amount of dopant.
 4. As MBE process is based on the evaporation of silicon and the dopants, hence no chemical reactions are involved in it.

Que 2.10. / Describe the silicon on insulator with neat diagram.

Discuss about the epitaxial defects.

AKTU 2016-17, Marks 10

Answer

A. Silicon on insulator (SOI) :

1. A schematic diagram of an SOI CMOS built on silicon dioxide is shown in Fig. 2.10.1.
2. Compared with CMOS built on a bulk Si substrate, also called bulk CMOS, SOI's isolation scheme is simplified and does not need complicated well structures. Device density can thus be increased.

3. The latch-up phenomenon inherent in bulk CMOS circuits is also eliminated.

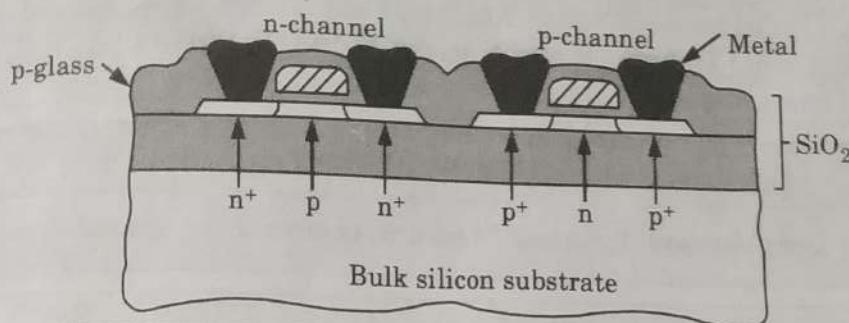


Fig. 2.10.1. Cross section of the silicon-on-insulator (SOI).

4. The parasitic junction capacitance in the source and drain regions can be significantly reduced with the insulating substrate.
 5. Additionally, significant improvement over bulk CMOS in radiation-damage toleration is achieved in SOI. This is because of the small volume of Si available for electron-hole pair generation by radiation. This property is particularly important for space applications.

B. Epitaxial defects : Refer Q. 2.7, Page 2-6F, Unit-2.

Que 2.11. What is latch up ? How latch up is avoided in CMOS technology ?

AKTU 2015-16, Marks 05

Answer

i. **Latch up :**

1. Latch up refers to short circuit formed between power and ground rails in an IC leading to high current and damage to the IC.
2. In CMOS transistor, latch up is the phenomenon of low impedance path between power rail and ground rail due to interaction between parasitic *pnp* and *npn* transistors.

ii. **Latch up avoided in CMOS technology :**

1. It is possible to design chips to be resistant to latch-up by adding a layer of insulating oxide that surround both the NMOS and the PMOS transistors. This breaks the parasitic silicon-controlled rectifier (SCR) structure between these transistors.
2. Devices fabricated in lightly doped epitaxial layers grown on heavily doped substrates are also less susceptible to latch-up.
3. Also to avoid the latch, a separate tap connection is put for each transistor.

PART-Z

Oxidation : Growth Kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxides Properties.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 2.12. Explain the growth mechanism of SiO_2 .

Answer

1. An oxide layer rapidly forms when silicon is exposed to an oxidizing agent because a silicon surface has a high affinity for oxygen.
2. The chemical reactions describing the thermal oxidation of silicon in oxygen or water vapour are given as :

$$\text{Si (solid)} + \text{O}_2 \longrightarrow \text{SiO}_2 \text{ (solid)}$$

$$\text{Si (solid)} + 2\text{H}_2\text{O} \longrightarrow \text{SiO}_2 \text{ (solid)} + 2\text{H}_2$$
3. The basic process involves shared valence electrons between silicon and oxygen; the silicon–oxygen bond structure is covalent.
4. During the course of the oxidation process, the $\text{Si}-\text{SiO}_2$ interface moves into the silicon. Its volume expands, however, so that the external SiO_2 surface is not coplanar with the original silicon surface.
5. Based on the densities and molecular weights of Si and SiO_2 , we can show that for growth of an oxide of thickness d , a layer of silicon with a thickness of $0.44d$ is consumed.
6. Fig. 2.12.1 shows the growth of SiO_2 . The framework of a model to describe silicon oxidation has been created.

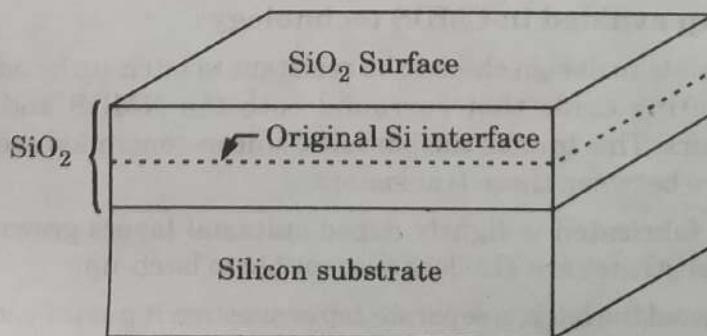


Fig. 2.12.1.

7. Radioactive tracer, marker, and infrared isotope shift experiments have established that oxidation proceeds by the diffusion of the oxidizing species through the oxide to the Si–SiO₂ interface, where the oxidation reaction occurs.

Que 2.13 Why oxidation is done ? Explain the chemistry and kinetics of growth using Deal-Grove's model.

AKTU 2015-16, Marks 10

Answer

A. **Reason :** Oxidation is done to form a high quality oxide in a controlled and repeatable manner. This mechanism serves as a mask against implant or diffusion of dopant into silicon and to provide surface passivation.

B. **Deal-Grove's model :**

1. Deal and Grove's model describes the kinetics of silicon oxidation.
2. The model is generally valid for temperatures between 700 and 1300 °C, partial pressures between 0.2 and 1.0 atm, and oxide thicknesses between 300 and 20,000 Å for oxygen and water ambient.
3. Fig. 2.13.1 shows the silicon substrate covered by an oxide layer that is in contact with the gas phase.

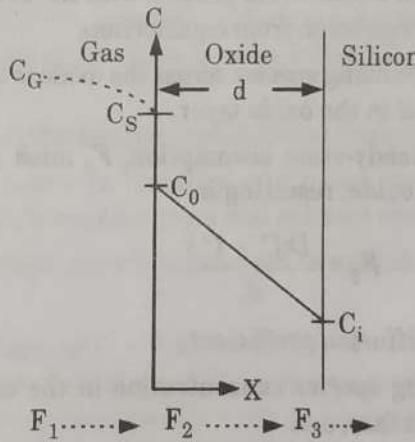


Fig. 2.13.1.

4. **The oxidizing species :**
 - i. are transported from the bulk of the gas phase to the gas-oxide interface with flux F_1 ,
 - ii. are transported across the existing oxide toward the silicon with flux F_2 , and
 - iii. react at the Si–SiO₂ interface with the silicon with flux F_3 .
5. For steady state, $F_1 = F_2 = F_3$. The gas-phase flux F_1 can be linearly approximated by assuming that the flux of oxidant from the bulk of the

gas phase to the gas-oxide interface is proportional to the difference between the oxidant concentration in the bulk of the gas C_G and the oxidant concentration adjacent to the oxide surface C_S ,

$$F_1 = h_G(C_G - C_S)$$

where h_G is the gas-phase mass transfer coefficient.

6. To relate the equilibrium oxidizing species concentration in the oxide, that in the gas phase, we have Henry's law,

$$C_o = H p_S$$

and

$$C^* = H p_G$$

where,

C_o = The equilibrium concentration in the oxide at the outer surface.

C^* = Equilibrium bulk concentration in the oxide.

p_S = The partial pressure in the gas adjacent to the oxide surface.

p_G = The partial pressure in the bulk of the gas.

7. Using Henry's law along with the ideal gas law :

$$F_1 = h (C^* - C_o)$$

where,

h = Gas-phase mass transfer coefficient.

8. Oxidation is a non-equilibrium process with the driving force being the deviation of concentration from equilibrium.
9. The flux of this oxidizing species across the oxide is taken to follow Fick's law at any point d in the oxide layer.
10. Following the steady-state assumption, F_2 must be the same at any point within the oxide, resulting in

$$F_2 = \frac{D(C_o - C_i)}{d_o}$$

where D is the diffusion coefficient,

C_i is the oxidizing species concentration in the oxide adjacent to the oxide-silicon interface, and

d_o is the oxide thickness.

11. Assuming that the flux corresponding to the Si-SiO₂ interface reaction is proportional to C_i ,

$$F_3 = k_s C_i$$

where k_s is the rate constant of chemical surface reaction for silicon oxidation.

Que 2.14 | Describe the effect of impurities and damage on the oxidation rate.

AKTU 2016-17, Marks 10

Answer**A. Effects of impurities are :****i. Water :**

1. A significant acceleration in the oxidation rate was observed by increasing the ppm of water vapour.
2. In these experiments, the oxygen was from a liquid source and the oxidation chamber was a double wall, fused-silica tube with N_2 flowing between the walls.
3. A precombustor and cold trap is used to achieve less than 1 ppm moisture level.

ii. Sodium : High concentration of sodium influence the oxidation rate by changing the bond structure in the oxide, thereby enhancing the diffusion and concentration of the oxygen molecules in the oxide.**iii. Halogen :**

1. Certain halogen species are intentionally introduced into the oxidation ambient to improve both the oxide and the underlying silicon properties.
2. Oxide improvements include a reduction in sodium ion contamination, increased dielectric breakdown strength, and a reduced interface trap density.
3. At or near the Si-SiO₂ interface, chlorine is instrumental in converting certain impurities in the silicon to volatile chlorides, resulting in gettering effect.
4. A reduction in oxidation-induced stacking faults is also observed.
5. Care must be taken in handling and using the halogens mentioned since the system's metallic parts and exhaust can corrode.
6. High concentration of halogen at high temperature can pit the silicon surface.

iv. Effect of damage : The silicon is usually damaged by ion-implantation of a non-electrically active species, or a group III or V dopant, separating damage effects from dopant effect is also difficult.**v. Group III and V elements :**

1. The common dopant elements in this group, when present in the silicon at high concentration levels, can enhance the oxidation behaviour.
2. The dopant impurities are redistributed at the growing Si-SiO₂ interface.
3. The effect results in a discontinuous concentration profile at the interface, the dopant segregates either into the silicon or into the oxide.
4. The redistribution of the impurity at the interface influences the oxidation behaviour.
5. If the dopant segregates into the oxide and remains there, the bond structure in the silica weakens.

6. This weakened structure permits an increased incorporation and diffusivity of the oxidizing species through the oxide, thus enhancing the oxidation rate.
7. Impurities that segregate into the oxide but then diffuse rapidly through it have no effect on the oxidation kinetics.

Que 2.15 Why oxidation is necessary in IC fabrication ? Calculate

the oxide thickness. Show that $\frac{X}{A/2} = \left[1 + \frac{t+\tau}{A^2/4B} \right]^{1/2} - 1$, reduces to

$X = \frac{B}{A}(t+\tau)$ for short time and to $X = \sqrt{B(t+\tau)}$ for long time,

where X = oxide thickness.

AKTU 2017-18, Marks 10

Answer

- A. **Reason :** Oxidation is done to form a high quality oxide in a controlled and repeatable manner. This mechanism serves as a mask against implant or diffusion of dopant into silicon and to provide surface passivation.
- B. **To show :**
 1. To calculate the rate of oxide growth, we define N_1 as the number of oxidant molecules incorporated into a unit volume of the oxide layer.
 2. Since the oxide has 2.2×10^{22} SiO₂ molecules/cm³ and one O₂ molecule is incorporated into each SiO₂ molecule, N_1 equals 2.2×10^{22} cm⁻³ for dry oxygen.
 3. The number for water-vapor oxidation is twice as big because two H₂O molecules are incorporated into each SiO₂ molecule.
 4. Combining various equations and assuming that an oxide may be present initially from a previous processing step or may grow before the assumptions in the model are valid, that is, $X = x$ at $t = 0$, the following equation can be generated,

$$X^2 + AX = B(t + \tau) \quad \dots(2.15.1)$$

where,

$$A = 2D \left[\frac{1}{k_s} + \frac{1}{h} \right] \quad \dots(2.15.2)$$

$$B = \frac{2DC^*}{N_1} \quad \dots(2.15.3)$$

$$\tau = \frac{x^2 + Ax}{B} \quad \dots(2.15.4)$$

5. The quantity τ represents a shift in the time coordinate to account for the presence of the initial oxide layer x .

6. Eq. (2.15.1) is the well-known, mixed linear-parabolic relationship.
 7. Solving eq. (2.15.1) for X as a function of time gives,

$$\frac{X}{A/2} = \left[1 + \frac{t + \tau}{A^2/4B} \right]^{1/2} - 1 \quad \dots(2.15.5)$$

8. One limiting case occurs for long oxidation times when $t \gg \tau$ and $t \gg A^2/4B$.

$$X^2 = Bt \quad \dots(2.15.6)$$

9. Eq. (2.15.6) is the parabolic law, where B is the parabolic rate constant. The other limiting case occurs for short oxidation times when $(t + \tau) \ll A^2/4B$.

$$X = \frac{B}{A}(t + \tau) \quad \dots(2.15.7)$$

10. Eq. (2.15.7) is the linear law, where B/A is the linear rate constant. Eq. (2.15.6) and (2.15.7) are the diffusion-controlled and reaction-controlled cases, respectively.

Que 2.16. Discuss the kinetics of thin oxide growth.

Answer

1. The structure of the oxide very close to the silicon-oxide interface and the oxidation process itself both involve uncertainties.
2. Thin oxide growth is influenced by the cleaning techniques used and the purity of the gases used.
3. The wafers were chemically cleaned, dried in nitrogen, and loaded into the furnace in an argon ambient.
4. Native oxide thickness and subsequent oxide growth when the ambient was switched to dry O_2 were measured using in situ ellipsometry.
5. The enhancement in oxidation rate was found to decay exponentially with thickness. The extent of thickness enhancement is not a strong function of surface orientation, doping level, or oxygen partial pressure.
6. Reduced pressure oxidation offers an attractive way of growing thin oxides in a controlled manner. Oxides between 30 and 140 Å thick have been grown at 900 to 1000°C using oxygen at a pressure of 0.25 to 2.0 Torr.
7. The observed kinetics are parabolic, and the rate constants agree with values extrapolated from atmospheric pressure.
8. Oxides obtained by this technique etch at the same rate as dry oxides obtained at 950°C and 1 atm.
9. The equal etch rate indicates a similar composition and structure between the two oxides. The intrinsic breakdown fields are high (10 to 13 MV/cm) and distributed over a narrow range.

10. All indications are that the reduced pressure oxides are very uniform, homogeneous, and similar to thicker oxides prepared at atmospheric pressure.
11. A two-step process sequence has been devised in which a uniform reproducible oxide of small defect density is formed at a moderate temperature (1000°C or less) using a dry $\text{O}_2\text{-HCl}$ ambient.
12. The second step consists of a heat treatment in N_2 , O_2 , and HCl at 1150°C to provide passivation and to bring the oxide thickness to the desired level.
13. Such a processing scheme takes advantage of beneficial effects occurring in both the lower and higher temperature ranges.

Que 2.17. What is pre-oxidation cleaning ?

Answer

1. Before being placed in a high temperature furnace, wafers must be cleaned to eliminate both organic and inorganic contamination arising from previous processing steps and handling.
2. Such contamination can degrade the electrical characteristics of the devices and can contribute to reliability problems.
3. Particulate matter is removed by either mechanical or ultrasonic scrubbing.
4. Immersion processing techniques were the preferred chemical cleaning methods until the development of centrifugal spray methods, which eliminate the build-up of contaminants as cleaning progresses.
5. The chemical cleaning procedure usually involves removing the organic contamination, followed by inorganic ion and atom removal.
6. A common cleaning procedure uses a $\text{H}_2\text{O}-\text{H}_2\text{O}_2-\text{NH}_4\text{OH}$ mixture to remove organic contamination by the solvating action of ammonium hydroxide and the oxidizing effect of the peroxide.
7. This process can also complex some group I and II metals. To remove heavy metals a $\text{H}_2\text{O}-\text{H}_2\text{O}_2-\text{HCl}$ solution commonly used.
8. This solution prevents replating by forming soluble complexes with the removed ions, and the process is performed between 75 and 85°C for 10 to 20 minutes followed by a quench, rinse, and spin dry.
9. The necessary consideration for optimizing the cleaning procedure for silicon wafers prior to high-temperature operations.
10. Modern diffusion (oxidation) furnaces are microprocessor controlled to provide repeatable sequencing, temperature control, and gas flow (mass flow control).
11. The microprocessor control provides a feedback loop for comparing the various parameters to the desired ones, and for making the appropriate changes.

Que 2.18. Explain plasma oxidation technique for the growth of oxide layer. Explain the application of SiO_2 layer in IC fabrication.

AKTU 2016-17, Marks 10

Answer

A. Plasma oxidation technique :

1. The anodic plasma-oxidation process offers the possibility of growing high-quality technique.
2. This process has all the advantages associated with low temperature processing, such as minimized movement of previous diffusions and suppression of defect formation.
3. Anodic plasma oxidation can grow reasonably thick oxides at low temperatures.
4. Plasma oxidation is a low temperature vacuum process, usually carried out in pure oxygen discharge.
5. The plasma is produced either by a high-frequently discharge or a DC electron source.
6. The growth rate of the oxide typically increases with increasing substrate temperature, plasma density, and substrate dopant concentration.

B. Application of SiO_2 layer in IC fabrication :

1. It acts as a diffusion mask permitting selective diffusions into silicon wafer through the window etched into oxide.
2. It is used for surface passivation which is nothing but creating protective SiO_2 layer on the wafer surface. It protects the junction from moisture and other atmospheric contaminants.
3. It serves as an insulator on the water surface. Its high relative dielectric constant, which enables metal line to pass over the active silicon regions.
4. SiO_2 acts as the active gate electrode in MOS device structure.
5. It is used to isolate one device from another.
6. It provides electrical isolation of multilevel metallization used in VLSI.

Que 2.19. Explain in detail about the masking properties of SiO_2 .

Answer

1. A silicon dioxide layer can provide a selective mask against the diffusion of dopant atoms at elevated temperatures.
2. A predeposition of dopant by ion-implantation, chemical diffusion or spin-on techniques typically results in a dopant source at or near the surface of the oxide.

3. During the high temperature drive-in step, diffusion in the oxide must be slow enough with respect to diffusion in the silicon that the dopants do not diffuse through the oxide in the masked region and reach the silicon surface.
4. The oxide thickness necessary to prevent the inversion of a lightly doped silicon substrate of opposite conductivity.
5. Oxides used for masking common impurities in conventional device processing are 0.5 to 0.7 μm thick.
6. The impurity masking properties result when the oxide is partially converted into a silica impurity oxide "glass" phase, and prevents the impurities from reaching the SiO_2 -Si interface.
7. The values of diffusion constants for various dopants in SiO_2 depend on the concentration, properties, and structure of the SiO_2 .
8. The commonly used *n*-type impurities *P*, Sb and As as well as the most frequently used *p*-type impurity *B*, all have very small diffusion coefficients in oxides and are compatible with oxide masking.

Que 2.20: Describe the various charges present in oxidation layer in detail.

AKTU 2016-17, Marks 7.5

Answer

1. Various charges and traps are associated with the thermally oxidized silicon, some of which are related to the transition region.
2. A charge at the interface can induce a charge of the opposite polarity in the underlying silicon, thereby affecting the ideal characteristics of the MOS device. This results in both yield and reliability problems.

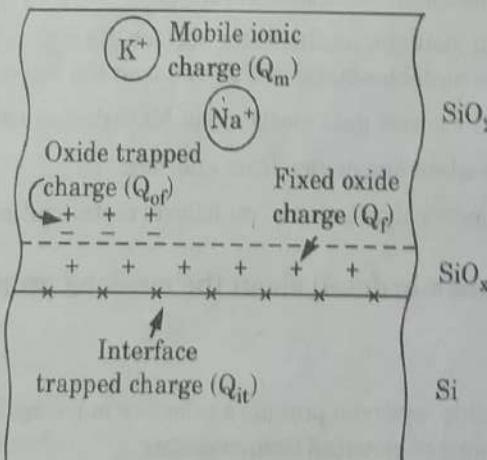


Fig. 2.20.1.

3. Fig. 2.20.1 shows general types of charges. These charges are described by $N = Q/q$,

where,

Q = The net effective charge per unit area
(Coulombs/cm²) at Si-SiO₂ interface,

N = The net number of charges per unit area at the
Si-SiO₂ interface, and

q = The electric charge.

4. Located at the Si-SiO₂ interface, interface-trapped charges Q_{it} have energy states in the silicon-forbidden bandgap and can interact electrically with the underlying silicon.
5. These charges are thought to result from several sources, including structural defects related to the oxidation process, metallic impurities, or bond-breaking processes.
6. The fixed oxide charge Q_f (usually positive) is located in the oxide within approximately 30 Å of the Si-SiO₂ interface. Q_f cannot be charged or discharged.
7. Its density ranges from 10¹⁰/cm² to 10¹²/cm², depending on oxidation and annealing conditions as well as orientation. Q_f is related to the oxidation process itself.
8. The mobile ionic charge Q_m is attributed to alkali ions such as sodium, potassium, and lithium in the oxide as well as to negative ions and heavy metals.
9. The alkali ions are mobile even at room temperature, when electric fields are present.
10. Densities range from 10¹⁰/cm² to 10¹²/cm² or higher and are related to processing materials, chemicals, ambient, or handling.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. What is epitaxial growth ? What are the advantages of epitaxial process over diffusion and Czochralski process ?

Ans. Refer Q. 2.1.

Q. 2. Describe dopant profile in brief.

Ans. Refer Q. 2.4.

Q. 3. Explain molecular beam epitaxy in detail. What are its advantages over VPE ?

Ans. Refer Q. 2.9.

Q. 4. Describe the silicon on insulator with neat diagram.
Discuss about the epitaxial defects.

Ans. Refer Q. 2.10.

Q. 5. Why oxidation is done? Explain the chemistry and kinetics of growth using Deal-Grove's model.

Ans. Refer Q. 2.13.

Q. 6. Describe the effect of impurities and damage on the oxidation rate.

Ans. Refer Q. 2.14.

Q. 7. Why oxidation is necessary in IC fabrication? Calculate

$$\text{the oxide thickness. Show that } \frac{X}{A/2} = \left[1 + \frac{t + \tau}{A^2 / 4B} \right]^{1/2}$$

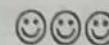
$$\text{reduces to } X = \frac{B}{A} (t + \tau) \text{ for short time and to } X = \sqrt{B(t + \tau)}$$

for long time, where X = oxide thickness.

Ans. Refer Q. 2.15.

Q. 8. Explain plasma oxidation technique for the growth of oxide layer. Explain the application of SiO_2 layer in IC fabrication.

Ans. Refer Q. 2.18.



3

UNIT

Lithography and Polysilicon Film Deposition

CONTENTS

- Part-1 :** Lithography : Optical **3-2F to 3-10F**
Lithography, Electron
Beam Lithography
Photomasks, Wet
Chemical Etching
- Part-2 :** Dielectric and Polysilicon **3-10F to 3-16F**
Film Deposition : Deposition
Processes of Polysilicon,
Silicon Dioxide, Silicon Nitride

PART-1

Lithography : Optical Lithography, Electron Beam Lithography, Photomasks, Wet Chemical Etching.

CONCEPT OUTLINE

- A lithograph is a less expensive picture made by impressing in turn several flat, embossed slabs, each covered with greasy ink of a particular colour, onto a piece of stout paper.
- Photoresists are of two types :
 - Negative resist
 - Positive resist.

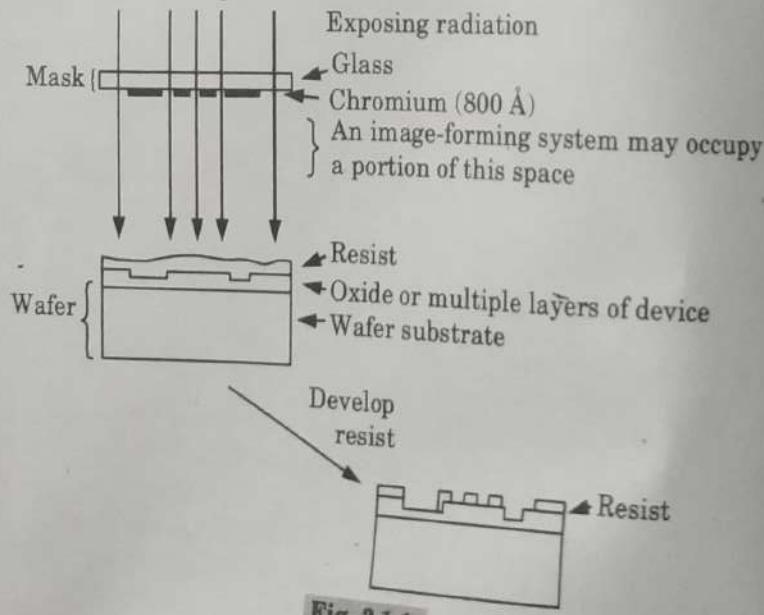
Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 3.1. Explain lithography with neat schematic diagram.

AKTU 2016-17, Marks 10

Answer

- Fig. 3.1.1 illustrates schematically the lithographic process used to fabricate circuit chips.



2. The exposing radiation is transmitted through the "clear" parts of a mask.
3. The circuit pattern of opaque chromium blocks some of the radiation. This type of chromium glass mask is used with ultraviolet (UV) light. Other types of exposing radiation are electrons, X-rays, or ions.
4. Shadow (proximity) printing may be employed where the gap between mask and wafer is small.
5. In the case of a non-existent gap, the method is called contact printing.
6. Or some sort of image forming system (a lens, for example) may be interposed between mask and wafer.
7. Therefore, lithography for integrated circuit manufacturing is analogous to the lithography of the art world.
8. The artist corresponds to the circuit designer. The slabs are masks for the various circuit levels.
9. The press corresponds to the exposure system, which not only exposes each level but also aligns it to a completed level.
10. The ink may be compared either with the exposing radiation or with the radiation-sensitive resist. And the paper can represent the wafer into which the patterns will be etched, using the resist as a stencil.
11. Optical lithography has penetrated the " $1 \mu\text{m}$ barrier" of resolution.
12. As other lithographic techniques such as those using electron, X-ray, or ion radiation have improved, so has optical lithography.
13. For these competing methods large teams of capable people have been working steadily for ten years or more.
14. Several methods have only one or two key problems remaining to be solved. Solution generally requires application of standard, but difficult and meticulous, engineering.

Que 3.2. Explain proximity printing and projection printing and compare these two.

AKTU 2017-18, Marks 10

Answer

A. Proximity printing :

1. Proximity printing has the advantage of longer mask life because there is no contact between the mask and the wafer.
2. Typical separations between mask and wafer are in the range of 20 to $50 \mu\text{m}$. Resolution is not as good as in contact printing or projection printing.
3. Proximity printing in the schematic form of a mask with a long slit of width W separated from a parallel image plane (wafer) by a gap g .

4. We assume that g and W are larger than the wavelength λ of the imaging light and that $\lambda \ll g < W^2/\lambda$ - the region of Fresnel diffraction.
5. Then the diffraction that forms the image of the slit is a function only of the particular combination of λ , W , and g which we shall call the parameter Q where;

$$Q = W\sqrt{2(\lambda g)}$$

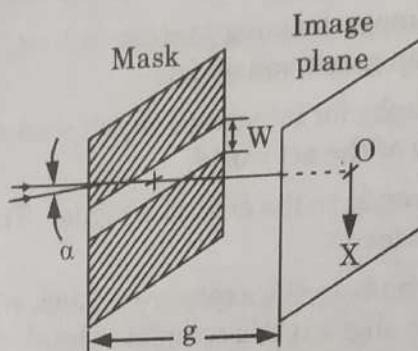


Fig. 3.2.1. Proximity printing.

B. Projection printing :

1. Projection printing offers higher resolution than proximity printing together with large separation between mask and wafer.
2. Four important performance parameters of a printer are resolution, level-to-level alignment accuracy, throughput, and depth of focus.
3. The resolution of an optical imaging system of numerical aperture $NA = \sin \alpha$ with light of wavelength λ is, according to Rayleigh's criterion, $0.61\lambda/\sin \alpha$ - the separation of two barely resolved point sources.
4. The Rayleigh depth of focus is given by $\pm \lambda/(2 \sin^2 \alpha)$. However, near the limiting resolution of the system, the contrast in the image is uselessly small.
5. Now, consider a general optical system with no aberrations.
6. An aberration is a departure of the imaging wavefront from the spherical form; that is, a spherical wave diverging from a point in the object plane is converted to a spherical wave converging to a point in the image plane.
7. The f number of the system is $F = D_i/2R$ and the numerical aperture is $NA = \sin \alpha = R/\sqrt{(D_i^2 + R^2)} \approx R/D_i$.

where, R is the radius of the exit pupil, and

D_i is the distance from this pupil to the image plane.

8. We want to recall briefly some results from the theory of image formation and to show how the transfer functions differ for coherent and incoherent imaging systems.
9. For coherent object illumination all points in the object have wave amplitudes with fixed phase relationships, and all phases have the same time dependence.
10. The field amplitude at point x_i, y_i in the image plane (the wafer) will be called $U_i(x_i, y_i)$.
11. It is caused by a field distribution $U_o(x_o, y_o)$ in the object plane (the mask).
12. We define a pupil function $P(x, y)$ to represent the transmission of the round exit pupil, or hole, shown in Fig. 3.2.2. For points (x, y) within the pupil, $P = 1$; for points outside, $P = 0$. The simplest object is a point source at $x_o, y_o = 0$.
13. The image of this source has the form

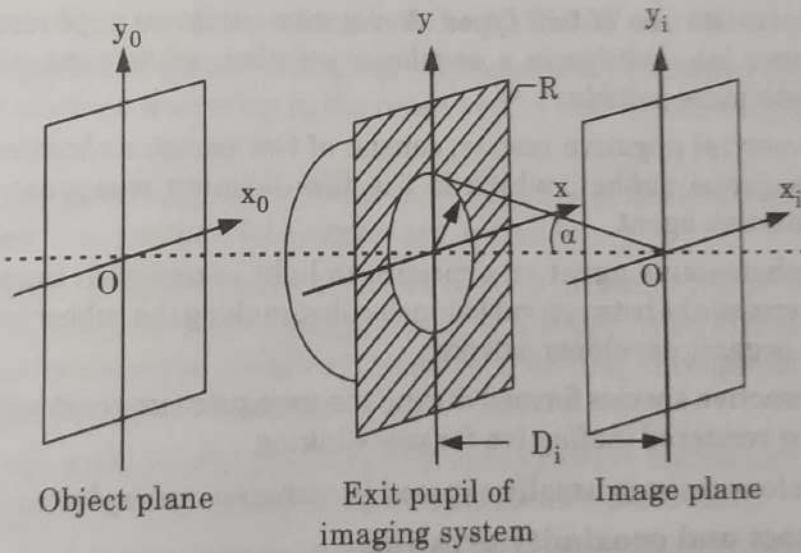


Fig. 3.2.2.

$$I_i(x_i, y_i) = \frac{\pi}{(2\lambda F)^2} [2J_1(s)/s]^2, s = \left(\frac{\pi}{\lambda F}\right) \sqrt{x_i^2 + y_i^2}$$

This is the well-known Airy pattern. J_1 is the first-order Bessel function.

14. It is also called the point-spread function because the projection system spreads the point into the circular image represented by the diameter (twice the distance from the origin to the first zero of J_1) of the pattern in $2.4 \mu F$.
15. Thus, the smaller the wavelength and the f number (or the larger the NA) of the projection system, the better the resolution.

Projection printing

C. Comparison :	Proximity printing	Projection printing offers low resolution.
S.No.	Proximity printing offers high resolution	There is low room for improvement.
1.	There is more room for improvement.	
2.		

Ques 3.3. Explain in detail about the optical lithography.

Answer

Optical lithography: Optical lithography comprises the formation of images with visible or ultraviolet radiation in a photoresist using contact proximity, or projection printing.

i. Optical resists :

1. Photoresists are of two types. A negative resist on exposure to light becomes less soluble in a developer solution, while a positive resist become more soluble.
2. Commercial negative resists, consist of two parts : a chemically inert polysoprene rubber, which is the film-forming components and a photoactive agent.

3. The photoactive agent on exposure to light reacts with the rubber to form crosslinks between rubber molecules, making the rubber less soluble in an organic developer solvent.
4. The reactive species formed during the exposure can react with oxygen and be rendered ineffective for crosslinking.
5. Therefore resist is usually exposed in nitrogen atmosphere.

ii. Contact and proximity printing :**a. Contact printing :**

1. In contact printing a photomask is pressed against the resist-covered wafer with pressures typically in the range of 0.05 atm to 0.3 atm and exposed by light of wavelength near 400 nm.
2. Very high resolution ($\leq 1 \mu\text{m}$ linewidth) is possible, but because of spatial nonuniformity of the contact, resolution may vary considerably across the wafer.
3. To provide better contact over the whole wafer, a thin (0.2 mm) flexible mask has been used; $0.4 \mu\text{m}$ lines have been formed in a $0.98 \mu\text{m}$ resist.

4. The contact produces defects in both the mask and the wafer so that the mask, whether thick or thin, may have to be discarded after a short period of use.

b. Proximity printing: Refer Q. 3.2, Page 3-3F, Unit-3.**iii. Projection printing:** Refer Q. 3.2, Page 3-3F, Unit-3.

Que 3.4. A proximity printer operates with a 10 mm mask-wafer gap and a wavelength of 420 nm. Another printer uses a 40 mm gap with wavelength 250 nm. Which offers higher resolution?

Answer

$$\text{We know that } \theta = W \sqrt{\frac{2}{\lambda g}}$$

- A. $\lambda = 0.43 \mu\text{m}$, $g = 10 \mu\text{m}$, $\theta = 0.68 \text{ W}$
B. $\lambda = 0.25 \mu\text{m}$, $g = 40 \mu\text{m}$, $\theta = 0.45 \text{ W}$

Therefore A gives higher resolution.

Que 3.5. Write a short note on electron lithography.

Answer

1. Electron lithography offers higher resolution than optical lithography because of the small wavelength of the 10-50 keV electrons.
2. The resolution of electron lithography systems is not limited by diffraction, but by electron scattering in the resist and by the various aberrations of the electron optics.
3. Scanning electron-beam systems have been under development for two decades, and commercial systems are available.
4. The EBES (Electron Beam Exposure System) machine has proved to be the best photomask pattern generator. It is widely used in mask shops. Because of the serial nature of the pattern writing, throughput is much less than for optical systems.
5. However, some special products such as microwave transistors have for many years been manufactured by direct wafer patterning.
6. In the first application to low-volume integrated circuits, some levels were patterned optically and some by electron beam.

Que 3.6. Explain in detail about the generation of photomask with suitable diagram.

Answer

1. The first use of electron-beam pattern generators has been in photomask making.
2. Fig. 3.6.1 shows two methods of making a photomask. On the left a reticle is patterned with an optical pattern generator that is a machine which under computer control, exposes and places pattern elements to form the chip image at $10 \times$ scale and which can make 60 to 100 exposures per minute.
3. The pattern element is the image of an illuminated aperture of variable size.

4. The reticle is then used as the object in a step-repeat camera, which steps the reduced image to fill the desired mask area.
5. Stepping accuracy is interferometrically controlled. The master mask produced may be used in a projection printer or copied and the copies used in a contact printer.
6. If an electron-beam pattern generator is used to make the reticle, the main advantage is speed in the case of complex chips.
7. A large, dense chip can require 20 hours or more of optical pattern generator time, but only two hours or less of electron-beam pattern generator time.
8. On the right, Fig. 3.6.1 shows the more efficient method of electron-beam patterning. The mask may be either a $1 \times$ mask or a $5 \times$ or $10 \times$ reticle for use in a wafer stepper.

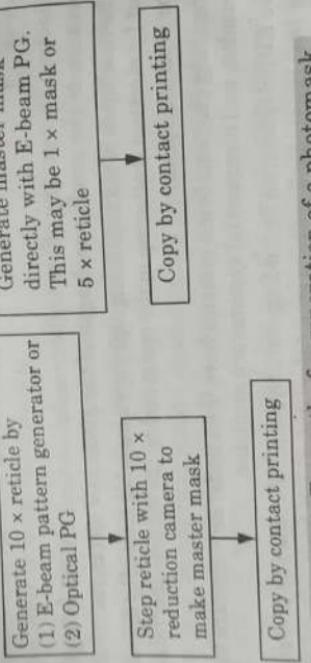


Fig. 3.6.1. Two paths for generation of a photomask.

Que 3.7. Explain the kinetics of wet etching. How gold is etched?

AKTU 2017-18, Marks 05

Answer

A. Wet chemical etching :

1. Wet chemical etching of any material can be considered as a sequence of three steps :
 - a. Transport of the reactant to the surface.
 - b. Reaction at the surface.
 - c. Movement of reaction products into the volume of etchant solution.
2. An etch process which is limited by the rate of surface reaction will tend to enhance surface roughness and promote faceting, since the surface activity is a strong function of localized defects and crystallographic orientation.
3. Etching can be limited by the rate of diffusion of the etchant through a non moving layer which covers the surface.

- Typically, a doubling of etch rate occurs with each 10°C rise in temperature.
4. temperature, the development of etch processes for use in a manufacturing environment requires that attention be paid to these factors, in addition to the choice of chemicals and their concentrations.
 5. The temperature-dependent characteristics of etching can be used to advantage in situations where it is essential to keep residual surface contamination to a minimum.
 6. Here, the strategy is to use a high dilution with deionized water, and maintain a reasonable etch rate by operating at an elevated temperature.
 7. In other situations, where precise etch control is desired, the use of a cooled etch solution is indicated.
 8. A number of chemical reagents, and their mixtures, are used for etching purposes.
 9. Many of these are available in "transistor-grade" purity and are preferred in order to minimize contamination of the semiconductor during processing.
 10. Water is an intrinsic component of all of these reagents. Moreover, deionized water is invariably used as a diluent.
 11. Mixtures of nitric acid and hydrochloric acid (in a mixing ratio of 1:3 also called aqua regia) are able to etch gold at room temperature.

- B. The very strong oxidative effect of this mixture stems from the formation of nitrosyl chloride (NOCl) via
- $$\text{HNO}_3 + 3 \text{ HCl} \longrightarrow \text{NOCl} + 2 \text{ Cl} + 2 \text{ H}_2\text{O}$$
1. While free Cl radicals formed in the solution keep the noble metal dissolved as Cl-complex (tetrachloro gold-(III)-acid = HAuCl_4).
 2. HNO_3/HCl mixtures are not stable and decompose accompanied by the formation of nitrogen oxides and Cl_2 .
 3. The etch rate of aqua regia for gold is approx. $10 \mu\text{m}/\text{min}$ (at room temperature) and can be increased to several $10 \mu\text{m}/\text{min}$ at elevated temperatures.

Ques 3.8. Explain semiconductor etching.

Answer

1. In semiconductor etching, the primary oxidizing species is $(\text{OH})^-$. Often this is formed by the dissociation of water, which is present in the etchant, as given by
- $$\text{H}_2\text{O} \rightleftharpoons (\text{OH})^- + \text{H}^+$$
2. The formation of an oxide presents a barrier to further oxidation of the semi-conductor, so that it is necessary to add additional chemicals for its dissolution into compounds or complexes,

3. Stirring removes these from the semiconductor surface so that further oxidation can proceed.
4. The choice of complexing agents for this purpose is quite wide; both acids and bases can be used, in addition to salts involving (CN_x^-) and (NH_x^-) groupings.
5. In practical systems, the choice is limited by the availability of high-purity reagents and by the desire to avoid metallic ion contamination.
6. Thus, hydrofluoric acid is the invariable choice for silicon etching systems.
7. GaAs systems often use sulfuric, phosphoric, and citric acid, or ammonium hydroxide.

Que 3.9. What are PR materials ? What are the properties of different PR ?

AKTU 2017-18, Marks 05

Answer

A. PR materials :

1. The photorefractive (PR) effect is a reversible photoinduced refractive index change in materials combining photosensitivity, transport, and electrooptical effects.
2. The materials which exhibit photorefractive effect are known as photorefractive (PR) materials.

B. Properties of photorefractive (PR) materials :

1. **Large effective nonlinearity :** One of the main features of photorefractive materials is the large effective nonlinearity with inherent optical real-time information processing properties using all three dimensions in space.
2. **Large nonlinear response :**
 - i. PR materials have a large nonlinear response at low intensities in the milliwatt range.
 - ii. The response time of the materials varies from microseconds for semiconductor materials to seconds for some electro-optic crystals.

3. Beam-coupling effect :

- i. An important property of a number of photorefractive crystals is the beam-coupling effect-a transfer of energy between two coherently intersecting beams inside the crystal.
- ii. This unique property of nonreciprocal energy transfer has led to a number of applications in the general context of image processing.

PART-2

Dielectric and Polysilicon Film Deposition : Deposition Processes of Polysilicon, Silicon Dioxide, Silicon Nitride.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 3.10. Explain in detail about the deposition process reactions.

Answer

1. The choice of a particular reaction is often determined by the deposition temperature, the film properties, and certain engineering aspects of the deposition.
2. The most common reactions for depositing silicon dioxide for VLSI circuits are oxidizing silane, SiH_4 , with oxygen at 400 to 450°C decomposing tetraethoxysilane, $\text{Si}(\text{OC}_2\text{H}_5)_4$, at 650 to 750°C and reacting dichlorosilane, SiCl_2H_2 , with nitrous oxide at 850 to 900°C.
3. Doped oxides are prepared by adding a dopant to the deposition reaction.
4. The hydrides-arsine, phosphine, or diborane are often used because they are readily available gases; however, halides or organic compounds such as phosphorus tribromide or trimethylphosphite can also be used.
5. Silicon nitride is prepared by reacting silane and ammonia at atmospheric pressure at 700 to 900°C, or by reacting dichlorosilane and ammonia at reduced pressure at 700°C.
6. Plasma-deposited silicon nitride is deposited by reacting silane with ammonia or nitrogen in a glow discharge between 200 and 350°C.
7. This reaction is useful for depositing passivation coatings over finished devices where higher temperatures cause unwanted reactions between the silicon and the metal conductors.

Que 3.11. Write a short note on polysilicon.

Answer

1. Polysilicon is used as the gate electrode in MOS devices. A metal or metal silicide, such as tungsten or tantalum silicide, may be deposited over the polysilicon gate to increase the electrical conductivity.
2. Polysilicon is also used for resistors, conductors, and to ensure ohmic contact to shallow junctions.
3. The polysilicon is deposited by pyrolyzing silane between 575 and 650 °C in a low-pressure reactor. The chemical reaction is
$$\text{SiH}_4 \longrightarrow \text{Si} + 2\text{H}_2$$
4. Further processing for polysilicon gates involves doping, etching, and oxidation.

5. Two low-pressure processes are common for depositing polysilicon.
6. One uses 100 % silane at a pressure of 25 to 130 Pa (0.2 to 1.0 Torr).
7. The other process is performed at the same total pressure but uses 20 to 30 % silane diluted in nitrogen.
8. Both processes deposit polysilicon on 10 to 200 wafers per run with thickness uniformities of $\pm 5\%$. The deposition rates are 10 to 20 nm/min.

Que 3.12. Explain the structure of polysilicon.

Answer

1. The structure of polysilicon is strongly influenced by dopants, impurities, deposition temperature, and post-deposition heat cycles.
2. Polysilicon deposited below 575 °C is amorphous with no detectable structure.
3. Polysilicon deposited, above 625 °C is polycrystalline and has a columnar structure.
4. Crystallization and grain growth occur when either amorphous or columnar polysilicon is heated.
5. After high-temperature heat cycles, there are no significant structural differences between polysilicon that is initially amorphous or columnar.
6. The deposition temperature at which the transition from amorphous to columnar structure occurs is well defined but depends on many variables, such as deposition rate, partial pressure of hydrogen, total pressure, presence of dopants, and presence of impurities (O , N , or C).
7. The transition temperature is between 575 and 625°C for depositions in an LPCVD reactor.
8. After deposition, polysilicon recrystallizes when heated; however, the crystallization temperature is strongly influenced by dopants and impurities.
9. Oxygen, nitrogen, and carbon impurities stabilize the amorphous structure to temperatures above 1000°C.

Que 3.13. How polysilicon can be doped ?

Answer

1. Polysilicon can be doped by diffusion, implantation, or the addition of dopant gases during deposition. All the three methods are used for device fabrication.
2. Diffusion is a high temperature process that results in low resistivities.
3. The dopant concentration in diffused polysilicon often exceeds the solid solubility limit, with the excess dopant segregated at the grain boundaries.

4. The resistivity of implanted polysilicon depends primarily on implant dose, annealing temperature and annealing time.
5. Once these traps are saturated with dopants, resistivity decreases rapidly and approaches the resistivity for implanted single crystal silicon.
6. Implanted polysilicon has about ten times higher resistivity than diffused polysilicon because of the differences in dopant concentrations.
7. Doped polysilicon that is crystalline when deposited shows almost no change in resistivity after annealing.

Que 3.14. Explain the properties of polysilicon.

Answer

1. The chemical and physical properties of polysilicon often depend on the film structure (amorphous or crystalline) or on the dopant concentration.
2. The etch rate of polysilicon in a plasma depends on the dopant concentration.
3. Polysilicon that is heavily phosphorus-doped etches at higher rates than undoped or lightly doped polysilicon.
4. Polysilicon is usually etched in a $\text{CF}_4 + \text{O}_2$ or a $\text{CF}_3\text{CH} + \text{Cl}_2$ plasma.
5. The optical properties of polysilicon depend on its structure. The imaginary part of the dielectric function is particularly structure sensitive.
6. Crystalline polysilicon has sharp maxima in the dielectric function near 295 and 365 nm (4.2 and 3.4 eV).
7. Other properties of polysilicon are its density, 2.3 g/cm^3 ; coefficient of thermal expansion, $2 \times 10^{-6}/^\circ\text{C}$; and temperature coefficient of resistance, $1 \times 10^{-3}/^\circ\text{C}$.

Que 3.15. Write a short note on oxygen doped polysilicon.

Answer

1. The addition of oxygen to polysilicon increases the film resistivity.
2. The resulting material, semi-insulating polysilicon (SIPOS), is used as a passivating for high voltage devices.
3. SIPOS is deposited when silane reacts with small amounts of nitrous oxide at temperatures between 600 and 700 $^\circ\text{C}$.
4. The two simultaneous reactions are

$$\text{SiH}_4 \longrightarrow \text{Si} + 2\text{H}_2$$

$$\text{SiH}_4 + x\text{N}_2\text{O} \longrightarrow \text{SiO}_x + 2\text{H}_2 + x\text{N}_2$$
5. The quantity of nitrous oxide in the reaction determines the film composition and resistivity.
6. SIPOS has a multi-phase microstructure containing crystalline silicon, amorphous silicon, silicon dioxide, and silicon monoxide.

7. The specific composition depends on the deposition temperature, the amount of nitrous oxide used in the reaction, and the time and temperature of post-deposition anneals.
8. SIPOS used in VLSI circuits contains between 25 and 40 at % oxygen.

Que 3.16. Discuss in about silicon dioxide (SiO_2).

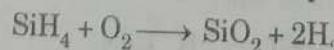
Answer

1. Silicon dioxide films can be deposited with or without dopants.
2. Undoped silicon dioxide is used as an insulating layer between multilevel metallizations, an ion-implantation or diffusion mask, a capping layer over doped regions to prevent outdiffusion during heat cycles, and to increase the thickness of thermally grown oxides.
3. Phosphorus-doped silicon dioxide is used as an insulator between metal layers, as a final passivation over devices, and as a gettering source.
4. Oxides doped with phosphorus, arsenic, or boron are used occasionally as diffusion sources.
5. The processing sequence for silicon dioxide depends on its specific use in the device.
6. Oxides used as insulators between conducting layers are deposited, densified by annealing, and etched to open windows.
7. A solution containing fluoride or a CHF_3 plasma etches the oxide.
8. Phosphorus-doped oxides, used in the flowed glass process, are heated to a temperature between 950 and 1100°C so that the oxide softens and flows, providing a smooth topography which improves the step coverage of the next metallization.
9. Phosphorus-doped oxides used for passivation are deposited at temperatures lower than 400 °C, and areas for bonding are opened by etching.

Que 3.17. Explain the deposition methods of silicon dioxide.

Answer

1. Several deposition methods are used to produce silicon dioxide. They are characterized by different chemical reactions, reactors and temperatures.
2. The chemical reactions for phosphorus doped oxides are



3. Under normal deposition conditions, hydrogen is formed rather than water. The deposition can be carried out at atmospheric pressure in a continuous reactor.

4. Silicon dioxide deposits at temperature near 900°C and at a reduced pressure by reacting dichlorosilane with nitrous oxide,

$$\text{SiCl}_2\text{H}_2 + 2\text{N}_2\text{O} \longrightarrow \text{SiO}_2 + 2\text{N}_2 + 2\text{HCl}$$
5. This deposition gives excellent uniformity and is used to deposit insulating layers over polysilicon, however, this oxide frequently contains small amounts of chlorine that may react with the polysilicon and cause film cracking.
6. Doped oxides are formed by adding small amounts of the dopant hydrides during the deposition. Because the dopant hydrides are very toxic, other dopant compounds are often used.
7. Dopant halides or organic compounds are safer than hydrides but less convenient because they must usually be vapourized from solid or liquid sources.

Que 3.18. | What are the properties of SiO_2 ?

Answer

Properties of SiO_2 are :

- i. **Composition :** SiO_2 deposited at low temperatures contains hydrogen. This hydrogen is bonded within the silicon-oxygen network as silanol (SiOH), hydride (SiH) or water (H_2O).
- ii. **Thickness :** Film thickness is measured by a stylus instrument, reflectance spectroscopy, ellipsometry, or a prism coupler. Automated instruments suitable for routine use are available for all these techniques. While all four techniques are generally suitable for measuring silicon dioxide films, each has specific limitations.
- iii. **Structure :** Deposited silicon dioxide has an amorphous structure consisting of SiO_4 . Its structure is similar to that of fused silica.
- iv. **Reactivity :** SiO_2 deposited at low temperature reacts with atmospheric moisture, especially if the oxide contains phosphorus. The phosphorus oxygen double bond undergoes a reversible hydrolysis.
- v. **Refractive index and stress :** The refractive index of SiO_2 is 1.458 at a wavelength of $0.6328 \mu\text{m}$. Stress in SiO_2 depends on deposition temperature, deposition rate, annealing treatments, dopant concentration, water content and film porosity.

Que 3.19. | How is the silicon nitride used ? Explain its deposition variables.

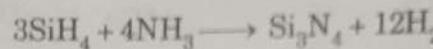
AKTU 2016-17, Marks 7.5

Answer

A. Silicon nitride used :

1. Silicon nitride (Si_3N_4) is used for passivating silicon devices because it serves as an extremely good barrier to the diffusion of water and sodium.

2. These impurities cause device metallization to corrode or devices to become unstable.
3. Silicon nitride is also used as a mask for the selective oxidation of silicon.
4. The silicon nitride oxidizes slowly and prevents the underlying silicon from oxidizing.
5. This process of selective oxidation produces nearly planar device structures.
6. Silicon nitride is chemically deposited by reacting silane and ammonia at atmospheric pressure at temperature between 700 and 900°C or by reacting dichlorosilane and ammonia at reduced pressure at temperatures between 700 and 800°C. The chemical reactions are



7. The reduced-pressure technique has the advantage of good uniformity and high wafer throughput.
8. Thermal growth of silicon nitride by exposing silicon to ammonia at temperatures between 1000 and 1100 °C has been investigated, but the resulting films contain oxygen and are very thin (≤ 10 nm).

B. Deposition variables :

1. Silicon nitride depositions at reduced pressure are controlled by temperature, total pressure, reactant concentrations, and temperature gradients in the furnace.
2. The temperature dependence of the deposition rate is similar to that of polysilicon.
3. The activation energy for the silicon nitride deposition is about 1.8 eV (41 kcal/mole).
4. The deposition rate increases with increasing total pressure or dichlorosilane partial pressure, and decreases with an increasing ammonia to dichlorosilane ratio.
5. A temperature ramp, with the furnace tube hotter at the exhaust end, is required for uniform depositions.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

- Q. 1. Explain lithography with neat schematic diagram.**
Ans. Refer Q. 3.1.

Q. 2. Explain proximity printing and projection printing and compare these two.

Ans. Refer Q. 3.2.

Q. 3. Explain the kinetics of wet etching. How gold is etched ?

Ans. Refer Q. 3.7.

Q. 4. What are PR materials ? What are the properties of different PR ?

Ans. Refer Q. 3.9.

Q. 5. Explain the structure of polysilicon.

Ans. Refer Q. 3.12.

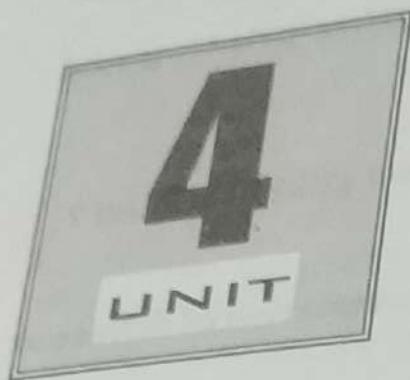
Q. 6. Discuss in about silicon dioxide (SiO_2).

Ans. Refer Q. 3.16.

Q. 7. How is the silicon nitride used ? Explain its deposition variables.

Ans. Refer Q. 3.19.





Diffusion & Ion-Implantation

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PART - 1

*Diffusion : Models of Diffusion in Solids, Fick's
1-Dimensional Diffusion Equation.*

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 4.1. Discuss diffusion. Find diffusion constant for :

- i. Interstitial diffusion
- ii. Substitutional diffusion

AKTU 2015-16, Marks 7.5

Answer**Diffusion :**

1. Diffusion is a relatively straightforward process by which impurities may be introduced into selected regions of a semiconductor, for the purpose of altering its electronic properties.
2. Both single and multiple diffusion steps can be used for this purpose.
3. Diffusion describes the process by which atoms move in a crystal lattice.
4. In silicon technology, diffusion allows the formation of :

 - a. Sources and drain for metal-oxide-semiconductor (MOS) devices.
 - b. The active region bipolar transistors.
 - c. It is extensively used because it is ideally adapted to batch processes where many slices are handled in a single operation.

Interstitial diffusion :

1. It involves impurity jumps via interstitial voids.
2. These voids are arranged tetrahedrally in the zinc-blende lattice. Although same are occupied by point defects, their equilibrium concentration is low, even at normal diffusion temperature ($700 - 1100^\circ \text{C}$).
3. Each tetrahedral void can readily accommodate an interstitial atom.
4. However, there is an energy barrier which must be surmounted in order for interstitially located impurity atoms to jump from one void to the next. This barrier for interstitial diffusers is periodic in nature, as shown in Fig. 4.1.1.
5. The jump frequency, v , is the frequency with which thermal energy fluctuations occur with sufficiently large magnitude to overcome this potential barrier.

Let,

$$E_m = \text{Activation energy of impurity migration, in eV}$$

$$\cdot T = \text{Temperature of the lattice, in K}$$

v_0 = Frequency of lattice vibrations, about 10^{13} - 10^{14} /s

6. This is the frequency with which atoms strike the potential barrier depicted in Fig. 4.1.1.
7. Assuming a Boltzmann energy distribution the probability that atom has an energy in excess of E_m is given by $e^{-E_m/kT}$.

$$v = 4v_0 e^{-E_m/kT} \quad \dots(4.1.1)$$

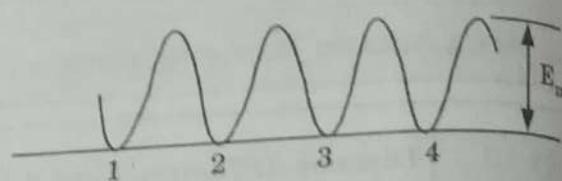
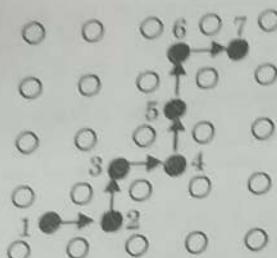


Fig. 4.1.1. Interstitial diffusion by jumping.

8. The diffusivity of an interstitial impurity is given by,

$$D = \frac{vd^2}{6} \quad \dots(4.1.2)$$

9. Substituting eq. (4.1.2) into eq. (4.1.1) then we get,

$$D = \frac{4v_0 d^2}{6} e^{-E_m/kT}$$

$$D = D_0 e^{-E_m/kT}$$

where D is the diffusivity,

D_0 is the diffusion constant, and

E_m is the activation energy of diffusion.

ii. Substitutional Diffusion :

1. The jumping of substitutional diffusers requires first that there be available vacant sites into which they can move.
2. These vacant sites are Schottky defect, with energy of formation given E_s ($= 2.6$ eV for silicon).
3. Thus the atoms fraction of such defects in a crystal is $e^{-E_s/kT}$. The charge state of these defects, which is related to the impurity concentration, must also be included in the calculation of diffusivity.
4. If the potential barrier associated with impurity migration by this process is E_n , then the probability of atoms having a thermal energy in excess of this value is $e^{-E_n/kT}$. Typical values for E_n range from 0.6 to 1.2 eV.
5. Finally, each lattice site has four tetrahedrally situated neighbours, so that each jump can be made in one of four different ways.

$$v = 4V_0 e^{-E_s/kT} e^{-E_n/kT}$$

$$= 4V_0 e^{-(E_s+E_n)/kT}$$

6. Values of $E_n + E_s$ ($= E_d$), predicted from this simple theory, are found to be slightly larger than those actually observed.
7. This is because the binding energy between an impurity atom and its neighboring atom is less than that between two adjacent atoms in the lattice.
8. The diffusivity for a substitutional impurity is thus

$$D = \frac{4v_0 d^2}{6} e^{-E_d/kT}$$

$$= D_0 e^{-E_d/kT}$$

Que 4.2. Explain Fick's law of diffusion.

OR

Derive the diffusion equation. How the depth of diffusion is controlled during diffusion process? Give the solution of Fick's Law.

AKTU 2017-18, Marks 10

Answer

Fick's law of diffusion :

1. Fick assumed that in a dilute liquid or gaseous solution, in the absence of convection, the transfer of solute atoms per unit area in a one-dimensional flow can be described by the following equation,

$$J = -D \frac{\partial C(x, t)}{\partial x} \quad \dots(4.2.1)$$

where, J is the rate of transfer of solute per unit area or the diffusion flux,

C is the concentration of solute,

x is the coordinate axis in the direction of the solute flow,

t is the diffusion time, and

D is the diffusivity or diffusion constant.

2. Eq. (4.2.1) states that the local rate of transfer (local diffusion rate) of solute per unit area per unit time is proportional to the concentration gradient of the solute, and defines the proportionality constant as the diffusivity of the solute.

3. The negative sign on the right-hand side of eq. (4.2.1) states that the matter flows in the direction of decreasing solute concentration (i.e., the gradient is negative).

4. Eq. (4.2.1) is called Fick's first law of diffusion.

5. From the law of conservation of matter, the change of solute concentration with time must be the same as the local decrease of the diffusion flux, in the absence of a source or a sink.

$$\text{i.e., } \frac{\partial C(x, t)}{\partial t} = - \frac{\partial J(x, t)}{\partial x} \quad \dots(4.2.2)$$

6. Substituting eq. (4.2.1) into eq. (4.2.2) yield Fick's second law of diffusion in one-dimensional form,

$$\frac{\partial C(x, t)}{\partial t} = \frac{\partial}{\partial x} \left[D \frac{\partial C(x, t)}{\partial x} \right] \quad \dots(4.2.3)$$

7. When the concentration of the solute is low, the diffusivity at a given temperature can be considered as a constant, and eq. (4.2.3) becomes,

$$\frac{\partial C(x, t)}{\partial t} = D \frac{\partial^2 C(x, t)}{\partial x^2} \quad \dots(4.2.4)$$

8. Eq. (4.2.4) is often referred to as Fick's second law of diffusion.

Que 4.3. What is Fick's law of diffusion? Boron is diffused into an n -type single crystal substrate with doping concentration of 10^{15} atm/cm 3 . Assume diffusion time is 1 hr, surface concentration = 1×10^{18} cm $^{-3}$ and depth of junction is 2 μ m, determine diffusivity.

AKTU 2015-16, Marks 05

Answer

- A. Fick's law of diffusion : Refer Q. 4.2, Page 4-4F, Unit-4.
 B. Numerical :

Given : $x = 2 \times 10^{-6}$ m = 2×10^{-4} cm, $t = 1$ hr = 3600 sec
 $C_s = 10^{18}$ cm $^{-3}$

To Find : Diffusivity.

1. The diffusion equation is,

$$C(x, t) = \frac{Q_T}{\sqrt{\pi D t}} \exp \left(-\frac{x^2}{4 D t} \right)$$

2. By setting $x = 0$ we obtain the surface concentration

$$C_s = C(0, t) = \frac{Q_T}{\sqrt{\pi D t}} = 10^{15} \text{ cm}^{-3}$$

where Q_T is the total impurity in atoms/cm 2 .

$$C_s = 10^{15} \exp \left[\frac{4 \times 10^{-8}}{4 \times 3600 D} \right]$$

$$10^{18} = 10^{15} \exp \left[\frac{10^{-10}}{36D} \right]$$

$$D = 4 \times 10^{-13} \text{ cm}^2/\text{s}$$

\Rightarrow

Que 4.4. If the measured phosphorus profile is represented by a Gaussian function with a diffusivity $D = 2.3 \times 10^{-13}$ atoms/cm 2 , the

measured surface dose is 10^{16} atoms/cm² and the junction depth is 1 μm at a surface concentration of 10^{15} atoms/cm³. Calculate the diffusion time.

AIKTU 2017-18, Marks 10

Answer

Given : $D = 2.3 \times 10^{-13}$ atoms/cm², $x = 10^{-6}$ m = 10^{-4} cm, $N_s = 10^{15}$ atoms/cm³.

To Find : Diffusion time.

1. We know, $N(x, t) = \frac{Q_T}{\sqrt{\pi D t}} \exp\left(-\frac{x^2}{4 D t}\right)$

or, $N(x, t) = N_s \exp\left(-\frac{x^2}{4 D t}\right)$

$$1 \times 10^{15} = 1 \times 10^{16} \exp\left(-\frac{(10^{-4})^2}{4 \times 2.3 \times 10^{-13} \times t}\right)$$

$$\exp\left(\frac{1.0869 \times 10^4}{t}\right) = 1000$$

$$t = \frac{1.0869 \times 10^4}{6.9077} = 1573 \text{ s} \approx 26 \text{ mins}$$

PART-2

*Diffusion of Impurities in Silicon and Silicon Dioxide,
Diffusion Equations, Diffusion Profiles.*

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 4.5. Describe the impurity behaviour in silicon.

Answer

1. The movement of impurities belonging to group III and V of the periodic table is caused by a combination of substitutional diffusion and interstitial diffusion.
2. Their motion is thus strongly influenced by the concentration and the charge state of lattice point defects.

3. They include the *p*-type impurities aluminium, boron, gallium and indium, as well as the *n*-type impurities antimony, arsenic and phosphorus.
4. Impurities which move interstitially in silicon belongs to groups I and VIII of the periodic table.
5. These include alkali metal such as lithium, potassium and sodium, and gases such as argon, helium and hydrogen.
6. They occupy interstitial sites in silicon and are usually electronically inactive.
7. Most transition elements diffuse by interstitial-substitutional mechanism and end up in both types of sites.
8. The dissociation of the substitutional into an interstitial and a vacancy is the mechanism involved in most cases.
9. The kick-out mechanism defines the diffusional movement of gold and platinum in silicon.

Que 4.6. Explain about the deep-lying impurities.

Answer

Deep-lying impurities can be described as follows :

- i.

 1. These impurities usually diffuse by an interstitial-substitutional mechanism, at about five to six orders of magnitude faster than substitutional diffusers.
 2. As a result, considerable error can occur from out-diffusion effects when the specimens are cooled to room temperature.
 3. Attempts at rapid quenching usually result in the generation of a large number of crystal defects and obscure the interpretation of data.

- ii.

 1. Their movement is described by a diffusivity which is a function of both concentration and temperature.

- iii.

 1. On freezing, most deep-lying impurities end up in both electronically active and electronically inactive sites. The fractions of each type differ widely from element to element.
 2. Thus about 90 % of the gold resides in active sites, while the corresponding figure for nickel is only 0.1 %.
 3. The analysis of the results is complex, since analytical techniques such as resistivity measurements only provide information on the part that is electronically active.
 4. On the other hand, secondary ion mass spectrometry techniques result in information on the entire impurity content.

- iv. The electronically active part of all these dopants exhibits one or more deep levels. Thus their average diffusion parameters cannot be measured by $p-n$ junction techniques, as for substitutional dopants.
- v. 1. The interaction energy between an interstitial-substitutional diffuser and the strain field associated with a dislocation tends to favor clustering in the neighborhood of this dislocation.
 2. Thus the diffusion process is dominated by the defect nature of the crystal, and the experimental data are difficult to interpret meaningfully.
 3. In addition, many of these impurities form compounds with silicon over certain ranges of diffusion temperature.
 4. These tend to segregate in clusters in the silicon lattice and are often electronically inactive.
 5. Material doped with these impurities is usually sensitive to heat treatments.

Que 4.7. Describe the term diffusion equation with the help of diagram.

Answer

1. Fick's second law may be derived by applying considerations of continuity.
2. Consider the flow of particles in a crystal of cross section A, between planes P_1 and P_2 separated by dx , as shown in Fig. 3.2.
3. The rate of accumulation of particles in the region between planes is $A \left(\frac{\partial N}{\partial t} \right) dx$.
4. This can also be written as the difference between the fluxes flowing into and out of the region.

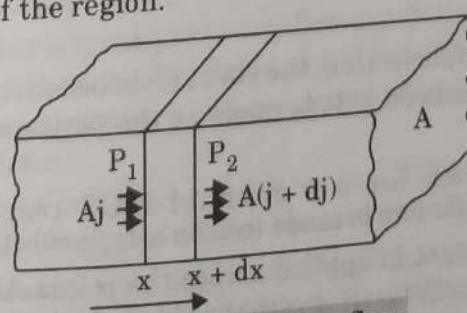


Fig. 4.7.1. Diffusing flux.

5. The flux entering the region at P_1 is Aj , and the flux leaving the region at P_2 is $A(j + dj)$. The net flux entering the region is thus $-A dj$. Hence,

$$A \frac{\partial N}{\partial t} dx = -A dj \quad \dots(4.7.1)$$

6. But $dj = (\partial j / \partial x) dx$. Hence,

$$\frac{\partial N}{\partial t} = \frac{\partial}{\partial x} \left(D \frac{\partial N}{\partial x} \right) \quad \dots(4.7.2)$$

7. Eq. (4.7.2) involves only measurable quantities such as volume concentration, diffusion depth and diffusion time.

Que 4.8. Define sheet resistance. Describe a method for its measurement.

AKTU 2015-16, Marks 05

Answer

A. Sheet resistance :

1. The resistance of a uniform structure of width w , thickness t , and length l is given by

$$R = \rho \frac{l}{tW} (\Omega) \quad \dots(4.8.1)$$

where ρ is resistivity of the material in $\Omega \text{ cm}$.

2. In integrated circuits, the diffusion lines are normally uniform in thickness, therefore, we can absorb t into resistivity ρ and define a new variable ρ_s , called sheet resistance, which has dimensions of Ohm (Ω).
 3. Thus, eq. (4.8.1) becomes

$$R = \rho_s \frac{l}{W} (\Omega) \quad \dots(4.8.2)$$

where $l = w$, the structure becomes square with $R = \rho_s$.

4. Thus sheet resistance of a layer is the resistance measured between the opposite sides of a square of that layer, regardless of its actual dimensions.
 Hence ρ_s is often express as Ω/\square (Ohm per square)

B. Method :

1. In microcircuit fabrication, the sheet resistance of a diffused layer can be directly measured if it is made in the patterned shape shown in Fig. 4.8.1.
 2. Here, as shown for a *p*-channel MOS transistor, a *p*-type source/drain diffusion is made into an *n*-type substrate.
 3. A constant current is applied across the points *AB*, and the voltage developed across *CD* is read with the aid of a high-impedance voltmeter. With reference to Fig. 4.8.1.

$$\rho_s = \frac{V W}{I l}$$

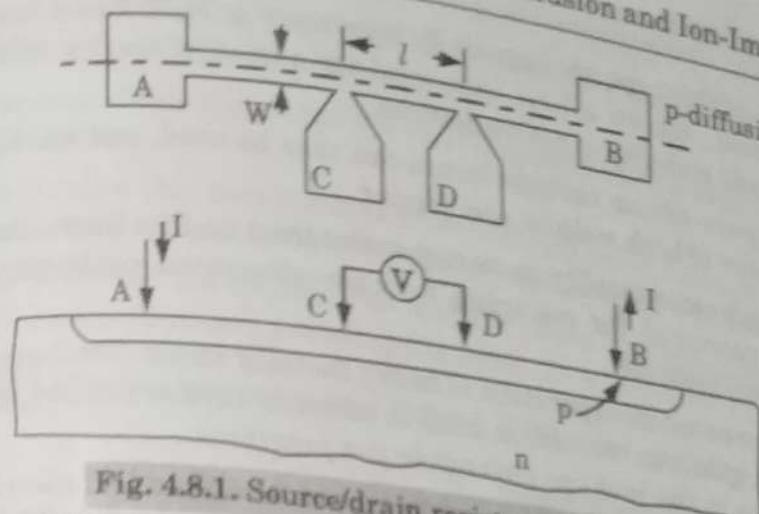


Fig. 4.8.1. Source/drain resistance test pattern.

4. Since W/l is known for a specific test pattern, the sheet resistance is directly found.

PART-3

Diffusion Furnace, Solid, Liquid and Gaseous Sources.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 4.9. Describe diffusion furnace.

Answer

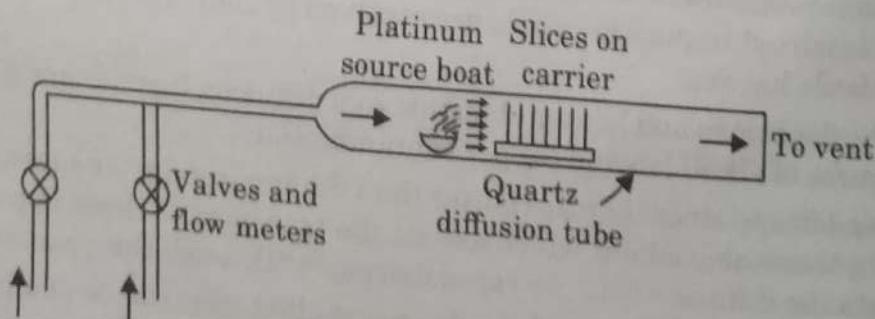
1. The diffusion furnace itself is a major source of impurity contamination. Commercial diffusion tubes, made of fused quartz, are typically 96-97 % pure, thus they must be cleaned upon installation, and also regularly during service.
2. Typically this is accomplished by flowing anhydrous hydrogen chloride gas through them for 15-30 min at diffusion temperatures. This tends to leach out impurities which are removed by conversion to their more volatile halides.
3. The firebricks and heater elements in a diffusion furnace are a major source of alkali ion and copper contamination.
4. In addition, since they are hotter than the semiconductor slices, there is a thermal gradient which assists the transport of these impurities into the diffusion tube, by rapid movement through the quartz walls.
5. The use of a high-purity, high-density mullite liner (made of mixtures of alumina and zirconia) is common practice since this serves as a barrier to the transport of alkali ions.

6. Liners of this type are especially important in MOS based fabrication processes, where alkali ions contamination critically affects the threshold stability of active devices.
7. Ultra-pure silicon carbide liners can also be used, and will block the transport of both sodium and copper.
8. Although considerably more expensive than mullite liners, they have great potential for reducing furnace-associated contamination in diffusion systems.
9. The unwanted incorporation of heavy metallic impurities (such as iron, copper, gold, etc.) results in a fall in minority carrier lifetime, and in an increase in the leakage current in $p-n$ junctions.
10. Thus their removal is important for bipolar as well as field effect devices. One approach here is to use dopant sources which are halogenic compounds.
11. With these the halogen is liberated during diffusion, and reacts with any metallic impurities in the incoming gas, as well as with impurities within the semiconductor that reach its surface during their rapid movement at high temperatures.
12. This reaction converts them to their more volatile halides, which leave the system by incorporation into the gas stream.
13. The use of a halogenic dopant source thus effectively getters the semiconductor.
14. These sources must be used with care, however, since excessive use can result in local dissolution of the semiconductor and cause its pitting.

Que 4.10. Write a short note on solid source diffusion system.

Answer

1. Fig. 4.10.1 shows a sketch of the diffusion system in which a platinum boat is used to hold a solid source of the dopant species upstream from the carrier with the semiconductor wafers.
2. In operation, the carrier gas transports vapors from this source and deposits them on the semiconductor slices.



3. Source shutoff is usually accomplished by moving the dopant source to a colder region of the furnace.
4. The success of this technique depends critically on the vapor pressure of the source.
5. In some cases, this necessitates a two-temperature furnace, with the source maintained at a lower temperature than is used for the diffusions.
6. Often, however, the source boat and the slices can be maintained at the same temperature, avoiding the need for a two-zone furnace.

Que 4.11. Discuss gaseous and liquid diffusion systems.

AKTU 2016-17, Marks 10

Answer

A. Gaseous source diffusion system :

1. Gaseous sources are even more convenient than the liquid ones.
2. Again, it is common practice to use an excess dopant gas concentration, so that these systems are relatively insensitive to the gas-flow rate.
3. Fig. 4.11.1 shows the schematic for a typical diffusion system using a gaseous dopant source.
4. Here provision is made for an ambient carrier gas in which the diffusion takes place.
5. In addition, a chemical trap is often incorporated to dispose of unreacted dopant gases, which are often highly dangerous.
6. All vapor transport methods rely on the fact that the surface concentration of the incorporated dopant is solid-solubility-limited, so that it is relatively insensitive to the vapor pressure of the reactant species.
7. Still, massive depletion of the source reactant is possible as it travels down the diffusion tube.

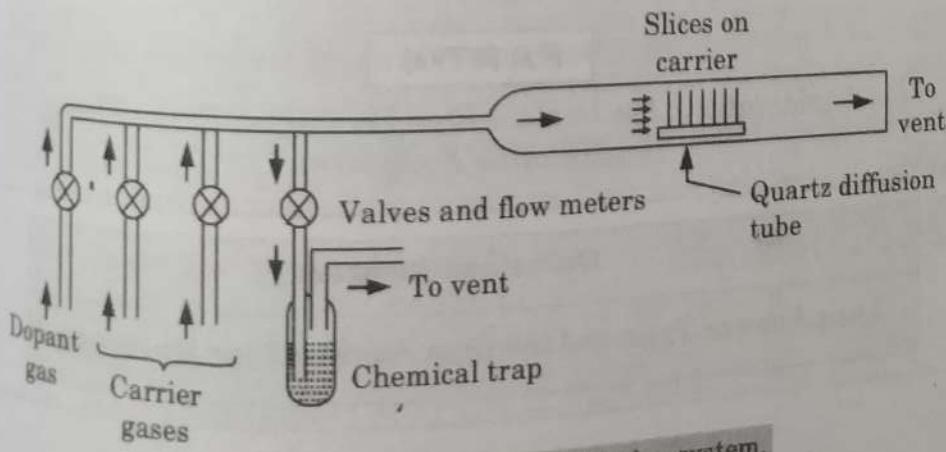


Fig. 4.11.1. Gaseous-source diffusion system.

8. Additional depletion occurs during transport of the reactant vapor between slices.
9. Thus, it is difficult to maintain doping uniformity over all the slices during a diffusion run, and even over the surface area of each individual slice.
10. Both these problems are exacerbated with the present trend towards large slice diameters, and the use of a large number of slices in a single run, which necessitates close spacing's between individual slices.

B. Liquid-Source diffusion system :

1. Liquid-source systems are extremely convenient since the doping process can be readily initiated (or terminated) by control of the gas through the bubbler.
2. In addition, the amount of dopant transported to the slices is relatively easy to control in these systems, by adjustment of the bubbler temperature.
3. Finally, a number of halogenic dopant compounds are available as liquids.
4. Use of these sources greatly reduces heavy metal contamination in diffusion systems.

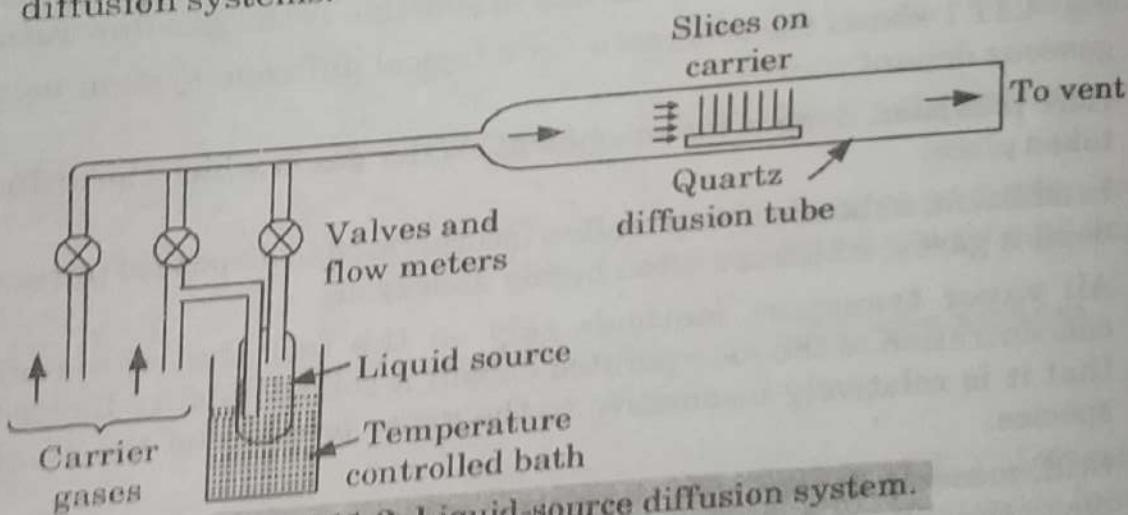


Fig. 4.11.2. Liquid-source diffusion system.

PART-4

Ion-Implantation : Ion-Implantation Technique, Range Theory, Implantation Equipment.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 4.12. Explain ion-implantation and mention its advantages over diffusion.

AKTU 2015-16, Marks 05

Answer

A. Ion-implantation :

1. During ion-implantation, dopant atoms are vaporized, accelerated, and directed at a silicon substrate.
2. They enter the crystal lattice, collide with silicon atoms, and gradually lose energy, finally coming to rest at some depth within the lattice.
3. The average depth can be controlled by adjusting the acceleration energy.
4. The dopant dose can be controlled by monitoring the ion current during implantation.
5. The principle side effect-disruption of the silicon lattice caused by the ion collisions -is removed by subsequent heat treatments.
6. Ion-implantation therefore satisfies the conditions for a generally useful doping process.
7. Implantation energies range from 1 keV to 1 MeV, resulting in ion distributions with average depths ranging from 100 \AA to $10\text{ }\mu\text{m}$.

B. Advantages :

1. Short process times, good homogeneity and reproducibility of the profiles.
2. Exact control of the amount of implanted ions by measuring the current.
3. Relatively low temperatures during the process.
4. Various materials can be used for masking, e.g., oxide, nitride, metals, and resist.
5. Implantation through thin layers, e.g., SiO_2 is possible.
6. Low penetration depth of the implanted ions.

Que 4.13. Explain the basic working principle of ion-implantation process with all necessary equations. Compare between the diffusion and ion-implantation process.

AKTU 2017-18, Marks 10

Answer

A. Ion-implantation : Refer Q. 4.12, Page 4-14F, Unit-4.

B. Comparison :

S. No.	Diffusion	Ion-implantation
1.	Diffusion can be defined as the motion of impurities inside a substance.	Ion-implantation is a low temperature process used to change the chemical and physical properties of materials.
2.	It done at high temperatures.	It done at low temperatures.
3.	Amount of dopant cannot be controlled.	Amount of dopant can be controlled.
4.	Comparatively less expensive.	More expensive because it require specific equipment.

Que 4.14. Discuss about the ion sources with one example.

Answer

1. Ion sources usually consist of :
 - i. Compounds of the desired species, and
 - ii. A means for their ionization prior to delivery to the accelerator column.
2. The choice of materials for ion sources is very wide, almost any ionizable compound can be used here.
3. Gaseous materials are more convenient to use than solid ones, since they avoid the necessity of using a vaporization chamber, and can be replenished without opening the system.
4. Ionization of the source material is usually done by passing the vapor through a hot cathode electronic discharge. Cold cathode and r.f. discharges are also used in some machines.
5. Electrons are accelerated towards an anode which is typically at 100 V. A magnetic field is provided so as to force the electrons to move in a spiral trajectory, thus increasing the ionizing efficiency of the source.
6. Also provided is a means for extracting the positive ions from this discharge by means of an anode biased at 15-20 kV.
7. As a consequence, the output of a source of this type consists of ions at an energy of 15-20 keV.
8. The outlet of the ionizer is either circular or in the form of a rectangular slit, and defines the geometry of the ion beam.
9. Fig. 4.14.1 shows a sketch of a gas-fed ion source and illustrates many of the features described here.

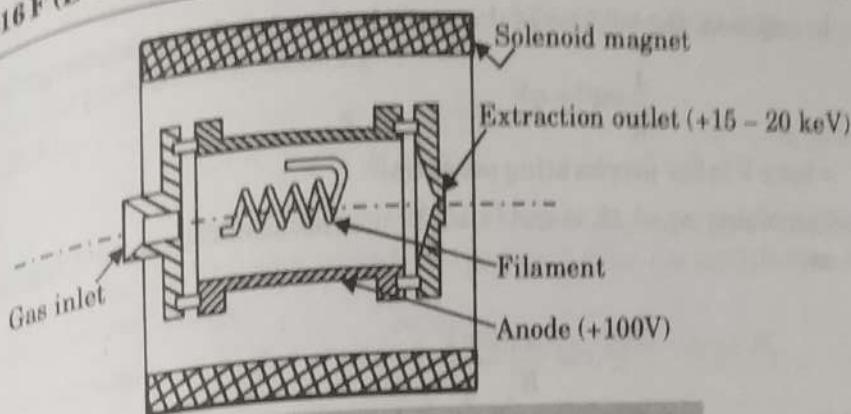


Fig. 4.14.1. A Nielsen-type gaseous source.

10. The effectiveness of an ion source is measured by the magnitude of ion current delivered to the accelerator, and ultimately to the target.
11. If I is the ion current (in amperes) for a species of charge state r , then the rate at which ions arrive at the target is I/qr per second, where q is the electronic charge in coulombs.
12. Thus a singly ionized beam delivers $6.25 \times 10^{18} I$ ions/s to the target.
13. Finally, if A is the target area in cm^2 , and t is the implantation time in seconds, the ion dose is given by

$$Q_0 = 6.25 \times 10^{18} \frac{It}{A} \text{ ions cm}^{-2}$$

14. A large beam current is thus highly desirable in commercial systems where many wafers must be handled with a minimum of machine time.

Que 4.15. Explain the details about mass separation.

Answer

1. The use of mass separation techniques provides a unique distinction between ion-implantation and diffusion, in that a variety of dopants can be handled in a single machine, with complete freedom from contamination with each other.
2. The most commonly employed technique utilizes a homogeneous-field magnetic analyzer.
3. Its principle is based on the dynamics of charged particles, of mass m and velocity v , moving at right angles to a uniform magnetic field with a flux density B .
4. These particles will experience a force F such that

$$F = q(v \times B)$$

...(4.15.1)

5. This tends to move them in a circular path of radius r . Thereby creating a centrifugal force mv^2/r . These forces must be equal and opposite.

6. In addition, the velocity of the particles is related to their energy by

$$\frac{1}{2}mv^2 = qV \quad \dots(4.15.2)$$
- where V is the accelerating potential.
7. Combining eq. (4.15.1) and (4.15.2), the radius of the ion path is given as

$$r = \frac{1}{B} \left(\frac{2mV}{q} \right)^{1/2}$$

8. Thus, for a given extraction voltage and magnetic flux density, the path radius is directly proportional to the square root of the mass.
9. Trajectories for three different masses are shown in Fig. 4.15.1.
10. From this, it is seen that ions of any particular mass can be selected by the appropriate placement of an exit slit.

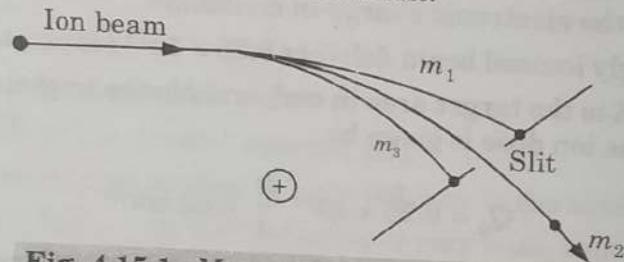


Fig. 4.15.1. Mass separation through a slit.

Que 4.16. How the range is distributed in ion-implantation ?

Answer

1. Each implanted ion has a random path as it moves through the target, losing energy by nuclear and electronic stopping.
2. Since each implantation dose contains more than 10^{12} ions/cm² their average behaviour can be well predicted.
3. The average total path length in silicon is called the range R , and is composed of a mixture of vertical and lateral motion.
4. The average depth of the implanted ions is called the projected range, R_p , and the distribution of ions about that depth can be approximated as Gaussian with standard deviation σ_p .
5. The lateral motion of the ions to a lateral Gaussian distribution with standard deviation σ . The ion ranges is shown schematically in the Fig. 4.16.1. Far from a mask edge, we can neglect the lateral motion and write the ion concentration $n(x)$ as

$$n(x) = n_0 \exp \left[\frac{-(x - R_p)^2}{2\sigma_p^2} \right] \quad \dots(4.16.1)$$

4-18F(EC-Sem-5)

6. If the total dose is ϕ , then integrating eq. (4.16.1) gives us an expression for the peak concentration n_0 :

$$n_0 = \frac{\phi}{\sqrt{2\pi} \sigma_p} = \frac{0.4\phi}{\sigma_p} \quad \dots(4.16.2)$$

7. In general, an arbitrary distribution $n(x)$ can be characterized in terms of its moments. The normalized first moment of an ion distribution is the projected range.

8. For convenience, higher moments are usually taken about R_p .

9. The second, third, and fourth moments are typically expressed in terms of the following parameters :

$$\text{(standard deviation)} \sigma_p = \sqrt{\frac{m_2}{\phi}} \quad \dots(4.16.4)$$

$$\text{(Skewness)} \gamma = \frac{m_3}{\sigma_p^3} \quad \dots(4.16.5)$$

$$\text{(Kurtosis)} \beta = \frac{m_4}{\sigma_p^4} \quad \dots(4.16.6)$$

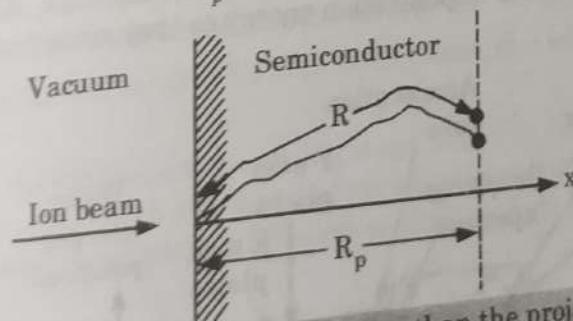


Fig. 4.16.1. The total path length R is longer than the projected range R_p .

10. Qualitatively, skewness measures the asymmetry of the distribution - positive skewness places the peak of the distribution closer to the surface than R_p .
11. Kurtosis measures how flat the top of a distribution is. Gaussian distributions have a skewness of 0 and a kurtosis of 3.
12. In cases where the kurtosis is not available, a universal expression is often used.

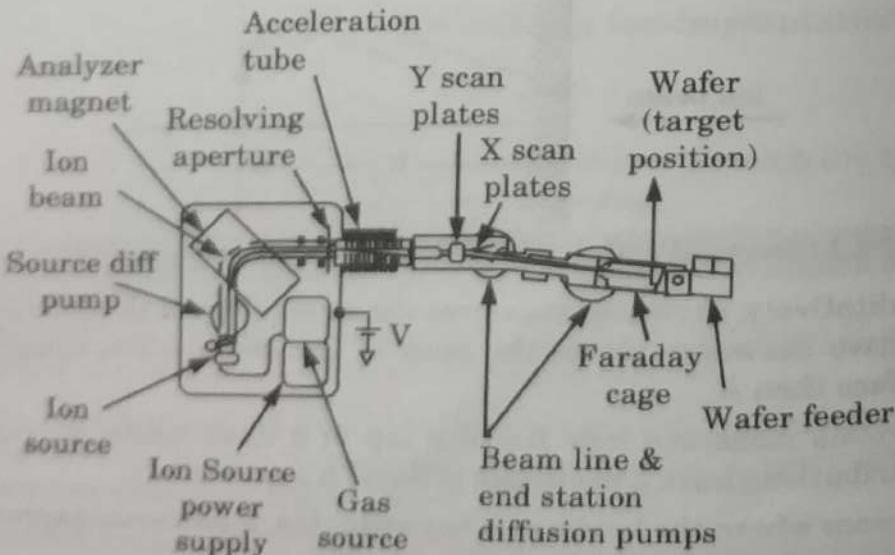
$$\beta \approx 2.8 + 2.4 \gamma^2 \quad \dots(4.16.7)$$

Que 4.17. Describe basic layout of implantation equipment.

AKTU 2016-17, Marks 10

Answer

1. The basic requirement for an ion-implantation system is to deliver a beam of ions of a particular type and energy to the surface of a silicon wafer.
2. Fig. 4.17.1 shows a schematic view of a medium-energy ion implanter. Following the ion path, we begin on the left-hand side with the high-voltage enclosure containing many of the system components.
3. A gas source feeds a small quantity of source gas such as BF_3 into the ion source where a heated filament causes the molecules to break up into charged fragments.
4. This ion plasma contains the desired ion together with many other species from other fragments and contamination.
5. An extraction voltage, around 20 kV, causes the charged ions to move out of the ion source into the analyzer.
6. The pressure in the remainder of the machine is kept below 10^{-6} Torr to minimize ion scattering by gas molecules.
7. The magnetic field of the analyzer is chosen such that only ions with the desired charge to mass ratio can travel through without being blocked by the analyzer walls.
8. Surviving ions continue to the acceleration tube, where they are accelerated to the implantation energy as they move from high voltage to ground.

**Fig. 4.17.1.**

9. Apertures ensure that the beam is collimated. The beam is then scanned over the surface of the wafer using electrostatic deflection plates.
10. The wafer is offset slightly from the axis of the acceleration tube so that ions neutralized during their travel, will not be deflected onto the wafer.

Que 4.18.

Write short note on annealing.

AKTU 2017-18, Marks 05

Answer

1. Annealing is required to repair lattice damage and put dopant atoms on substitutional sites where they will be electrically active.
2. The success of annealing is often measured in terms of the fraction of the dopant that is electrically active, as found experimentally using a Hall effect technique.
3. The Hall effect measures an average effective doping, which is an integral over local doping densities and local mobilities evaluated per unit of surface area.

$$N_{\text{Hall}} = \frac{\left(\int_0^{x_j} \mu n \, dx \right)^2}{\int_0^{x_j} \mu^2 \, ndx}$$

where μ is the mobility, n is the number of carriers, and x_j is the junction depth.

4. If the mobility is not a strong function of depth, N_{Hall} measures the total number of electrically active dopant atoms.
5. If annealing activates all of the implanted atoms, this will be equal to the dose Φ .
6. For VLSI, the challenge in annealing is not simply to repair damage and activate dopant, which any long, high-temperature anneal will achieve, but to do while minimizing diffusion so that shallow implants remain shallow.
7. This has motivated much recent work in rapid thermal annealing (RTA), where annealing times are on the order of seconds.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

- Q.1. Discuss diffusion. Find diffusion constant for :

- i. Interstitial diffusion
- ii. Substitutional diffusion

Ans. Refer Q. 4.1.

Q. 2. What is Fick's law of diffusion ? Boron is diffused into an n -type single crystal substrate with doping concentration of 10^{15} atm/cm³. Assume diffusion time is 1 hr, surface concentration = 1×10^{18} cm⁻³ and depth of junction is 2 μm , determine diffusivity.

Ans. Refer Q. 4.3.

Q. 3. If the measured phosphorus profile is represented by a Gaussian function with a diffusivity $D = 2.3 \times 10^{-13}$ atoms/cm², the measured surface dose is 10^{18} atoms/cm² and the junction depth is 1 μm at a surface concentration of 10^{15} atoms/cm³. Calculate the diffusion time.

Ans. Refer Q. 4.4.

Q. 4. Define sheet resistance. Describe a method for its measurement.

Ans. Refer Q. 4.8.

Q. 5. Discuss gaseous and liquid diffusion systems.

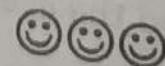
Ans. Refer Q. 4.11.

Q. 5. Explain the basic working principle of ion-implantation process with all necessary equations. Compare between the diffusion and ion-implantation process.

Ans. Refer Q. 4.13.

Q. 6. Describe basic layout of implantation equipment.

Ans. Refer Q. 4.17.





Metallization and Packaging of VLSI Devices

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PART-1

Metallization : Metallization Application, Metallization Choices,

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 5.1. Explain metallization.

Answer

1. Metallization use in bipolar devices is similar to that in MOSFET.
2. In a bipolar transistor, the central region is the semiconductor (base), and is directly in contact with the metal.
3. The two neighbouring region are now called emitter and collector, and are also directly in contact with metal.

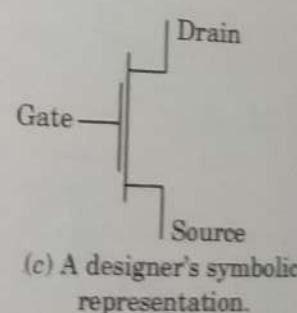
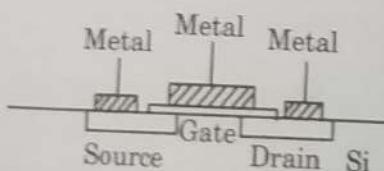
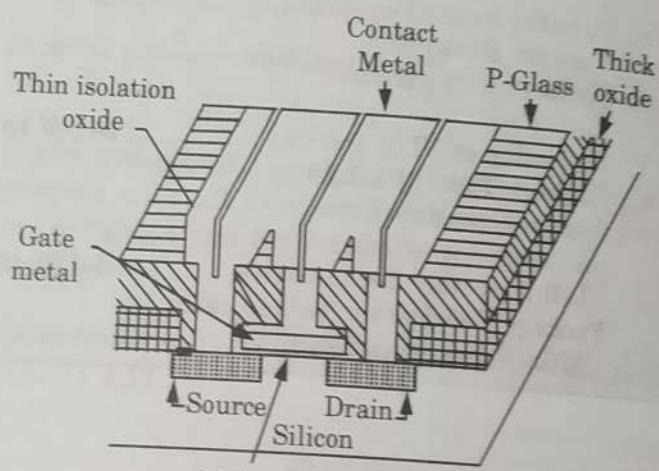


Fig. 5.1.1. A typical MOSFET.

4. The metal work function plays an important role in all three regions in determining the current flow characteristics, in a manner similar to that in the source and drain regions of the MOSFET.
5. Primary metallization application can be divided into three groups :
 - i. Gate,
 - ii. Contact, and
 - iii. Interconnects.
6. Interconnection metallization, which interconnects thousands of MOSFETs or bipolar devices using fine-line metal patterns, is generally the same as gate metallization.
7. All metallization directly in contact with semiconductor is called contact metallization. As mentioned earlier, polysilicon film has been the form of metallization used for gate and interconnection MOS devices.
8. Aluminium has been used as the contact metal on devices and as the second-level interconnection to the outside world.
9. Several other metallization schemes have been proposed to produce ohmic contacts to semiconductor.
10. In several cases a multiple-layer structure involving a diffusion barrier has been recommended.
11. Platinum silicide (PtSi) has been used as a Schottky barrier contact and also simply as an ohmic contact for deep junctions.
12. Titanium/platinum/gold or titanium/palladium/gold beam lead technology has been successful in providing high-reliability connection to the outside world.

Que 5.2. Explain any two applications of metallization.

Answer

The applications of metallization are :

i. Gates and interconnection :

1. Gate and interconnection metallization plays two important roles. First, it controls the speed of the circuit by virtue of the resistance of the interconnection runners.
2. The RC time constant of these runners varies as $R_s L^2/d_{ox}$, where R_s is the ohm per-square (sheet) resistance, L is the length of the runner, and d_{ox} is the oxide thickness.
3. For faster circuits, a reduction in R_s is essential.
4. Besides its role in circuit speed, metallization also controls the so-called flat-band voltage V_{FB} .

5. V_{FB} is the voltage required to counter balance the work function difference between metal and semiconductor so that a flat-band condition is maintained in the semiconductor.
6. In absence of any other charges in the oxide or at the oxide-semiconductor interface

$$V_{FB} = \phi_m - \phi_s = \phi_{ms} \quad \dots(5.2.1)$$

where ϕ_m and ϕ_s are the work functions of the metallization (at the gate) and the semiconductor, respectively.

ii. Ohmic contacts :

1. A good ohmic contact, usually formed by depositing a metal on the semiconductor, does not perturb device characteristics and is stable both electrically and mechanically.
2. It has a resistance, called contact resistance, which should be negligible compared to the device resistance.
3. The specific contact resistance R_c ($\Omega\text{-cm}^2$) is defined as,

$$R_c = \left(\frac{dV}{dJ} \right)_{v=0} \quad \dots(5.2.2)$$

which can be obtained from current density (J) and voltage (V) characteristics.

Que 5.3. Calculate the RC time constant for a 1 cm long doped polysilicon interconnection runner on 1 μm thick SiO_2 . The polysilicon has a thickness of 5000 Å and a resistivity ρ of 1000 $\mu\Omega\text{-cm}$.

Answer

Given : $L = 1 \text{ cm}$, $\rho = 1000 \mu\Omega\text{-cm}$ $d_{\text{poly-Si}} = 5000 \text{ \AA}$, $d_{\text{ox}} = 1 \mu\text{m} = 10^{-4} \text{ m}$
 To Find : RC

1. We have,

$$RC = \frac{R_s L^2 \epsilon_{\text{ox}}}{d_{\text{ox}}} = \frac{\rho}{d_{\text{Poly-Si}}} \frac{L^2 \epsilon_{\text{ox}}}{d_{\text{ox}}}$$

where,

2. Substituting the given values and changing farads into coulombs per volt, we get

$$RC = \frac{1000 \times 10^{-6}}{5000 \times 10^{-8}} \frac{1^2 \times 3.5 \times 10^{-13}}{10^{-4}} \text{ s}$$

$$= 7 \times 10^{-8} \text{ s}$$

$$= 70 \text{ ns}$$

Ques 5.4. What are the possible metallization choices for integrated circuits?

Answer

Table 5.4.1 lists the possible metallization choices. Of these, polysilicon has been the usual gate metallization for MOS devices. Only recently, polysilicon/refractory metal silicide bilayers have replaced polysilicon so that lower resistance can be achieved at the gate and interconnection level.

Table 5.4.1. Possible metallization choices for integrated circuits

S.No.	Application	Choices
1.	Gates and interconnection and contacts.	Polysilicon, silicides, nitrides, carbides, borides, refractory metals, aluminum, and combinations of two or more of above.
2.	Diffusion barrier.	Nitrides, carbides, borides, Ti-W alloy, silicides.
3.	Top level.	Aluminum.
4.	Selectively formed metallization on silicon only.	Some silicides, tungsten, aluminum.

- By preserving the use of polysilicon as the "metal" in contact with the gate oxide, well-known device characteristics and processes have been unaltered.
- Refractory silicides, formed on top of polysilicon, have provided the highest compatibility.
- For contacts, aluminum has been the preferred metal because of the ease of processing.
- Aluminum's ability to reduce native SiO_2 , which is always present on silicon wafers exposed to atmosphere, and its low resistivity.
- However, the lower melting point of aluminum, limits its use to processing steps after which no high-temperature (normally greater than 450°C) operation is permitted.

7. In spite of this limitation, aluminum has satisfied the required metallization criteria.
8. The use of a silicide as contact metallization will require a diffusion barrier to protect the silicide from interaction with aluminum used as the top metal. Aluminum interacts with most silicides in the temperature range of 200-500 °C.
9. Because of their high chemical and thermodynamical stabilities, transition metal nitrides, carbides, and borides offer potential applicability as a diffusion barrier between silicide (or silicon) and aluminum.

Que 5.5. Explain the metallization and describe the problems associated with this process. Explain DC sputtering method of metallization.

AKTU 2017-18, Marks 10

Answer

- A. Metallization :** Refer Q. 5.1, Page 5-2F, Unit-5.
- B. DC sputtering method :**
1. Sputter deposition, or sputtering, is considerably more versatile than vacuum evaporation, and is extensively used in the deposition of thin films in micro circuit technology.
 2. The reasons for its popularity are :
 - i. The ability to deposit a wide variety of metals and insulators, as well as their mixture,
 - ii. The replication of target composition in the deposited film, and
 - iii. The capability for in situ cleaning of the substrate prior to film deposition.
 3. Sputter deposition is carried out in a self-sustained glow discharge which is created by the breakdown of a heavy inert gas such as argon.
 4. Here, a DC electric field is impressed across two water-cooled electrodes which are located in this gas.
 5. At sufficiently low electric field intensities, a very small current will flow, primarily by the transport of electrons between these electrodes.
 6. These electrons may be produced by photoemission or by cosmic ray stimuli, and are always present to some degree in any gaseous medium.
 7. Fig. 5.5.1(b) shows the nature of the discharge. The most important region here is the Crook's dark space across which nearly all of the applied voltage is dropped.
 8. Both ions and electrons created at breakdown are primarily accelerated across this region.

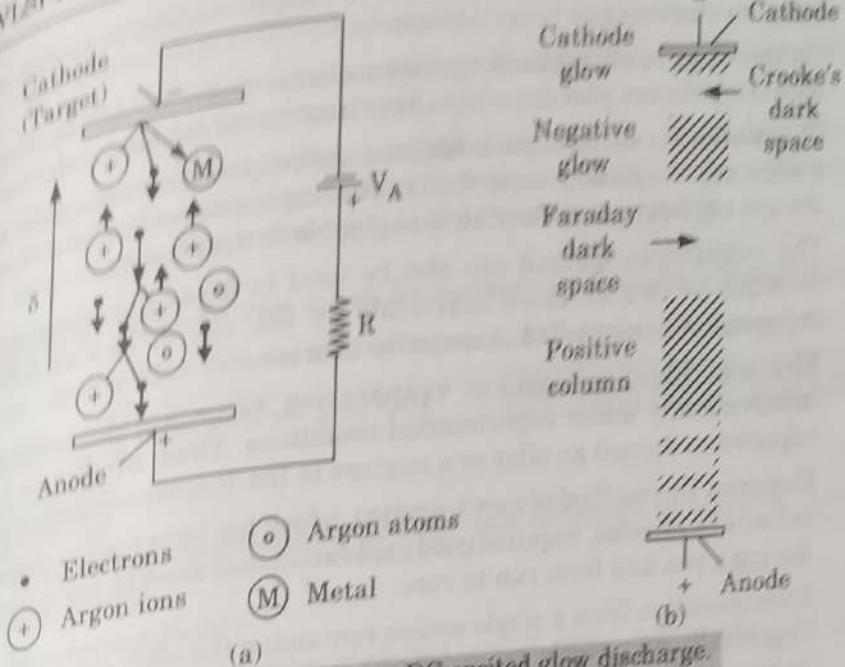


Fig. 5.5.1. Sputtering in a DC excited glow discharge.

PART-2

*Physical Vapor Deposition, Vacuum Deposition,
Sputtering Apparatus.*

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 5.6. Explain the types of physical vapor deposition.

Answer

There are two types of physical vapor deposition methods:

i. Evaporation :

1. In the evaporation method, a film is deposited by the condensation of the vapor on a substrate, which is maintained at lower temperature than that of vapor.
2. All metals vaporize when heated to sufficiently high temperatures. Several methods such as resistive, inductive, electron bombardment, or laser heating, can be used to attain these temperatures.

3. For transition metals, especially the refractory metals, evaporation using an electron gun is very common.
4. On the other hand, e-gun evaporation cause radiation damage, but high temperature post deposition heat treatments can anneal this out.
5. This method is advantageous because the evaporation takes place at pressures considerably lower than sputtering pressures and, therefore, the gas entrapment in the film is negligible or nonexistent.
6. The evaporation method can also be used to deposit an alloy or a mixture of two or more materials by the use of two or more independently controlled evaporation sources.
7. The individual component evaporation rates are determined independently under experimental conditions. Then, conditions are adjusted to deposit an alloy or a mixture in the desired composition.
8. However, this method of coevaporation, which has been used to deposit refractory silicides, requires good calibration that must be maintained during a run and from run to run.
9. Coevaporation from a single source containing the alloy constituents is generally not possible, because fractionation occurs as the evaporation proceeds.

ii. Sputtering :

1. In sputter deposition, the target material is bombarded by energetic ions to release some atoms. These atoms are then condensed on the substrate to form a film.
2. Sputtering processes, are very well controlled and generally applicable to all materials-metals, alloys, semiconductors, and insulators.
3. Radio frequency, DC, and DC-magnetron sputtering can be used for metal deposition. Alloy-film deposition by sputtering from an alloy target is possible because the composition of the film is locked to the composition of the target.
4. This is true even when there is considerable difference between the sputtering rates of the alloy components.
5. At the early stages of sputtering the component with high sputtering rate is sputtered off the target preferentially, leaving the target surface deficient in this component.
6. The deficient region soon becomes deficient enough to compensate for the higher sputtering rate, leading to deposits of a composition similar to that of the target.
7. The difference between the target and film compositions depends on the type of the equipment, the sputtering parameters, and the alloy constituent.
8. By proper choice of the equipment and sputtering parameters, several complex alloys have been deposited with identical composition in the target and the film.

9. Alloys can also be deposited with excellent control of composition by use of individual component targets.
10. In certain cases, the compounds can be deposited by sputtering the metal in a reactive environment.
11. Thus, gases such as methane, ammonia or nitrogen, and diborane can be used in the sputtering chamber to deposit carbide, nitride, and boride, respectively. This technique is called reactive sputtering.

Que 5.7. What do you mean by sputtering? Explain sputtering yield. Draw the schematic diagram of signal parallel-plate sputtering system and its working.

AKTU 2015-16, Marks 7.5

Answer

A. Sputtering : Sputtering is a widely used technique to fabricate thin-film coatings.

B. Sputtering Yield :

1. It is defined as the number of ejected surface atoms per incoming ion at a given ion energy.
2. Yield plots for many ion-surface combinations have been determined.
3. The sputtering yield changes with the angle of the ion flux.
4. As the flux angle is moved away from the surface normal the maximum sputtering yield occurs because fewer collisions close to the surface are required to eject an atom.

C. Parallel-plate sputtering system :

1. A geometry used for plasma/cathode sputtering is the parallel-plate configuration, the RF glow discharge version of which illustrated in Fig. 5.7.1.

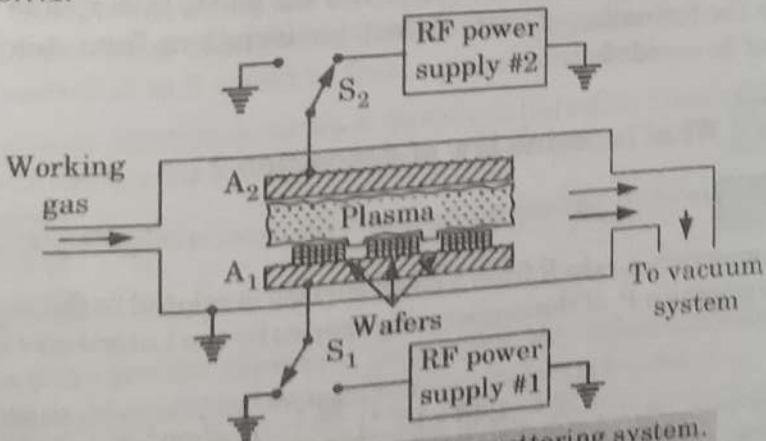


Fig. 5.7.1. Parallel plate sputtering system.

2. For sputter deposition of workpieces, the upper electrode is energized by RF.

3. A sufficiently high sheath voltage to cause sputtering of this electrode can be maintained in following two ways :
- a. One method is by a negative DC bias on the electrode imposed by a separate power supply.
 - b. i. A second method is by maintaining a large ratio between the area of the grounded electrode on which the workpieces are mounted, and the energized electrode area. In this configuration, sputtered atoms transit the RF glow discharge plasma and are deposited on workpieces mounted on the opposite grounded electrode.
 - ii. This configuration has the advantage of being able to operate at higher plasma densities, but the disadvantage of greater difficulty in achieving sheath potentials high enough to produce useful sputtering rates.

Que 5.8. Explain why sputtering is needed for the deposition of refractory materials like tantalum. AKTU 2015-16, Marks 7.5

Answer

1. Refractory metals such as tantalum produced by diode sputtering in an inert gas alone are suitable for thin film resistors because of their high resistivity and low temperature coefficient of resistivity.
2. However, residual gases in the vacuum chamber such as O₂, N₂, CO, and CH₄, are a source of impurities that lead to the formation of different phases.
3. These impurities affect the resistivity, but are not necessarily detrimental.
4. In fact, nitrides formed with the tantalum can yield excellent resistive properties.
5. Bias sputtering gives better control over the purity of tantalum resistors, but in the formation of oxide dielectrics deviations from stoichiometry cannot be avoided.

Que 5.9. What is cosine law of deposition ?

Answer

1. The evaporation rate R from a clean surface is related to the equilibrium vapor pressure P_e of the evaporating species by the Langmuir expression.

$$R = 4.43 \times 10^{-4} \left(\frac{M}{T} \right)^{1/2} P_e \text{ g/cm}^2 \cdot \text{s} \quad \dots(5.9.1)$$

where,

P_e = Vapour pressure (in pascals)

M = Molecular weight of the evaporating species in grams, and

T = Temperature in degrees or Kelvin.

- ▶ The directionality and spatial distribution of the evaporated species in the evaporating chamber can be calculated following Holland's discussion of evaporation from various types of sources.
- ▶ For evaporation from a small-area source and deposition on a plane receiver, the geometric relationships are shown in Fig. 5.9.1.
- ▶ In such a case, the mass deposited per unit area is given as,

$$R_D = \frac{M_e}{\pi r^2} \cos \phi \cos \theta \quad \dots(5.9.2)$$

where M_e is the total mass of the evaporated material.

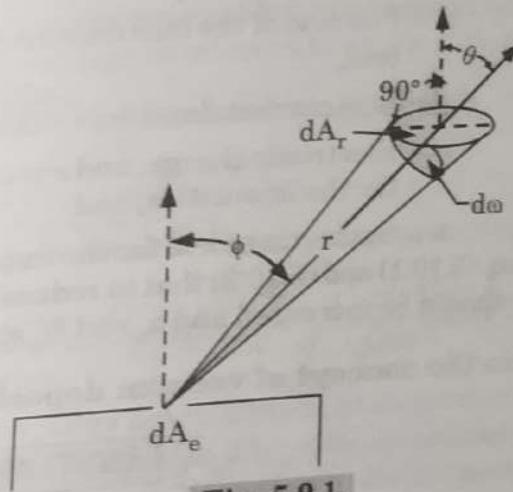


Fig. 5.9.1.

5. Eq. (5.9.2), known as the cosine law of deposition, clearly shows that emission from finite-area evaporation sources is not spherically symmetrical as it would be from a point source.
6. Maximum deposition occurs in directions normal to the emitting surface, where $\cos \phi$ is maximum, that is, ϕ is zero.

Que 5.10. Explain impurity trapping during deposition.

Answer

1. There are several sources of impurities, the deposition source and the gaseous environment being the most important ones.
2. The source will release impurities in the gas phase. These impurities and those in the environment will then bombard the surface of the growing film and get trapped during continued deposition.

3. The fraction f_i of the species i trapped in the film is given by,
- $$f_i = \frac{\alpha_i N_i}{\alpha_i N_i + R} \quad \dots(5.10.1)$$
- where,
- N_i = Number of atoms of species i that bombard the film per unit area per unit time,
- α_i = Effective sticking coefficient of species i during deposition, and
- R = Deposition rate of the film.

5. In the case of sputtering, where a bias may be applied to the substrate, Eq. (5.10.1) is modified.

$$f_i = \frac{\alpha_i N_i - (j/q)(As - \beta)}{\alpha_i N_i - (j/q)(As - \beta) + R} \quad \dots(5.10.2)$$

where

$$A = \frac{\alpha_i N_i + \beta j q^{-1}}{\alpha_i N_i + j(s + \beta)q^{-1}}$$

β = Fraction of the bias current due to the impurity ions,

j = Bias current density,

q = Electronic charge, and s is the sputtering yield for the impurities, and

s = Sputtering yield for the impurities.

6. It is clear from eq. (5.10.1) and (5.10.2) that to reduce contamination, the deposition rate should be increased and α_i and N_i should be reduced.

Que 5.11. Explain the concept of vacuum deposition.

AKTU 2016-17, Marks 7.5

Answer

1. The arrangement of metallization process using vacuum deposition technique is shown in Fig. 5.11.1.

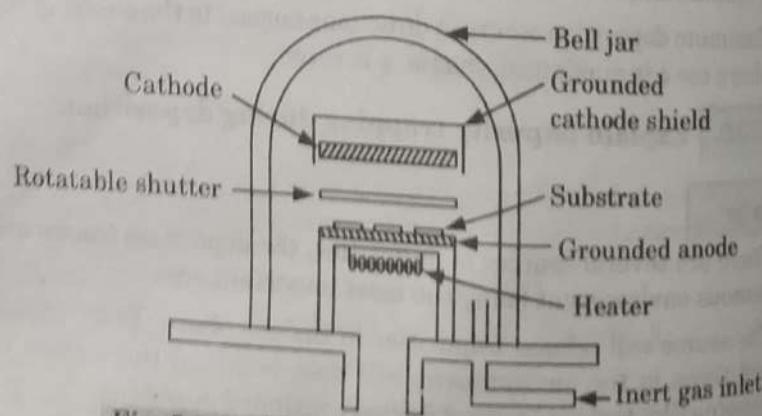


Fig. 5.11.1. Arrangement for vacuum deposition.

2. The silicon wafers are placed face down around the bell jar, with the source of metal in the centre.
3. The vacuum pressure is lowered to below 5×10^{-6} Torr before the metal deposition commences.
4. The silicon is then heated to a temperature range of 100 to 300°C, which causes the deposited metal to chemically react with the silicon dioxide and adhere to the wafer surface.
5. Upward evaporation is also used to prevent impurities, which may be generated by the heat source, from falling onto the wafers.
6. The metal film is normally of 1 μm thickness. The thickness can be monitored by including a quartz crystal oscillator in the vacuum, whose frequency can be set with the amount of metal to be deposited on its surface.
7. After evaporation, the wafers are heated at about 1500°C in an inert gaseous (e.g., nitrogen) atmosphere. This causes the metal to alloy well with the silicon surface so that low resistance is achieved in the interface between the two. This is referred to as a low ohmic contact joint.

Que 5.12. Explain the sputtering apparatus.**Answer**

1. The processing curves for the reactive sputtering process do exhibit hysteresis effects.
2. In addition, avalanche-like transitions occur at the edges of the hysteresis region.
3. It is not easy to judge how different processing parameters affect the overall processing behaviour. This calls for a model capable of predicting the influence of different parameters on the process.
4. It should be understood, however, that a model taking into consideration all aspects of this process would be very complex and therefore not so useful for the common user.
5. However, a model has been suggested that has successfully reduced the number of necessary parameters but still enables the users to predict the general behaviour of the outcome of defined reactive sputtering processes.
6. Despite the simplicity of this model, it is frequently used as the base for more detailed treatments of reactive sputtering processes.
7. The starting point for developing a model is to try to define the processing conditions as correct as possible. Simplifications must be made to keep the complexity down without losing contact with reality.
8. We start with showing a schematic of a simplified reactive sputtering processing chamber as shown in Fig. 5.12.1.

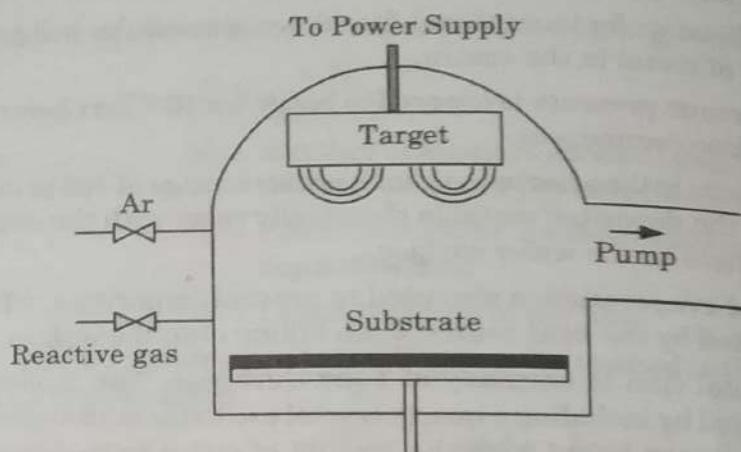


Fig. 5.12.1. A simple reactive sputtering system.

9. Fig. 5.12.1 illustrates the flux of sputtered particles from the target as well as the flux of reactive gas molecules arriving to the substrate.
10. A fraction (θ_t) of the target area (A_t) has reacted with the reactive gas and formed a compound layer at the target surface.
11. This is illustrated so that a fraction θ_c of the target surface area consists of the compound.
12. A similar situation will exist at the collecting (= substrate) area (A_c) but the reacted fraction (θ_c) of this area will not be the same as at the target.
13. During sputtering of the target, an out coming flux of sputtered metal atoms F_m will be generated.

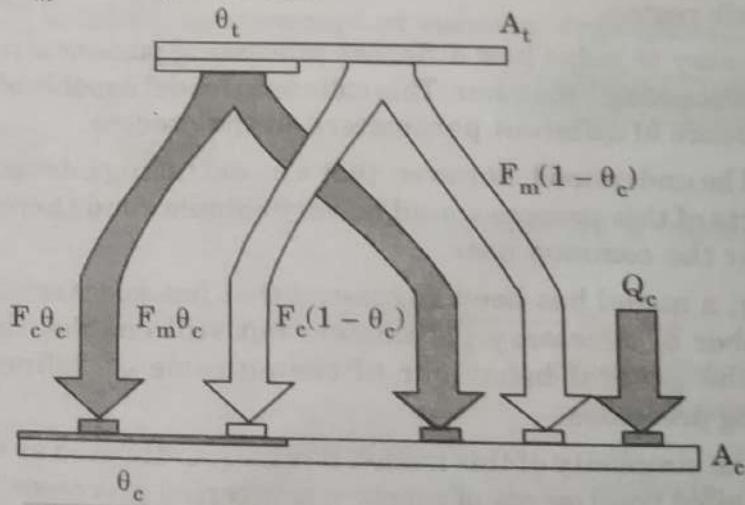


Fig. 5.12.2. Particle fluxes to the substrate area A_c .

PART-3

Packaging of VLSI Devices : Package Types, Packaging Design Consideration.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.13.

Discuss different types of packaging.

Answer

- There is a wide variety of package types that can be selected for VLSI devices. Recently there has been a proliferation of package types both for through-hole mounting and surface-mounting to PWBs.
- Fig. 5.13.1 illustrates the different methods of mounting to PWBs in use today.

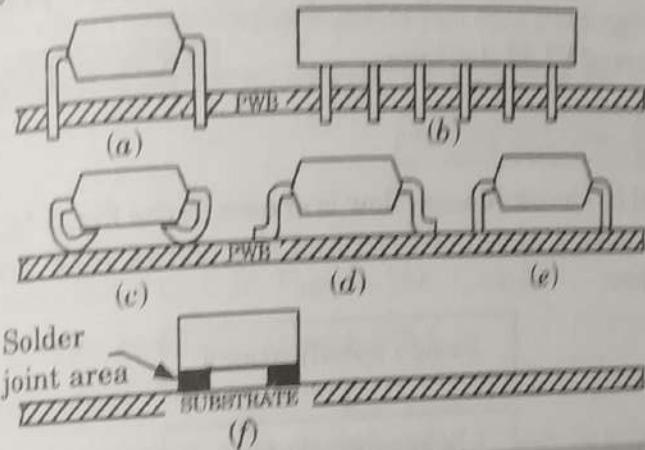


Fig. 5.13.1. (a) Dual-in-line package (b) Pin-grid-array package
 (c) "J" leaded packages, (d) Gull-wing-leaded packages
 (e) Butt-leaded package, (f) Leadless type.

- The through-hole (TH) types include the venerable dual-in-line package (DIP) and the newer pin-grid array (PGA), covering the range of I/Os from 8 through 300. Both types are available in hermetic ceramic and plastic types.
- In a hermetic package, the chip environment is decoupled from the external environment by a vacuum-tight enclosure. The finer-pitch through-hole packages present a challenge to PWB manufacturers to improve their process capability.
- The availability of new surface-mount (SM) packages has expanded greatly, although their acceptance has not advanced as quickly as foreseen.
- Reasons for the slow growth are the lack of availability of devices at a competitive price, lack of confidence in placing and soldering surface-mount packages, and unforeseen technical difficulties such as lead-coplanarity maintenance and differences in thermal coefficients of

- expansion (TCE) between packages (especially ceramic types) and PWB materials.
7. For SM package I/Os up to 28 terminals, the designer has a choice of a dual-in line type known as small outline (SO), available in plastic only, and the quad types known as chip carriers (CC) and flat packs, both available in hermetic ceramic and plastic.
 8. Above 28 I/O terminals, all SM packages are quad types only (Hermetic ceramic and plastic).
 9. CC packages are available in leaded plastic (PLCC) and leaded ceramic (LDCC) for mounting to PWB's, or leadless ceramic (LLCC) for mounting to boards with matching TCE or socketing.
 10. Leads may be of different geometric form ("J" versus gull wing), and located either on 1.27 or 0.635 mm pitches.

Que 5.14. Discuss and describe the various process design consideration of VLSI devices.

AKTU 2015-16, Marks 10

Answer

1. The VLSI IC circuits design flow is shown in the Fig. 5.14.1. The various levels of design are numbered and the blocks show processes in the design flow.

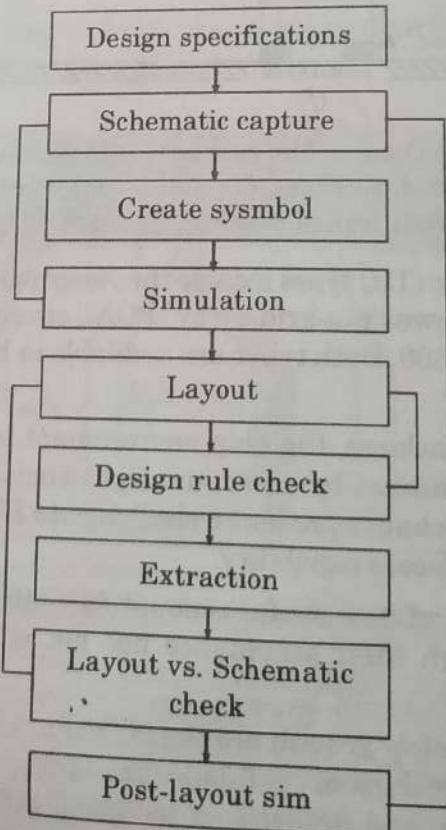


Fig. 5.14.1.

- VLSI Technology
 1. Specification and comes
 interface, and the a
 Behavioral descrip
 functionality, perfor
 specifications.
 4. RTL description is
 to test functionality
 5. RTL description is
 synthesis tools. A g
 of gates and connec
 6. Finally, a physical
 fabrication.

Que 5.15. Write sh
VLSI Technology. W

Answer

- A. Package types :
- B. Packaging des
- i. VLSI Design R
1. The establishme yields in VLSI p
2. Rules must be g must be compat
3. As the I/O coun space required f the chip area. N to produce qual
- ii. Thermal Desi
1. The objective o temperature of to temperatur acceptabl
2. The overall the sum of two the

2. Specification comes first, they describe abstractly, the functionality, interface, and the architecture of the digital IC circuit to be designed.
3. Behavioral description is then created to analyze the design in terms of functionality, performance, compliance to given standards, and other specifications.
4. RTL description is done using HDLs. This RTL description is simulated to test functionality. From here onwards we need the help of EDA tools.
5. RTL description is then converted to a gate-level netlist using logic synthesis tools. A gatelevel netlist is a description of the circuit in terms of gates and connections between them, which are made in such a way that they meet the timing, power and area specifications.
6. Finally, a physical layout is made, which will be verified and then sent to fabrication.

Que 5.15. Write short note on package types and packaging design VLSI Technology. What is meant by DIP ? Explain in brief.

AKTU 2017-18, Marks 10

Answer

- A. Package types : Refer Q. 5.13, Page 5-15F, Unit-5.
 B. Packaging design considerations are :

i. **VLSI Design Rules :**

1. The establishment of good chip design rules so that to achieve high yields in VLSI package assembly are absolutely essential.
2. Rules must be generated for the particular package type used and must be compatible with the assembly equipment to be used.
3. As the I/O count grows and the active VLSI device-size shrinks, the space required for interconnection could represent a major function of the chip area. Not only the pitch decrease, but the tolerance required to produce quality bonds must also decrease.

ii. **Thermal Design Considerations :**

1. The objective of thermal design is to keep the operating junction temperature of silicon die low enough to prevent the failure rate due to temperature-activated failure mechanisms from exceeding the acceptable limit for a particular application.
2. The overall thermal resistance in this model can be considered as the sum of two thermal resistance components θ_{jc} and θ_{ca} and defined as

$$\theta_{ja} = \theta_{jc} + \theta_{ca} \text{ } (\text{°C / watt})$$

$$\theta_{jc} = [T_j - T_c] / P$$

$$\theta_{ca} = [T_c - T_a] / P$$

θ_{ja} = Junction-to-ambient thermal resistance
 θ_{jc} = Junction-to-case thermal resistance
 θ_{ca} = Case-to-ambient thermal resistance
 T_j = Average die or junction temperature ($^{\circ}\text{C}$)
 T_c = Average case temperature ($^{\circ}\text{C}$)
 T_a = Ambient temperature ($^{\circ}\text{C}$)
 P = Power (Watts)

iii. Electrical Considerations :

1. Electrical performance at the IC-package level recently has been of general interest for silicon devices.
2. Several electrical performance criteria are of interest namely : low ground resistance, short signal leads, minimum power-supply spiking due to signal lines simultaneously switching, short paralleled-signal runs, short-length signal runs near a ground plane, and the maximum use of matched impedances to avoid signal reflection.
3. These criteria are, of course, not all mutually independent.
4. They may be related through simple geometric variables, such as conductor cross section and length, dielectric thickness, and dielectric constant of the packaging body.

iv. Mechanical Design Considerations :

1. As the size of VLSI die increases, it presents new challenges to the package designer.
2. Ideally, one would prefer to use materials in package construction that are matched in physical properties, in particular the TCE.
3. In the real world, however, we see that the materials currently in use have TCE that vary by orders of magnitude.
4. In the case of SSI and MSI the designer could achieve better matches by making engineering tradeoffs that did not degrade the packaged-device yields, performance, or reliability.

For example, in SSI plastic molded packages, the die (silicon) is attached directly to the lead frame (typically Alloy 42).

5. Alloy 42 has poor thermal conductivity but closely matches the TCE of silicon. The use of Alloy 42 minimizes thermal stresses and has negligible impact on the thermal design because of the low power levels encountered in SSI.
6. In VLSI, however, the use of a die with large Alloy 42 leadframe could bring on higher thermal stresses, resulting in die cracking and/or "popoff," or in degradation of performance and reliability due to high junction temperatures during normal operating conditions.

Que 5.16. What is the junction-to-ambient thermal resistance for a device dissipating 550 mW into an ambient of 70 °C and operating at a junction temperature of 125 °C ?

Answer

Given : $T_j = 125 \text{ }^{\circ}\text{C}$, $T_a = 70 \text{ }^{\circ}\text{C}$, $P = 550 \text{ mW}$
 To Find : Junction-to-ambient thermal resistance.

1. We have,

$$\theta_{ja} = \theta_{jc} + \theta_{ca}$$

$$\theta_{ja} = \frac{T_j - T_c}{P} + \frac{T_c - T_a}{P}$$

or,

$$\theta_{ja} = \frac{T_j - T_c + T_c - T_a}{P} = \frac{T_j - T_a}{P}$$

2. By putting the values,

$$\theta_{ja} = \frac{125 - 70}{0.550} = 100 \text{ }^{\circ}\text{C/W}$$

PART-4

VLSI Assembly Technologies, Package Fabrication Technologies, CMOS Fabrication Steps.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.17. Write a short note on die interconnection.

Answer

1. Die interconnection consists of two steps.
2. In the first step, the back of the die is mechanically attached to an appropriate mount medium, such as a ceramic substrate, multilayer-ceramic-package-piece part, or metal leadframe.
3. This attachment sometimes enables electrical connections to be made to the back of the die. The two common die-bonding methods are hard solders (or eutectic) and polymers.
4. In the second step, the bond pads on the circuit side of the die are electrically interconnected to the package.

5. The three common schemes of interconnection to the chip bond pads are wire bonding, TAB, and flip-chip solder bonding, also called Controlled-Collapse Bonding (CCB). All three processes are extensively used for SSI and MSI packaging.
6. Wire bonding is further split into different processes, such as thermosonic and thermocompression ball-and-wedge using Au wire, and ultrasonic wedge-wedge using both Au and Al wires. All of these processes are directly applicable to the VLSI die.
7. The most popular bonding process in general use for VLSI die up to 132 I/Os is the thermosonic ball-to-wedge process. TAB and area-array solder interconnections are also in use today.

Que 5.18. Explain the die bonding.

Answer

1. Die size is steadily growing, in proportion to the emergence of improved VLSI technology capabilities. Increased die size places more stringent demands on the processing and reliability of die bonding.
2. Die-Bonding technology for a large VLSI die requires special attention to thermal and stress management.
3. In addition, similar care must be exercised in the selection of a die-bond process for the particular application and in the implementation of stringent process controls to assure high-quality bonds.
4. VLSI die size also impacts wafer fabrication guidelines and assembly automation. These issues influence equipment selection and determine how easily a controllable process can be achieved.
5. The major choices for a die-attach process include hard solder (or eutectic), polymers (epoxies and polyimides), and Ag-filled glasses.
6. A comparison of the die-attach processes for hermetic, ceramic and plastic packages shows two emerging technologies for VLSI, eutectic for hermetic ceramic and polymers for plastic.
7. The eutectic process is essentially contamination-free, has excellent shear strength, and assures low-moisture packages.
8. The major disadvantages are that it is difficult to automate and that it places high thermal stresses on the die due to the high process temperature.
9. New ceramic substrate materials such as AlN, whose TCE closely matches that of silicon, make this process more viable for large VLSI die in hermetic ceramic packages.
10. The polymer die-attach process has two materials that are contenders for VLSI in plastic.

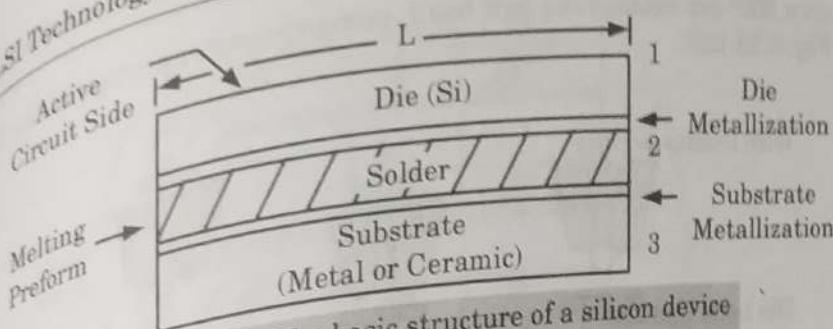


Fig. 5.18.1. The basic structure of a silicon device die bonded with a metal preform.

11. Epoxies (with and without Ag flakes for electrical and thermal conduction) have the advantage of being easy to automate, and require low-temperature curing which minimizes thermal stress in large die.
12. Polyimides (with and without Ag) are also easy to automate. They require higher curing temperatures, leading to high thermal stress, especially when used with high TCE copper leadframes.
13. Copper is the preferred material for handling the power dissipation requirements of VLSI.
14. On the other hand, epoxies are higher in hydrolyzable ions that could have a direct impact on reliability. Epoxy suppliers have improved their materials to remove the major objections and these materials are being widely used today for VLSI.
15. Polyimides are difficult to process without voids, which affect thermal performance and have contributed to die cracking.
16. The use of polyimides should be limited to packages using bonding media with a closely matched TCE, such as Alloy 42 leadframes and ceramic substrates.

Que 5.19. Discuss in brief wire bonding.

Answer

1. Wire bonding is always performed on ICs after they have been die-bonded to the appropriate piece part, be it a leadframe paddle or the cavity of a ceramic package or substrate.
2. Typically, gold wire is ball-wedge bonded (thermosonic or thermocompression); that is, ball-bonded to the chip bond pad (typically aluminium) and wedge-bonded to the package substrate (typically Au or Ag), as shown in Fig. 5.19.1.
3. One advantage of ball-wedge bonding comes from the symmetrical geometry of the capillary tip.
4. The ball bond is formed by the inner portion of the tip as shown in Fig. 5.19.1(b), and then the wedge bond can be performed anywhere

on a 360° arc around the ball bond, using the outer portion of the tip
Fig. 5.19.1(d).

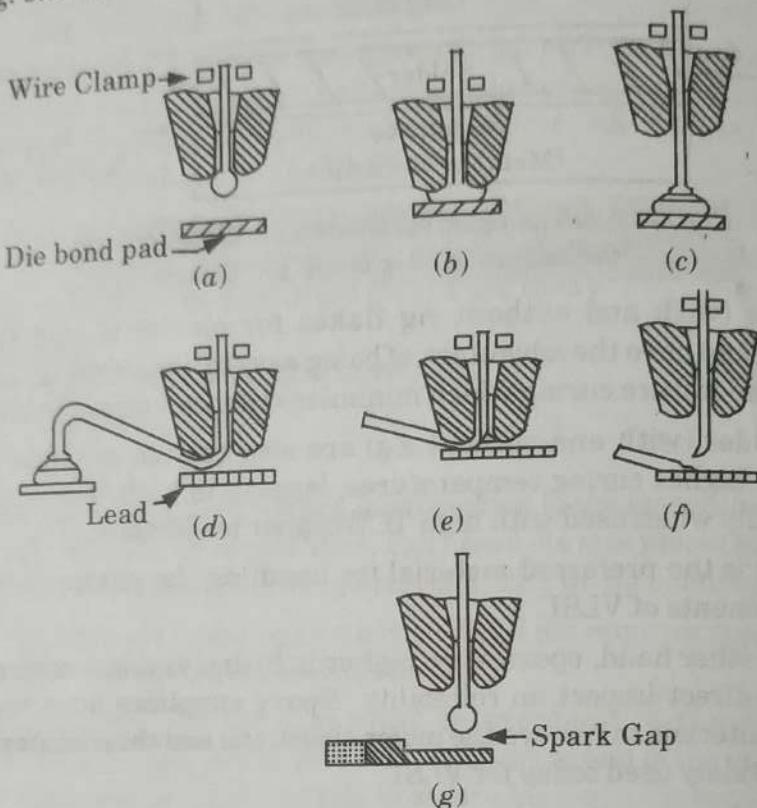


Fig. 5.19.1. Tailless ball-and-wedge bonding cycle.

- This capability to dress the wire in any direction from the ball is the key factor that makes this process attractive for high-speed automated bonding *i.e.*, the bonding head or package table does not have to rotate to form the wedge bond.

Que 5.20. Discuss the ceramic package technology with the help of diagram.

Answer

- Fig. 5.20.1 illustrates multilayer ceramic technology. A dispersion or slurry of ceramic powder and liquid vehicle is first prepared, and then cast into thin sheets by passing a leveling or doctor blade over the slurry.
- After drying, the sheets are cut to size, via-holes and cavities are mechanically punched into the sheet, custom wiring paths are screened onto the surface and the via-holes are filled with metal.
- Several of these sheets are press-laminated together in a precisely aligned fixture, and the entire structure is fired at 1600°C to form a monolithic sintered body.

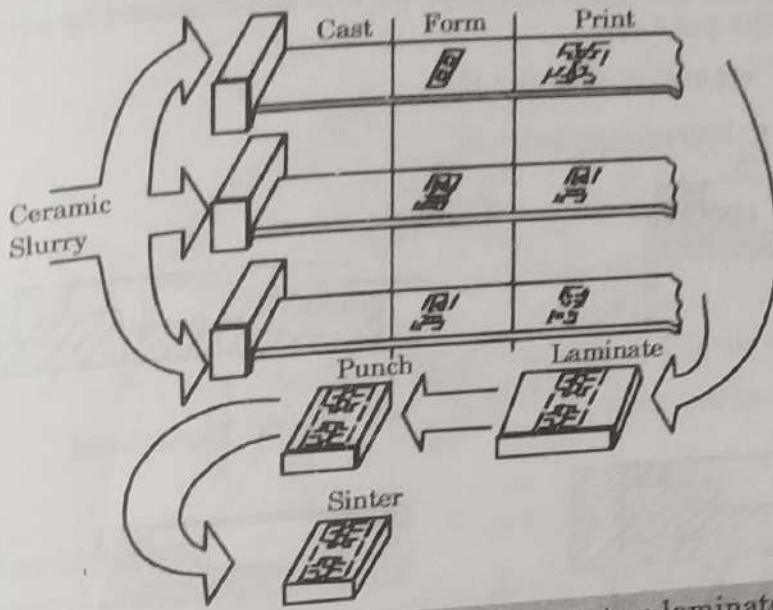


Fig. 5.20.1. Process sequence to create a laminated refractory-ceramic product starting from a ceramic slurry.

4. The refractory ceramic technology is a complex process requiring careful process control throughout.
 5. After the laminate is sintered, it is ready for the finishing operations of lead attachment and metallization plating. Nickel is plated over the tungsten in preparation for lead brazing.
 6. The lead material is a Fe-Ni-Co alloy called Kovar; the brazing material is a silver-copper eutectic alloy.
 7. All exposed metal surfaces are electro- or non-electroplated (usually gold over nickel) for bondability and environmental protection.
 8. Multilayer ceramic packages can be made up to 100 by 100 mm in lateral dimensions to a tolerance of $\pm 0.5\%$, and with up to 30 layers in the most advanced processes.
 9. Ceramic package technology is very effective for constructing complex packages with many signal, ground, power, bonding, and sealing layers.
- Types of ceramic package :**
1. Fig. 5.20.2 illustrates a variety of potential refractory-multilayer-ceramic package types.
 2. Packages can have brazed pins or leads, and edge or array pinouts.
 3. The package designer has the option of locating the die cavity either on the side with the pins or the side away from the pins.
 4. Devices requiring good thermal-dissipation characteristics are packaged with the cavity on the leadend side.
 5. This provides a direct thermal path to the surface (facing away from the PWB), which is exposed to the air flow.

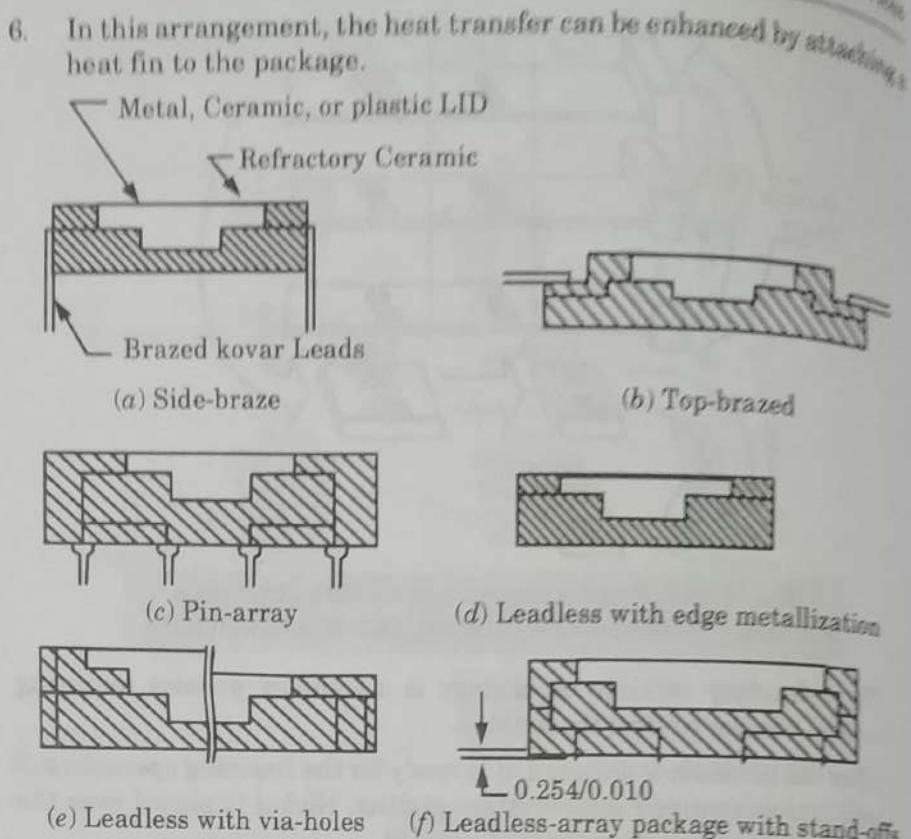


Fig. 5.20.2. Cross-sectional sketches of several package types.

Que 5.21. Explain the plastic molding technology with its diagram.

Answer

1. Fig. 5.21.1 shows a cross section of a plastic DIP. The two basic types of molded devices are postmolded and premolded devices.
2. The postmolded package is the lower-cost of the two and is the predominant package technology in use today.
3. This technology uses thermosetting (crosslinking) epoxy resins and is molded around the leadframe-chip subassembly after the chip is wire-bonded to the leadframe.
4. The postmolding process is relatively harsh.
5. To avoid the exposure of the die and its wire bonds to viscous molding material, the premolded-package concept was developed.
6. Here the package is molded first, and then the chip and interconnects are added.
7. The molding may be performed with the thermoset mentioned above or with thermoplastic (melting) polymers, such as polyphenylene sulfide.

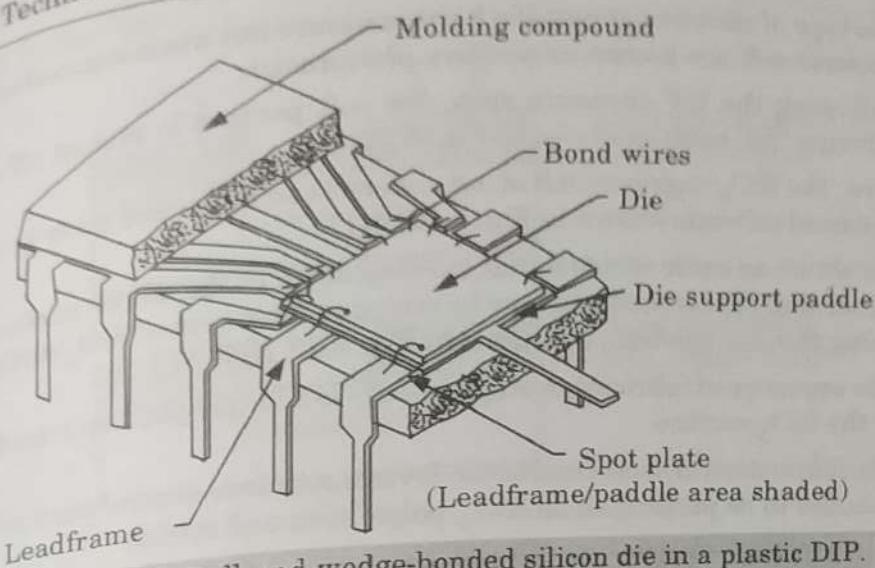


Fig. 5.21.1. Ball-and-wedge-bonded silicon die in a plastic DIP.

8. The premolded package is the plastic equivalent of the refractory-ceramic-cavity package and has great future potential for VLSI devices.
9. The polymers most commonly used for IC packaging are epoxies. The original epoxy resin, used to mold ICs, was made by condensing epichlorohydrin with bisphenol-A to produce a material called Epoxy-A.
10. An excess of epichlorohydrin was used to leave epoxy groups on each end of the low-molecular-weight polymer.

Que 5.22. Write short notes on MOS IC fabrication technique.

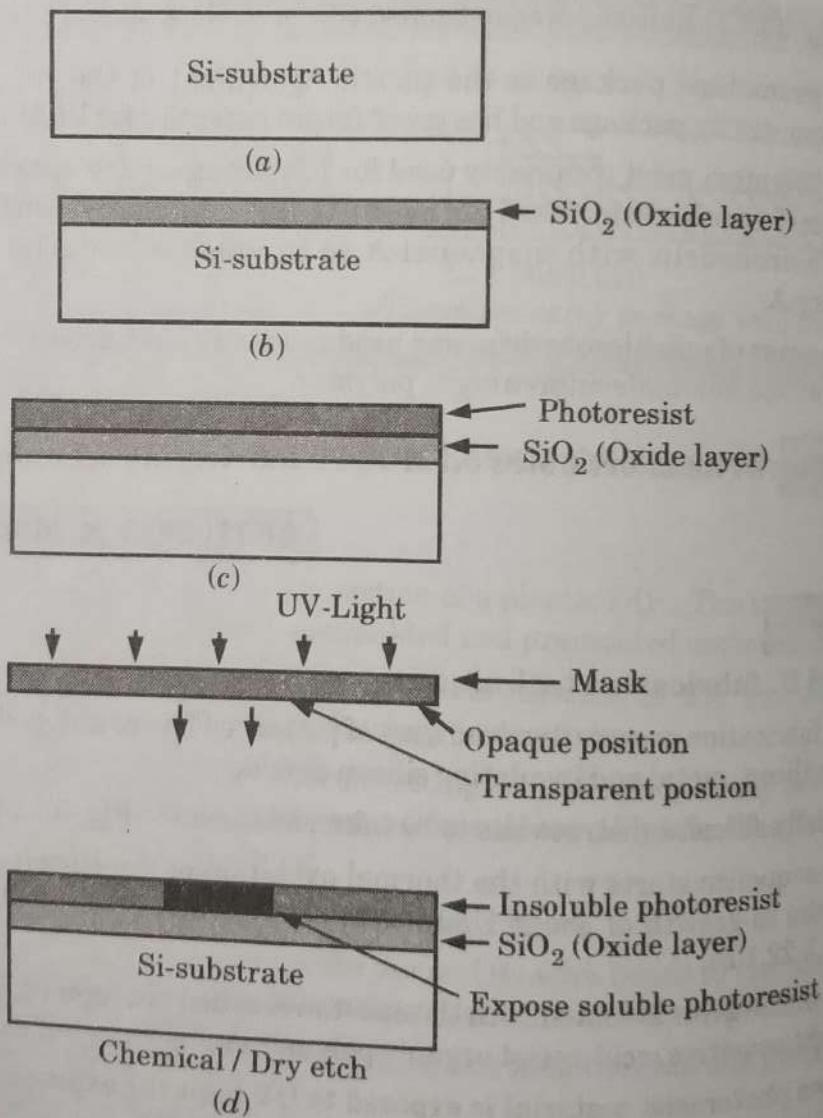
AKTU 2015-16, Marks 05

Answer

MOS IC fabrication technique :

1. The fabrication process involved a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide.
2. Initially silicon substrate has to be taken as shown in Fig. 5.22.1(a).
3. The sequence starts with the thermal oxidation of the silicon surface, results in growth of about 1 mm thickness of SiO_2 layer as shown in Fig. 5.22.1(b).
4. The entire layer is coated with the substance called photoresist, which is a light sensitive, acid-resist organic polymer as shown in Fig. 5.22.1(c).
5. When photoresist material is exposed to UV light the exposed portion become soft so that solvents can easily etch that portion.
6. To select the specified position for exposure we use mask, it allows the passage of UV light from its transparent portion as shown in Fig. 5.22.1(d).

7. The type of photoresist initially hard in nature but when exposed to light becomes soft are known as positive photoresist.
8. Following the UV exposure step, the soft portion is etched off using solvents (HF acid) as shown in Fig. 5.22.1(e).
9. Now, the SiO_2 region which is not covered can be etched away by using chemical solvents shown in Fig. 5.22.1(f).
10. We obtain an oxide window that reaches down to the silicon surface, the remaining photoresist can now be stripped from rest of SiO_2 surface by using another solvents as shown in Fig. 5.22.1(g).
11. The sequence of fabrication step actually is a single pattern transfer on to the SiO_2 surface.
12. The fabrication of semi-conductor devices requires several such pattern transfer to be performed on SiO_2 , polysilicon and metal.



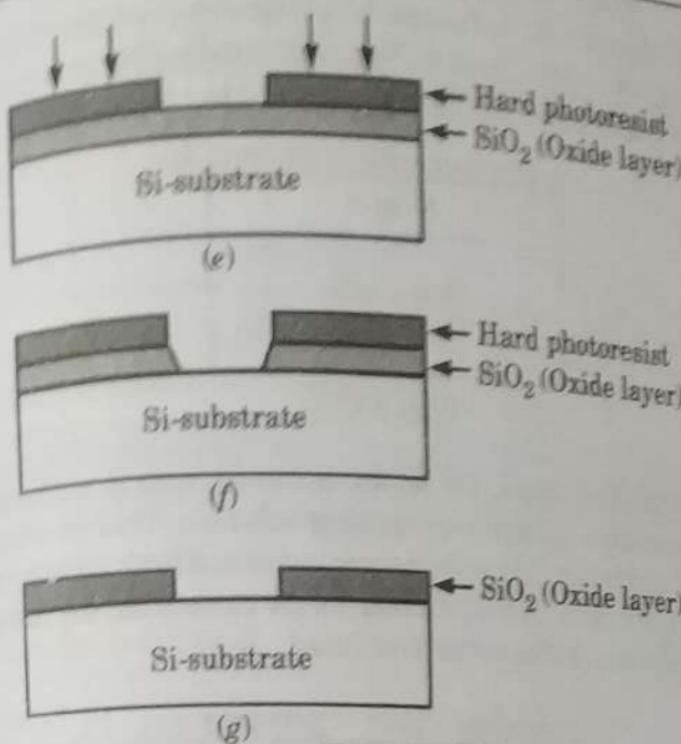


Fig. 5.22.1.

Que 5.23. How a *NPN* transistor can be fabricated? Explain all the steps of fabrication. Also compare it with NMOS fabrication.

AKTU 2017-18, Marks 10

Answer**A. Steps of fabrication NPN transistor :**

- Initially, we take a piece of *p*-type Si-substrate as shown in Fig. 5.23.1.

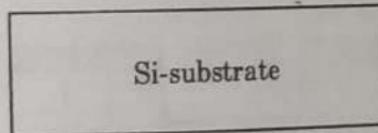


Fig. 5.23.1. ~

- The *N*-type layer is grown by the placing the wafer in a special furnace called reactor. This process is called as epitaxial.

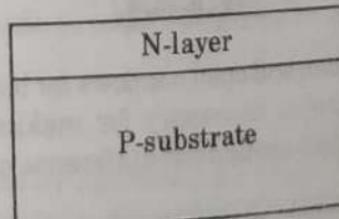


Fig. 5.23.2.

3. A thin layer of silicon dioxide SiO_2 is grown over the N -type layer by exposing the wafer of oxygen. This layer is commonly called an insulating layer or oxide layer. This process is called as oxidation.

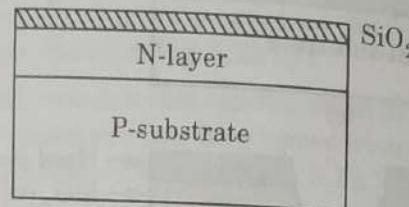


Fig. 5.23.3.

4. After oxidation again, the wafer is coated with a uniform film of a photosensitive emulsion or etching solution. This process is called photolithography. The wafer is now immersed in an etching solution by hydrofluoric acid. This acid removes the oxide from the areas through which the impurities are to be diffused.

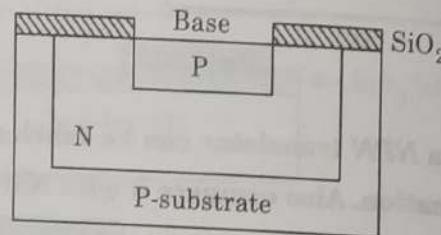


Fig. 5.23.4.

5. After that the oxidation, the photoresist and masking process is repeated. This creates windows in the silicon dioxide layer as shown in Fig. 5.23.8. The next is to introduce impurities such as phosphorus by similar diffusion process i.e., N -type emitter is now diffused into the base of p -type layer as shown in Fig. 5.23.5.

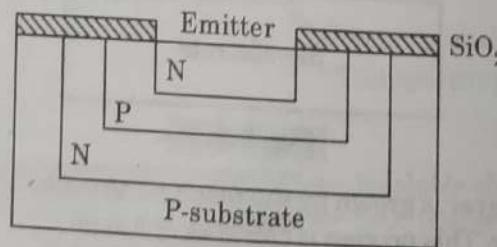


Fig. 5.23.5.

6. After that the oxidation and open windows for base, emitter, and collector contact. Metallization is necessary for making interconnections and providing bonding pads around circumference of the chip for connection of wires.

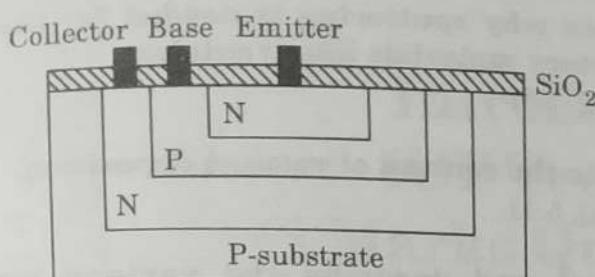


Fig. 5.23.6.

B. Comparison :

S.No.	NMOS fabrication process	NPN fabrication process
1.	Field oxide growth Oxide etch Source-drain diffusion	Thermal oxidation HF etch Boron diffusion
2.	Oxide etch Gate oxide growth	HF etch Thermal oxidation
3.	Via hole etch	HF etch
4.	Aluminum metal deposition Aluminum etch Contact anneal and surface state reduction	Evaporation Wet chemical etch Furnace anneal in H ₂ /N ₂

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

- Q. 1. Explain the metallization and describe the problems associated with this process. Explain DC sputtering method of metallization.**

Ans: Refer Q. 5.5.

- Q. 2. What do you mean by sputtering? Explain sputtering yield. Draw the schematic diagram of signal parallel-plate sputtering system and its working.**

Ans: Refer Q. 5.7.