Practice Problems for Topic 10

CIS*2030: Structure and Application of Microcomputers

The practice problems below are important, but will *not* be marked. Their purpose is to ensure that you understand the major concepts covered in Topic 10. Doing these problems by yourself is imperative, as a portion of the marks on the final exam will be based on questions related to Topic 10.

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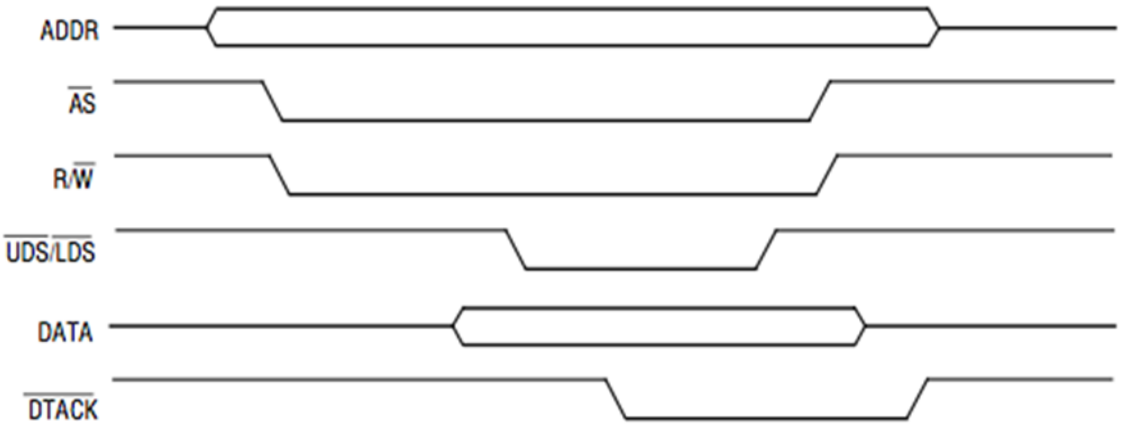
1. In the context of the 68000's ISA, describe what is meant by the following three terms: Clock Cycle, Bus Cycle, and Instruction Cycle.

2. Assume that a 68000 processor is driven by external clock with a frequency of 12 Megahertz. What is the clock period in nanoseconds?

3. Assume that the external clock used to drive a 68000 processor has a period of 0.5 microseconds. What frequency is the 68000 running at in Megahertz?

4. The 68000 does not connect the least-significant bit of an address to (i.e., A_0) to an address pin (i.e., bus signal). How, then, does the 68000 perform read or write operations on bytes?

5. Use the timing-diagram below for a 68000 bus cycle to answer the questions that follow:



a) Does the timing diagram illustrate a *read* cycle or *write* cycle? Explain.

b) Does the bus cycle indicate a *byte* or *word* data transfer? Explain.

c) Annotate the timing diagram above to show the *handshaking* that takes place between the processor and the device that it is communicating with. Use the same method as used in class (i.e., hello, goodbye, circles, arrows).

6. The table below shows a loop consisting of 3 instructions, as well as a single instruction outside of the loop that may be considered as overhead. The number of clock cycles required to perform each instruction is also shown for each instruction. Notice that the last BNE instruction comes in two forms depending on whether the branch is taken. In particular, the branch takes 10 clock cycles each time it is taken, but only 8 clock cycles when the branch is not taken.

Instructions		Clock cycles	
		Overhead	**Loop**
	MOVE.B #10,D0	8	
LOOP	ADD.W (A1)+,D3		8
	SUBQ.B #1,D0		4
	BNE LOOP		10 (8)

a) How many total clock cycles does the previous code require to execute?

b) If the first instruction in the code fragment is replaced with MOVE.B #N,D0, where N is the number loaded into D0, what is the maximum number of clock cycles?

c) What is the execution time (in microseconds) of the code in the able assuming that the 68000 is running at a clock frequency of 8 MHz?

7. According to Appendix D of your textbook, the instruction MOVE.L #1,(A0) requires 20 clock cycles to execute. These clock cycles are based on the need for 3 bus cycles to fetching the operation word and two extension words containing the immediate value, and 2 bus cycles for storing the 32-bit value in memory.

    a) If the 68000 is running at a clock frequency of 10 MHz, what is the execution time of the instruction in microseconds?

    b) Now assume that the memory is "slow" causing the processor to insert one additional wait state for each read/write bus cycle. How long does the instruction take to execute?

8. A faulty memory causes a watchdog timer to generate a BERR exception. This causes the top 7 words to appear on top of the supervisor stack:

   $0009
   $0100
   $1234
   $4247
   $0701
   $00A1
   $1C40

   a) Was a read or write memory transaction being performed?

   b) Was data or an instruction being accessed?

   c) Was the operating system or a user program running?

   d) What address was being accessed?

   e) What is the operation word contained in the processor's instruction register?

   f) What were the values of the CCR flags?

   g) What was the next instruction to be executed had the exception not been generated?