Practice Problems for Topic 11

CIS*2030: Structure and Application of Microcomputers

The practice problems below are important, but will *not* be marked. Their purpose is to ensure that you understand the major concepts covered in Topic 11. Doing these problems by yourself is imperative, as a portion of the marks on the final exam will be based on questions related to Topic 11.

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1. With isolated I/O the
    a) memory and I/O devices share the processor's address space
    b) memory and I/O devices have separate address spaces
    c) all instructions can be used to access the ports of I/O devices
    d) None of the above

2. To help alleviate the slower operating speeds of I/O devices compared to processors, I/O interfaces and controllers use
    a) Control registers
    b) Buffered ports
    c) Status registers
    d) None of the above

3. The I/O strategy that requires the processor to continuously interrogate a status flag in the I/O interface or controller is called
    a) Memory-mapped I/O
    b) Interrupt-Driven I/O
    c) Polling
    d) DMA

4. How many priority levels of interrupts does the 68000's ISA define?
    a) Seven
    b) Six
    c) Eight
    d) None of the above

5. If a level-4 interrupt occurs while a 68000 processor is servicing a level-5 interrupt, the processor will
    a) Ignores the level 4 interrupt request
    b) Holds the level 4 interrupt pending until the level-5 interrupt service routine completes
    c) Service the level-4 interrupt immediately
    d) None of the above

6. When an auto-vectored interrupt occurs, the vector number is provided by the
    a) 68000 Processor
    b) Interrupting device
    c) Interrupt-service route
    d) Priority level of the interrupt

7. Input-Output strategies that employ a clock as part of the communication protocol they use to send and receive data are
    a) Synchronous
    b) Parallel
    c) Asynchronous
    d) Serial
    e) None of the above

8. A 68000-based system uses a 68681 DUART for serial communication with a dumb terminal. The base address of the DUART is 0x00F001. In each case below, write a single 68000 instruction to program the DUART as indicated. Use absolute long addressing for the destination operand.

    a) To use 8 data bits and even parity.
    b) To use one stop bit.
    c) To send and receive data at 4800 baud.
    d) To turn on both the sender and receiver ports.

9. Assuming the configuration in the previous problem

    a) How many seconds would be required to transfer 512 characters? Show your work.

    b) What is the overhead in percent used by the control bits in each character? Show your work.

10. Below, you will find pseudo-code for an interrupt-service route. The ISR is designed to transfer 1K bytes from an I/O device to memory. [2 marks]

    [1] Initialize an address register with the destination memory address. (4)
    [2] Initialize a data register with the number of bytes (1K) to transfer (4)
    [3] Start Loop
    [4] Load a byte from the I/O device (8)
    [5] Store byte at address in address register (8)
    [6] Add 1 to the address in the address register (4)
    [7] Subtract 1 from the data register indicating one fewer byte to transfer (4)
    [8] Continue loop while the value in the data register is not zero (10)

    At the end of each line above is a value in parenthesis. Each value is the number of clock cycles required to execute that step of the ISR.

    Assuming that overhead associated with processing the interrupt via the 68000's exception-processing mechanism is 40 clock cycles, how many total clock cycles are required to run the ISR in order to transfer the 1K bytes from and I/O device to memory?

11. This question refers to the previous question. Now assume that the system contains a DMA controller that requires 80 clock cycles for initialization and overhead. Also, assume that each DMA transfer takes 2 clock cycles to transfer one byte from the I/O device to the memory. How many total clock cycles are required to transfer the 1K bytes from the I/O device to memory using DMA?