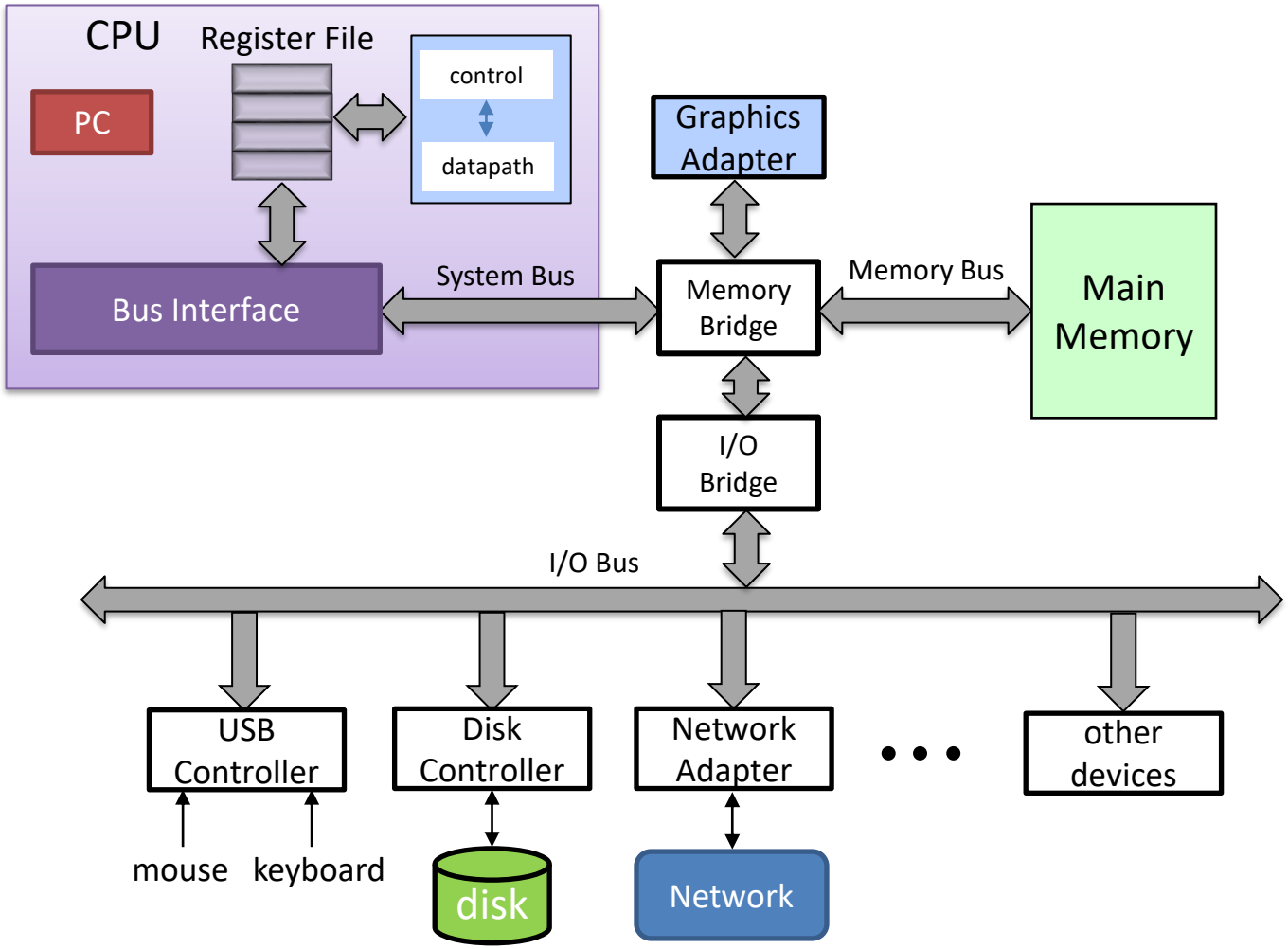
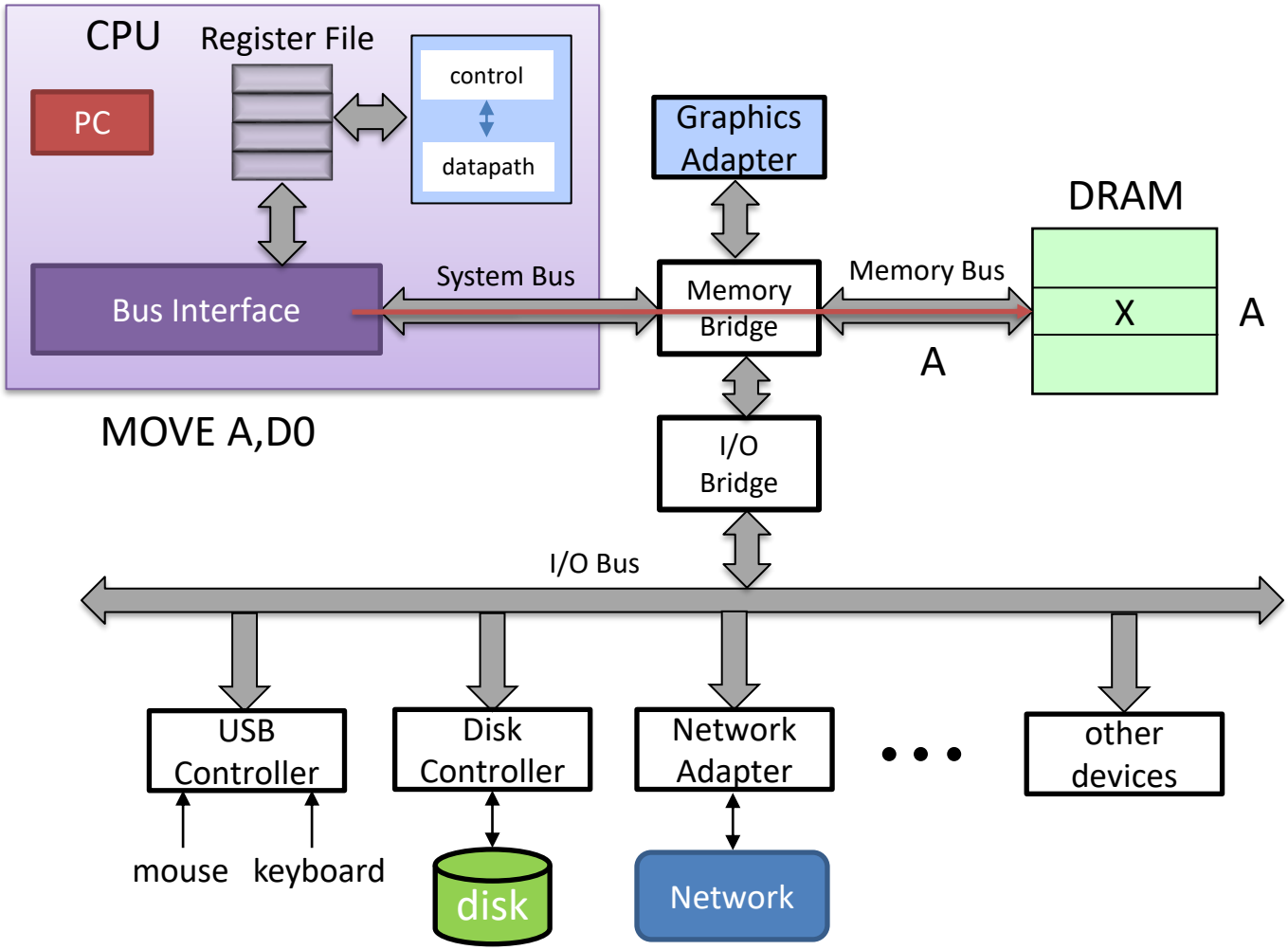
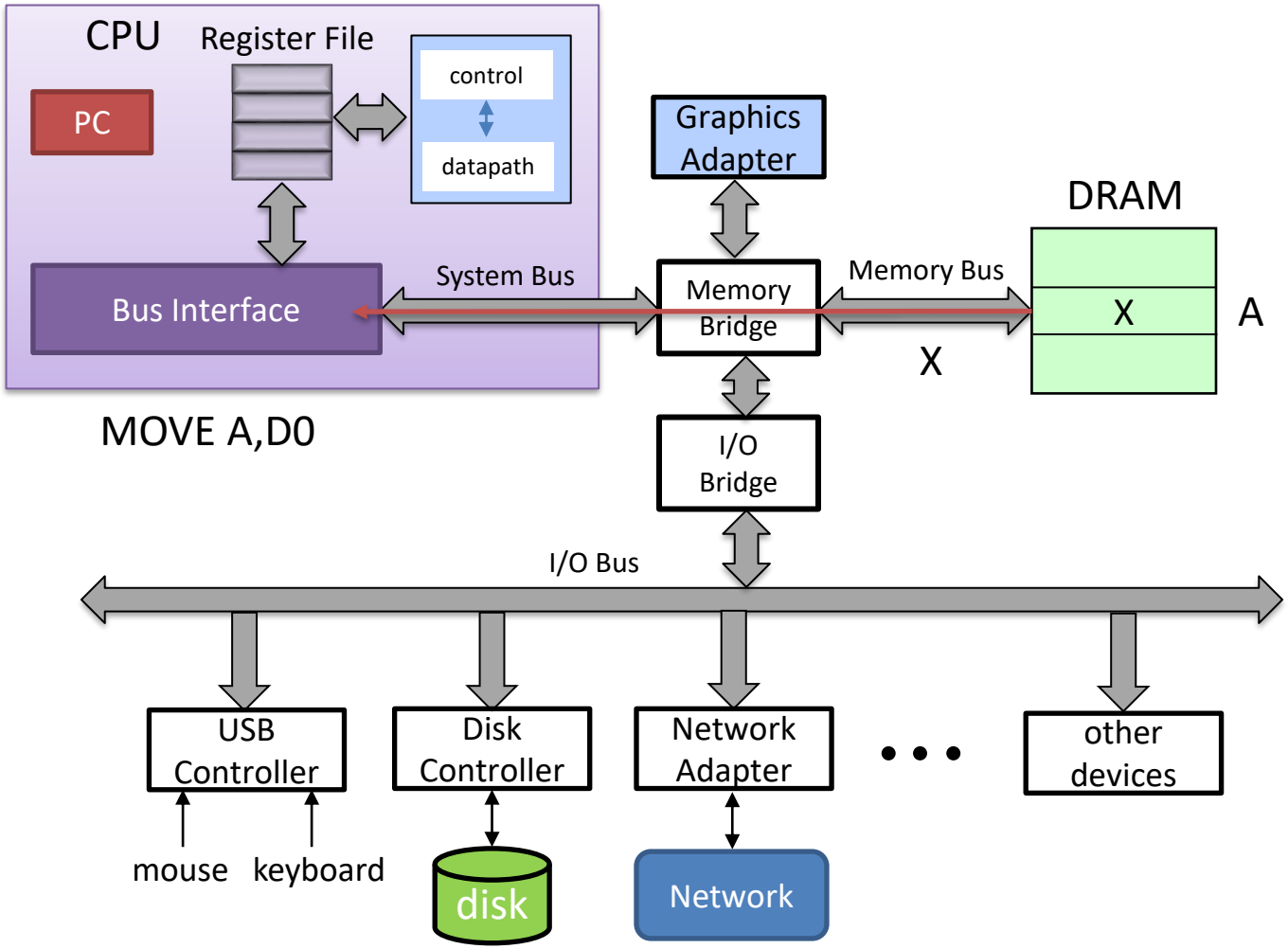
Logical View of a Traditional Computer



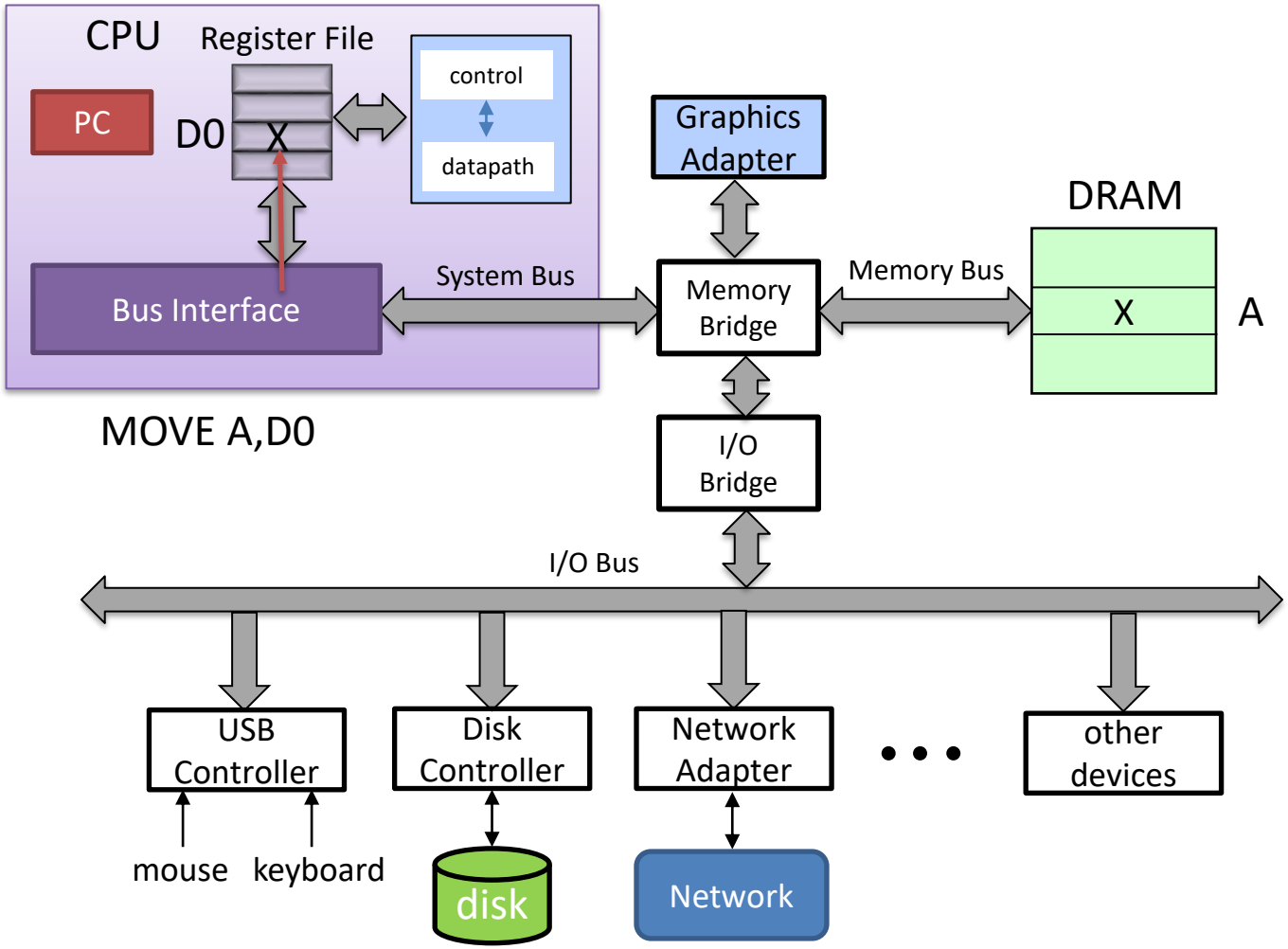
Logical View of a Traditional Computer



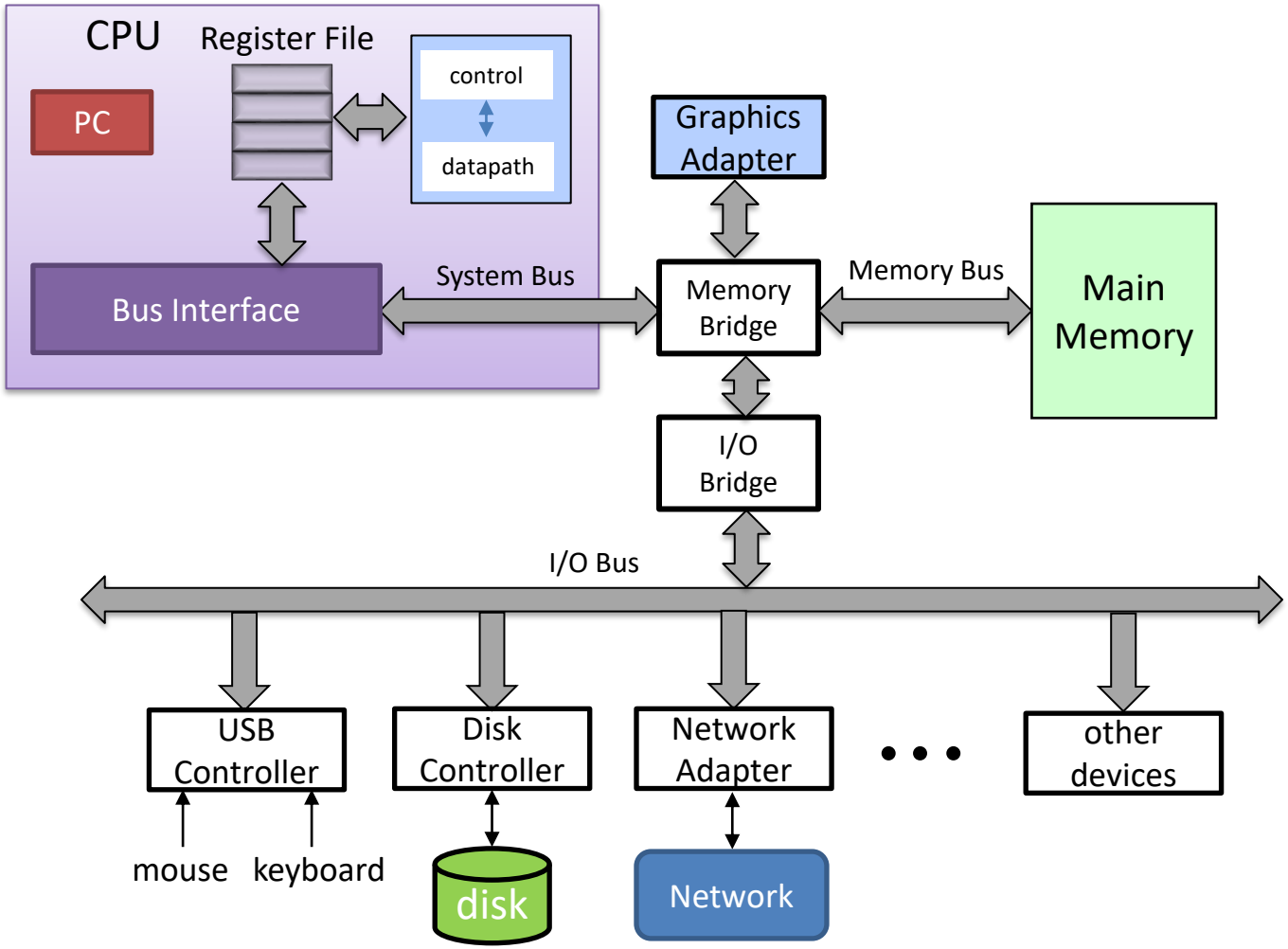
Logical View of a Traditional Computer



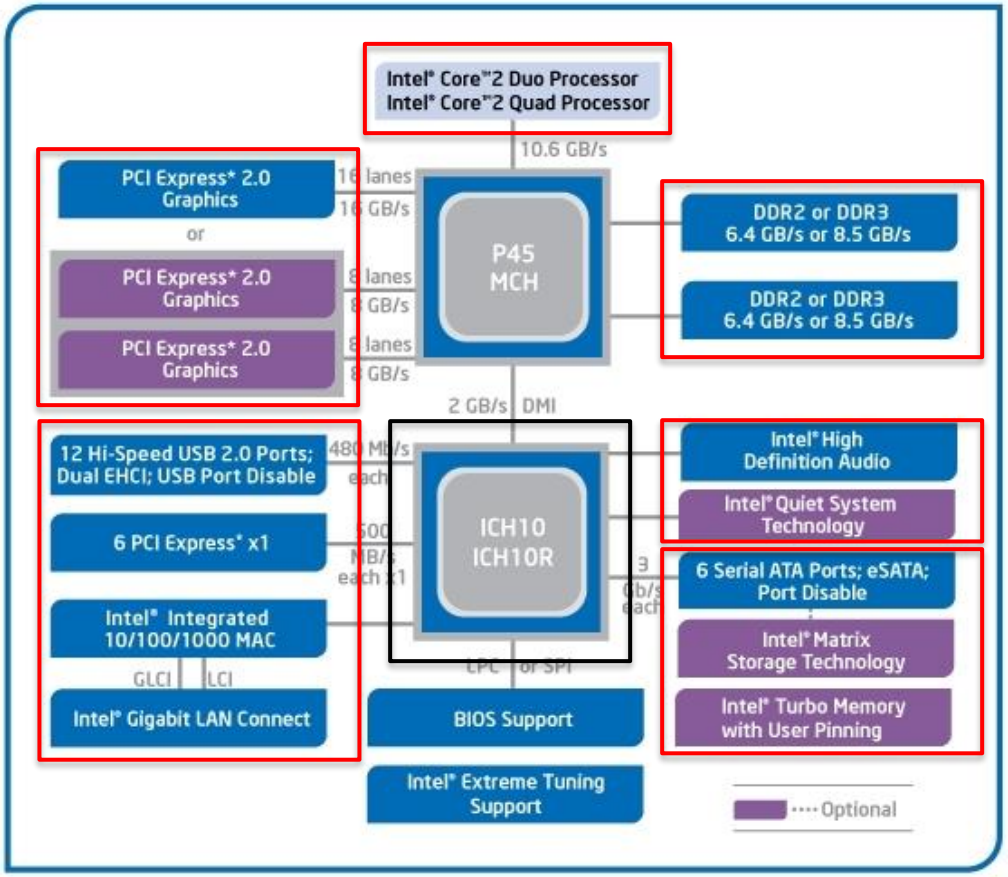
Logical View of a Traditional Computer



Logical View of a Traditional Computer

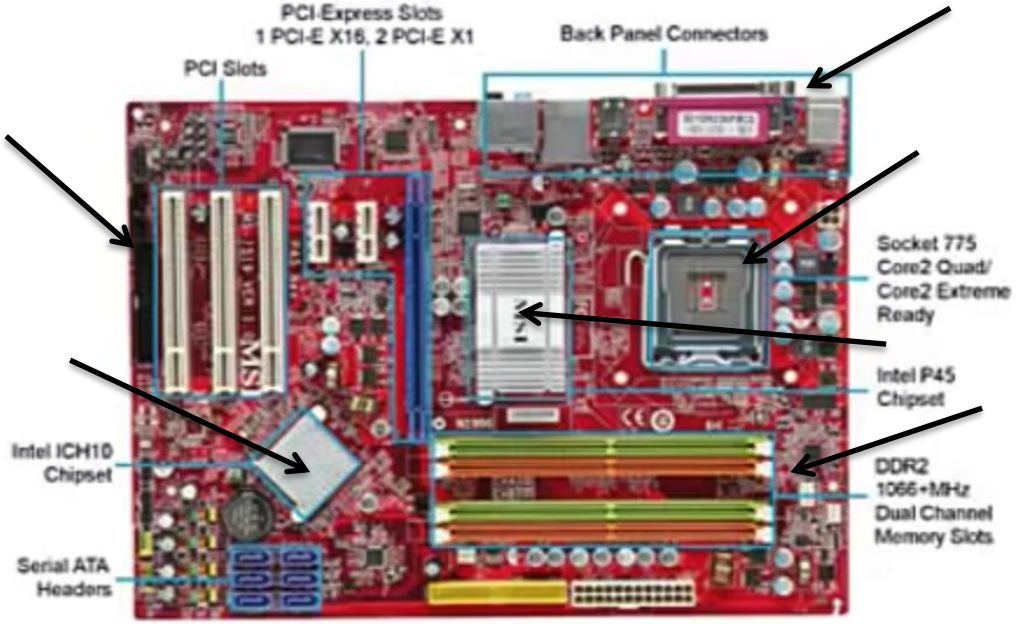


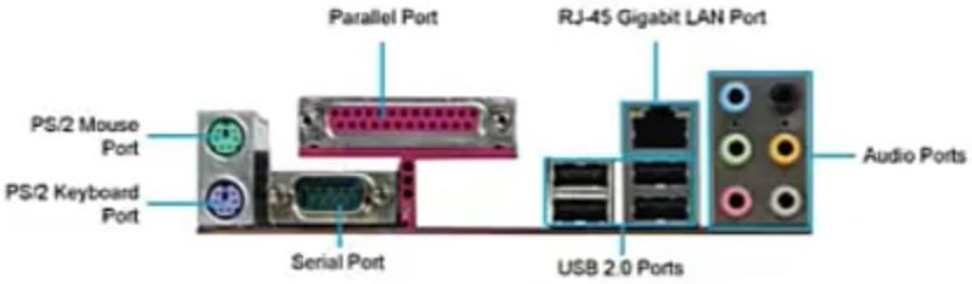
Semi-Logical View of Traditional Computer



Intel® P45 Express Chipset Block Diagram

Physical View of Computer

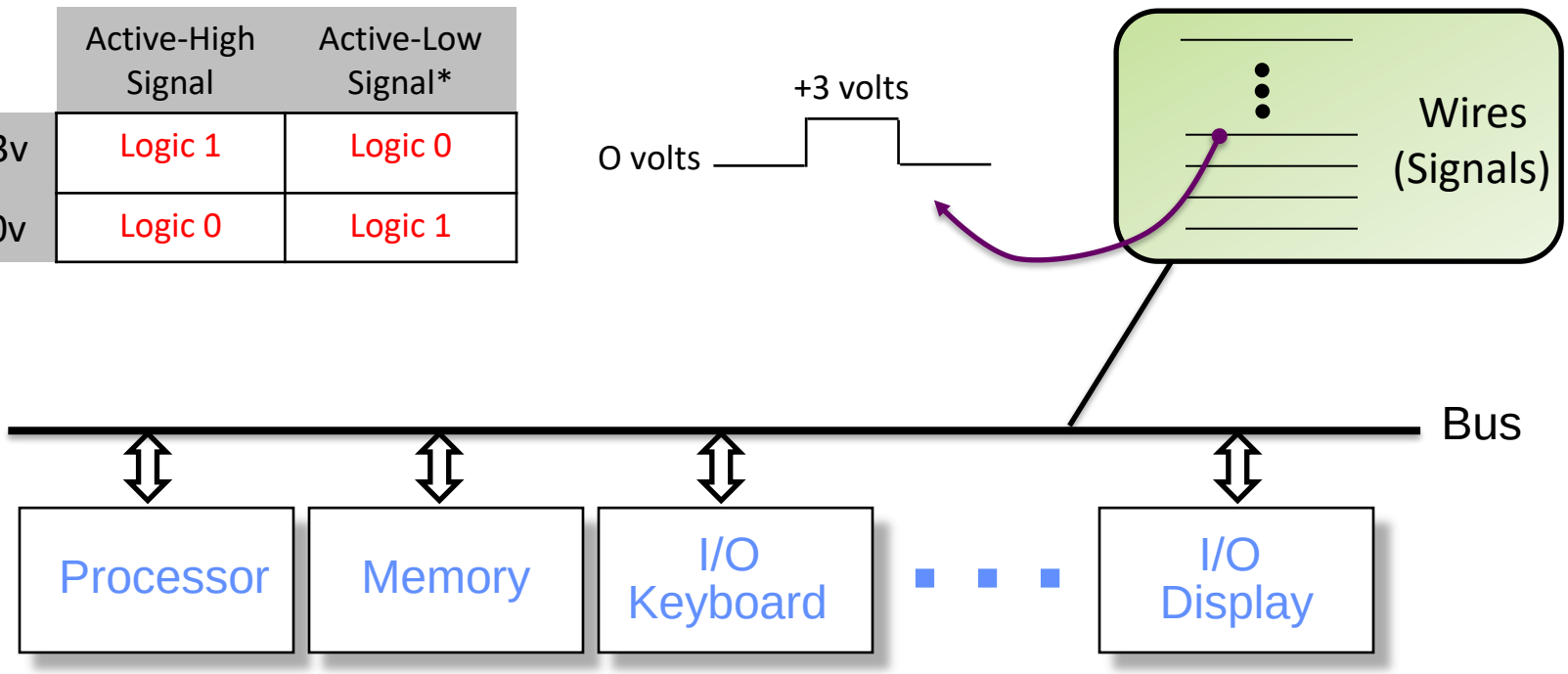




Buses

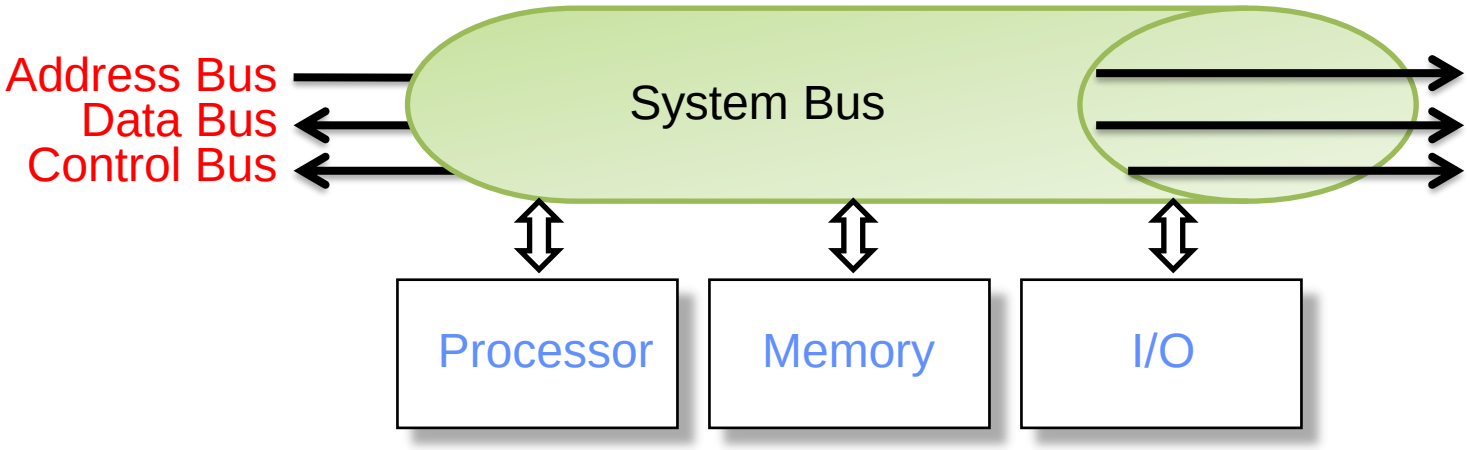
- Traditional way to connect CPU, main memory, and I/O devices
  - A set of parallel wires for carrying bits which is shared by a number of devices

	Active-High Signal	Active-Low Signal*
+3v	Logic 1	Logic 0
0v	Logic 0	Logic 1



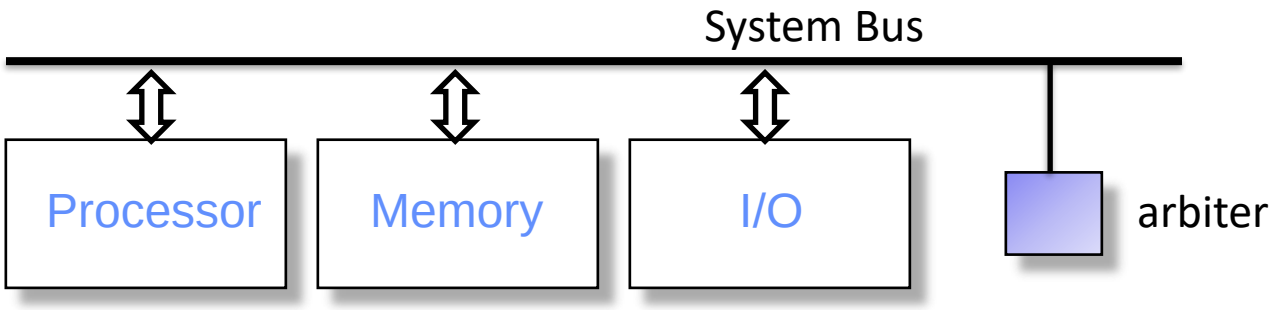
System Bus Sub-Assemblies

- The system bus consists of individual signals organized into three sub-assemblies
  - Address bus transports addresses of memory and I/O devices
  - Data bus transports data and instructions
  - Control bus transports synchronization signals



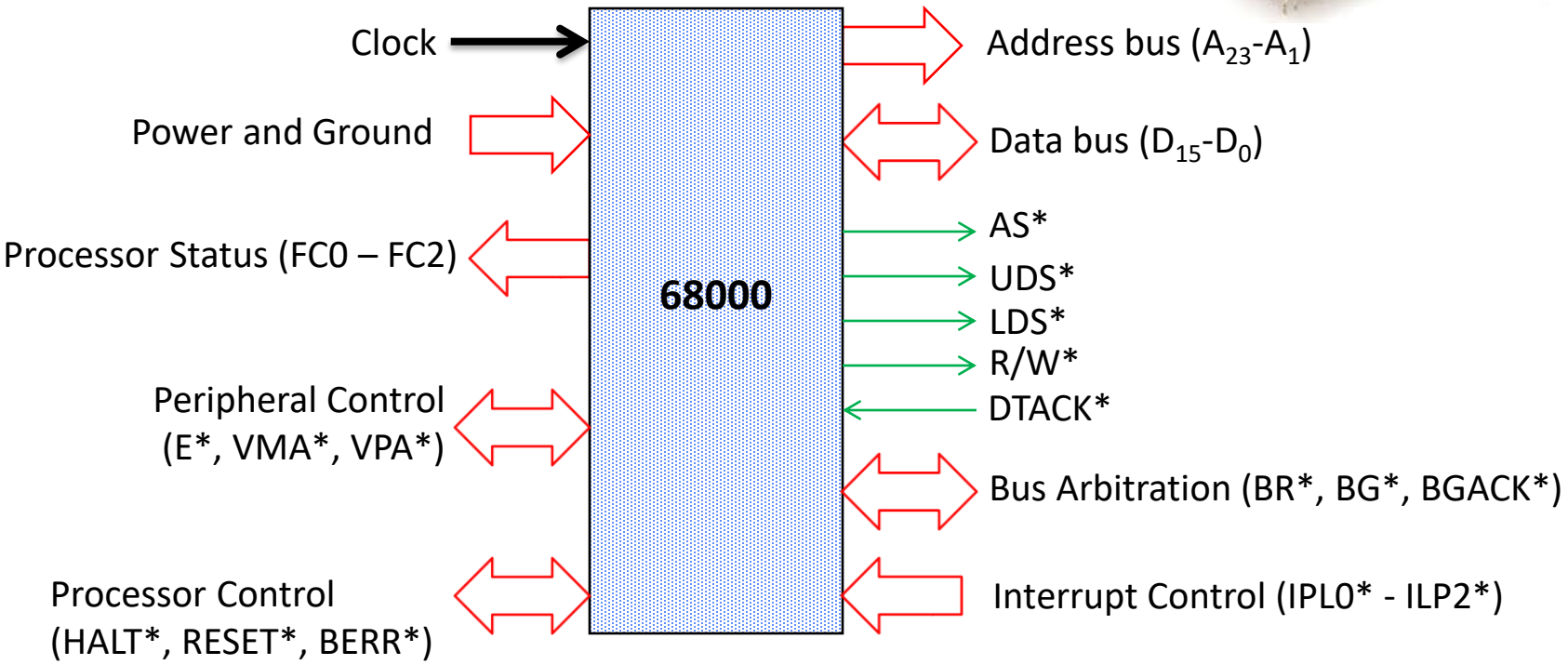
Buses: The Good, the Bad, and the Ugly

- Buses are a shared medium
  - Nice properties
    - Reduces the number of connections in the computer
    - Expansion simple
    - Broadcast, serialization
  - Drawbacks
    - Slow – one transaction at a time
    - Needs a clock that is much slower than the CPU clock
    - Electrically ugly – discontinuities limit operating speed
    - Closed-loop systems



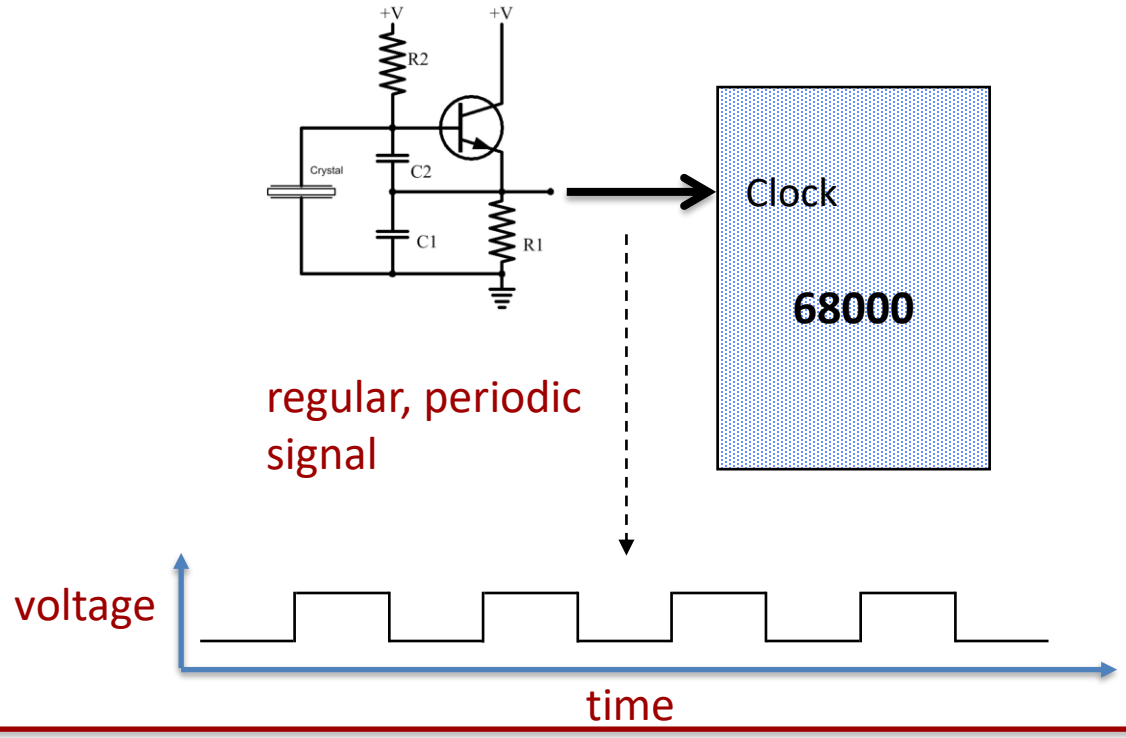
68000 Bus Signals

- The 68000's bus contains a total of 64 signals



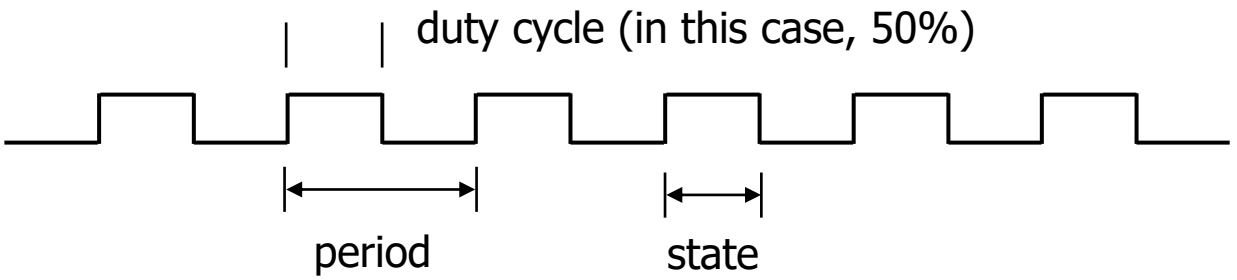
Clock

- External signal used to keep time in synchronous systems, like processors
  - Forces system to make internal decision about current state or hardware configuration; sets base frequency (tempo) in computer



Clock Terminology

- Clocks are regular periodic signals
  - Clock Tick – two reference edges (positive and negative)
  - Clock Period – time between ticks; measured in fractions of seconds; also known as “cycle time”
  - Clock Frequency – the inverse of the clock period; measured in cycles per second or Hertz (Hz)
  - Duty-cycle – time clock is high between ticks; expressed as a % of period
  - State (68000) – ½ clock cycle



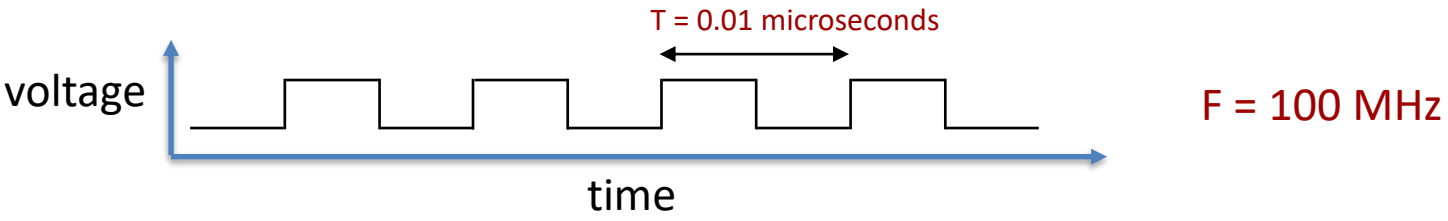
frequency = 1 / period

Problem

- A processor is clocked at a frequency of 3 GHz. What is the period or cycle time of the clock?

Aside – Clock Speed Can Change!

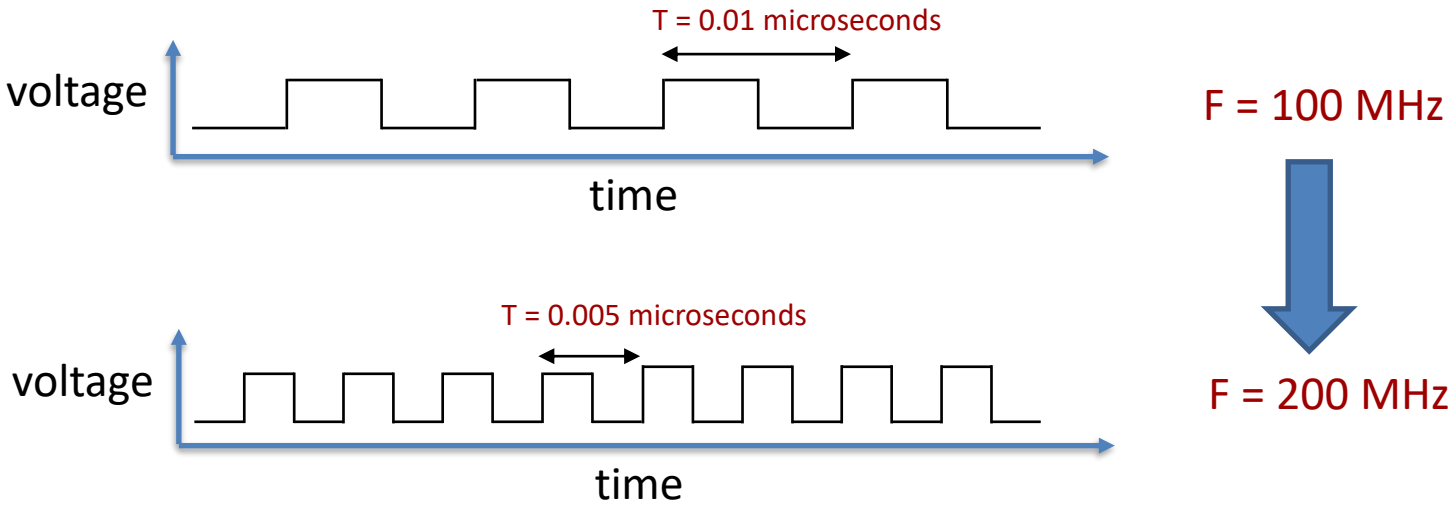
- Base clock frequency of the 68000 system described in your textbook is approximately 3.68 MHz
- Base clock frequency of a typical PC is approximately 100 MHz
  - But clock speed can be throttled up (or down) for more or less performance or power consumption



F = 100 MHz

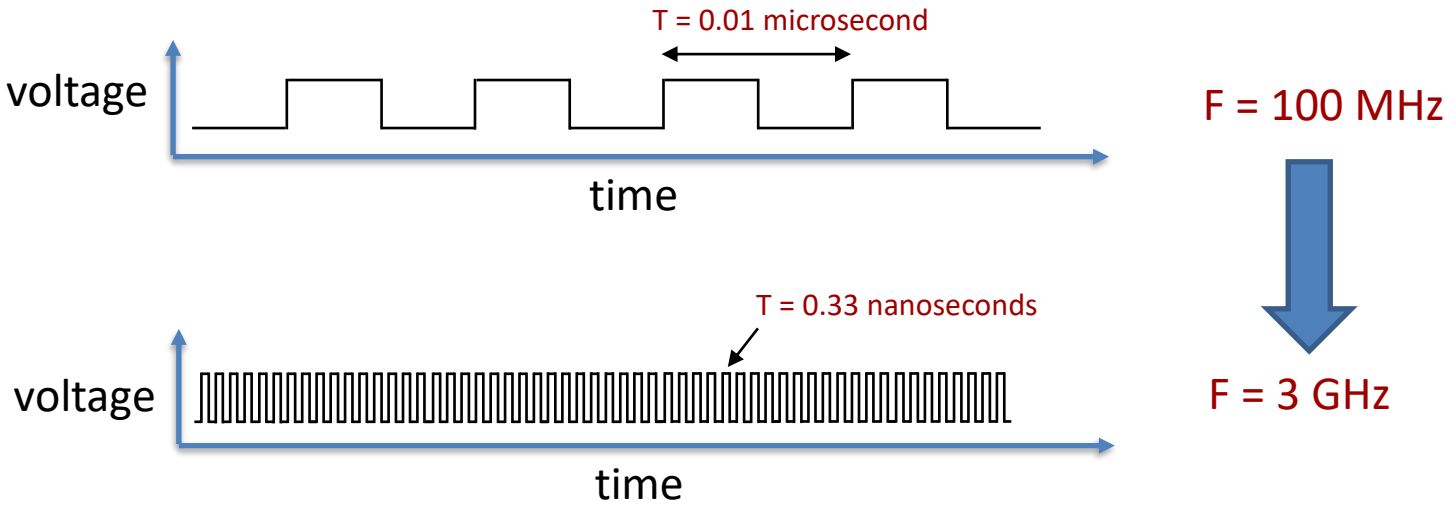
Aside - Clock Speed Can Change!

- Base clock frequency of the 68000 system described in your textbook is approximately 3.68 MHz
- Base clock frequency of a typical PC is approximately 100 MHz
  - But clock speed can be throttled up (or down) for more or less performance or power consumption



Aside - Clock Speed Can Change!

- Base clock frequency of the 68000 system described in your textbook is approximately 3.68 MHz
- Base clock frequency of a typical PC is approximately 100 MHz
  - But clock speed can be throttled up (or down) for more or less performance or power consumption



Common Units for Clock Frequency and Cycle Time

Clock Cycle Time (Clock Period) is typically measured in fractions of a second

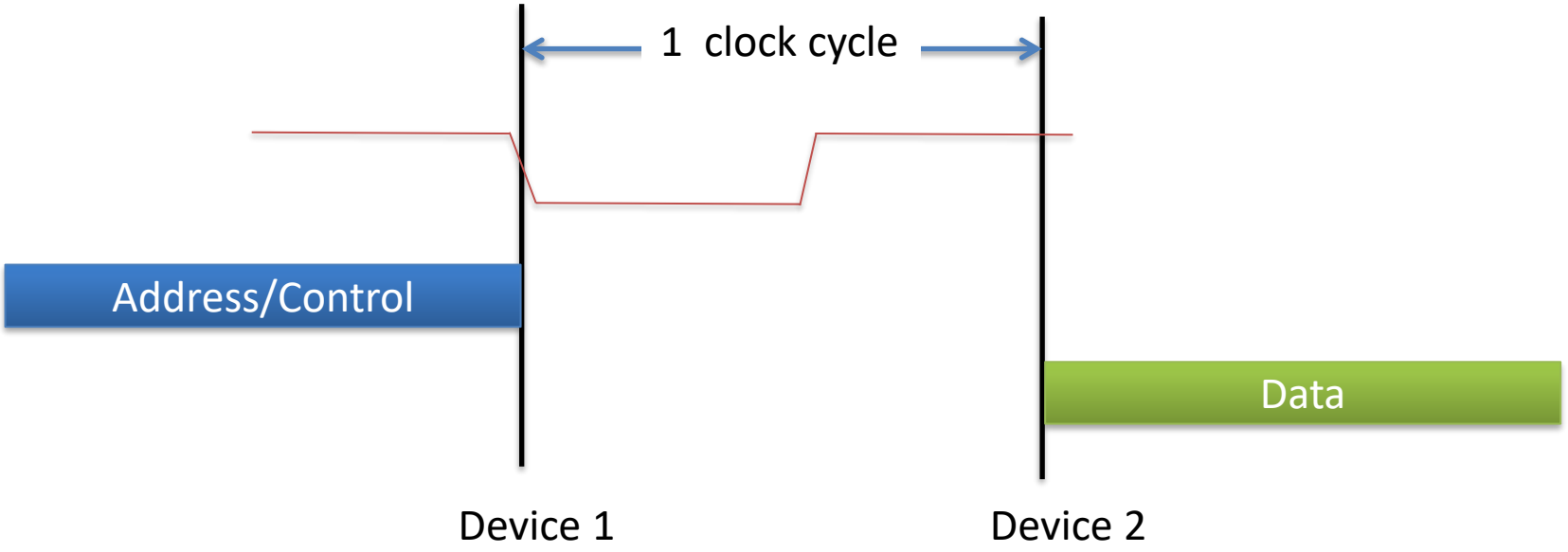
Seconds	Units
0.001s	milliseconds (ms)
0.000 001	microseconds (us)
0.000 000 001	nanoseconds (ns)

Clock frequency is measured in cycles per second (Hertz)

Cycles/Second	Units
1000	Kilohertz (KHz)
1 000 000	Megahertz (MHz)
1 000 000 000	Gigahertz (GHz)

Synchronous Bus

- Synchronous Bus
  - Includes a clock in control lines
  - Fixed protocol for communication relative to the clock



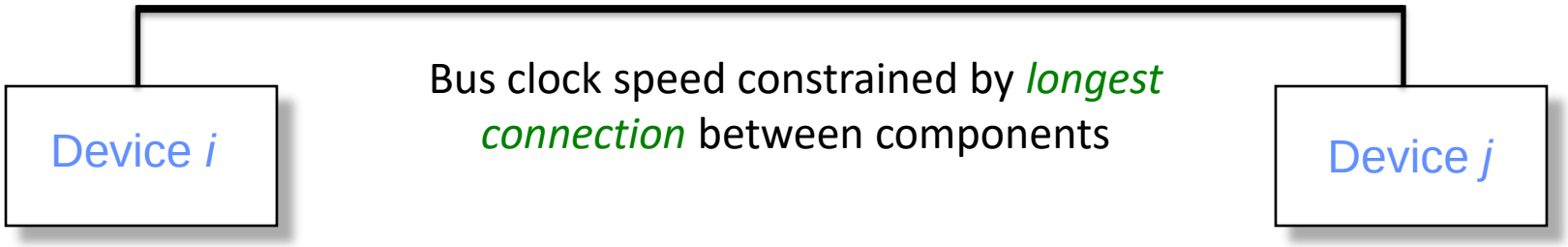
Synchronous Bus

- Synchronous Bus
  - Includes a clock in control lines
  - Fixed protocol for communication relative to the clock
  - Advantages
    - Involves very little logic to implement
  - Disadvantages
    - Every transfer on the bus must run at the same clock rate
    - Bus cannot be long if it is fast

Maximum Length of Bus

- Any signal put on the bus has to travel between any two components that share the bus in any single (Bus) clock cycle
  - Assumptions
    - Light travels at 3×10^8 m/s
    - Bus clock frequency = 3×10^9 cycles/second (Gigahertz)

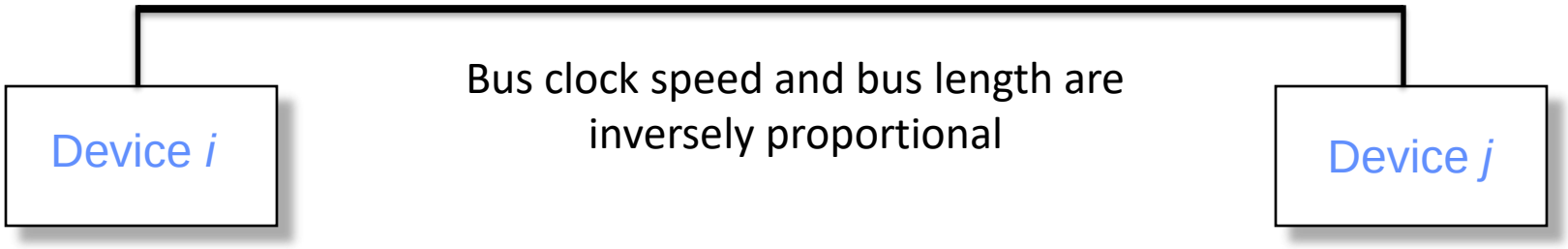
$$\text{distance}_{ij} = \frac{3 \times 10^8 \text{ meters / second}}{3 \times 10^9 \text{ cycles / second}} = 0.1 \text{ meters / cycle}$$



Maximum Length of Bus

- Any signal put on the bus has to travel between any two components that share the bus in any single (Bus) clock cycle
  - Assumptions
    - Light travels at 3×10^8 m/s
    - Bus clock frequency = 33×10^6 cycles/second (Megahertz)

$$\text{distance}_{ij} = \frac{3 \times 10^8 \text{ meters / second}}{33 \times 10^6 \text{ cycles / second}} = 9.1 \text{ meters / cycle}$$



Asynchronous Buses

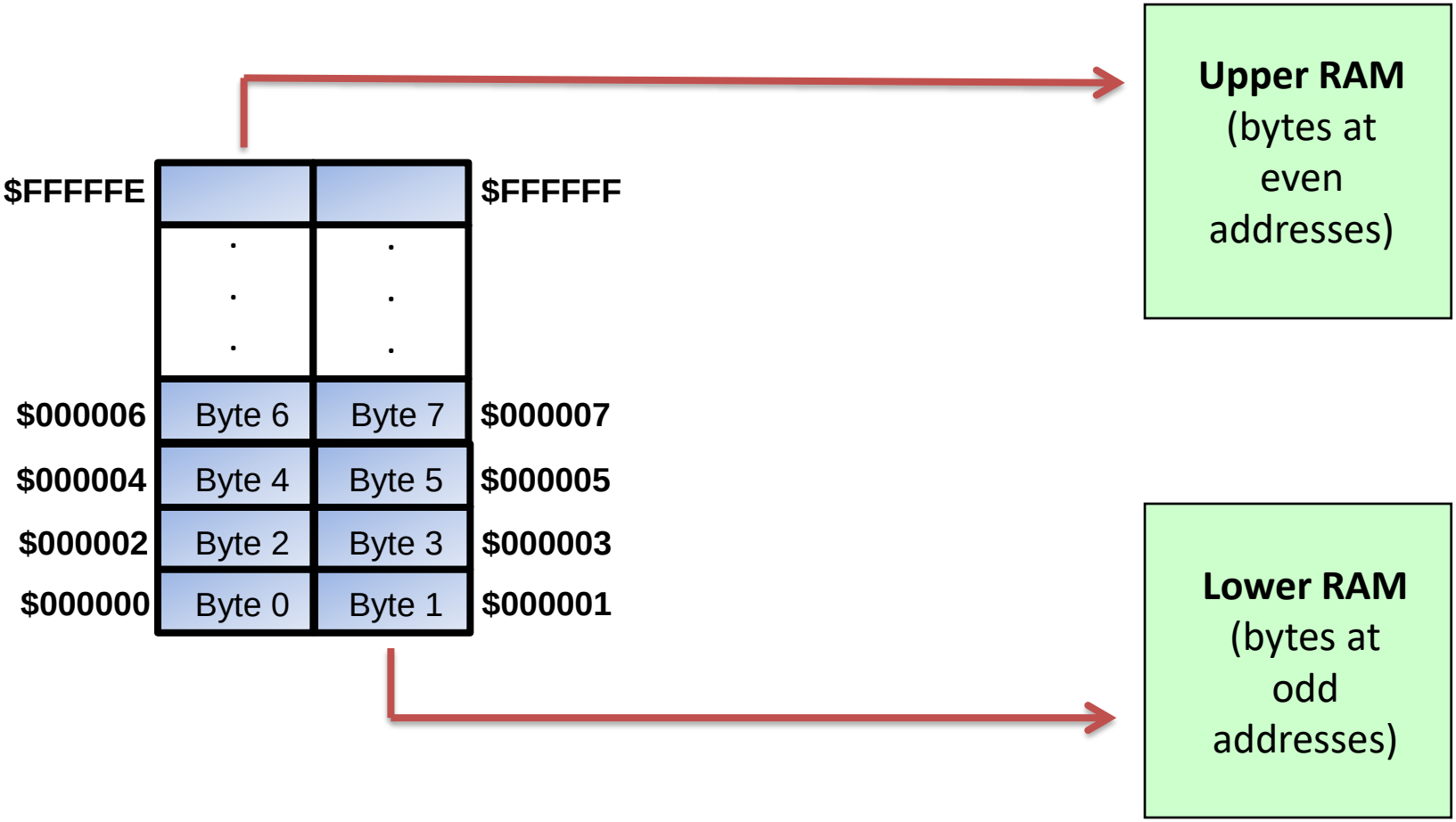
- Asynchronous Bus
  - No clock control line
    - Requires handshaking
  - Advantages
    - Can easily accommodate a wide range of devices that operate at different speeds
    - No clock skew problems, so bus can be quite long
  - Disadvantages
    - Potentially slower than synchronous buses, but…

Asynchronous Bus Control on the 68000

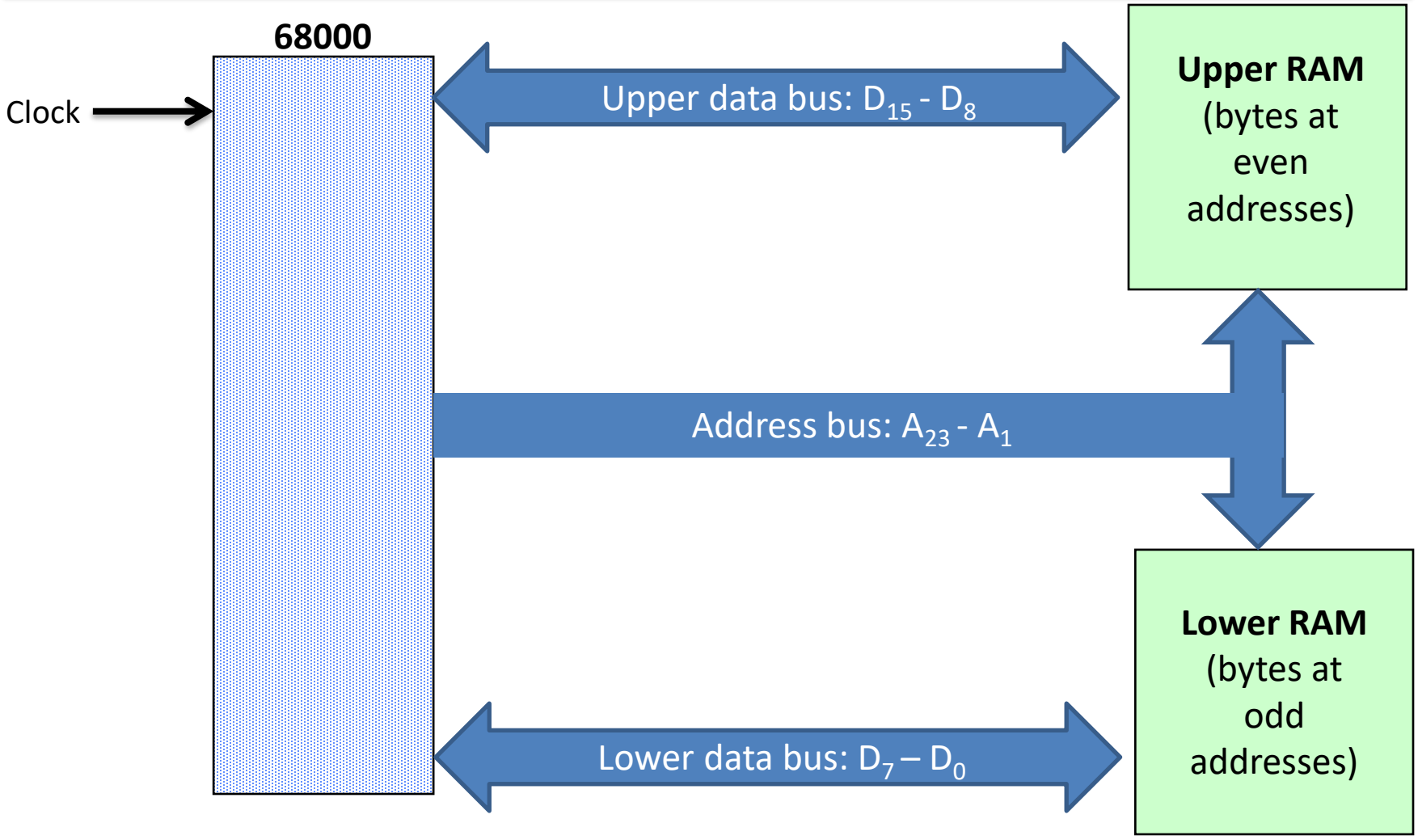
Signal	Active	Purpose	Direction
Address Strobe (AS)*	Low	Indicates a valid address exists on the address bus	Output signal
Read/Write (R/W*)	Read=high Write = low	Determines whether a read or write operation is to be performed	Output signal
Upper Data Strobe (UDS*)	Low	Controls transfer of byte (at even address) over upper byte of data bus	Output signal
Lower Data Strobe (LDS*)	Low	Controls transfer of byte (at odd address) over lower byte of data bus	Output signal
Data Acknowledgement (DTACK*)	Low	Informs processor that data transfer has completed	Input signal

* means active low

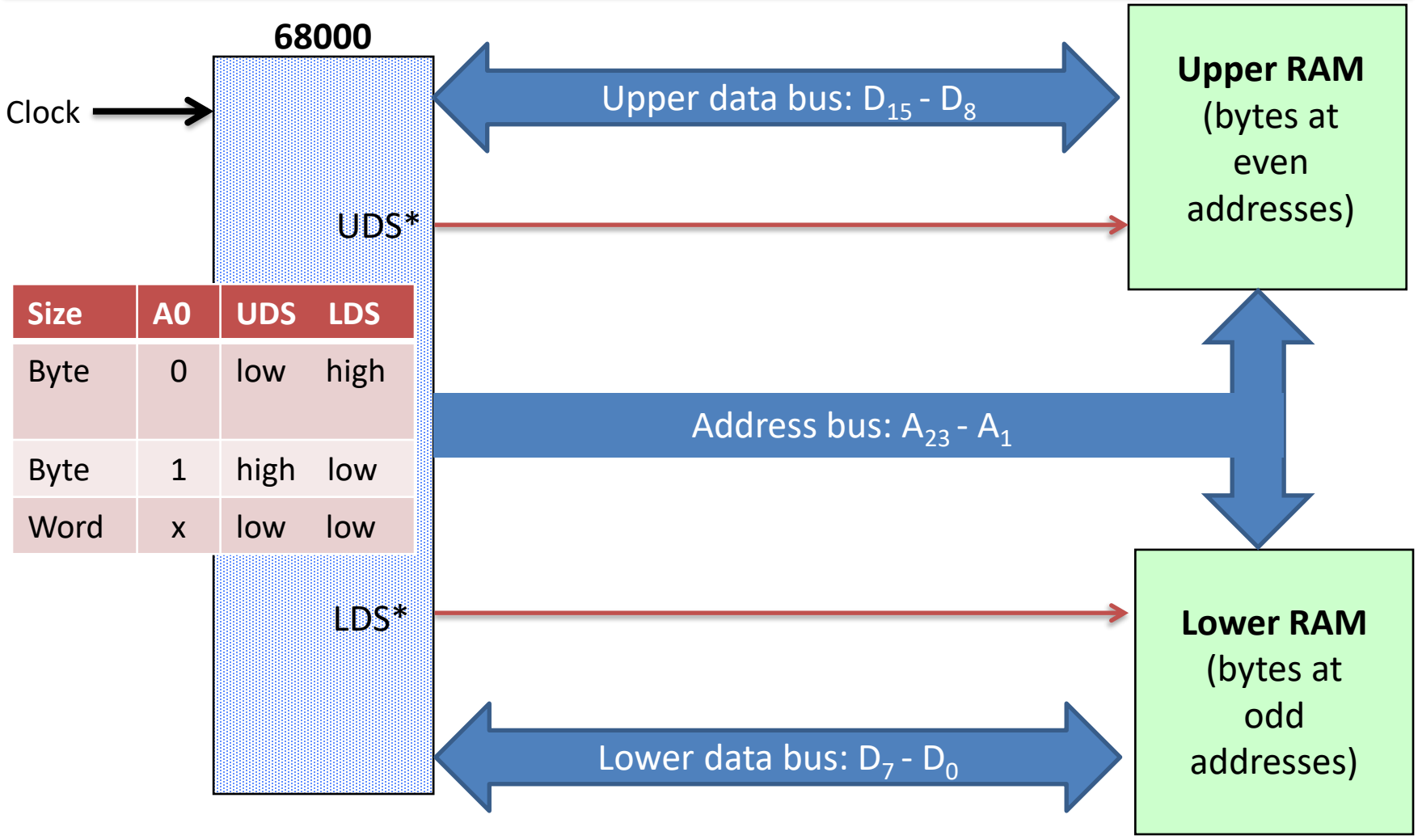
Dual Memories



Upper and Lower RAMs/Data Buses

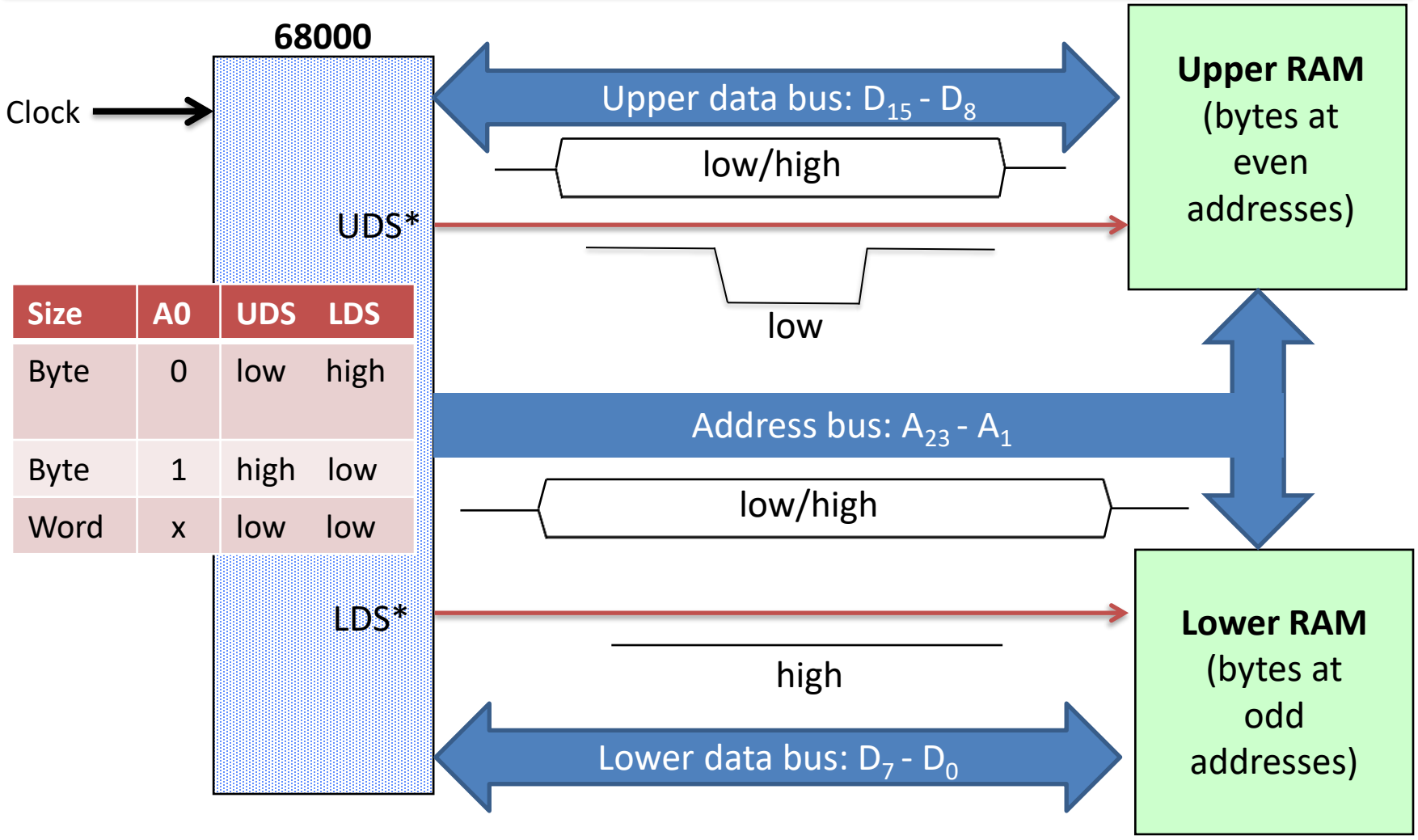


Upper and Lower RAMs and UDS and LDS



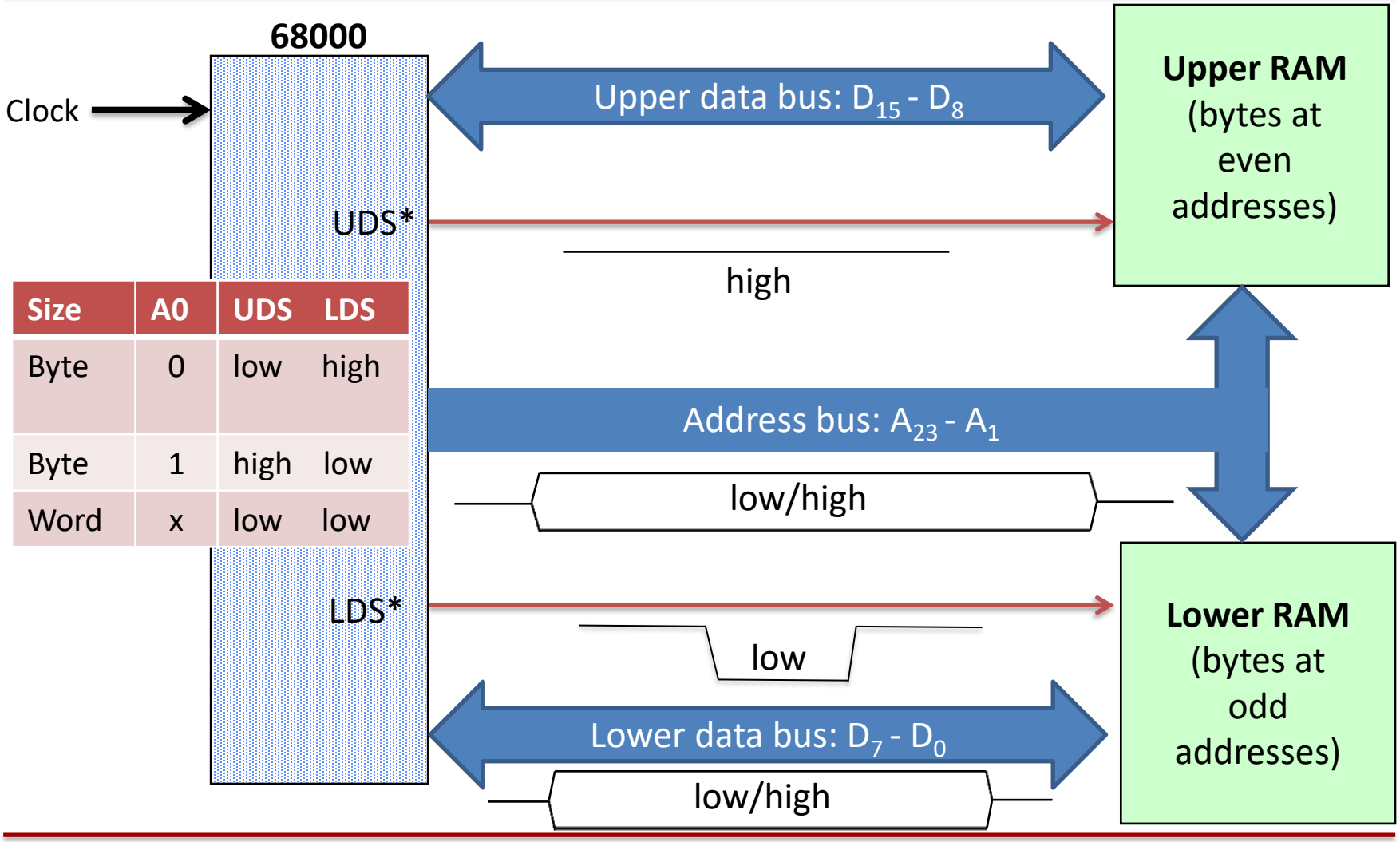
Size	A0	UDS	LDS
Byte	0	low	high
Byte	1	high	low
Word	x	low	low

MOVE.B $008000,D0



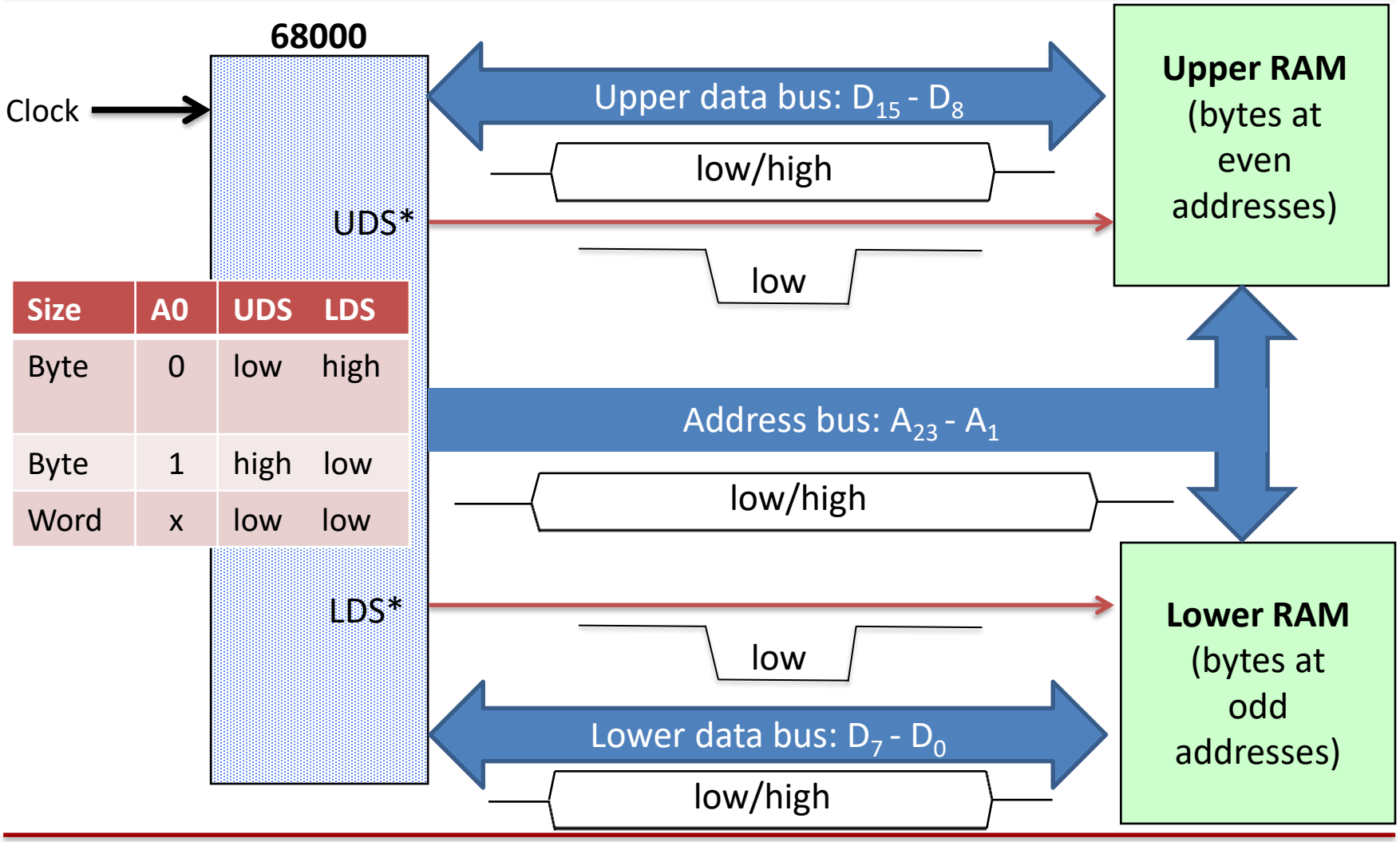
Size	A0	UDS	LDS
Byte	0	low	high
Byte	1	high	low
Word	x	low	low

MOVE.B $008001,D0



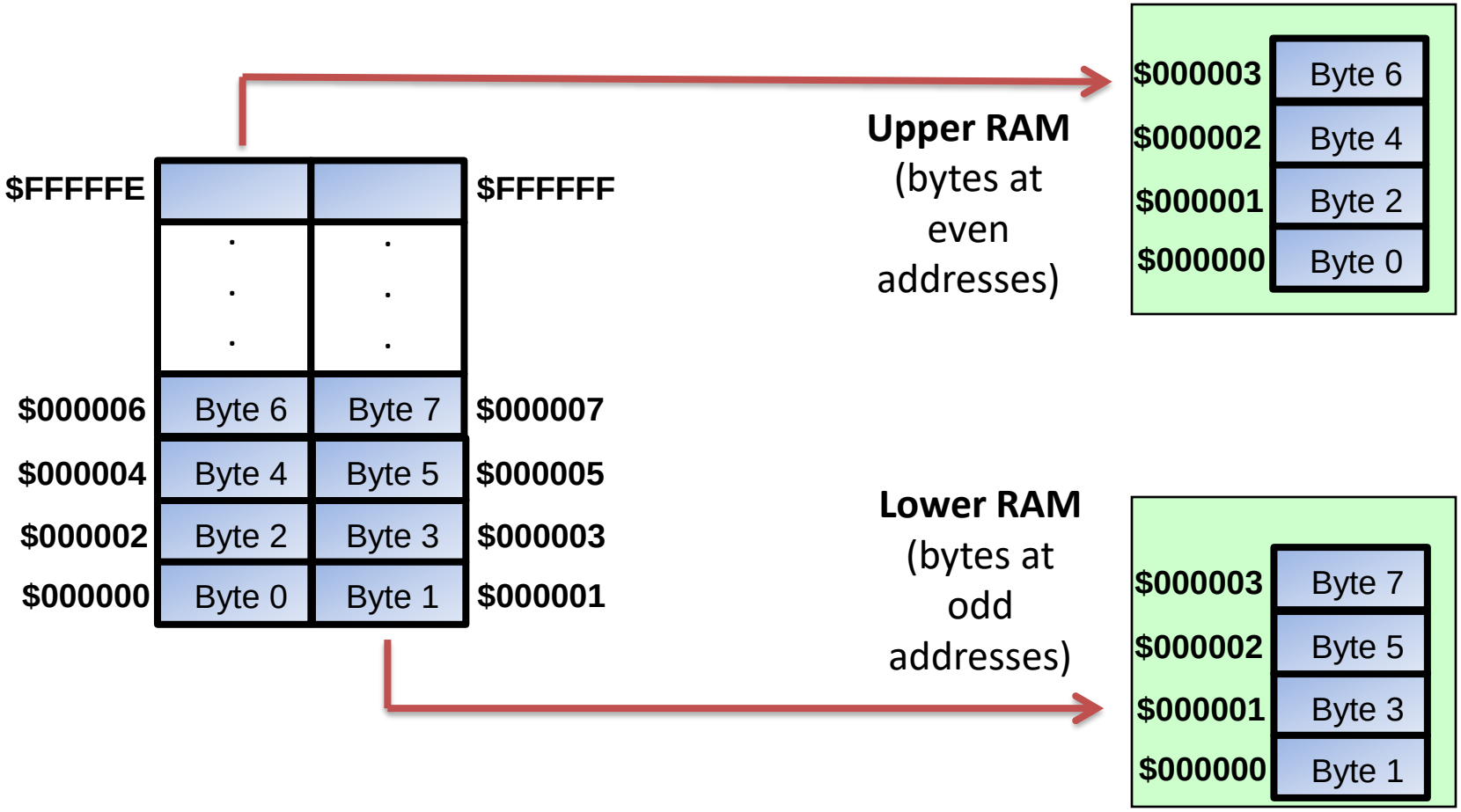
Size	A0	UDS	LDS
Byte	0	low	high
Byte	1	high	low
Word	x	low	low

MOVE.W $008000,D0



Size	A0	UDS	LDS
Byte	0	low	high
Byte	1	high	low
Word	x	low	low

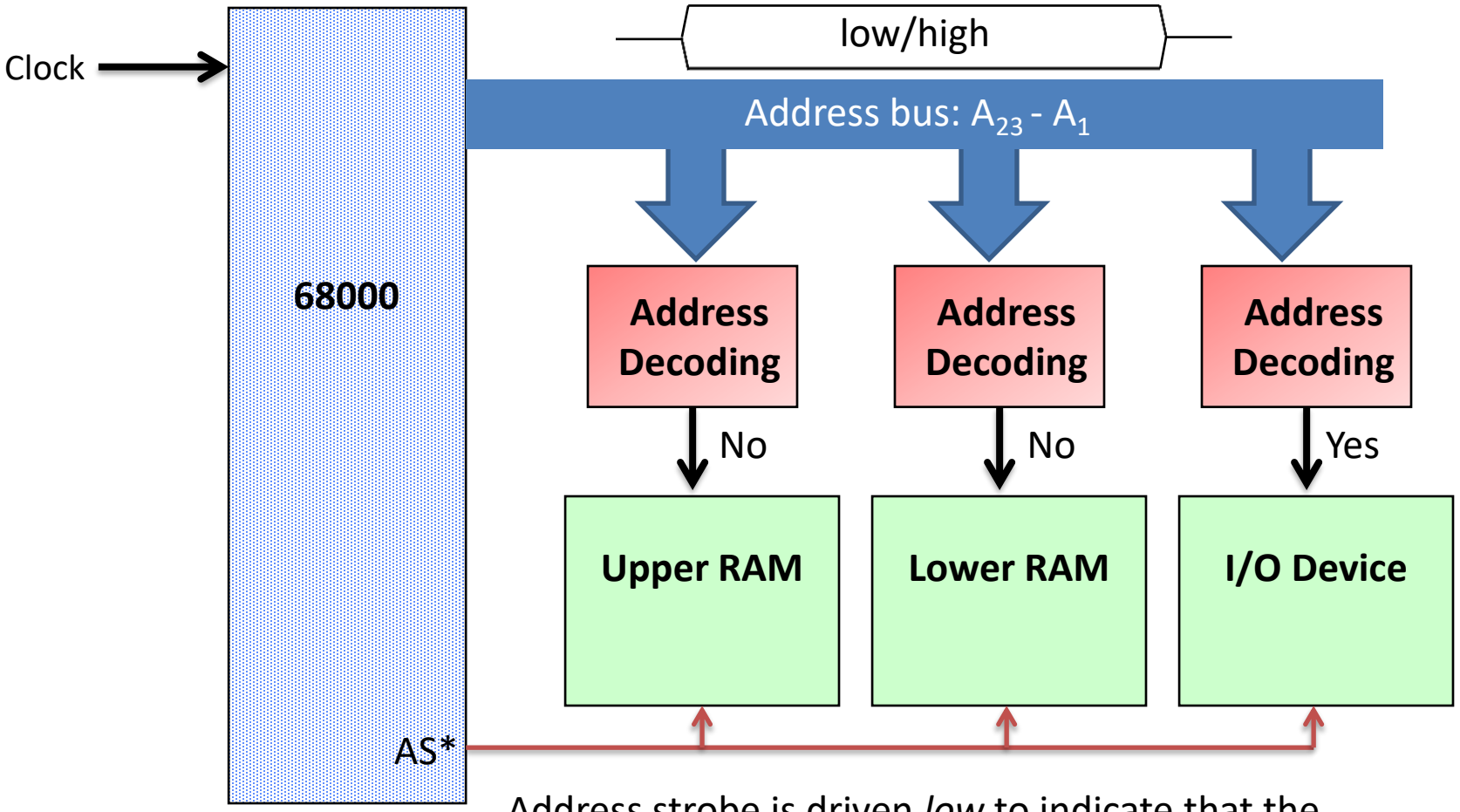
Words/Longwords Must be at Even Addresses



Problem

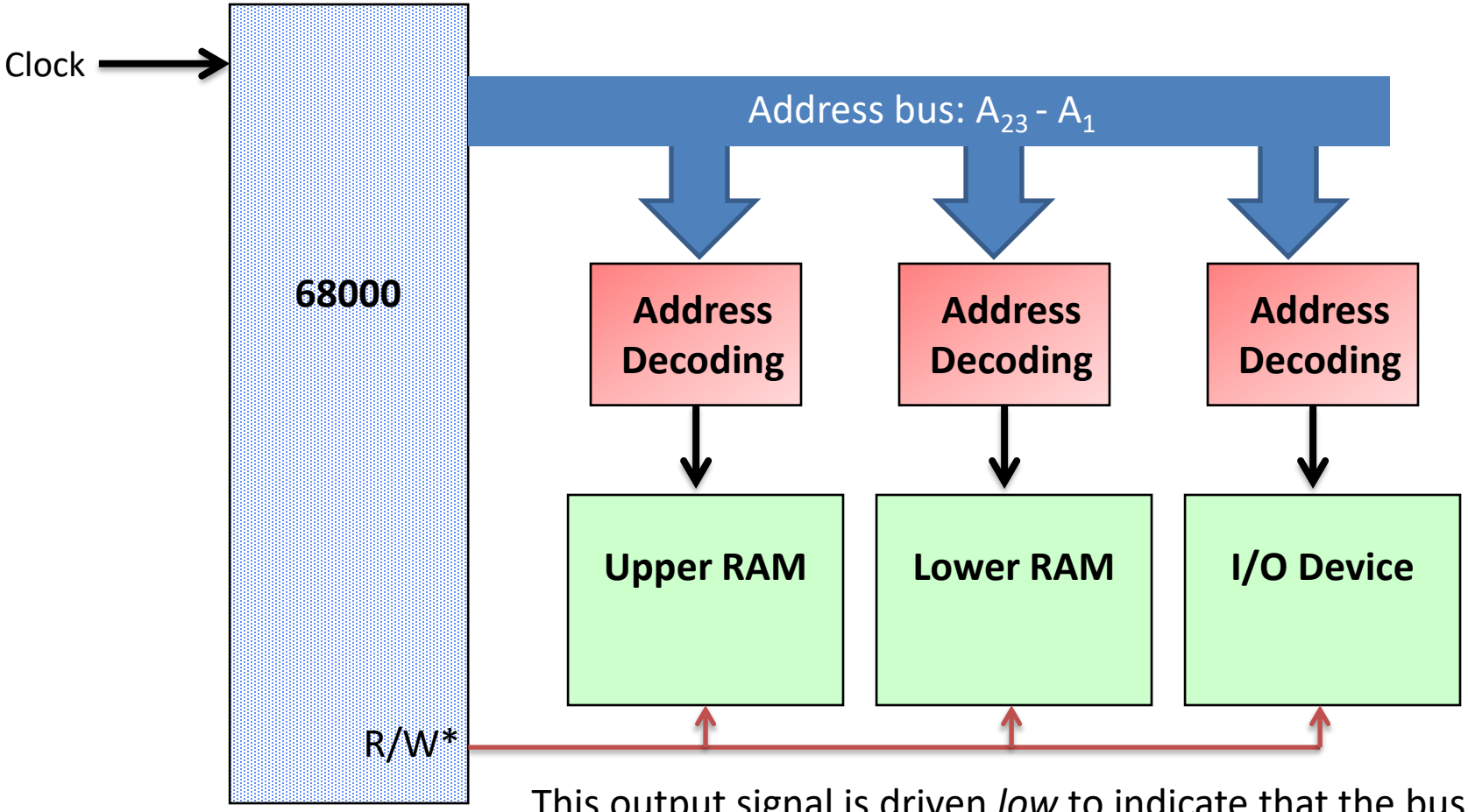
- Indicate the states (low or high) of UDS* and LDS* when the processor is involved in the following memory accesses:
  - A byte written to address 3000
  - A byte written to address 3001
  - A word written to address 3000

Address Strobe



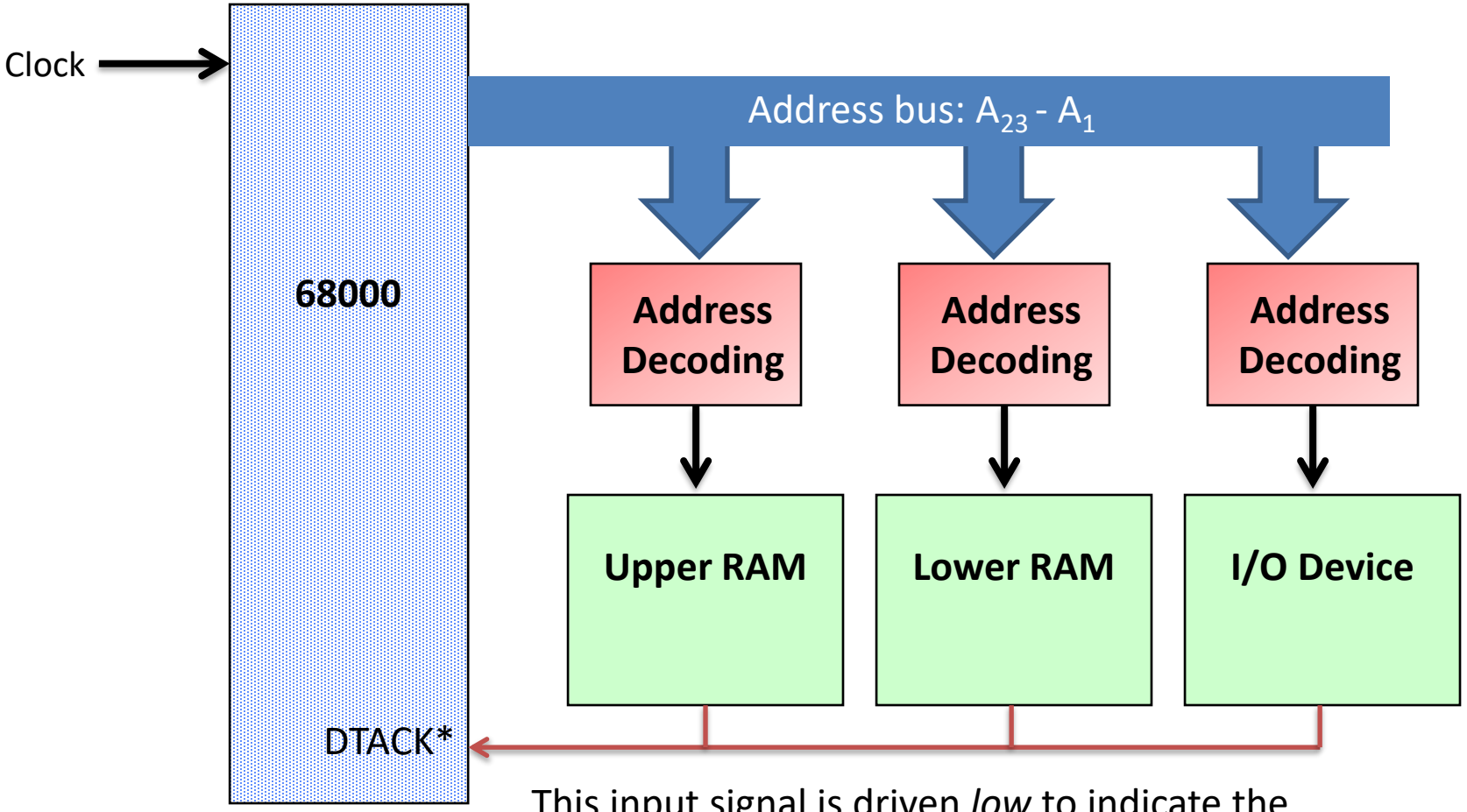
Address strobe is driven *low* to indicate that the address on the address bus is valid

Reading and Writing



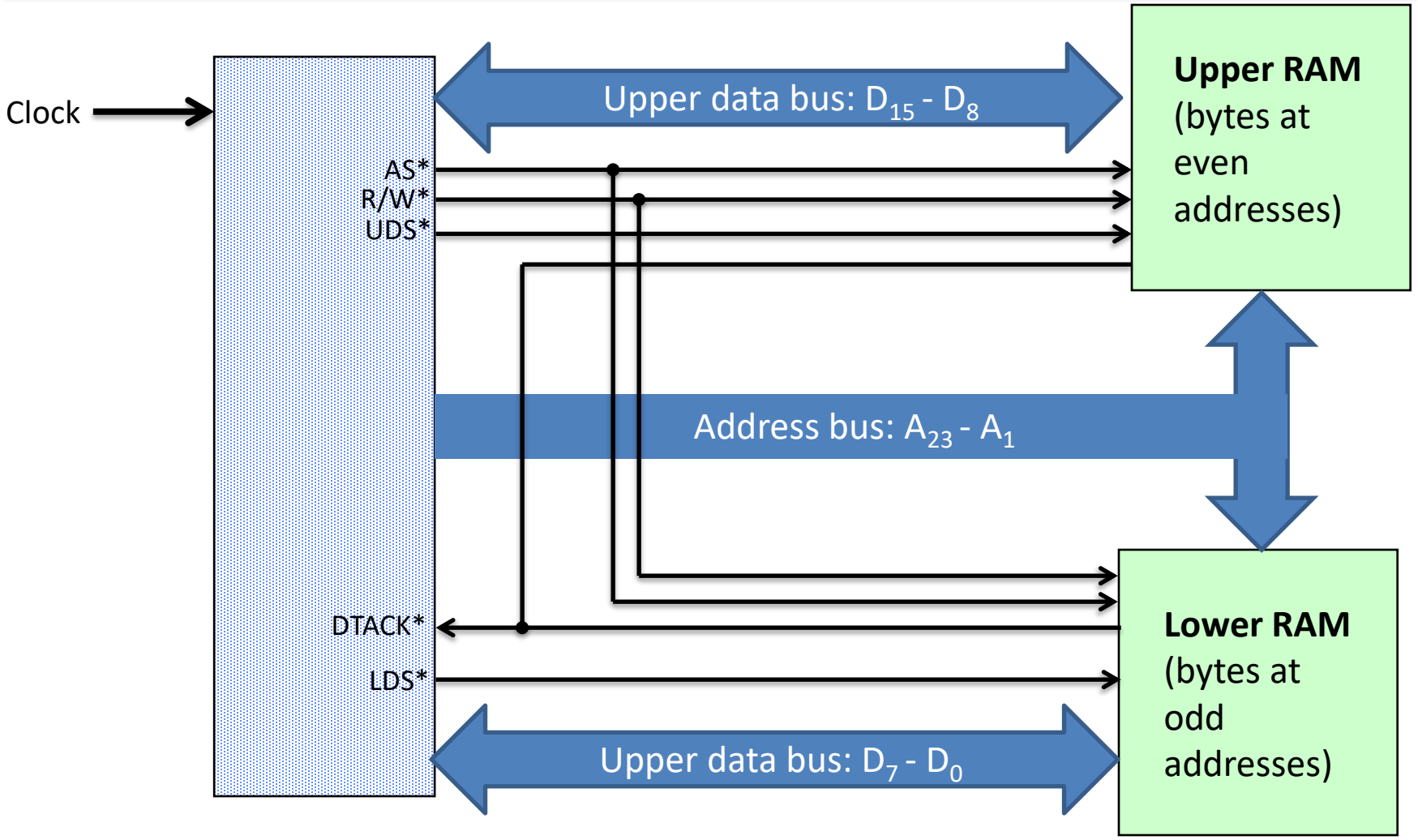
This output signal is driven *low* to indicate that the bus transfer is a write, and *high* to indicate that it is a read

Data Transfer Acknowledge



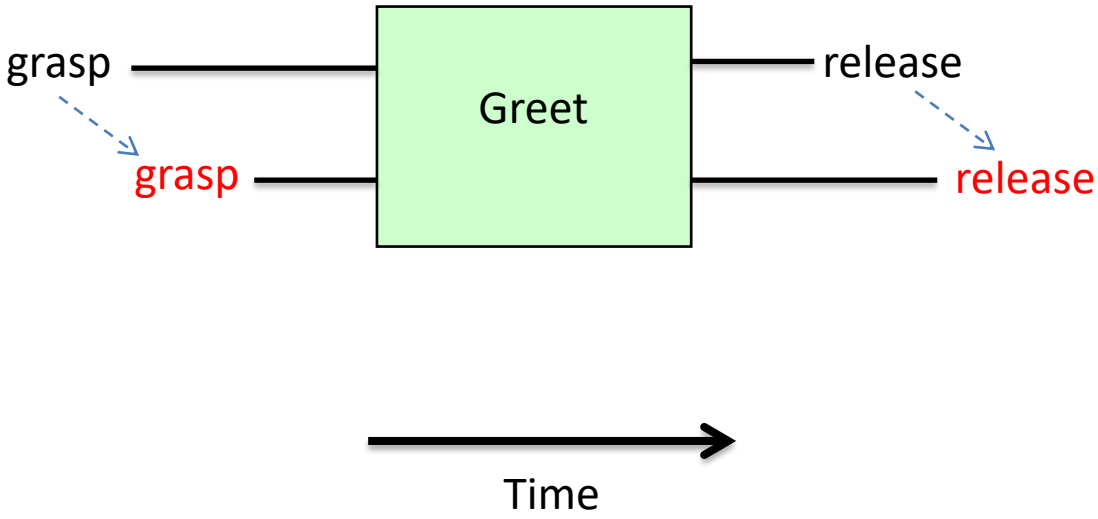
This input signal is driven *low* to indicate the completion of a data transfer

Processor/Memory Interface

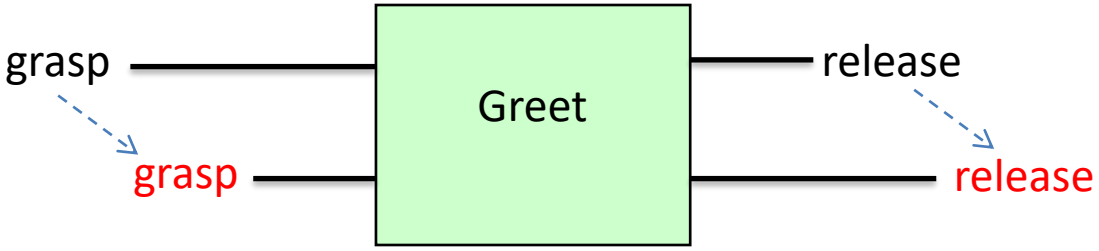


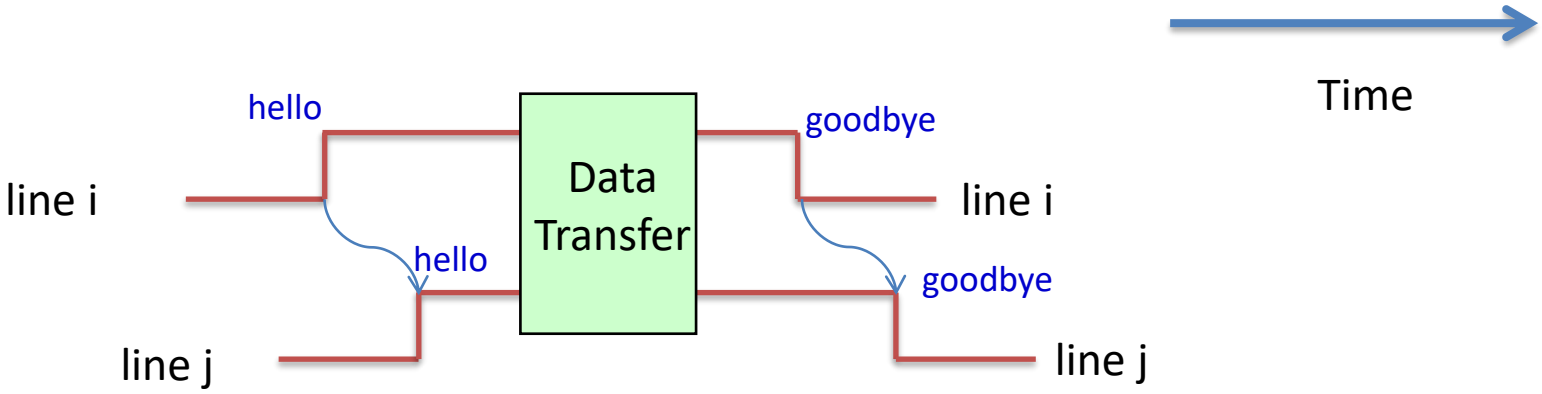
Handshaking

- Communication requires a protocol to structure and synchronize communication
  - Connection: start and stop communication
  - Data Transfer

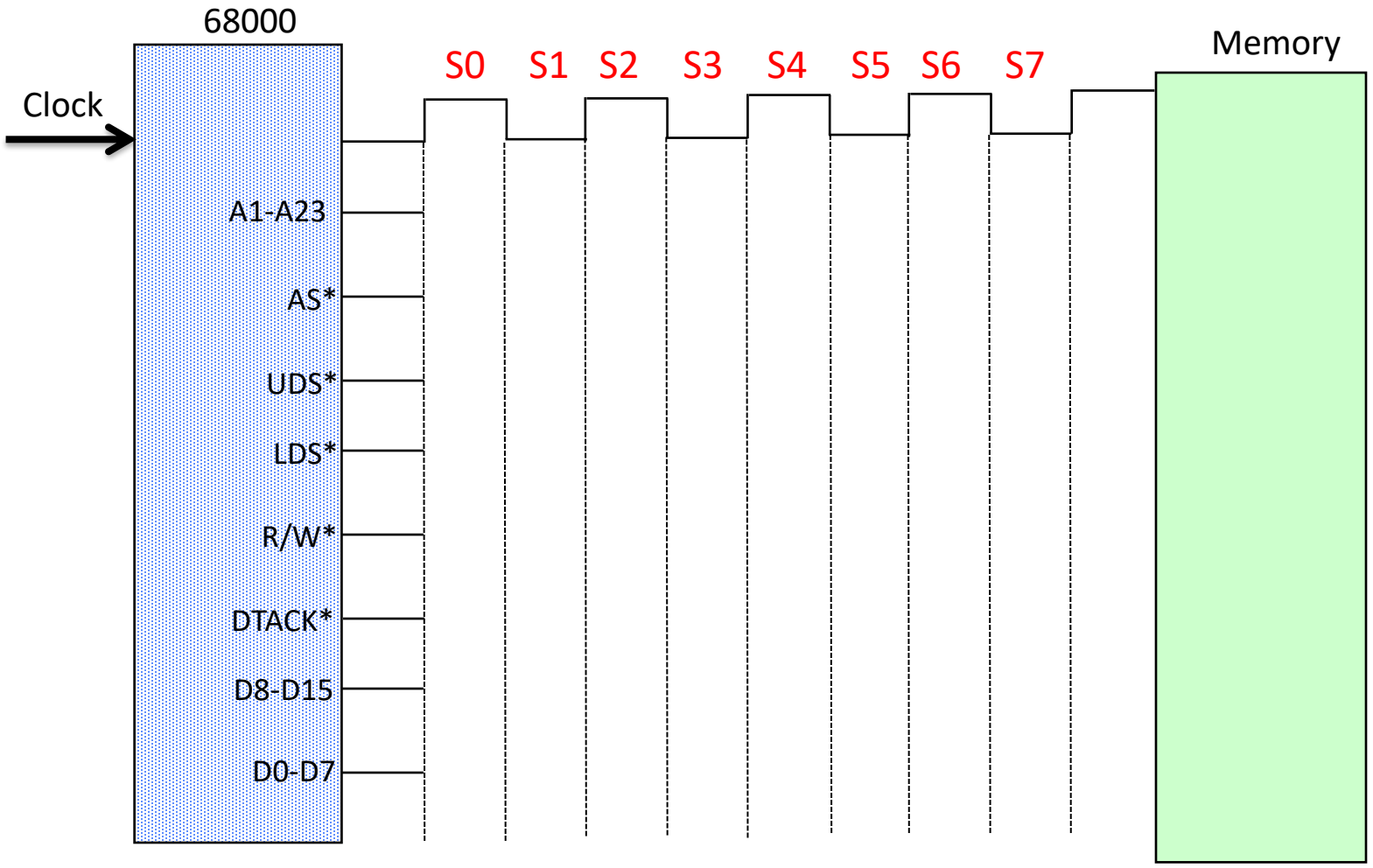


Handshaking with Hardware Devices

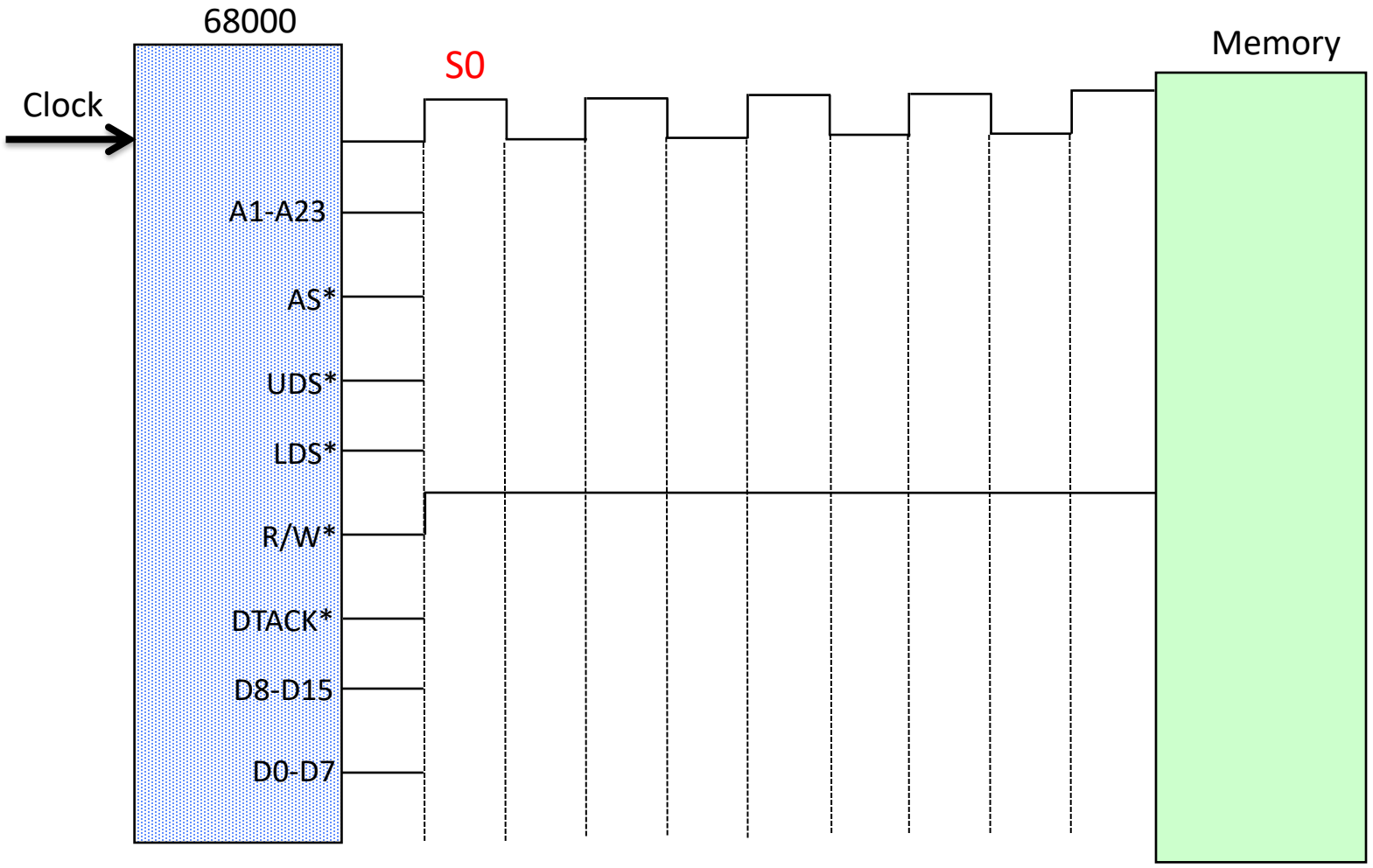




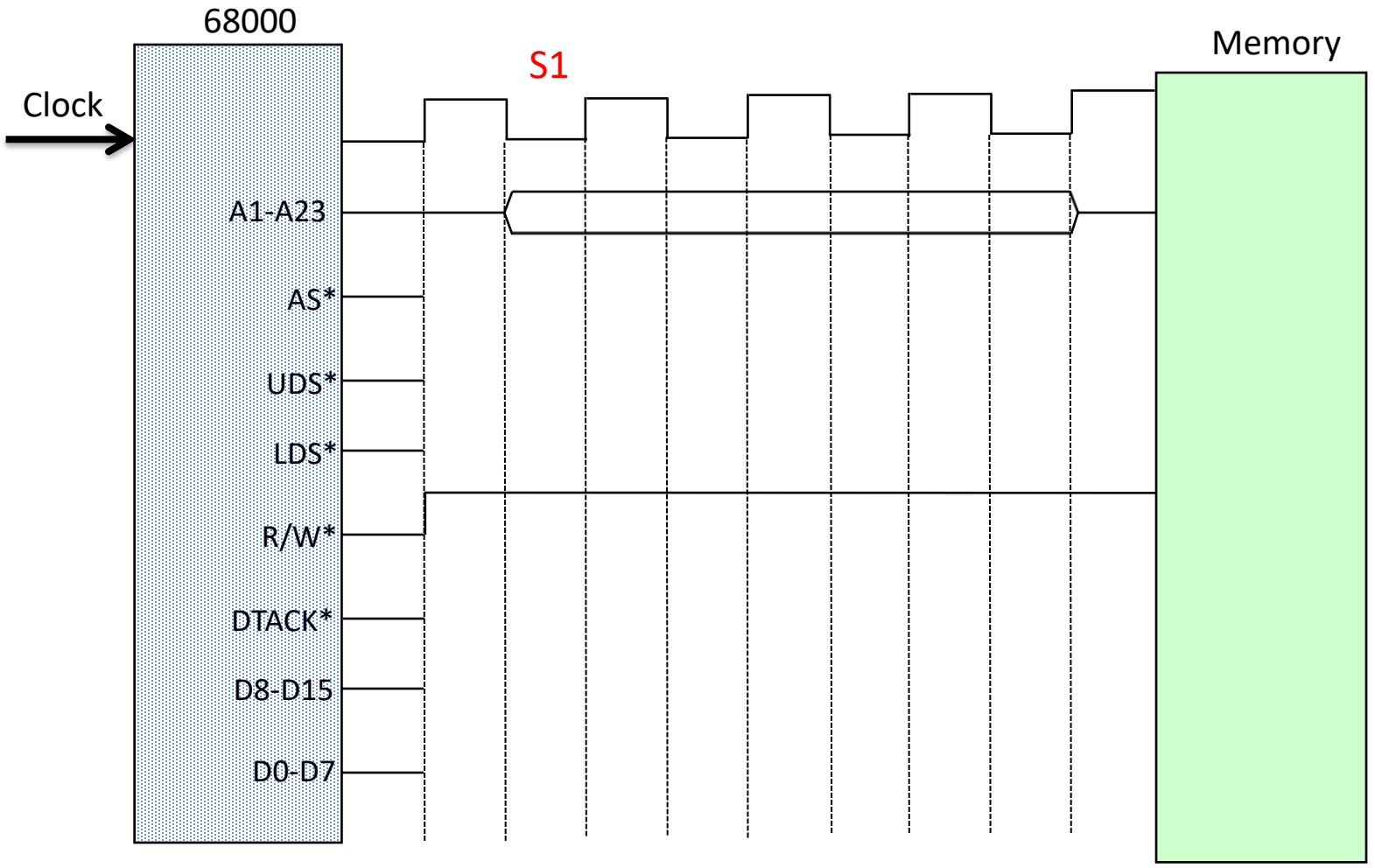
Read Cycle for a Word



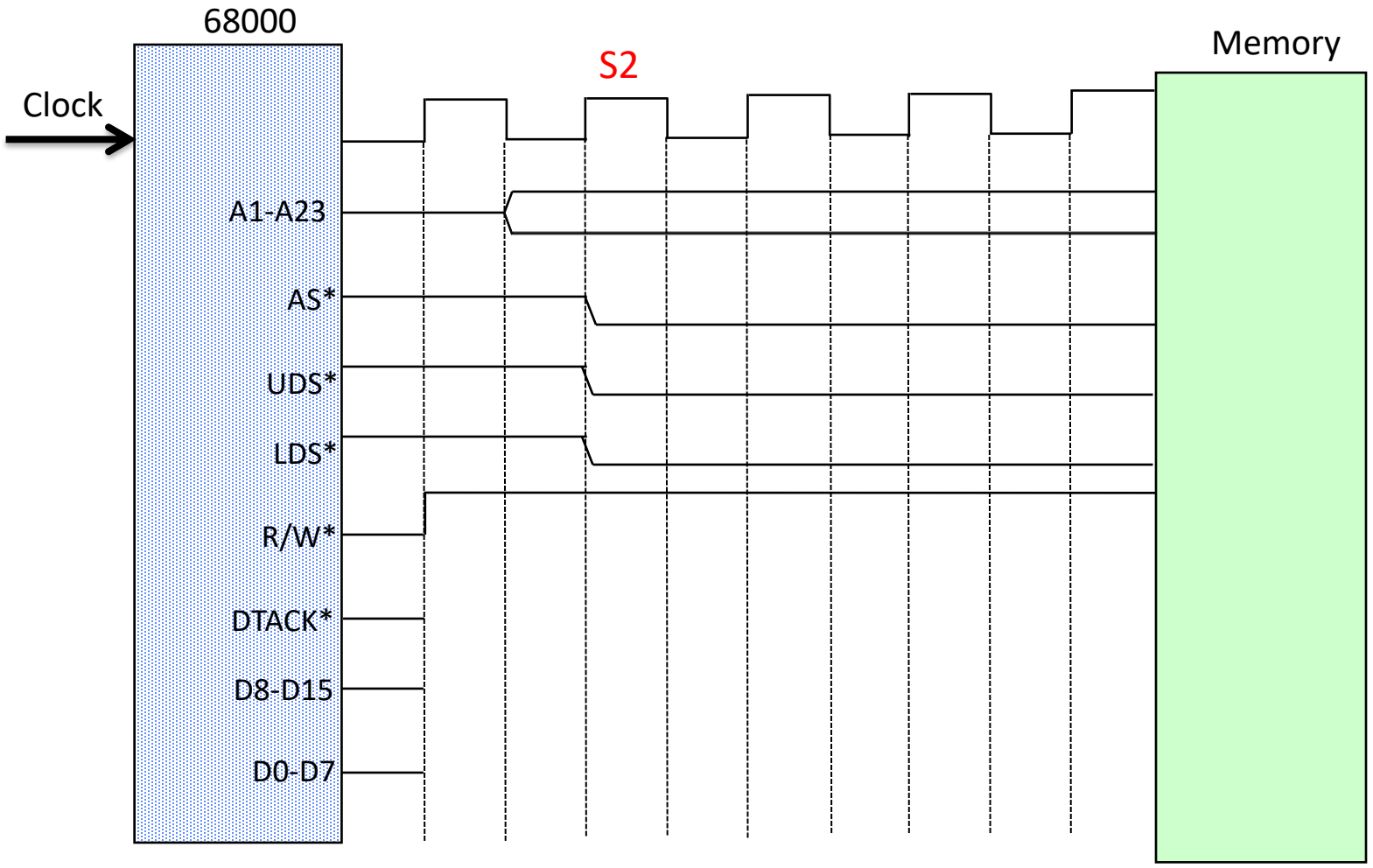
Read Cycle for a Word



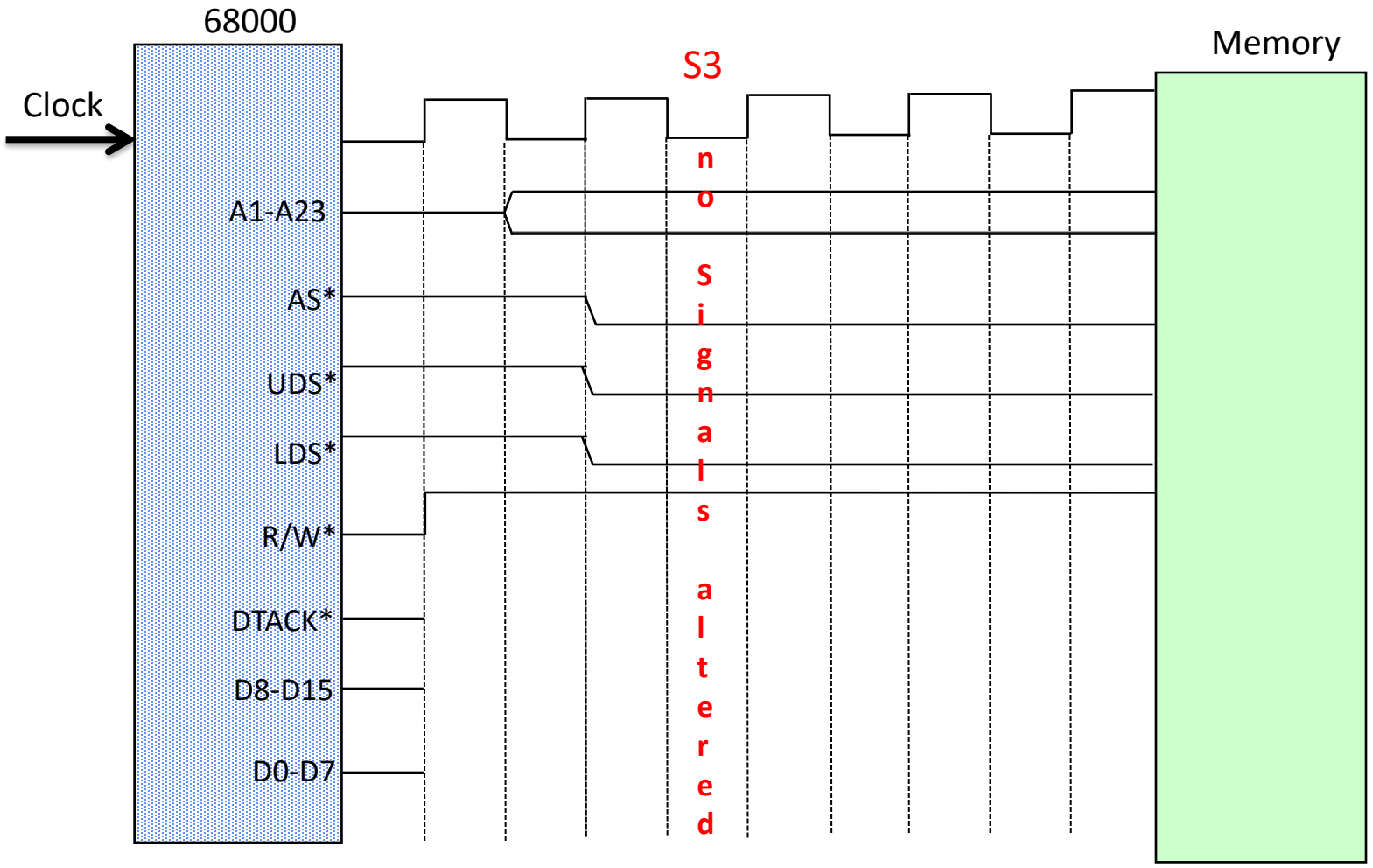
Read Cycle for a Word



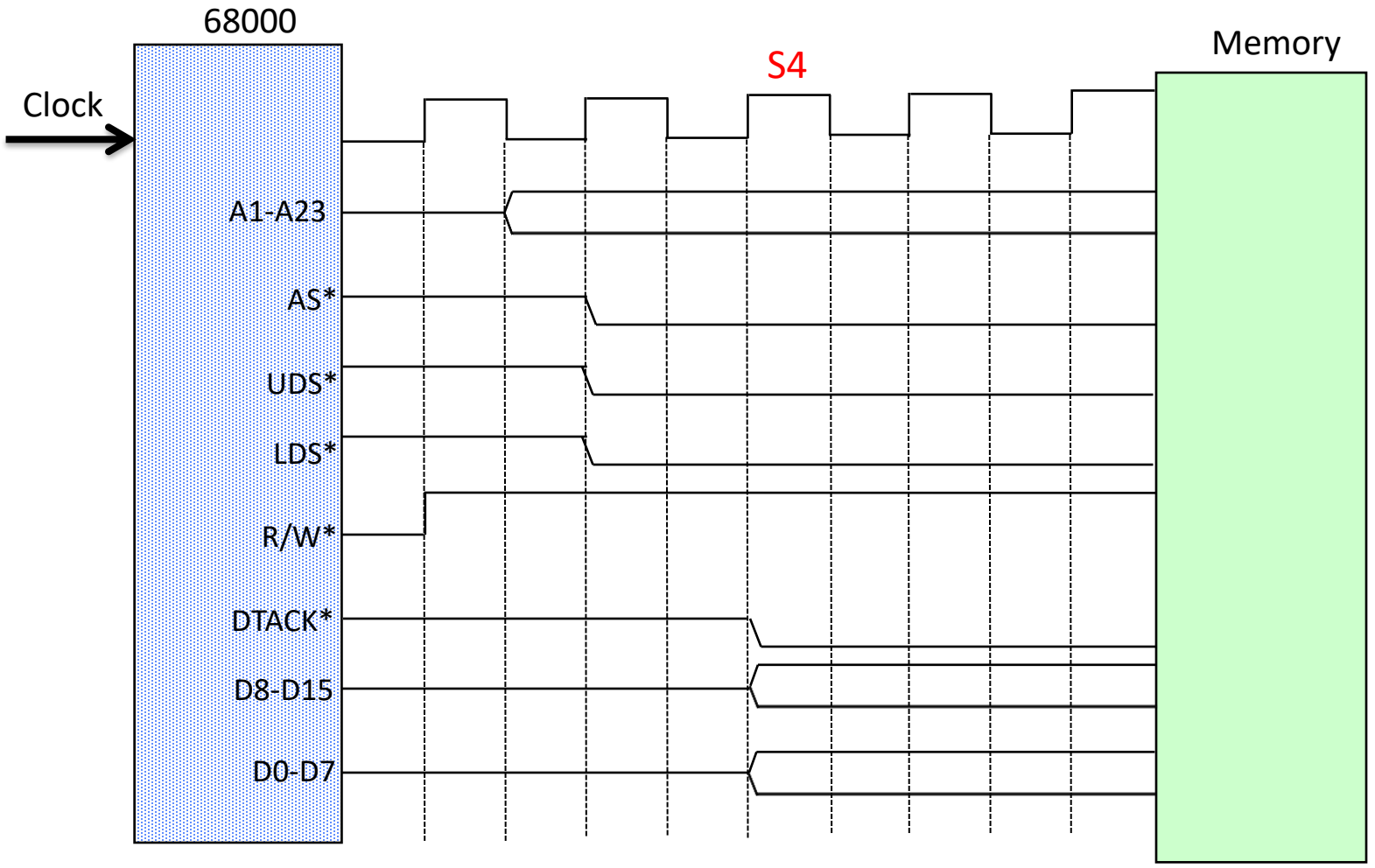
Read Cycle for a Word



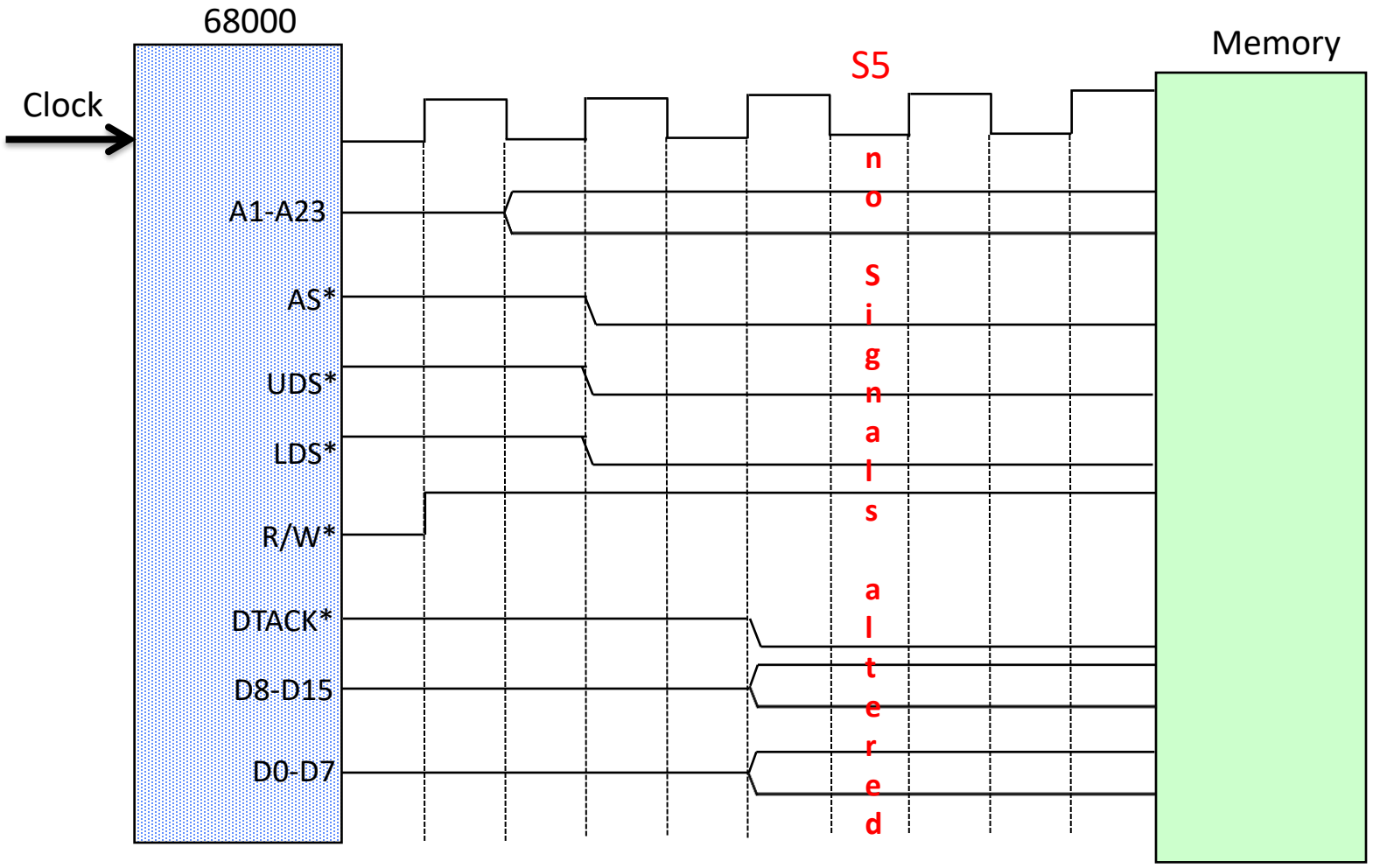
Read Cycle for a Word



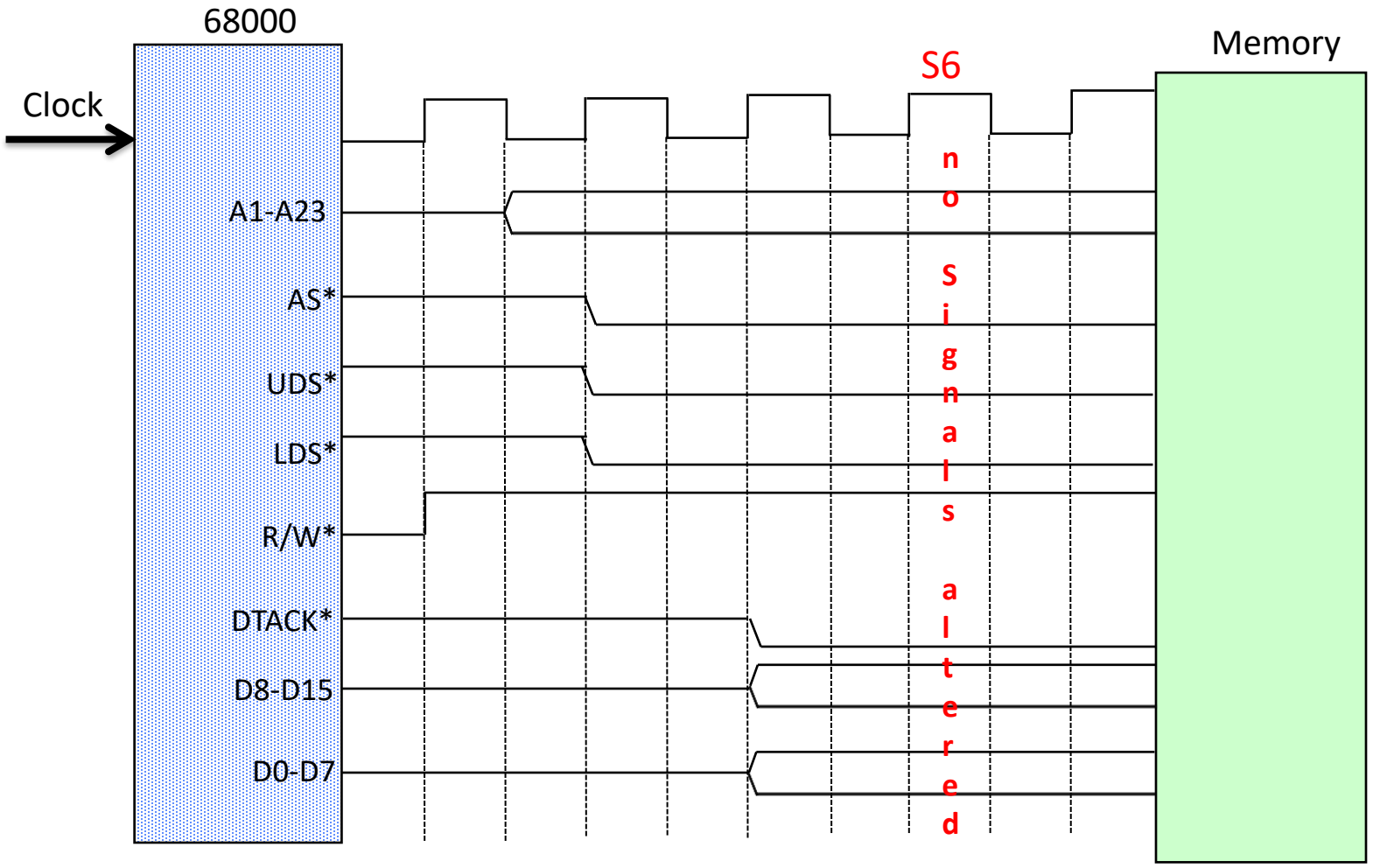
Read Cycle for a Word



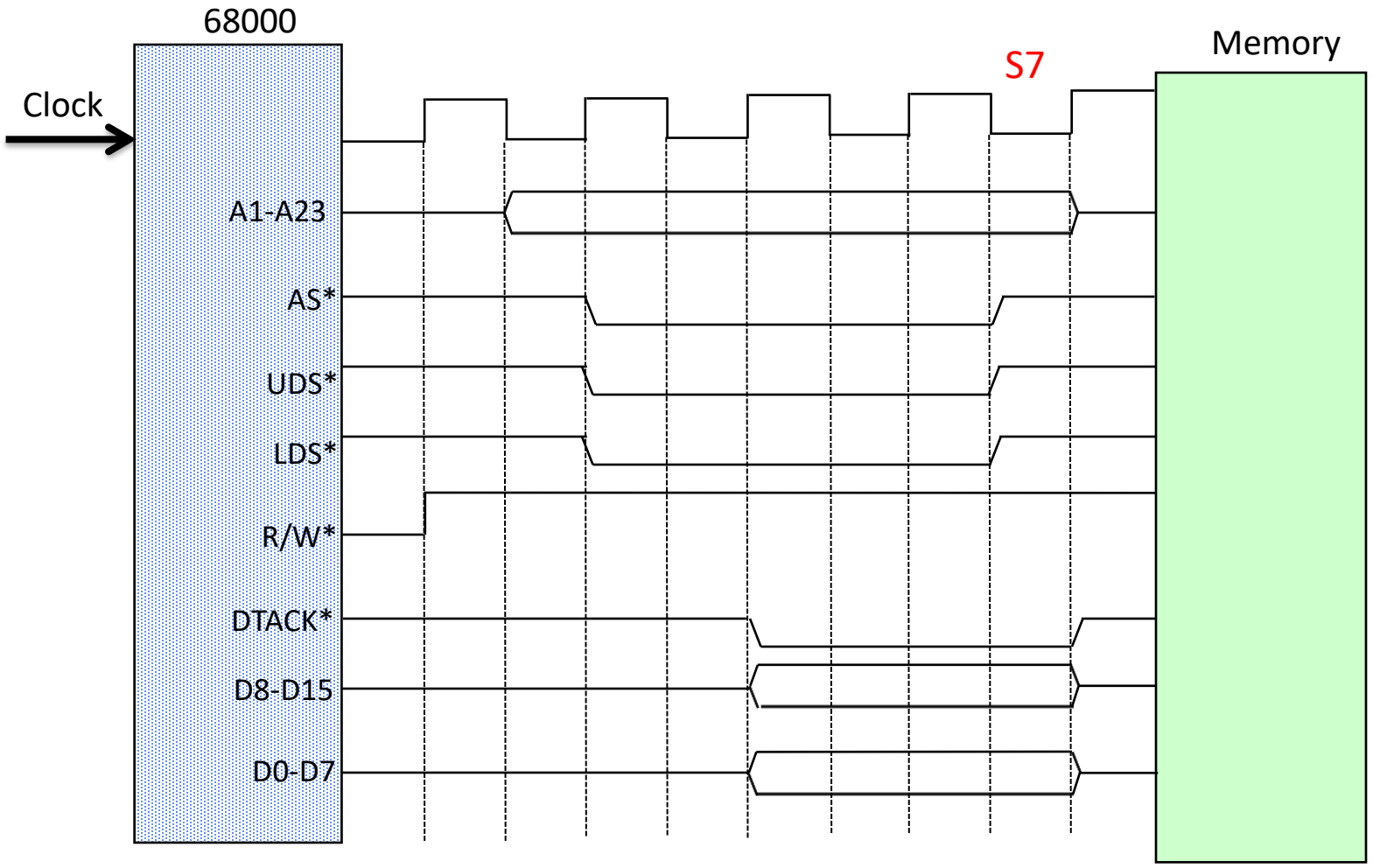
Read Cycle for a Word



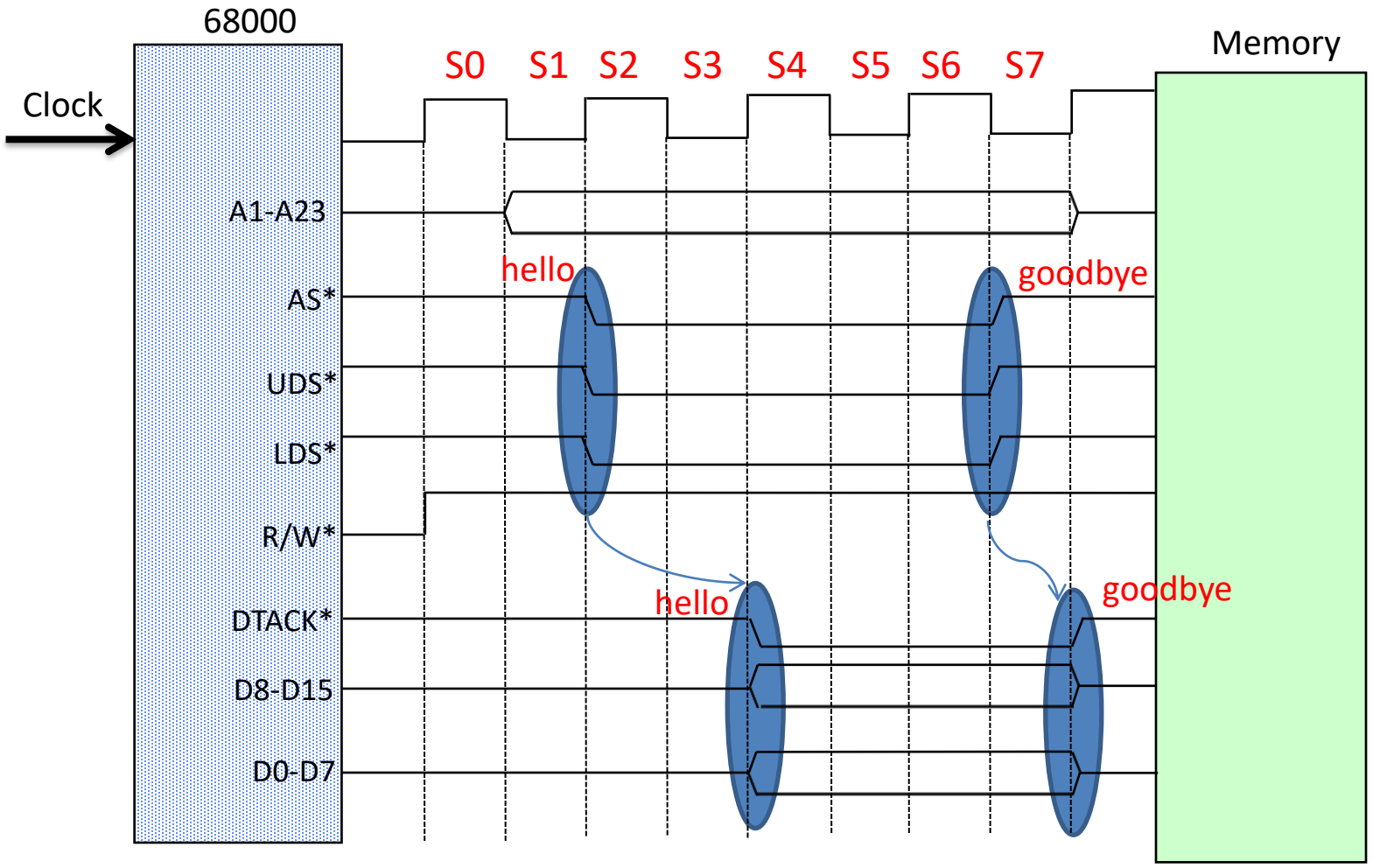
Read Cycle for a Word



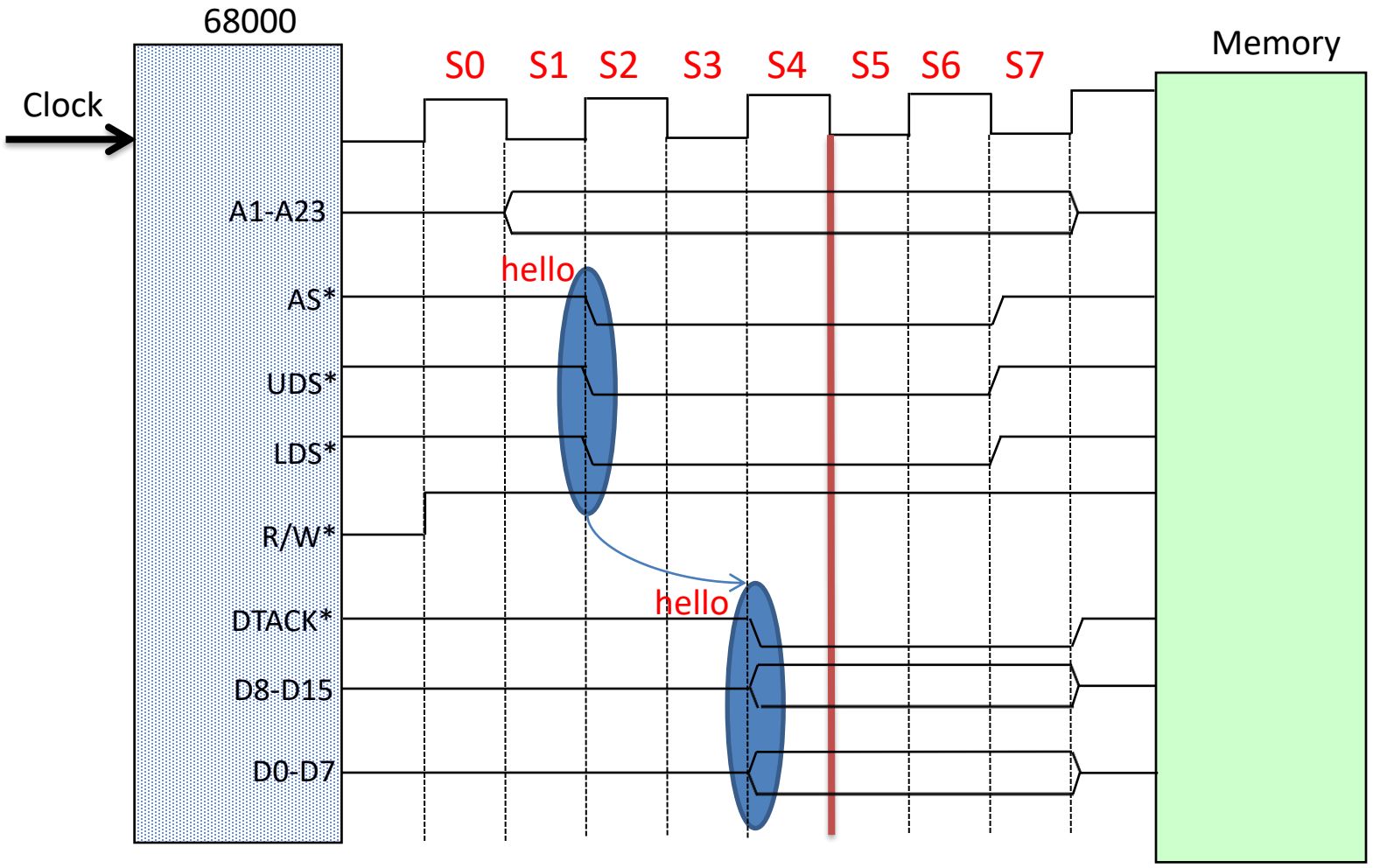
Read Cycle for a Word



Read Cycle for a Word

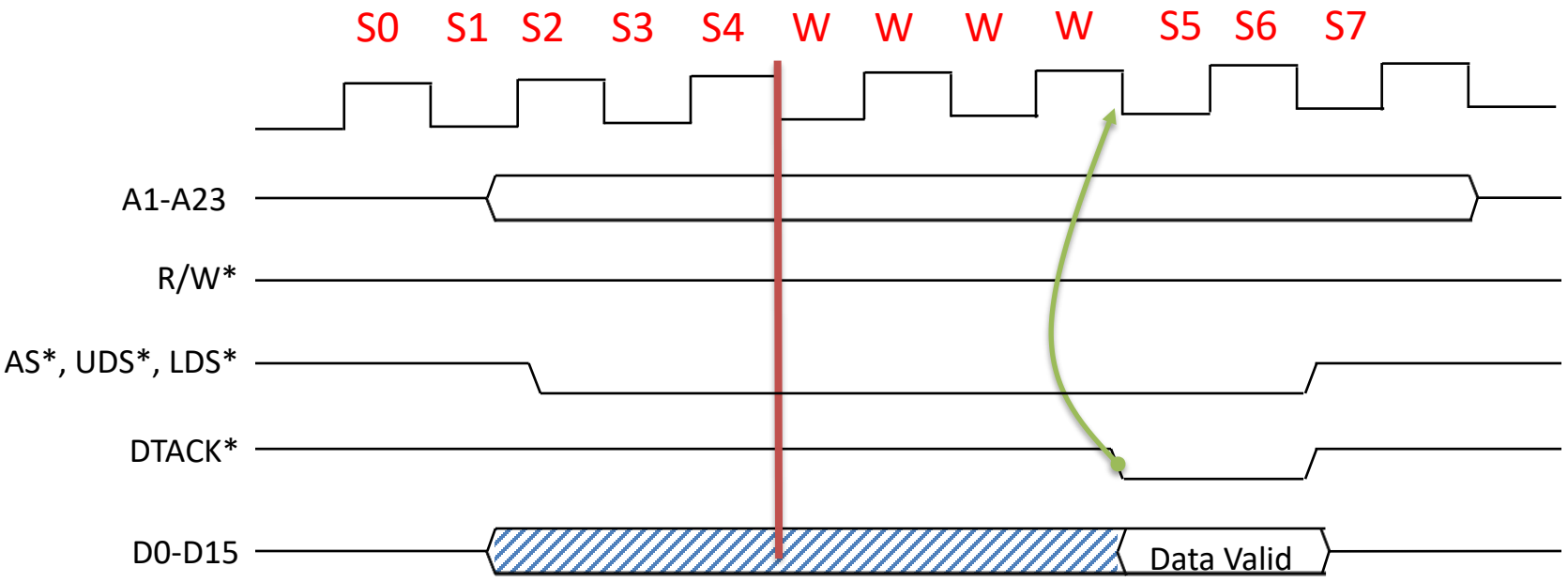


DTACK Must be Asserted Before the End of S4



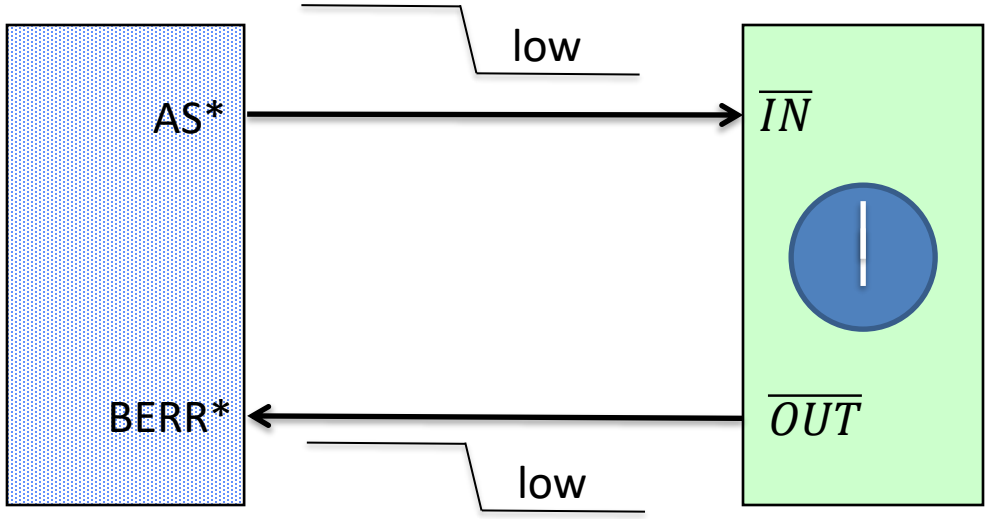
Wait States

- A wait state is an extra clocking period that lengthens the bus cycle
  - Inserted between S4 and S5 until DTACK arrives
  - Allows processor to operate with a mixture of both fast and slow components



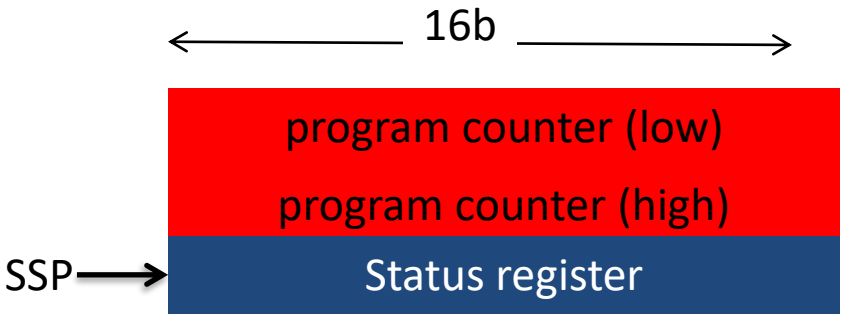
Watchdog Timer

- A watchdog timer can be used to terminate a bus cycle if DTACK never arrives



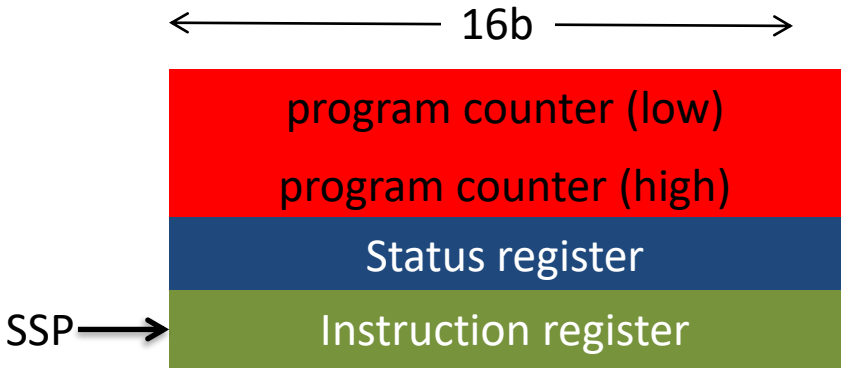
Bus Error Exception

- A bus error indicates that something has gone seriously wrong
  - More information is stored on the exception stack than is stored for either a group 1 or 2 exception



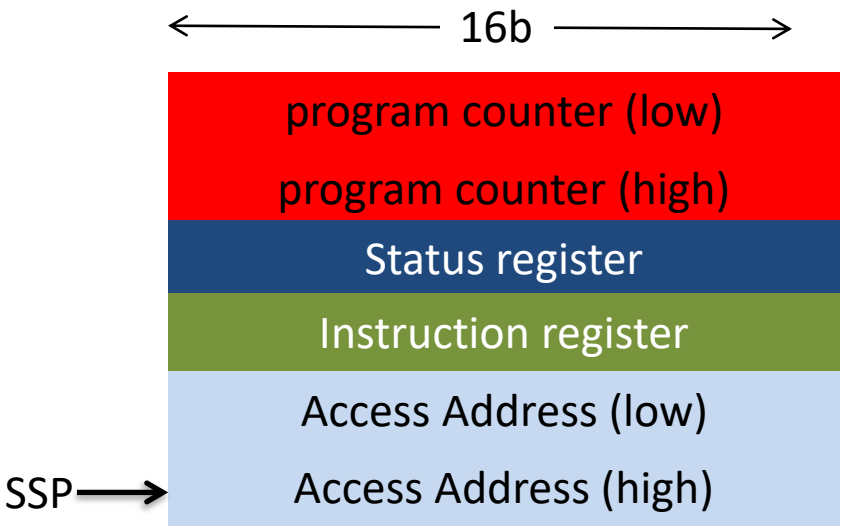
Bus Error Exception

- A bus error indicates that something has gone seriously wrong
  - More information is stored on the exception stack than is stored for either a group 1 or 2 exception



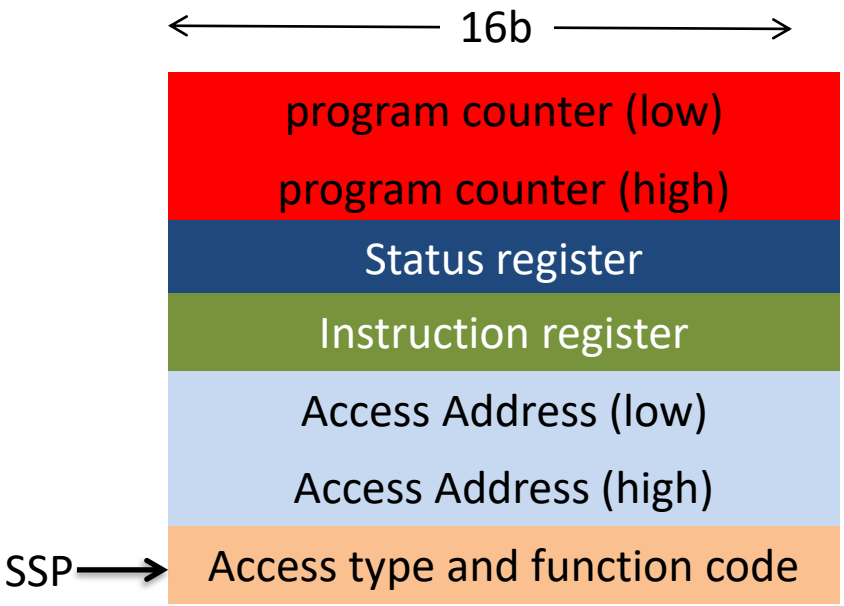
Bus Error Exception

- A bus error indicates that something has gone seriously wrong
  - More information is stored on the exception stack than is stored for either a group 1 or 2 exception



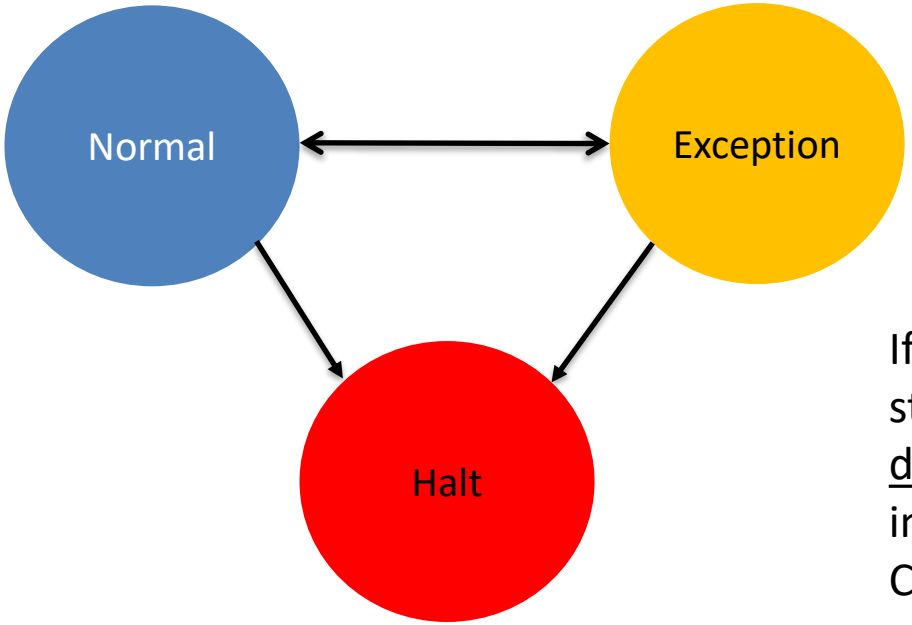
Bus Error Exception

- A bus error indicates that something has gone seriously wrong
  - More information is stored on the exception stack than is stored for either a group 1 or 2 exception



Bus Error Exception

- A bus error indicates that something has gone seriously wrong
  - More information is stored on the exception stack than is stored for either a group 1 or 2 exception



If bus error occurs while stacking information, a double bus fault will occur, in which case resetting the CPU is the only solution

Function Codes

- Function codes indicate the type of bus cycle currently being executed

FC0	FC1	FC2	Processor Cycle Type
0	0	0	Reserved
0	0	1	User Data
0	1	0	User Program
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	Interrupt Acknowledge

Problem 1

- The (CPU) clock driving the bus on a particular 68000 system has a frequency of 10 Megahertz. How long does the following instruction take to execute on the system?

MOVE.W D0,(A0)

Problem 2

- The (CPU) clock driving the bus on a particular 68000 system has a frequency of 10 Megahertz. However, the 68000 system inserts one wait state per read or write cycle. How long does the following instruction now take to execute on the system?

MOVE.W D0,(A0)

Problem 3

- A certain processor and memory share a 32-bit bus running at 100 MHz. Eight clock cycles are required to access a 32-bit value from memory. What is the bandwidth of the bus, where bandwidth is the number of bytes that can be transferred per second over the bus?

Summary

- A bus is a group of signals that are used to communicate among the devices in a computer system
- Multiple buses exist in a computer system
- The major signal groups of a bus are address lines, data lines, and control lines
- Two methods are used for data transfer
  - Synchronous
  - Asynchronous
- The 68000 communicates with memory (and I/O devices) through its system bus using an asynchronous communication protocol
  - Bus signal names and functions
    - A23-A1, D15-D0, UDS*, LDS*, AS*, R/W*, DTACK*
  - General signal relationship and timing based on Handshaking
  - Read/Write operations typically take 4 clock cycles