# Practice Problems for Topic 9

## CIS*2030: Structure and Application of Microcomputers

---

The practice problems below are important, but will *not* be marked. Their purpose is to ensure that you understand the major concepts covered in Topic 9. Doing these problems by yourself is imperative, as a portion of the marks on the final exam will be based on questions related to Topic 9.

---

1. Why do most ISAs, like the Motorola 68000, have both a supervisor state and a user state?

2. An exception is always processed in what state?

3. Show how the ANDI instruction can be used to clear the S-bit in the SR while leaving all other bits unaffected.

4. Assume that the contents of the status register are SR = 0x0000 immediately before the instruction in the previous question executes. What will be the result of executing the instruction?

5. What is the vector number and vector address for a privilege-violation exception?

6. Whom or what defines the vector addresses for each exception handler?

7. Does the 68000's ISA defines exceptions for the Divide by zero, overflow, and syntax errors?

8. What is the the 68000's trace exception is used for?

9. Consider the listing file below:

```
00008000                              0     ORG     $8000
00008000  21FC 0000CF62 000C          1     MOVE.L  #$CF62,12
00008008  41F9 0000900D               2     LEA     $900D,A0
0000800E  4290                        3     CLR.L   (A0)
   8010
```

Where does the PC point after the final CLR instruction executes?

10. What exception has the highest priority?

11. Show the memory locations that are altered, and the new data in them, if exception processing begins with the following register values: SSP = $00FF4600, PC = $000034C2, and SR = $8000.

12. What exception condition initiates exception processing at the address found in memory location 0x00001C?

13. Write an instruction sequence to cause the previous exception to be generated.

14. Assume that each exception handler and interrupt service routine save all data registers and all address registers (except for A7). How many levels of nested exceptions are possible with a stack of size 1K bytes?

15. The contents of the first eight memory locations are shown below. What is loaded into the initial program counter and what is loaded into the initial system stack pointer when a reset exception occurs? [2 marks]

| Address | Contents |
|---|---|
| 000000 | 0000 |
| 000002 | 9000 |
| 000004 | 0000 |
| 000006 | 0400 |