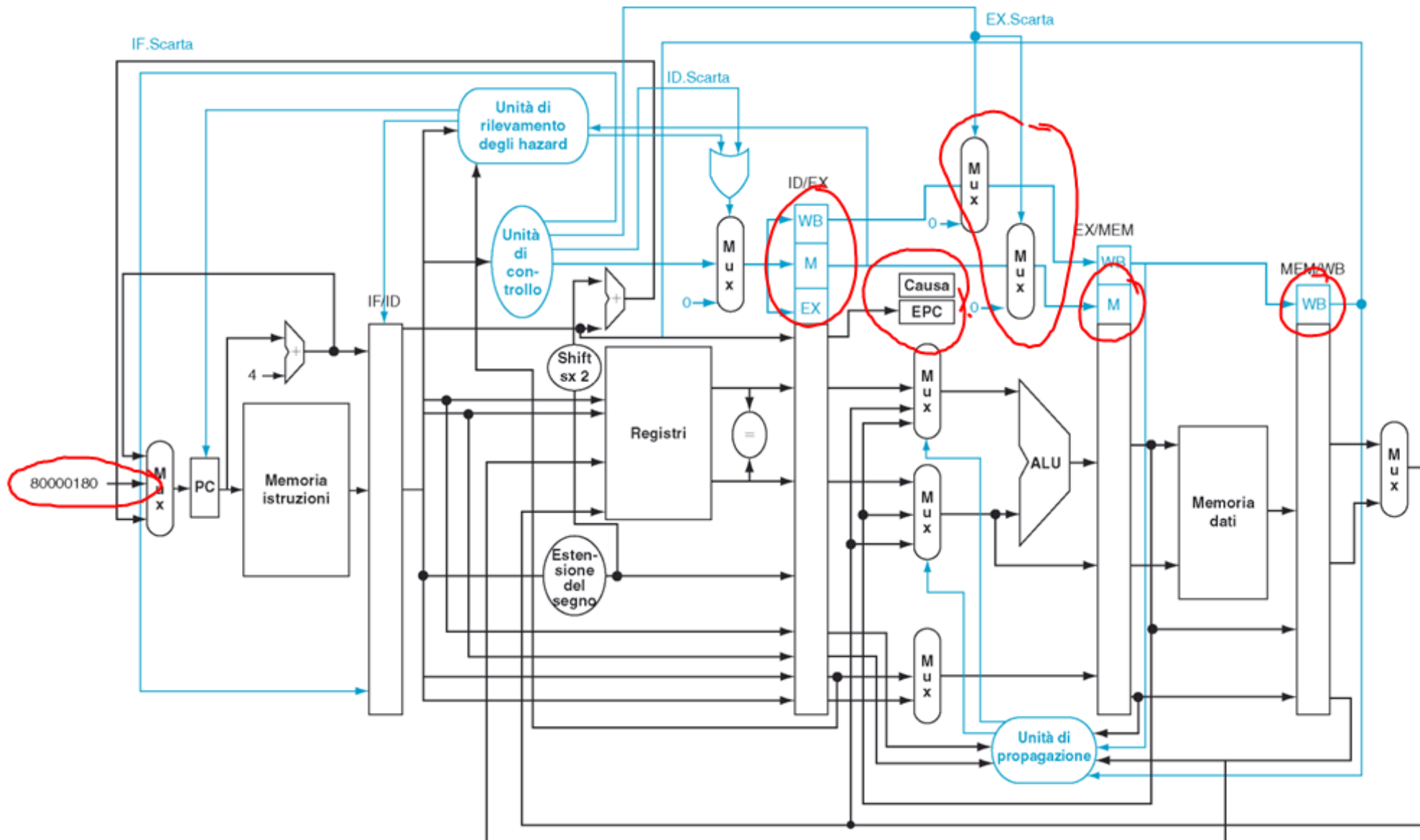


Modifiche per le eccezioni



CPU MIPS a due canali

