EE32 Device Simulation Lab

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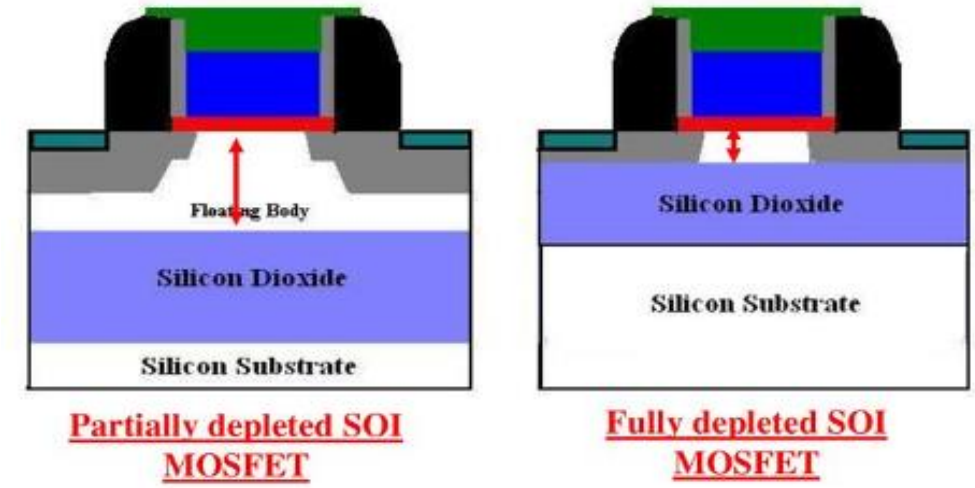
Lab 2: Design and Analysis of 32-nm FD SOI and PD SOI while incorporating measures to reduce short channel effects

Apart from designing the PDSOI and FDSOI's, it is important to incorporate measure for short channel effects to amplify the characteristic behavior of these MOSFETS. It includes fabricating spacers, implanting low doped drain structures, implantation of halo regions as well as due to scaling down the gate oxide thickness reduces too and to such a parameter that it is possible for electrons to tunnel through thereby leading to the deviation from ideal behavior.



What are Spacers?

Spacers are vertical sidewall portions which protect gate stack and gate oxide during subsequent processing as well as they are to reduce parallel overlap capacitances in the MOSFET structure. They also shield it from the fringing field effect of the gate.

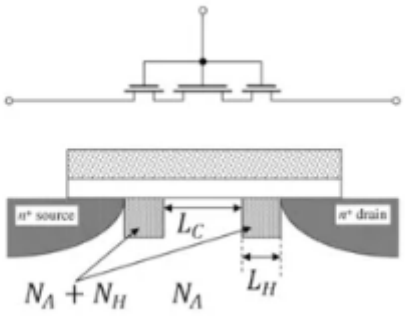
What are LDDs (Low Doped Drains)?

LDD structures reduce the horizontal electric field between source and drain regions. This is to reduce the injection of hot electrons into the oxide as they would not be accelerated to high velocities. On aggressive scaling, electric fields grow unproportionally thus leading to hot

electrons (Transport of high energetic electrons over the oxide barrier) Also these electrons might get trapped in the oxide region therefore reducing the threshold voltages over time.

What are Halo Implants?

Halo Implants are used to increase the threshold voltage to a appropriate value as it degrades on scaling down. It becomes more and more difficult to turn off the device as we scale down therefore, Halo Implants as shown in figure equivalently constitute as another pair of transistors but with higher threshold thereby on the whole the threshold voltage increases

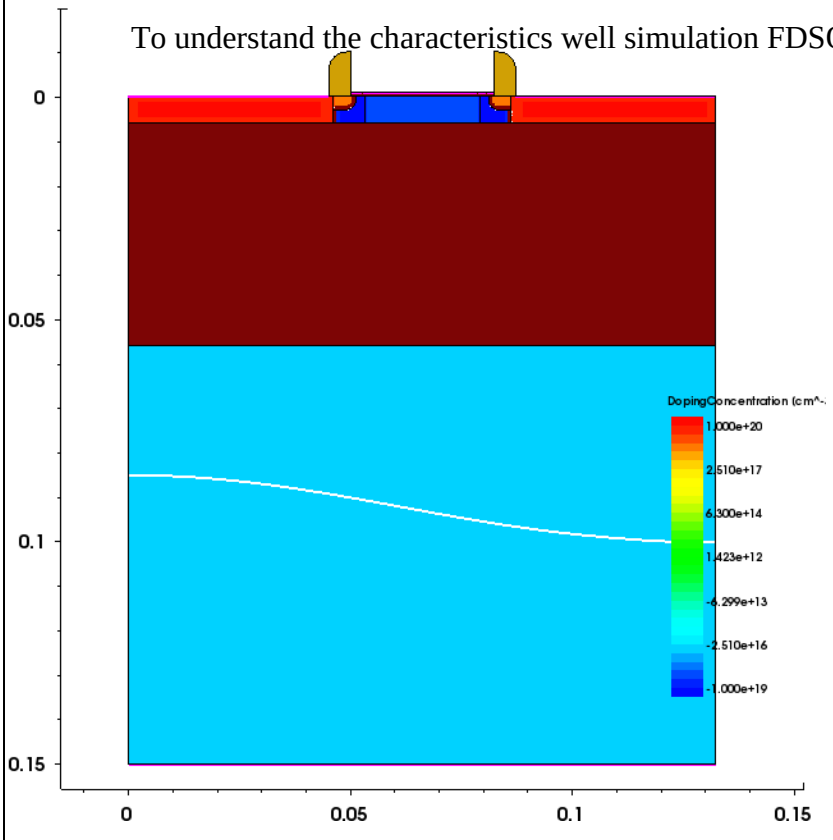


High k dielectric for Gate oxide?

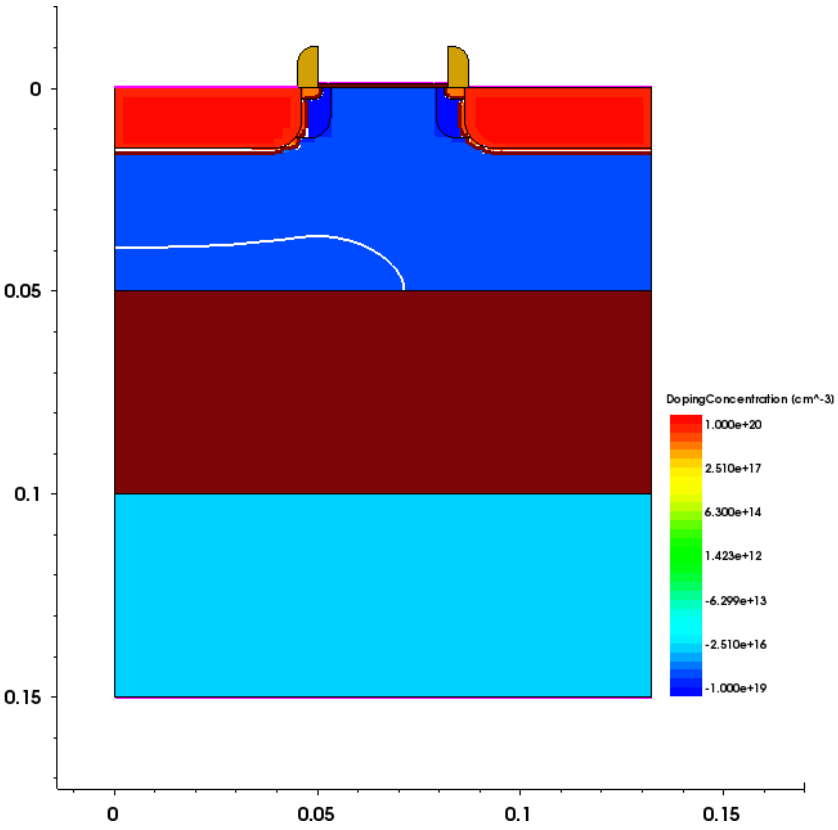
One of the measures to counter for the increasing tunneling current which reduces power efficiency as well as affects the device reliability as high k dielectric would have to go with higher thickness for the same gate capacitance. And this increase in thickness safeguards the device from tunneling current.

Device Specifications:

To understand the characteristics well simulation FDSOI and PDSOI has been done

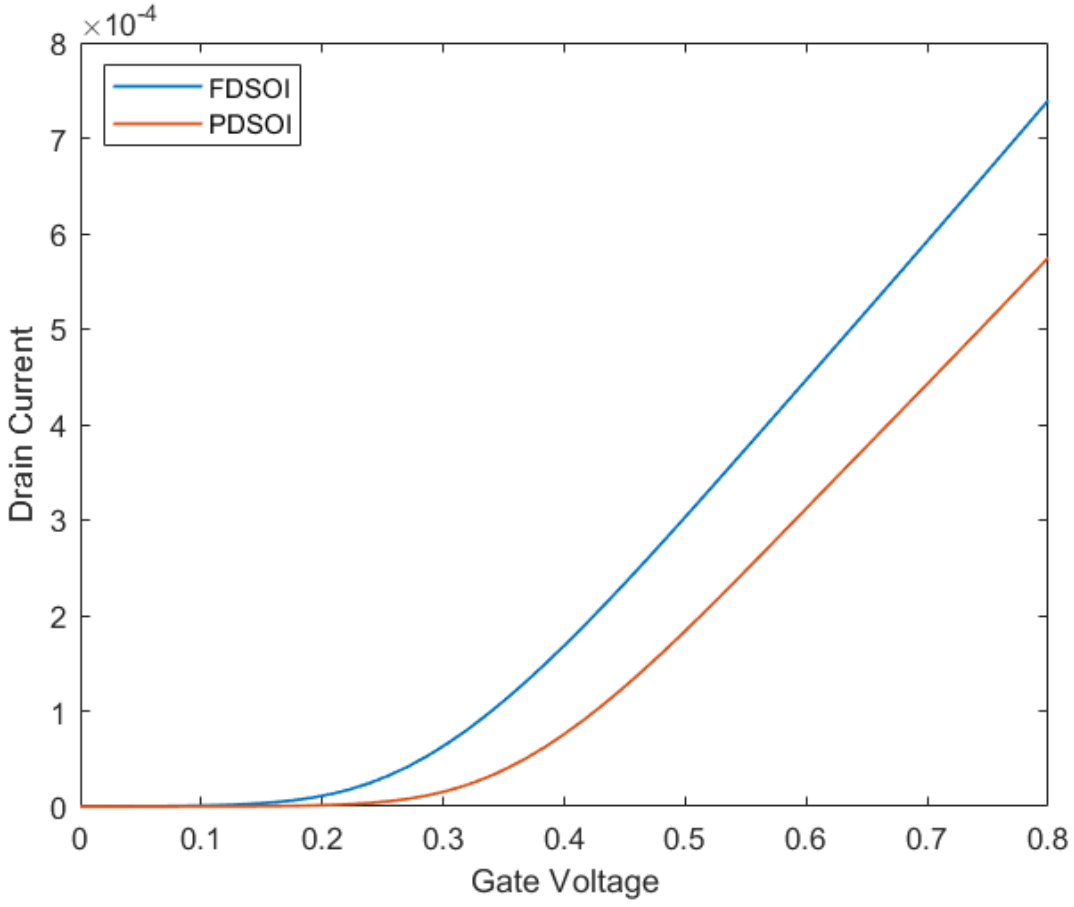


Gate Length (L_G):	32nm
Silicon Thickness (T_{Si}):	6nm
Gate Oxide Thickness (T_{OX}):	0.9nm
BOX thickness	50nm
Body doping:	1e+18
Source/ Drain doping:	1e+20
Halo Doping	1e+19
LDD Doping	3e+18
Gate work function:	4.3eV
Decay length:	0.2nm
Interface length:	0.2nm
Spacer Height	10nm
Spacer Width	5nm



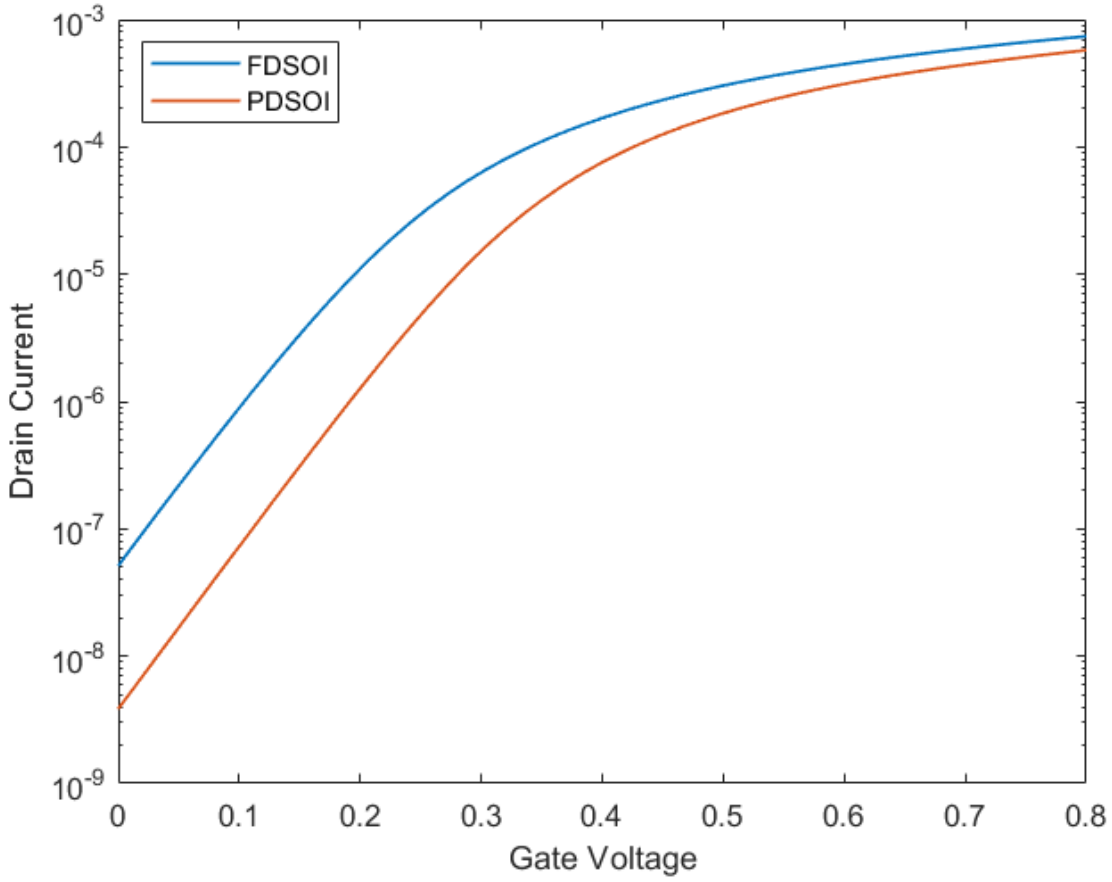
Gate Length (L_G):	32nm
Silicon Thickness (T_{Si}):	50nm
Gate Oxide Thickness (T_{OX}):	0.9nm
BOX thickness	50nm
Body doping:	1e+18
Source/ Drain doping:	1e+20
Source/ Drain depth	15nm
Halo Doping	1e+19
LDD Doping	3e+18
Gate work function:	4.3eV
Decay length:	0.2nm
Interface length:	0.2nm
Spacer Height	10nm
Spacer Width	5nm

For the structures designed above, the Id-Vd characteristics observed are as shown below:

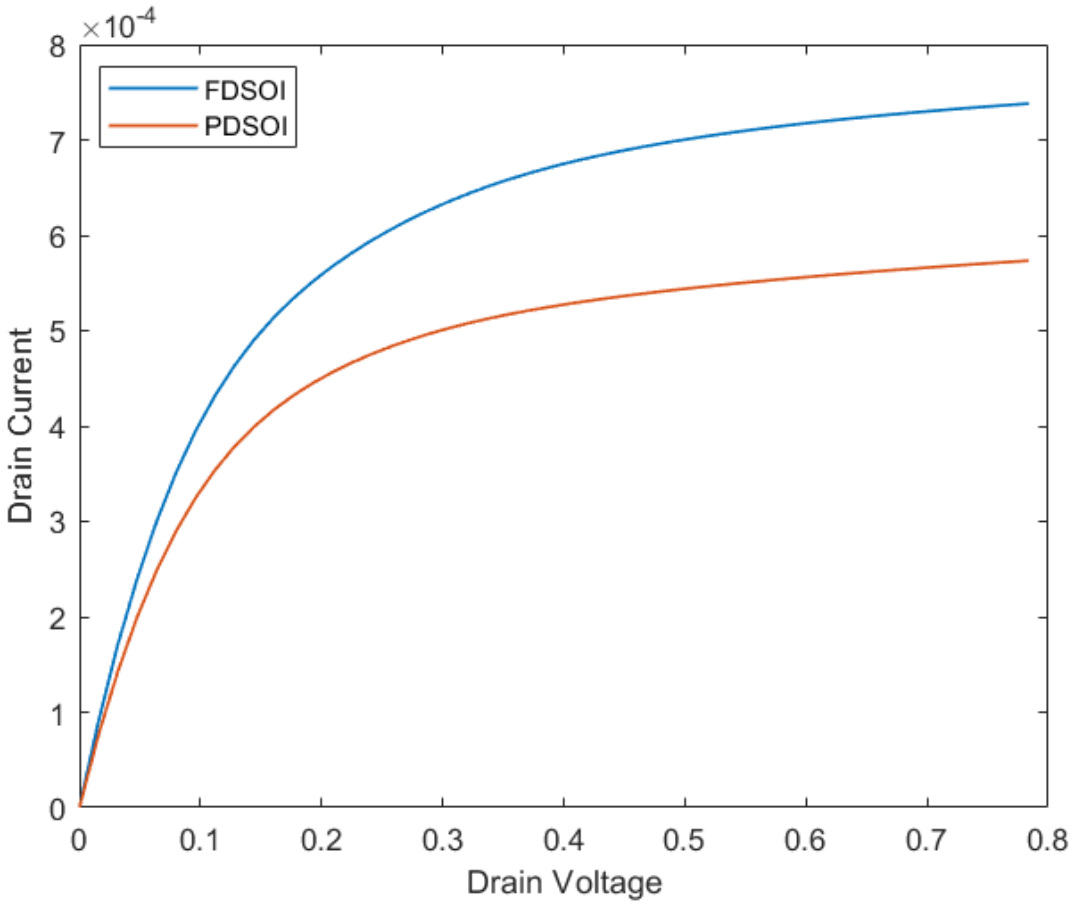


As could be seen, FDSOI has higher on current. One of the prime reasons is that since the region of depletion is completely contained, all of it serves for the conduction thus leading to high drain current. Whereas if you look at the off current in log plot as shown below, it shows higher value for FDSOI again. Similar explanation goes for it as being contained, even with low bias, there is higher probability that the structure design directs the carriers from source to drain.

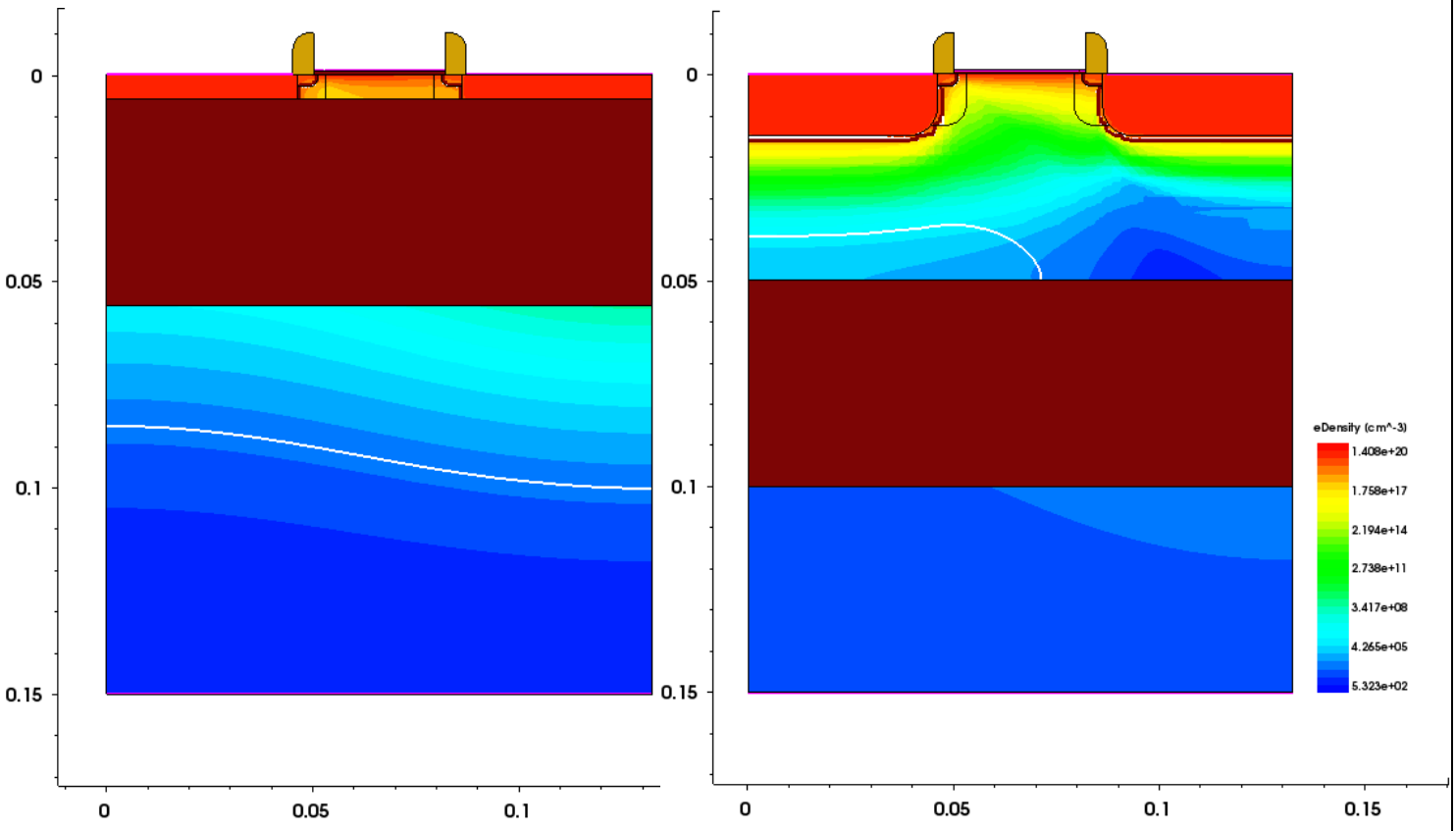
Due to this FDSOI has usually lower threshold voltage as compared to PDSOI.



It might also be important to observe the Drain Current - Drain Voltage characteristics for analog and digital applications. It shows a higher Rout for FDSOI as compared to PDSOI but lower Ron for FDSOI. Thus, according to the characteristics relevant application can be switched to.



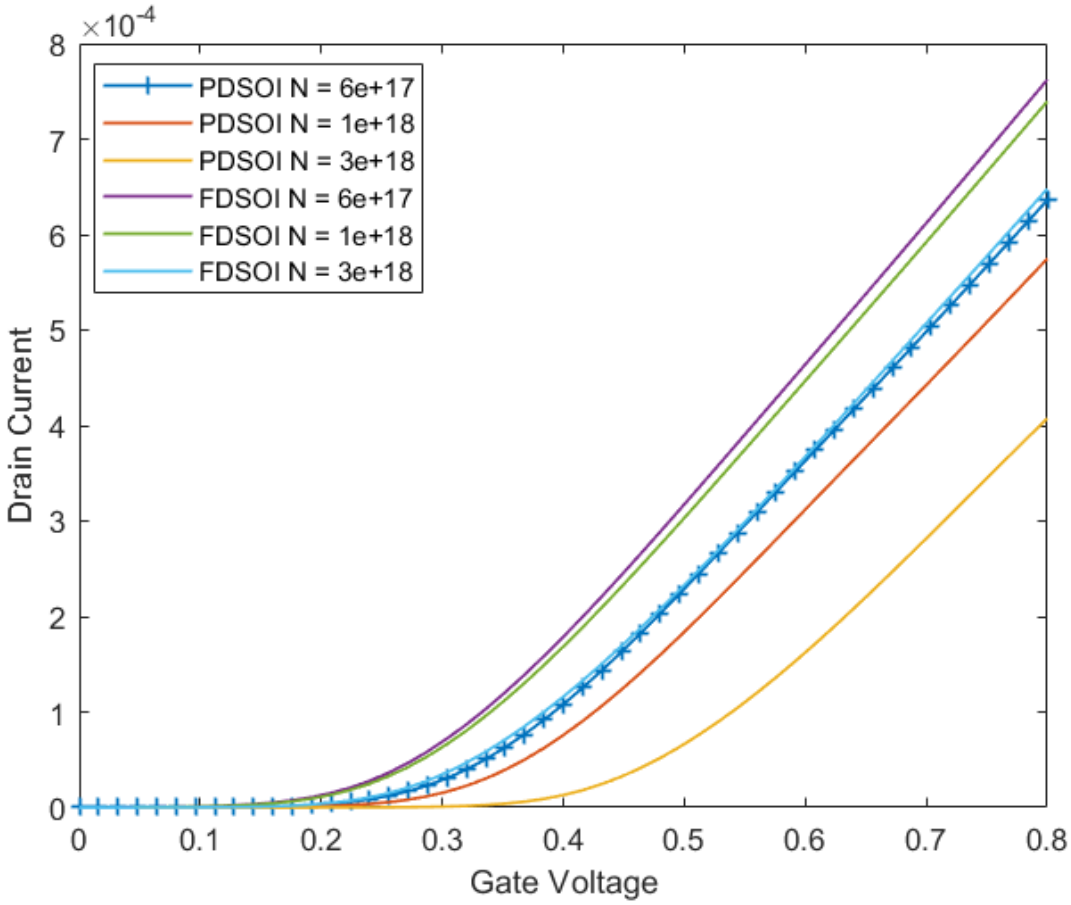
It is important to note that the PDSOI behavior might become same if the thickness of silicon falls to such a value that all of it gets depleted. In that case there would not m=be much difference in their behavior. To analyze the device properly, we might look at electron density or holes density for both of them.



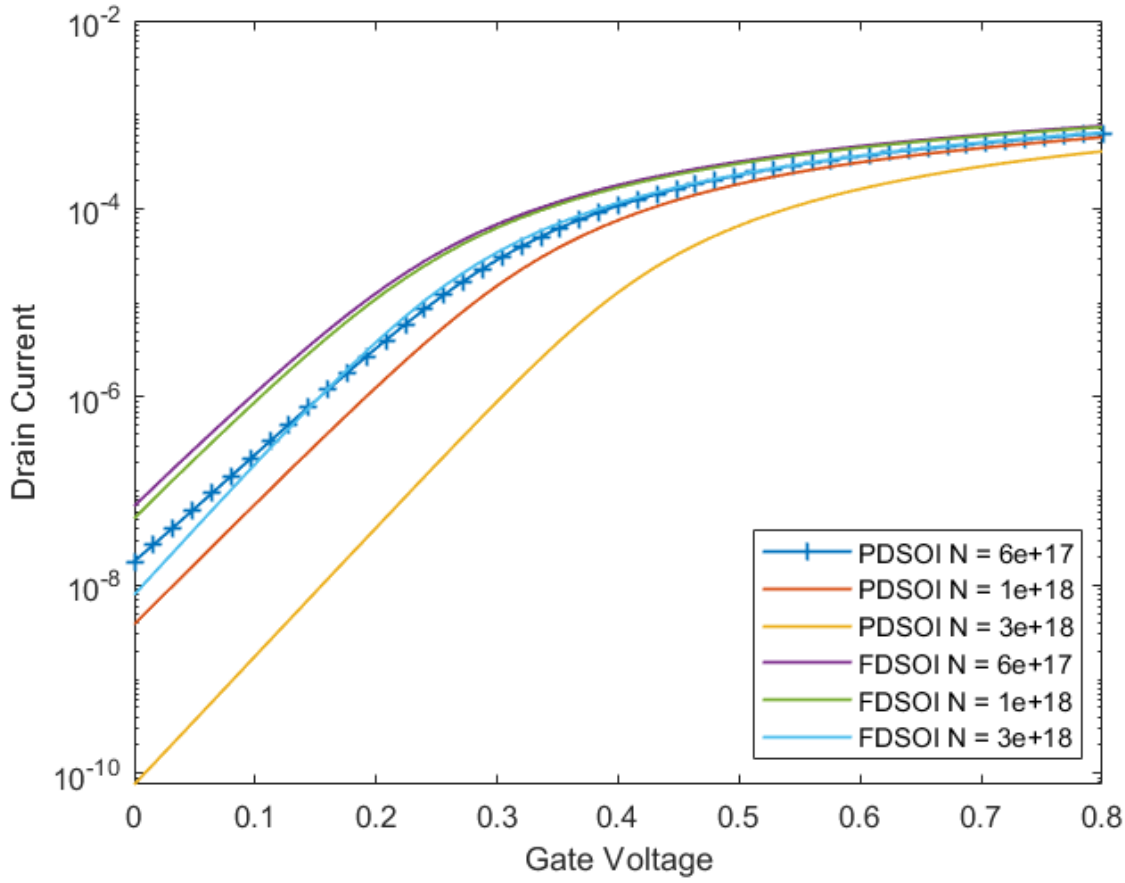
Since we are accounting for measures to reduce SCEs (Short Channel Effects), after deciding upon a structure, the doping of a particular structure is very important. Therefore, we would account for change of doping for LDDs, Halo implants and Body and look for how exactly and how critical each parameter is.

Variation of doping concentration for Body in FDSOI and PDSOI

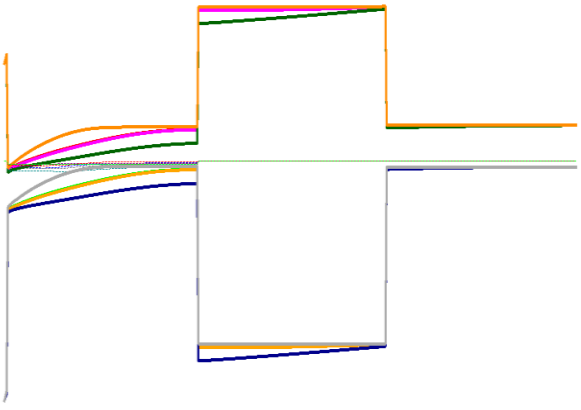
The doping concentration for the body was varied around 1e+18 and results were observed. It is believed that for lower body doping even the PDSOI would tend to deplete completely thus reaching the similar characteristics as of an FDSOI, however the structure limits the behavior in leakage current characteristics.



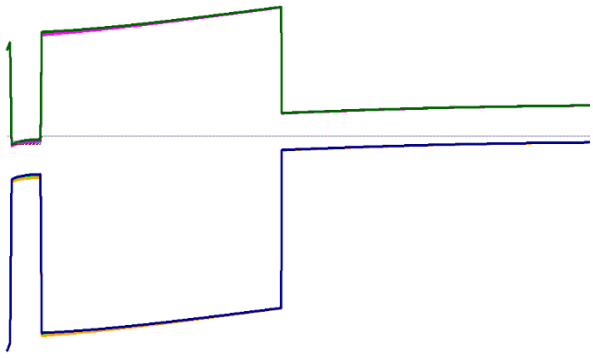
However, the subthreshold swing being different for the two structures, their subthreshold behavior varies.



For body Doping, it is important to visualize the band diagram too and formation of depletion regions



PDSOI Band Diagram

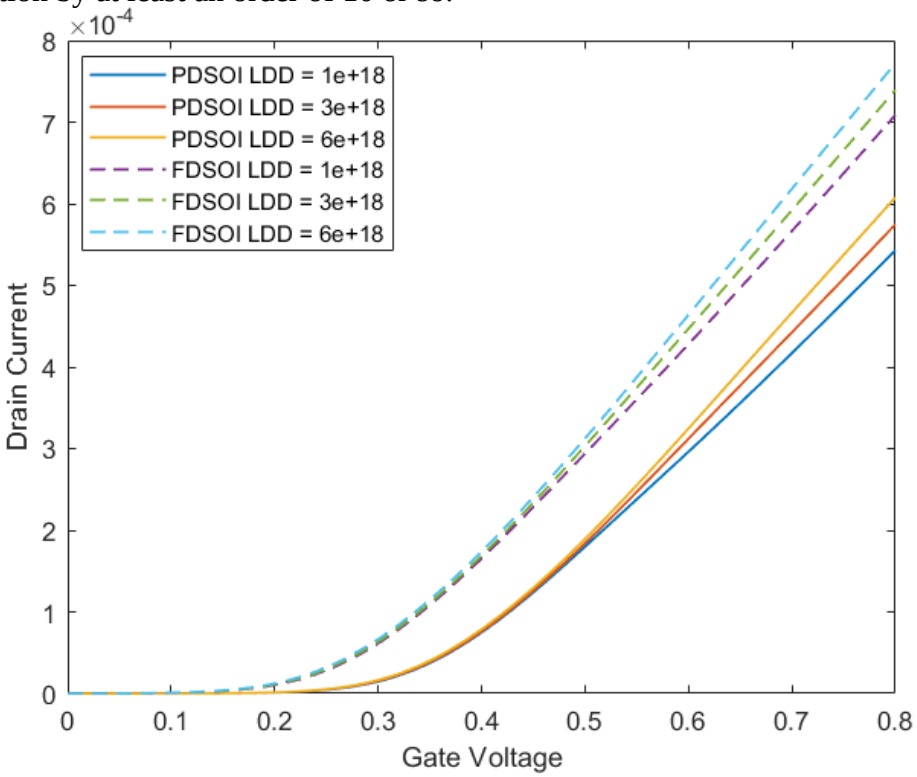


FDSOI Band Diagram

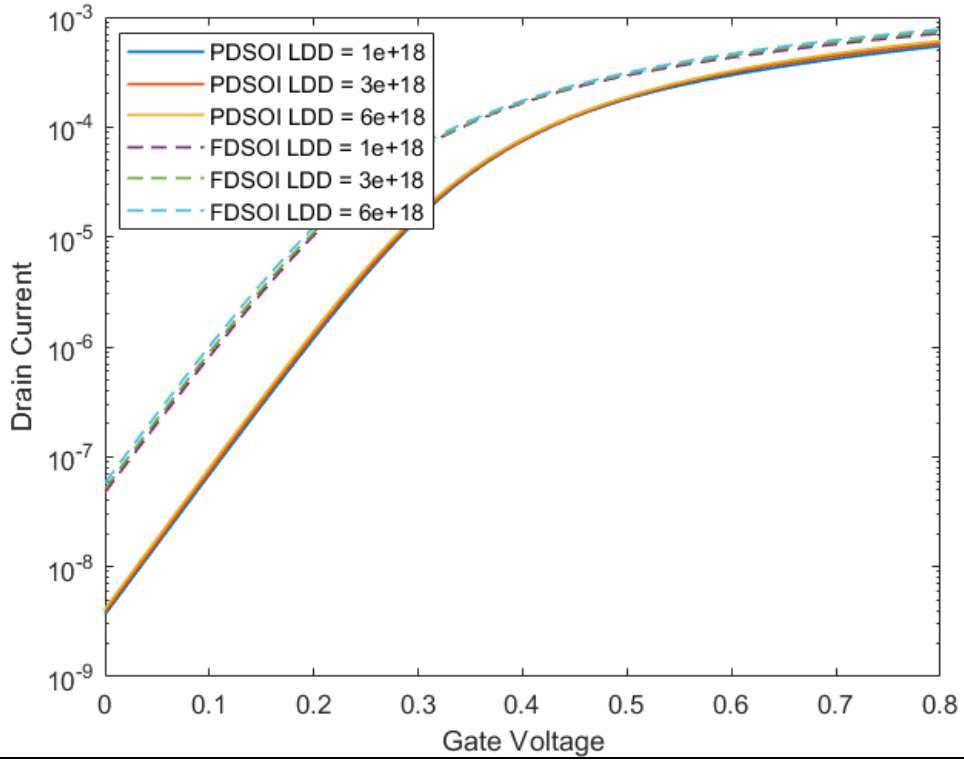
As could be seen from the band diagram too, low doping in substrate leads to more depletion whereas not all the region is depleted whereas in FDSOI all of the silicon body is depleted

Variation of doping concentration for LDD in FDSOI and PDSOI

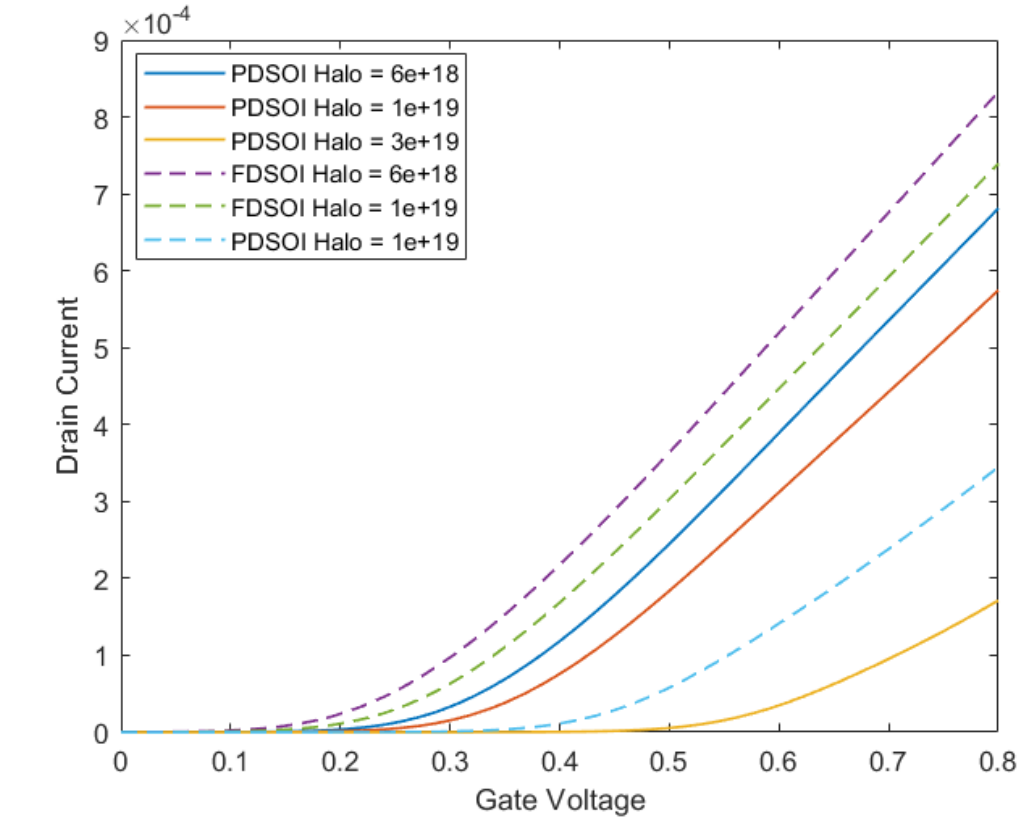
Decrease in concentration of doping in LDD would result in lower Ion and the electric field would be reduced. However, it is comparably a weaker parameter as compared to body doping for the given structure. To reduce the ON current by a significant amount you need to reduce the concentration by at least an order of 10 or so.



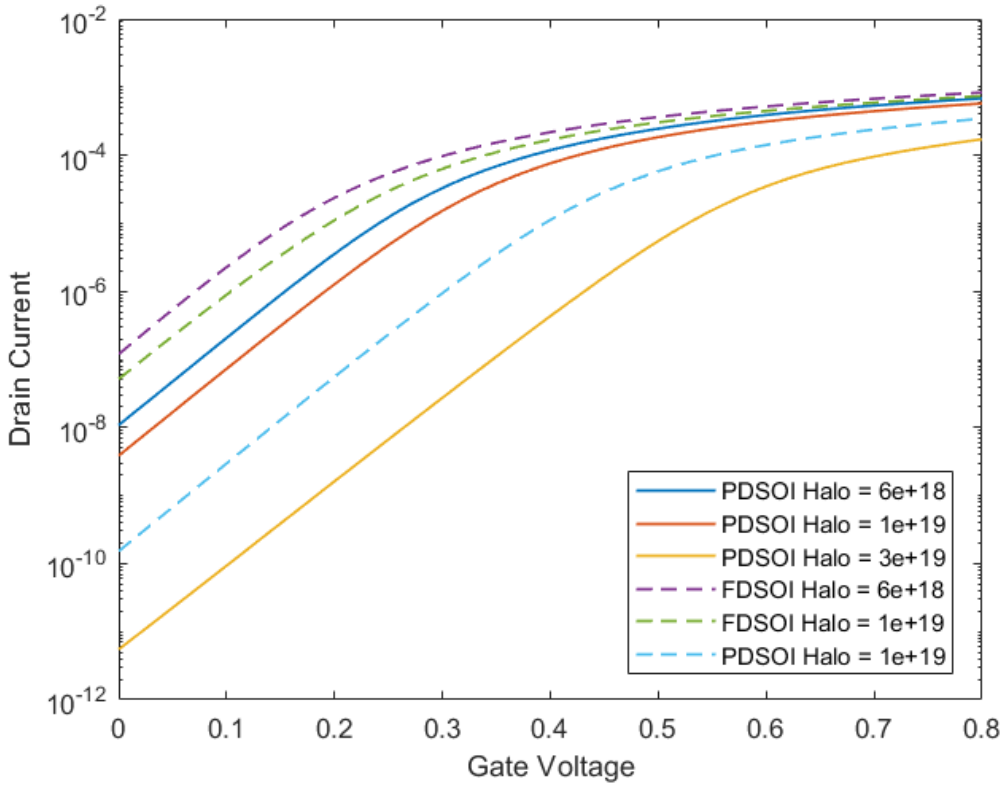
Drain Current on log scale to visualize the subthreshold characteristics. Almost little to no changes are for subthreshold behavior.



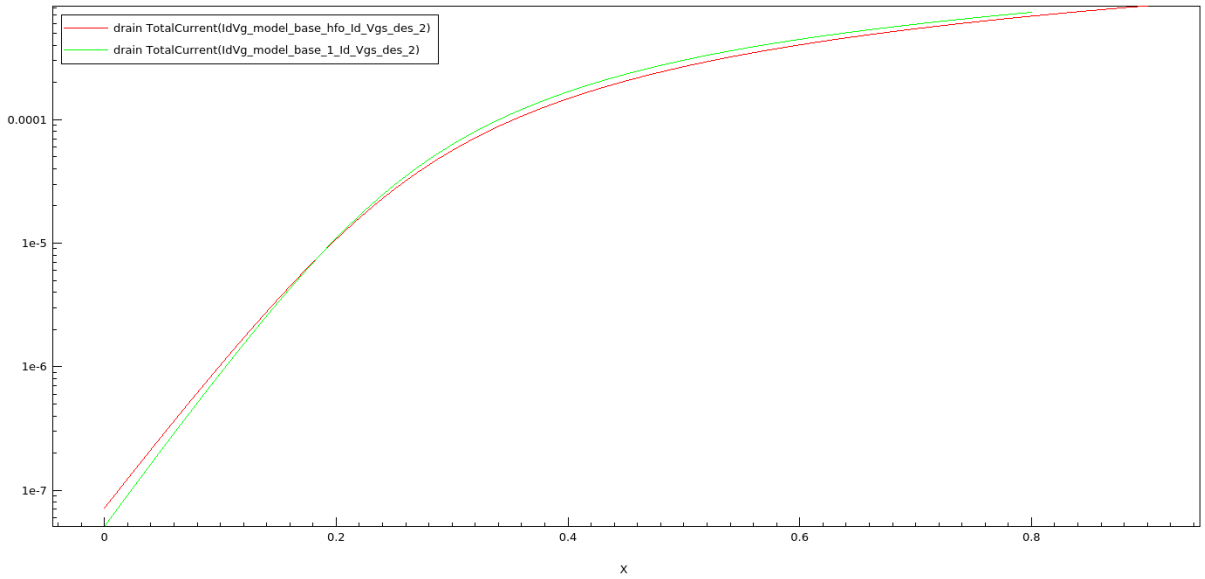
Variation of doping concentration for Halo Implants in FDSOI and PDSOI



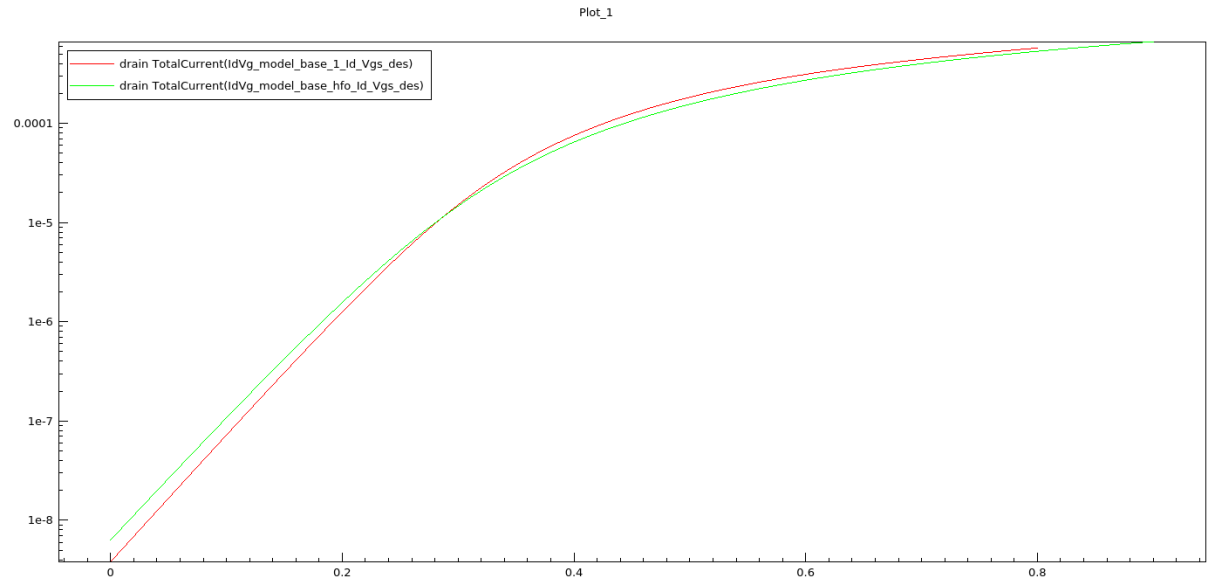
The figure above clearly depicts that halo implants doping is very critical, in consideration with its design, and significantly affects the subthreshold behavior too. High doping in halo leads to very low off current and limits Isat too. Thus, it plays a critical role in the characteristics.



Using HfO_2 in place of SiO_2 for Gate Oxide



FDSOI with HfO2 and SiO2 as Gate Oxide



FDSOI with HfO2 and SiO2 as Gate Oxide

To account for the performance metrices, DIBL, Ion/Ioff, Ron, Rout and other parameters were found out for each configuration. They are tabulated as below:

FDSOI							
Body Doping	1.00E+18	6.00E+17	3.00E+18	1.00E+18	1.00E+18	1.00E+18	1.00E+18
LDD Doping	3.00E+18	3.00E+18	3.00E+18	1.00E+18	6.00E+18	3.00E+18	3.00E+18
Halo Doping	1.00E+19	1.00E+19	1.00E+19	1.00E+19	1.00E+19	6.00E+18	3.00E+19
Ioff	5.13E-08	6.94E-08	7.91E-09	4.73E-08	5.77E-08	1.19E-07	1.52E-10
Idsat	7.39E-04	7.62E-04	6.48E-04	7.09E-04	7.72E-04	8.33E-04	3.45E-04
Vth	0.3000	0.2943	0.3413	0.3030	0.2995	0.2698	0.4840
Gmmax	0.00148	0.00150	0.00141	0.00143	0.00154	0.00157	0.00109
Rout	521.33	400.59	2981	568.68	459.92	212.74	1.72E+05
Ron	0.6749	0.6629	0.707	0.6998	0.6476	0.6365	0.9127
Ion/Ioff	1.44E+04	1.10E+04	8.19E+04	1.50E+04	1.34E+04	6.98E+03	2.26E+06
Vth @ 0.8V I = 1e-7	0.023	0.013	0.079	0.026	0.019		0.221
Vth @ 0.08V I = 1e-7	0.049	0.038	0.106	0.051	0.046	0.027	0.231
DIBL	36.359	34.389	37.660	35.501	37.810	36.806	14.956
Subthreshold Slope	78.59	81.23	71.42	79.14	78.22	75.44	77.16

And for the PDSOI, they are as shown below

PDSOI							
Body Doping	1.00E+18	6.00E+17	3.00E+18	1.00E+18	1.00E+18	1.00E+18	1.00E+18
LDD Doping	3.00E+18	3.00E+18	3.00E+18	1.00E+18	6.00E+18	3.00E+18	3.00E+18
Halo Doping	1.00E+19	1.00E+19	1.00E+19	1.00E+19	1.00E+19	6.00E+18	3.00E+19
Ioff	3.85E-09	1.79E-08	7.62E-11	3.66E-09	4.14E-09	1.08E-08	5.49E-12
Idsat	5.75E-04	6.36E-04	4.08E-04	5.43E-04	6.08E-04	6.81E-04	1.71E-04
Vth	0.3688	0.3418	0.4767	0.3728	0.3722	0.3352	0.5898
Gmmax	0.00133	0.00139	0.00126	0.00127	0.00142	0.00147	0.00081
Rout	6894	1764	321807	7269	6384	2454	5.12E+06
Ron	0.749	0.719	0.792	0.785	0.702	0.68	1.209
Ion/Ioff	1.49E+05	3.55E+04	5.35E+06	1.48E+05	1.47E+05	6.29E+04	3.12E+07
Vth @ 0.8V I = 1e-7	0.111	0.066	0.228	0.113	0.107	0.075	0.346
Vth @ 0.08V I = 1e-7	0.151	0.113	0.260	0.152	0.149	0.124	0.364
DIBL	55.62	65.70	44.02	54.60	57.56	69.20	24.63
Subthreshold Slope	78.125	89.44	73.47	78.29	77.59	77.93	81.89

Conclusion:

- It is important to note that always same doping concentrations are not used for PDSOI and FDSOI for body. Usually, undoped or low doped body is used for FDSOI which depletes very easily comparably. Consecutively its current characteristics change too, and they might contain kink effect as well.
- Halo Implant structure affects a lot too. It needs to be designed carefully and need to be investigated further.
- High k dielectric showed no major changes in the behavior. One of the reasons could be that hot electrons are not modelled. Also, the temperature for the whole device was taken to be constant and fixed whereas it is known that insulation of heat is one of the major challenges for SOI.