EE32 Device Simulation Lab

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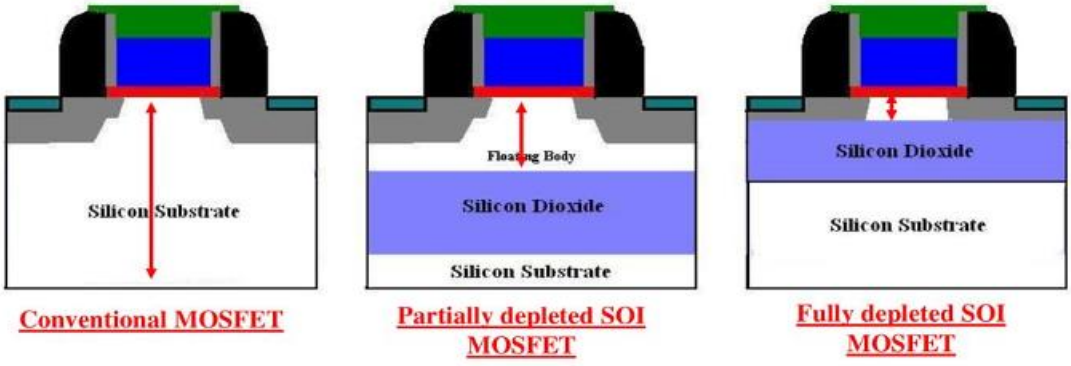
Lab 2: Design and Analysis of 32-nm SOI for digital and analog applications

SOI refers to Silicon on Insulator technology which is associated with fabrication of semiconductor devices on a silicon-insulator-silicon substrate. Due to the inherent design, it reduces parasitic capacitance which results in improved performance and higher power efficiency. The insulating layer and topmost silicon layer vary widely with the intended application.

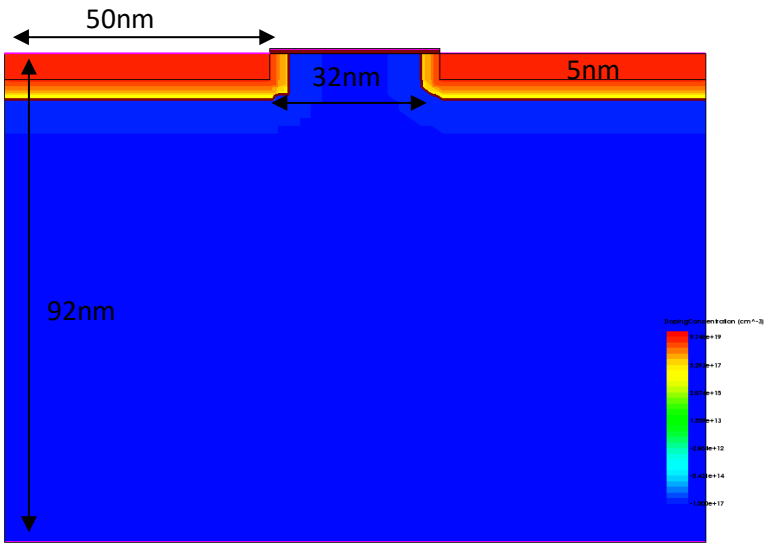
There are two types of SOI devices: Fully Depleted SOI (FD-SOI) and Partially Depleted SOI (PD-SOI). In PD-SOI, the floating body is large such that the depletion region formed between the BOX (buried oxide) and Gate Oxide cannot fully cover it whereas, all of it gets depleted in FD-SOI. Both of the structures have their characteristics properties and advantages over the Conventional MOSFET



Applications of SOI involve areas where superior analog performance is required, RF applications, space application sensitive to radiation hardening, silicon photonics, and many more applications like MEMS and other areas.

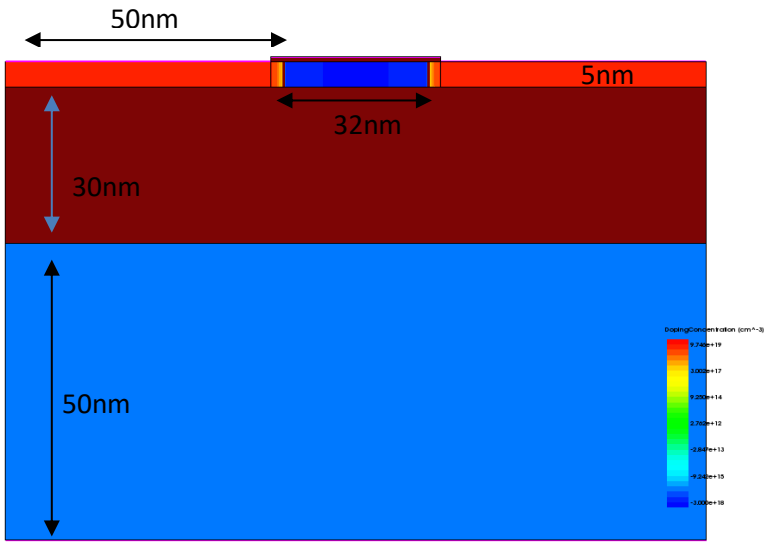
Device Specifications:

To understand the characteristics well simulation of Bulk MOSFET of same dimensions is done along with the PD-SOI and FD-SOI. It is important to note that although for devices as small as 32nm high k dielectrics are used to avoid the leakage effects. It is only for simplification purposes that SiO_2has been used here as gate oxide.



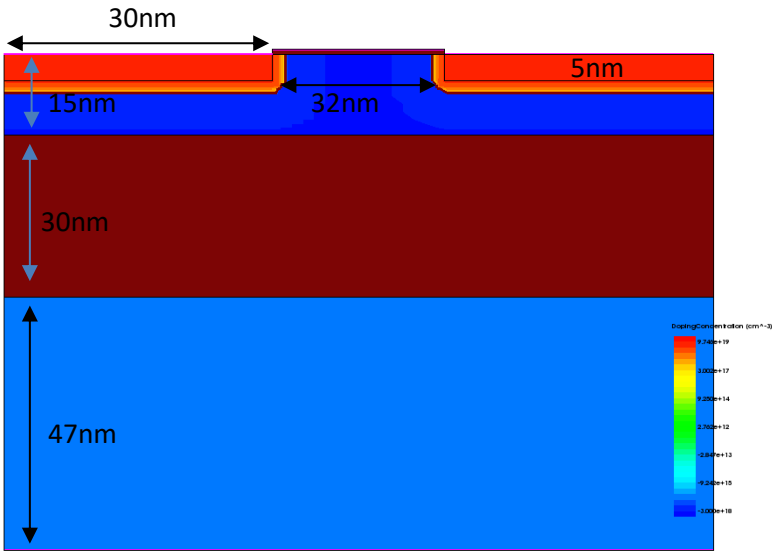
Bulk MOSFET

Gate Length (L_G):	32nm
Silicon Thickness (T_{Si}):	92nm
Gate Oxide Thickness (T_{OX}):	0.9nm
Substrate doping:	1e+17
Source/ Drain doping:	1e+20
Gate work function:	4.3eV
Decay length:	1.5nm
Interface length:	0.2nm
Other Parameters	



FD-SOI

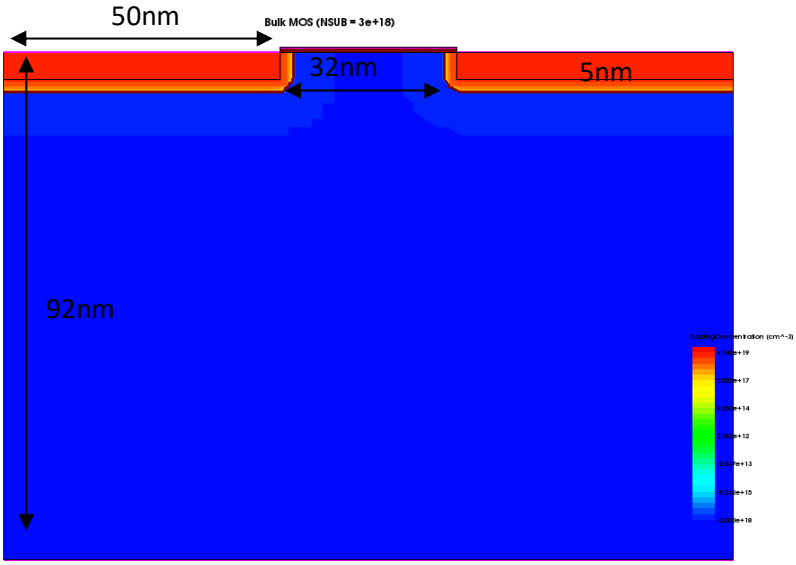
Gate Length (L_G):	32nm
Silicon Thickness (T_{Si}):	5nm
Gate Oxide Thickness (T_{OX}):	0.9nm
Substrate doping:	1e+17
Source/ Drain doping:	1e+20
Gate work function:	4.3eV
Decay length:	1.5nm
Interface length:	0.2nm
Other Parameters	T_{BOX} = 30nm; Body Doping = 3e+18



PD-SOI

Gate Length (L_G):	32nm
Silicon Thickness (T_{Si}):	15nm
Gate Oxide Thickness (T_{OX}):	0.9nm
Substrate doping:	1e+17
Source/ Drain doping:	1e+20
Gate work function:	4.3eV
Decay length:	1.5nm
Interface length:	0.2nm
Other Parameters	T_{BOX} = 30nm; Body Doping = 3e+18

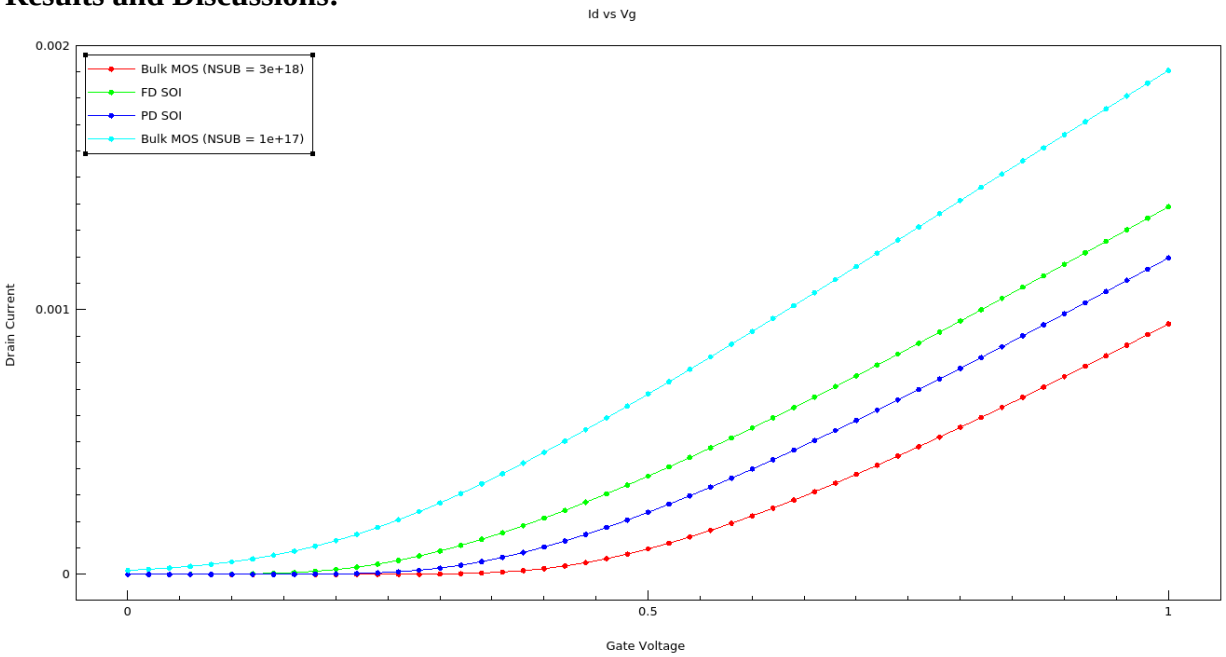
Also, to illustrate the properties in case of substrate having the same concentration as the floating body in the Bulk MOSFET i.e. NSUB = 3e+18 simulation has been carried out although this doping is very high for a substrate.



Bulk MOSFET (NSUB = 3e+18)

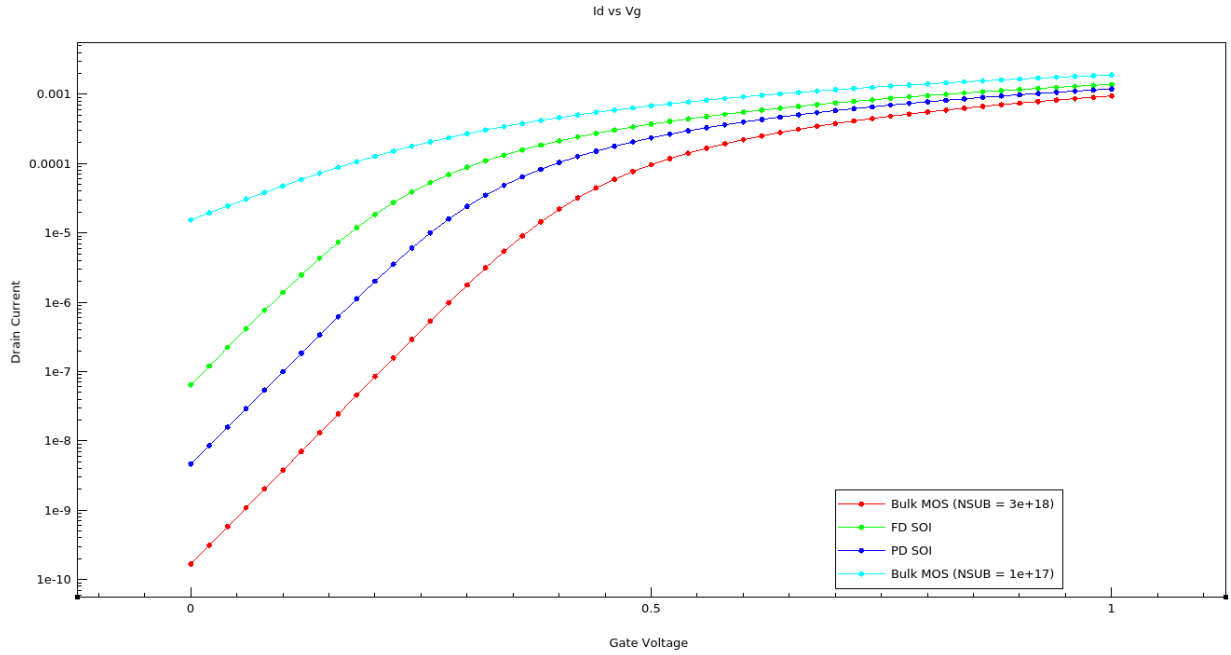
Gate Length (L_G):	32nm
Silicon Thickness (T_{Si}):	15nm
Gate Oxide Thickness (T_{OX}):	0.9nm
Substrate doping:	3e+18
Source/ Drain doping:	1e+20
Gate work function:	4.3eV
Decay length:	1.5nm
Interface length:	0.2nm
Other Parameters	

Results and Discussions:



The Id-Vg for all the devices are as shown above. It is important to realize that as channel grows shorter and shorter, leakage current increases which makes it difficult to turn off the device. You need to scale down depletion regions too for proper scaling of all the characteristics for which substrate doping needs to be increased. It becomes difficult to increase the substrate doping beyond a limit and if you don't increase the doping, there is significant increase in off current as could be seen in the graph shown below. This brings in the requirement of better designs of semiconductor devices.

The FD-SOI FET, PD-SOI FET simulated show a reliable off current as well as higher value of current compared to the conventional MOSFET which would have been obtained for higher substrate doping. This would result in higher performance for the same Vdd.



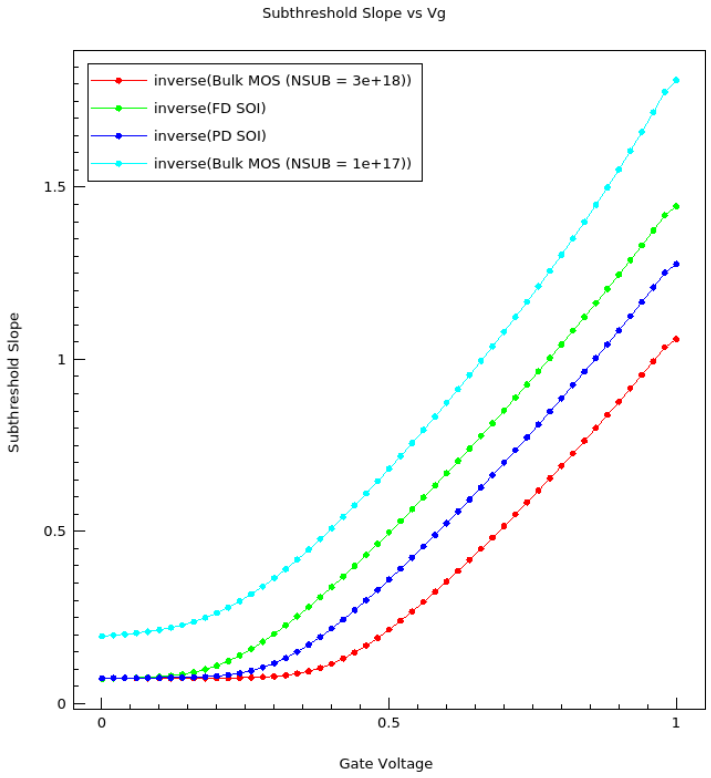
As of other performance characteristics, they have been tabulated below:

	Bulk MOSFET I (NSUB = 3e+18)	FD-SOI	PD-SOI	Bulk MOSFET II (NSUB = 1e+17)
Threshold Voltage	0.530203	0.363641	0.436	0.233693
IOFF (Amp)	1.68E-10	6.45E-08	4.66E-09	1.54E-05
ION (Amp)	9.47E-04	1.39E-03	1.20E-03	1.90E-03
ION/IOFF	5.65E+06	2.15E+04	2.57E+05	1.23E+02
Subthreshold Slope (mV/dec)	73.28	78.24	75.18	214.37
DIBL (mV/V)	37.23	49.68	68.25	-

As could be seen from above, threshold voltage in case of Bulk MOSFET I is really high due to extensive doping of the substrate, whereas in Bulk MOSFET II its extremely low, as the device finds it difficult even to switch off. PD-SOI and FD-SOI give reasonable values of threshold voltage such that they can be used with scaled down voltages of 0.9-1.1V of supply too.

On to off current ratio is improved by an order of 2 as compared to Bulk MOSFET II and an order of 3 in PD-SOI. Subthreshold slope is within considerations too and so is the DIBL for both of the SOI.

The performance benchmark set by Bulk MOSFET I is closely approached by SOI technology and along with that the simplistic design allows the scaling down of the device as well therefore supporting the Moore's Law.



Conclusion:

Tuning with the Oxide thickness, BOX thickness and doping and thickness of floating body, SOI characteristics can be analyzed further to fine tune the voltage, Ion. Ioff and other performance metrices to give a high-power efficiency and increased performance. It is quite significant for scaling of devices beyond 65nm to devices of technology node of 22nm and 10nm too