EE32 Device Simulation Lab

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Lab 1: Design and analysis of 180-nm N-MOSFET using 2D process simulation

Device Specifications:

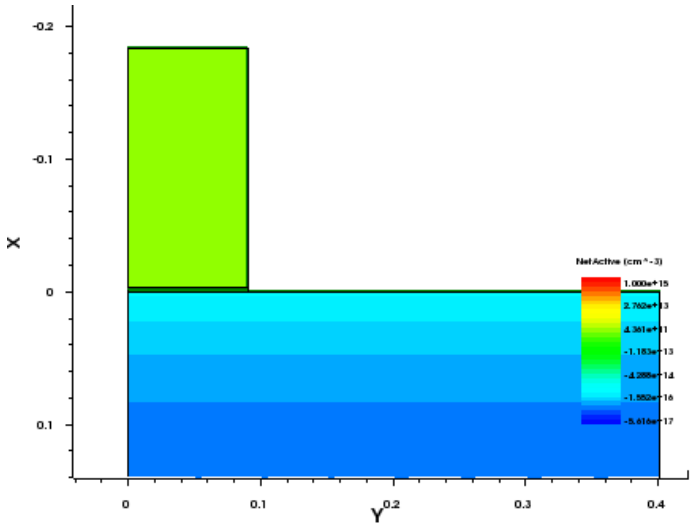
Gate Length (L_G):	180nm
Gate Oxide Thickness (T_{OX}):	2.9nm
Substrate doping: • Pwell • Retrograde Doping • Vt correction	Boron dose: 2e+13cm^{-2}, energy: 200KeV Boron dose: 1e+13cm^{-2}, energy: 80KeV Boron dose: 2e+12cm^{-2}, energy: 25KeV Diffuse temp.: 1050° C for 10s
LDD:	Arsenic dose: 4e+14cm^{-2}, energy: 10KeV Diffuse temp.: 1050° C for 0.1s
Halo:	Boron dose: 0.25e+13cm^{-2}, energy: 20KeV at an angle of 30° in all 4 directions
Spacer:	Nitride
Source/Drain Doping:	Arsenic dose: 5e+15cm^{-2}, energy: 40KeV Diffuse temp.: 1050° C for 10s
Add other parameters required for the design	Junction Depth = 60nm

Process Simulation:

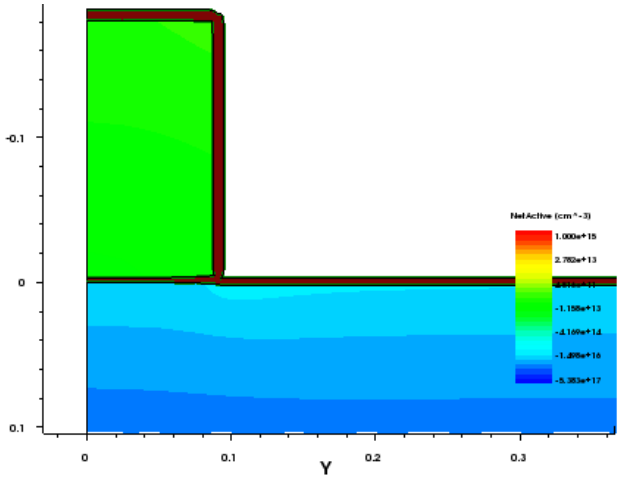
Intially a n type substrate is used with phosphorous concentration of 1015cm-3 and processed under successive stages of boron implantations, one to create a pwell, to provide retrograde doping and for Vt adjustment.

It is followed by growth of gate oxide at 850°C for 10 minutes in pure oxygen ambient.

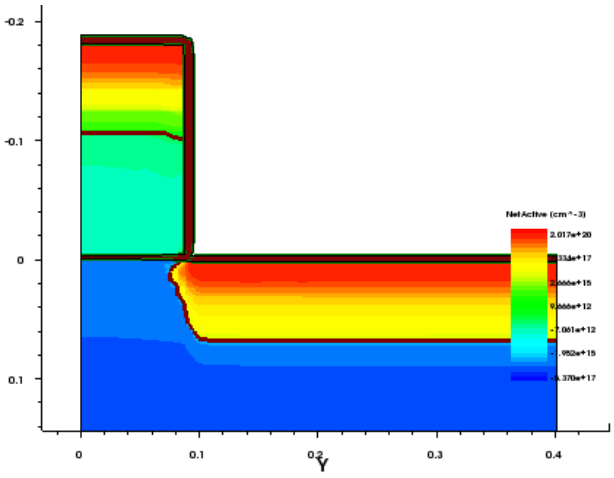
Now the polysilicon gate is created and is etched such that it remains only on the gate.

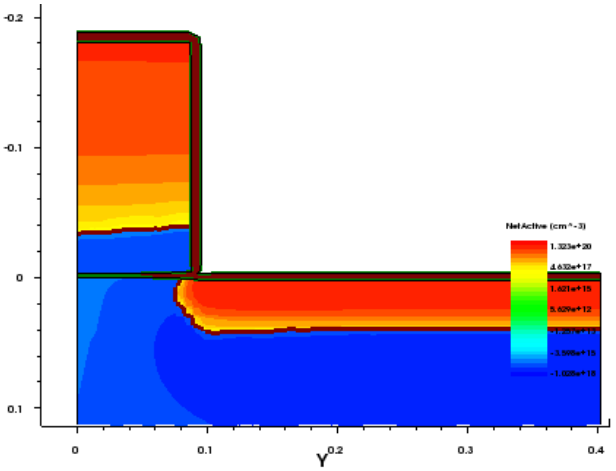


It is followed by polysilicon reoxidation which results in covering the entire surface with oxide

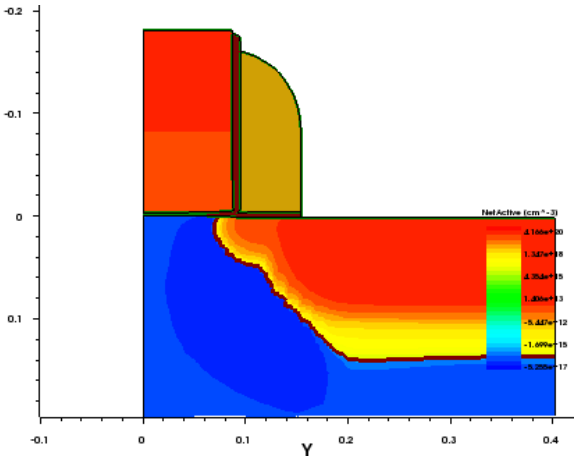


Post reoxidation, fabrication involves creation of LDD and Halo implants. Aprropriate dose, energy and diffusion temperature ensures the desirable structure.



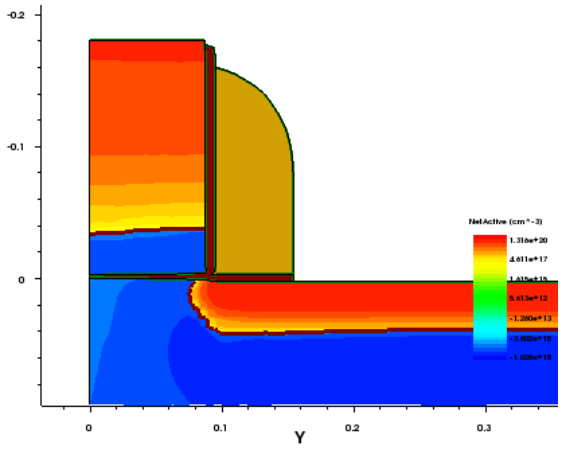


It is further followed by creation of nitride spacers and anisotropic etching is done to etch away excess of nitride and the oxide deposited during poly reoxidation.



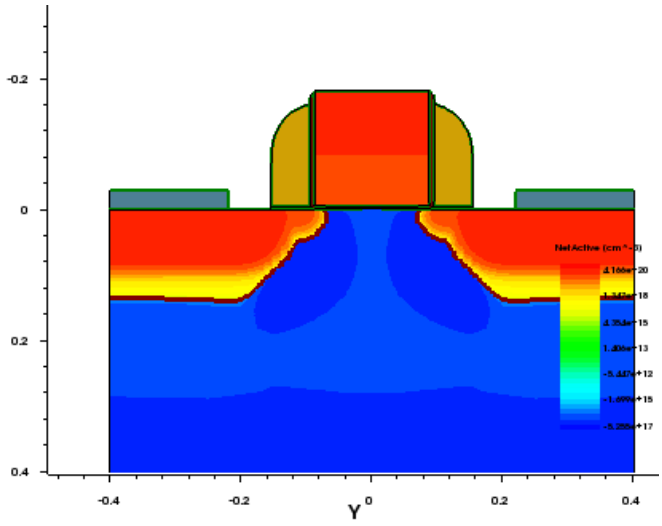
Source and drain regions are implanted using high energy and heavy dose of Arsenic which is diffused at a comparably higher temperature.

Finally metal pads are defined of Aluminium which are initially deposited and etched from undesirable places.



It is important to note that remeshing is done multiple times to get a more defined structure and to make sure ctitical regions are defined appropriately in the simulation.

Also, for the whole process in the simulation we modelled half the mosfet and in the end same is duplicated for the other side.

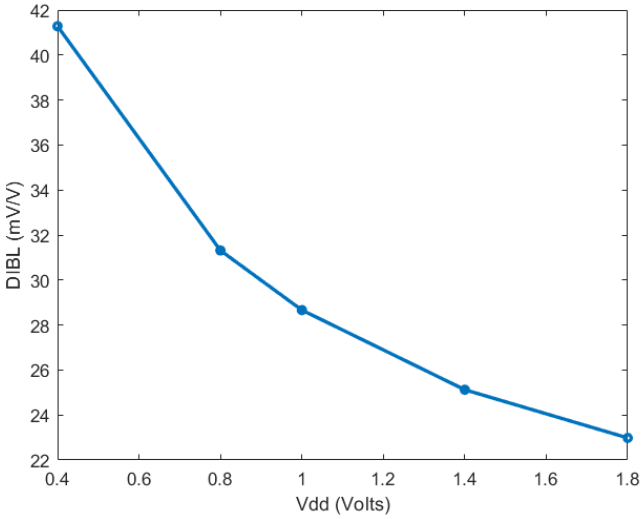


Results and Discussion:

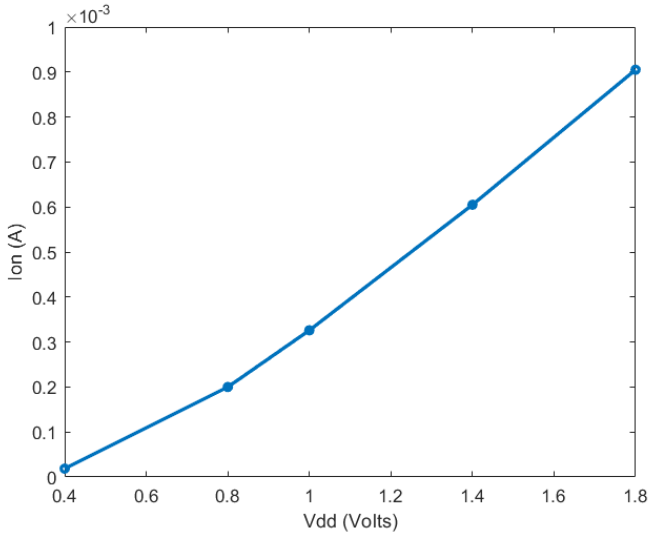
Using Inspect element to evaluate for different Vdd and to evaluate the how it affects different metrices.

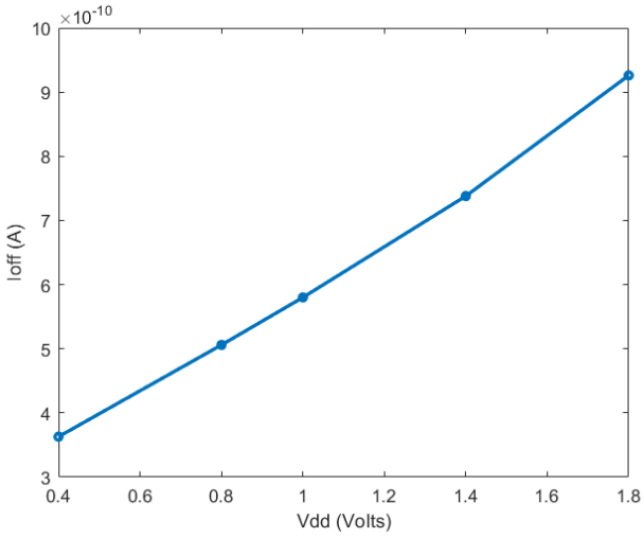
Vdd	SSsub	DIBL	Ion	Ioff	Vti	Vtgm	gm	Vgm	VtVdsat
0.4	72.394	0.04127841833	1.86E-05	3.63E-10	0.189	0.32	1.78E-04	0.397	0.177
0.8	72.738	0.03131237317	2.00E-04	5.06E-10	0.189	0.355	2.44E-04	0.591	0.167
1	72.943	0.02866330769	3.26E-04	5.80E-10	0.189	0.355	2.46E-04	0.589	0.164
1.4	73.35	0.02512318289	6.05E-04	7.38E-10	0.189	0.355	2.49E-04	0.541	0.157
1.8	73.736	0.02298251097	9.05E-04	9.26E-10	0.189	0.354	2.52E-04	0.514	0.15

DIBL increases with increase in Vdd, which is quite expected. This is because of the increase in the contribution of charge by the electric field around the drain region.

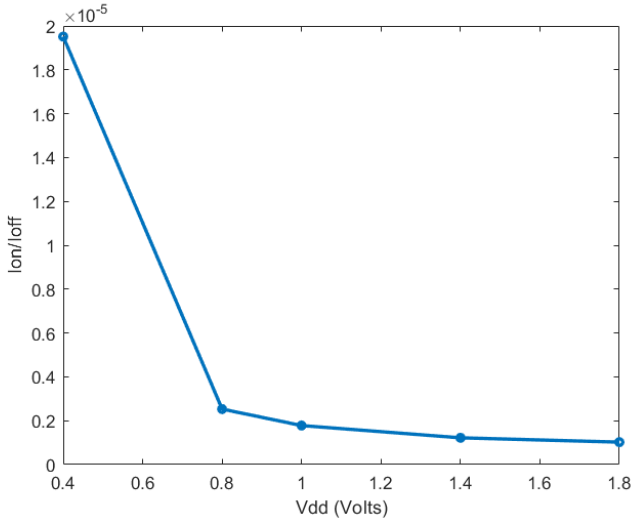


Another important metric would be Ion and Ioff

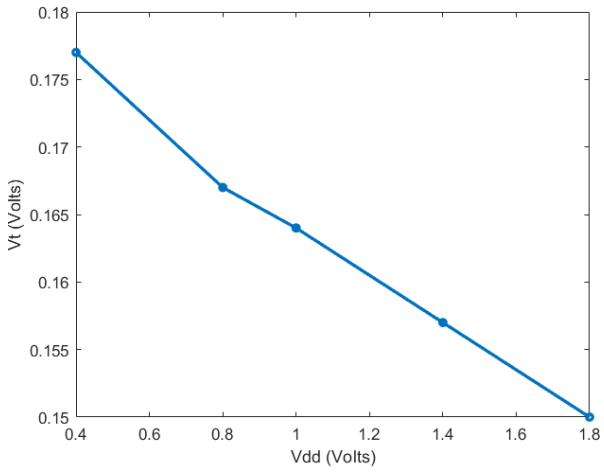




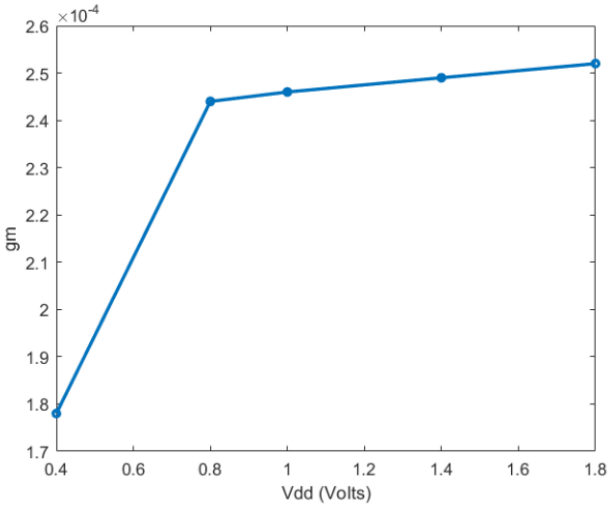
Although both increase with increase of Vdd and hence it would make much more sense visualizing the ration over the variation. It decreases as Vdd increases. Also, it seems to have a really high value in subthreshold region.Thats due to extremely low off current.

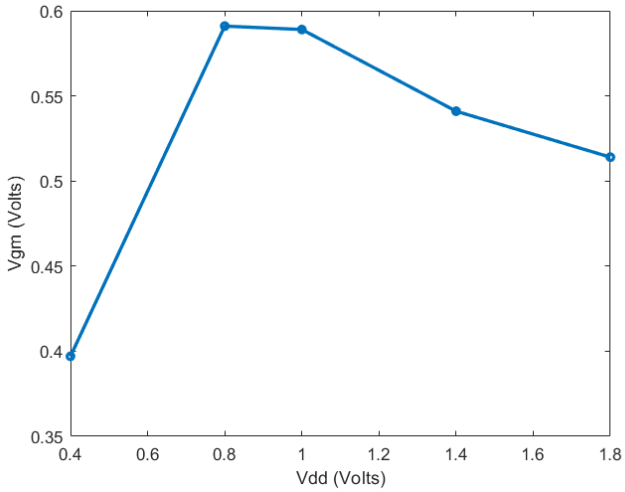


Threshold voltage decreases with increase in voltage across the source and drain. It is similar to whats expected by the DIBL as seen earlier

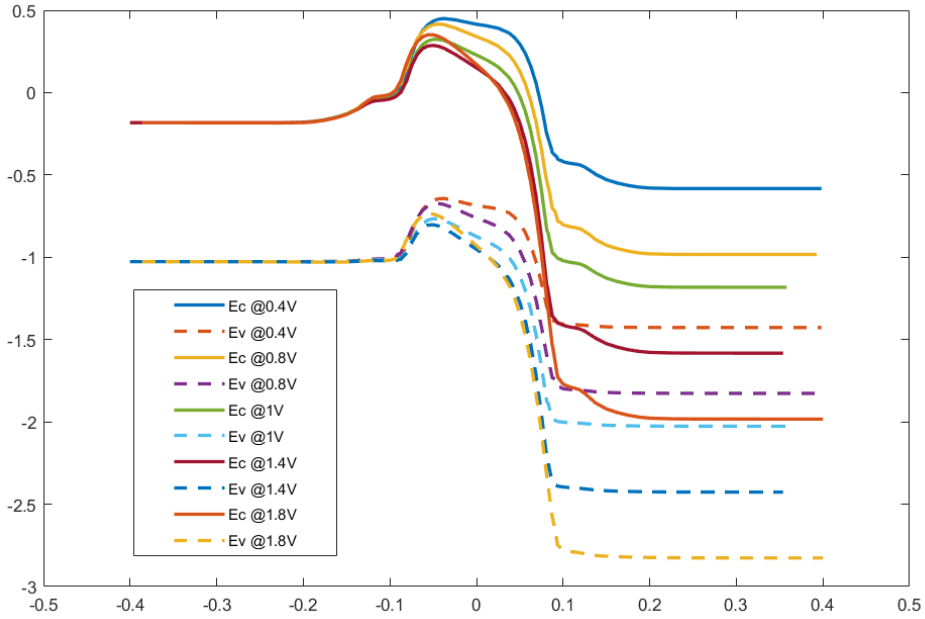


For analog applications, it is quite a necessity to know the gm and the voltages at which it achieves maximum gm. It can be seen easily that gm sees a significant value beyond 0.8 and also the voltage at which gm maximises itself decreases too.





It might also be important to visualize the band diagram to get an insight of how the energy band changes over change in Vdd. It is shown as below



Conclusion:

TSMC 180 nm technology allows the creation of a feature size limited by 180nm. Therefore, all the lateral dimensions that can be made with the fabrication process would have to be bigger than 180nm. Gate Oxide thickness is around 3-4 nm and junction depth to be around 50-74nm as decided by ITRS 1997 and for TSMC180 nm Oxide thickness is fixed over 4.1nm. Doping of Substrate and junctions are application-specific and have variation among the values. The ascertained voltage values for 180nm technology are around 1-1.8V.