EE32 Device Simulation Lab

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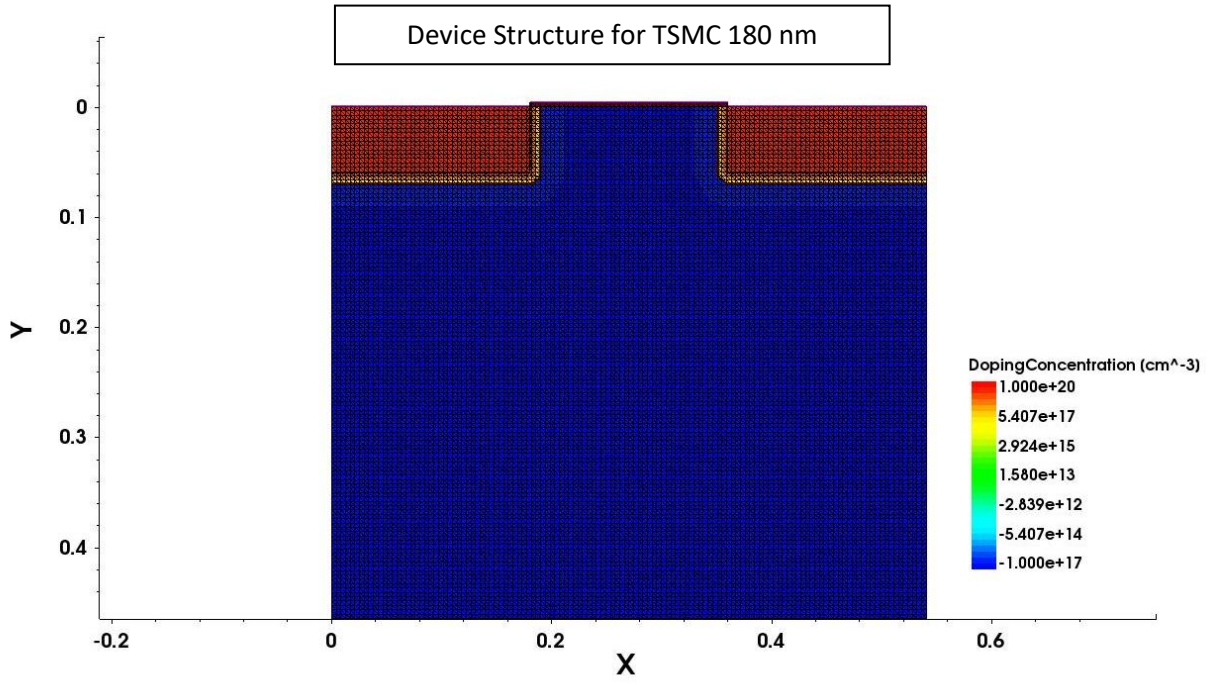
Lab 1: Design and analysis of 180-nm N-MOSFET for digital and analog applications.

Device Specifications:

Gate Length (L_G):	180nm
Silicon Thickness (T_{Si}):	500nm
Gate Oxide Thickness (T_{OX}):	4.1nm
Substrate doping:	1e+17
Source/ Drain doping:	2e+20
Gate work function:	4.3eV
Decay length:	5nm
Interface length:	1.4
Add other parameters required for the design	Junction Depth = 60nm

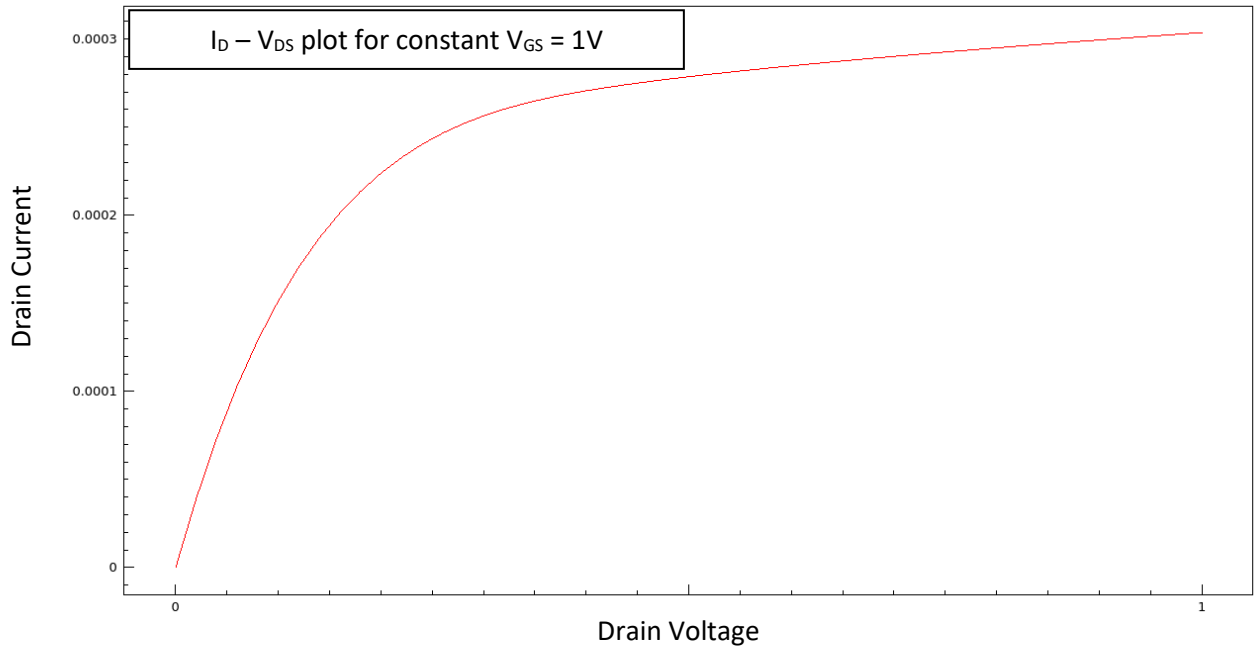
Results and Discussions:

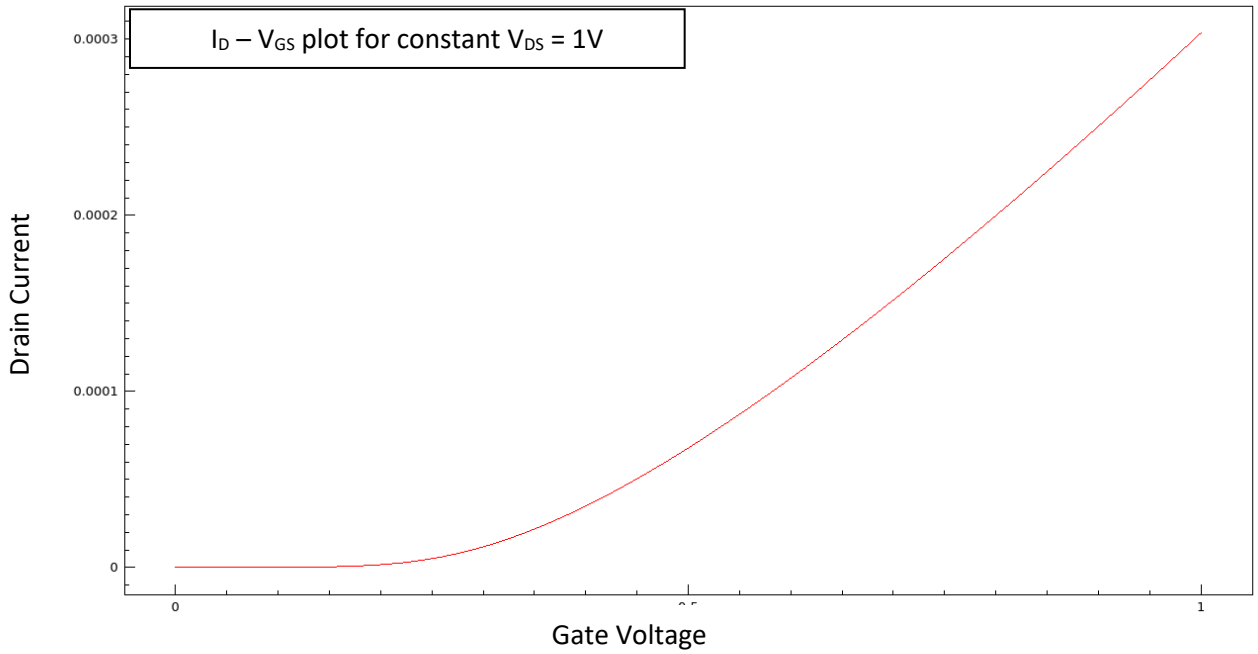
NMOS structure is created with source and drain regions of length 180nm and a channel length of 180nm too. The thickness of the substrate is taken to be 500nm. Assuming no change in other fabrication processes thus lateral diffusion and interface length are assumed to be the same.



The transfer characteristics obtained for the device are shown below. As compared to any higher technology node, operating voltages and threshold voltage are reduced. Moreover, consequently, the current is reduced too.

A saturation current of 0.322 mA is observed with a bias of 1V across the gate and 1V across source-drain junctions. Threshold voltage observed is around 0.434 V



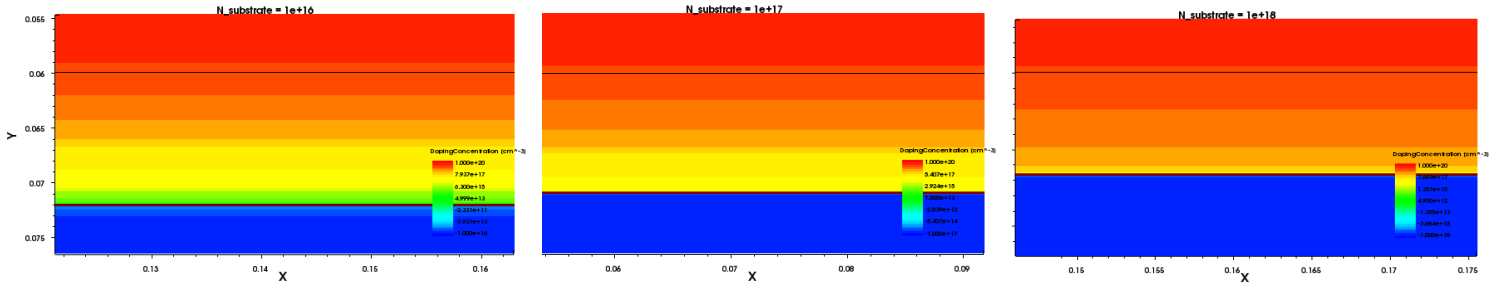


Essential Characteristics of MOS:

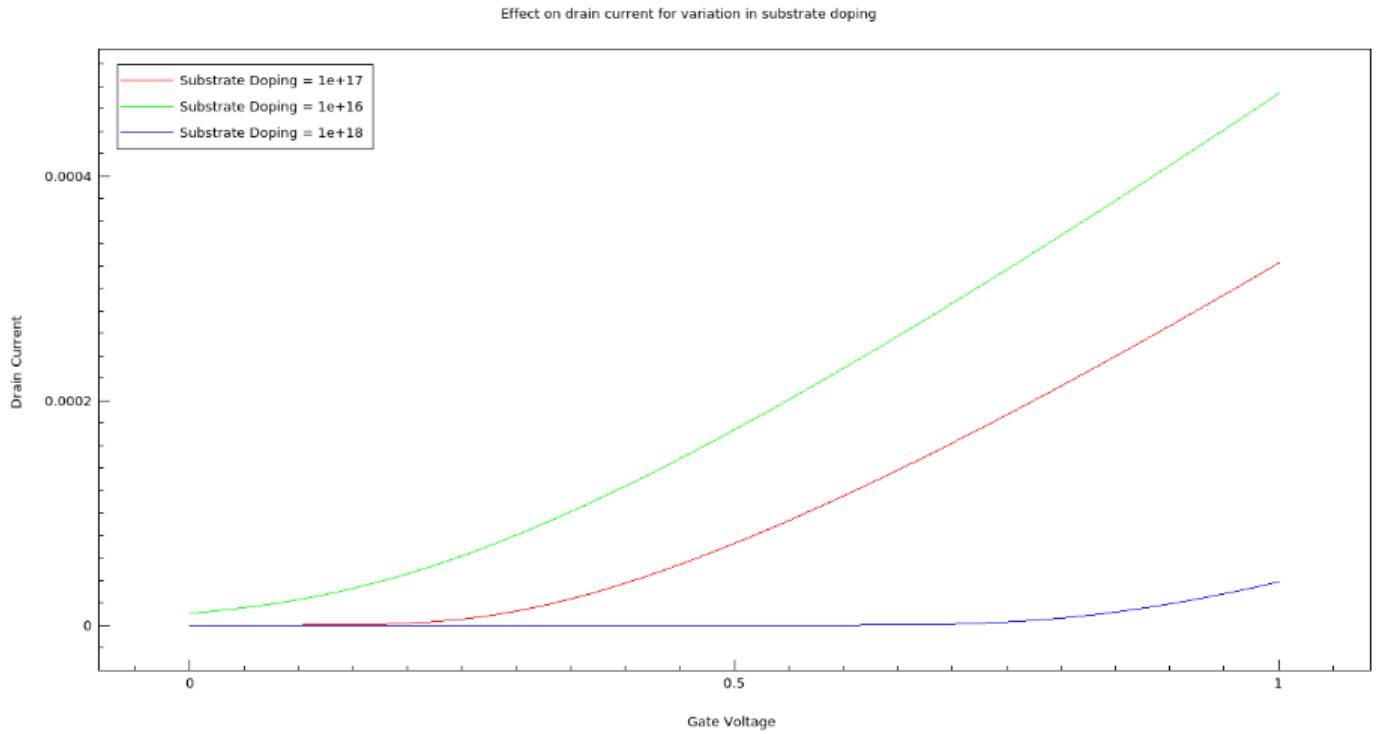
- I_{ON}/I_{OFF}: A figure of merit determining the performance of a semiconductor device. High performance is determined by higher on current and low leakage is determined by lower off current. Thus, a higher ratio is desired, and typically a higher ratio is a symbol of better gate control.
- DIBL: It determines the change in threshold voltage due to change of bias across drain/source junctions and since bias on drain should not affect the threshold voltage, ideally its zero.
- Subthreshold Slope: It is a measure of the responsiveness of the MOSFET. It determines the value of gate voltage required to change the magnitude of drain current by an order.

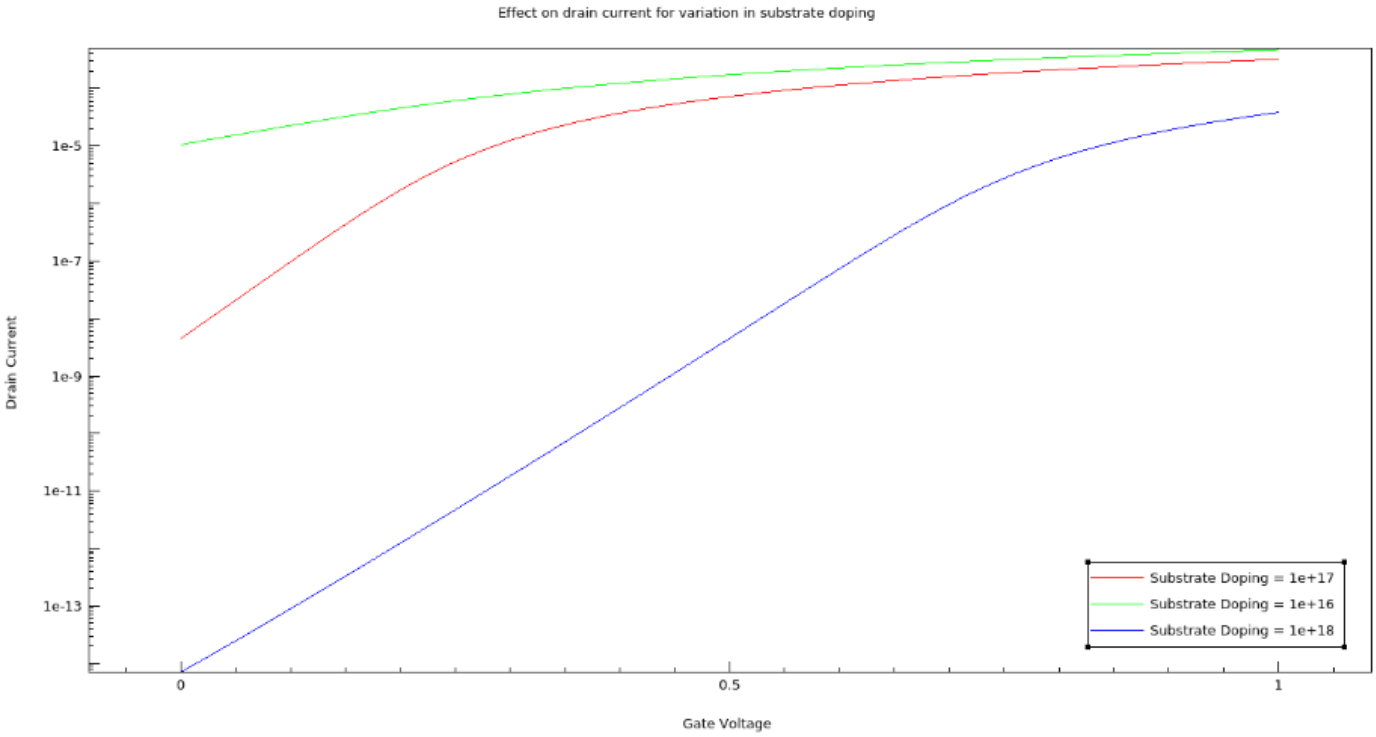
Understanding the variation of Substrate Doping:

With the increase of Substrate doping, the threshold voltage is affected as the inversion charge density is a function of the substrate doping. Also, it affects the diffusion of source and drain junctions.



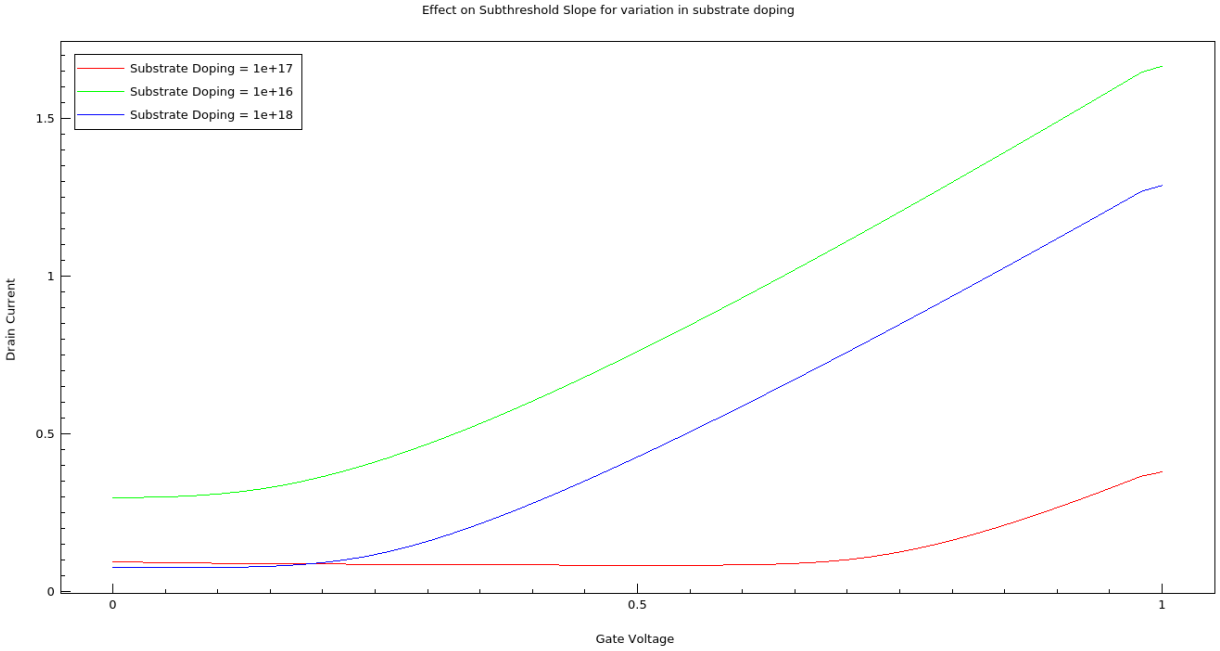
With the increase of doping density, the threshold voltage increases. Also, a highly doped substrate has very low leakage current whereas low doped substrate has higher leakage current as could be seen below.



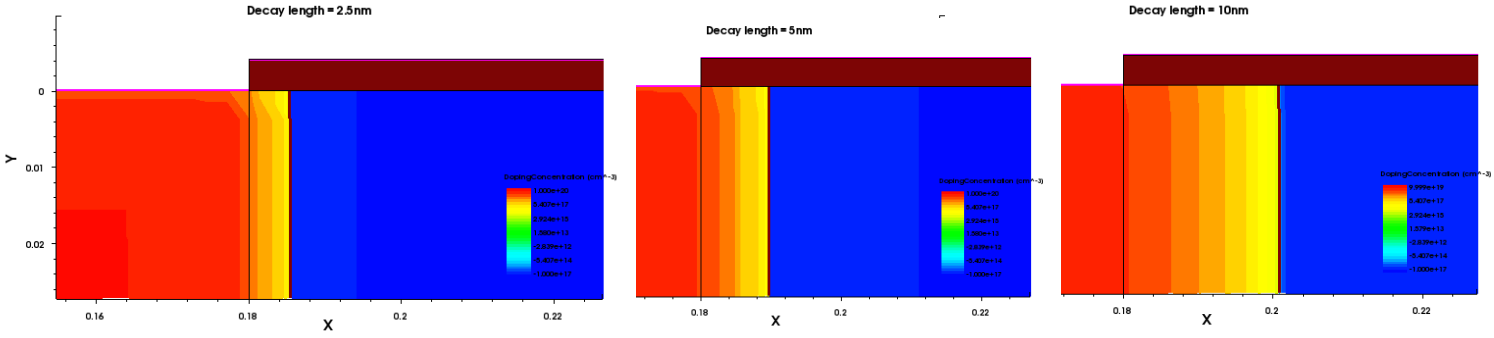


The characteristics of MOS devices based on the variation of substrate doping as listed below:

	NSUB = 10^{16}	NSUB = 10^{17}	NSUB = 10^{18}
I_{OFF} (Amp)	1.06×10^{-5}	4.53×10^{-9}	7.23×10^{-15}
I_{ON} (Amp)	4.73×10^{-4}	3.22×10^{-4}	3.8655×10^{-5}
I_{ON}/I_{OFF}	4.73×10^{1}	7.10×10^{4}	5.3×10^{9}
DIBL (mV/V)		52.22	10.33
Subthreshold Slope (mV/Dec.)	297.2	93.01	74.4

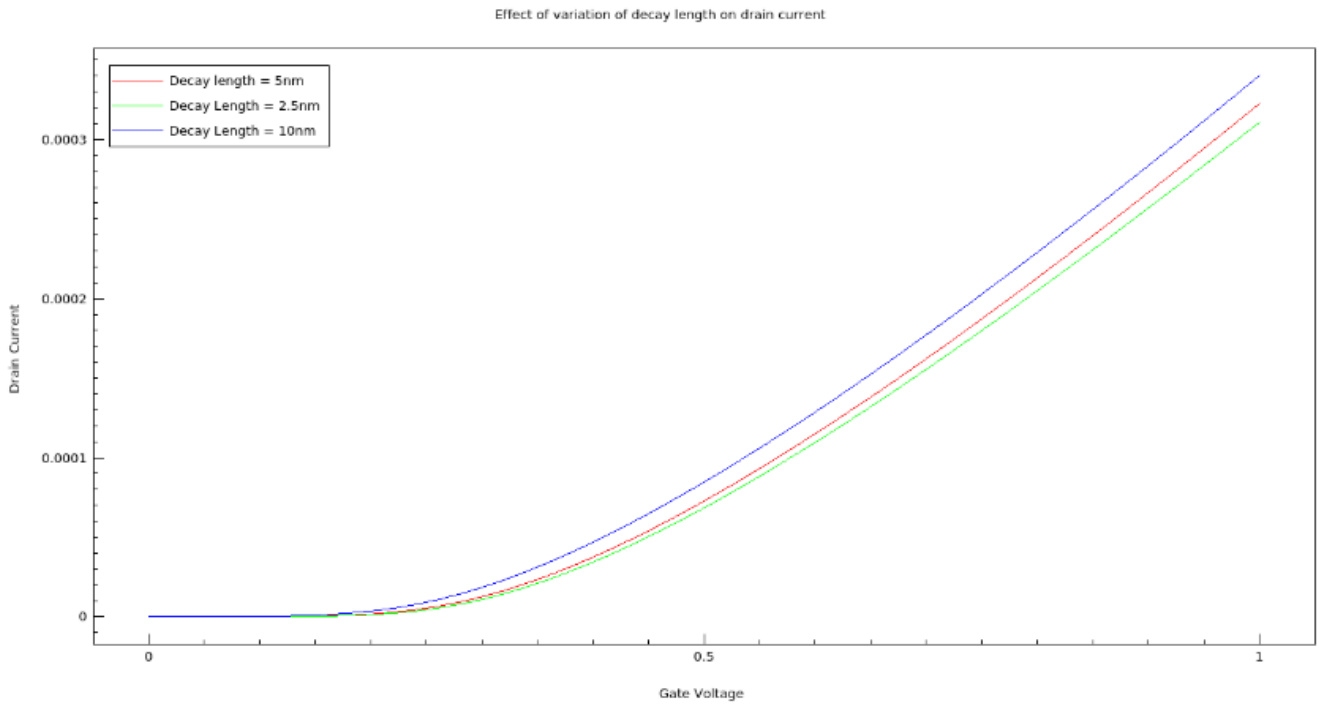


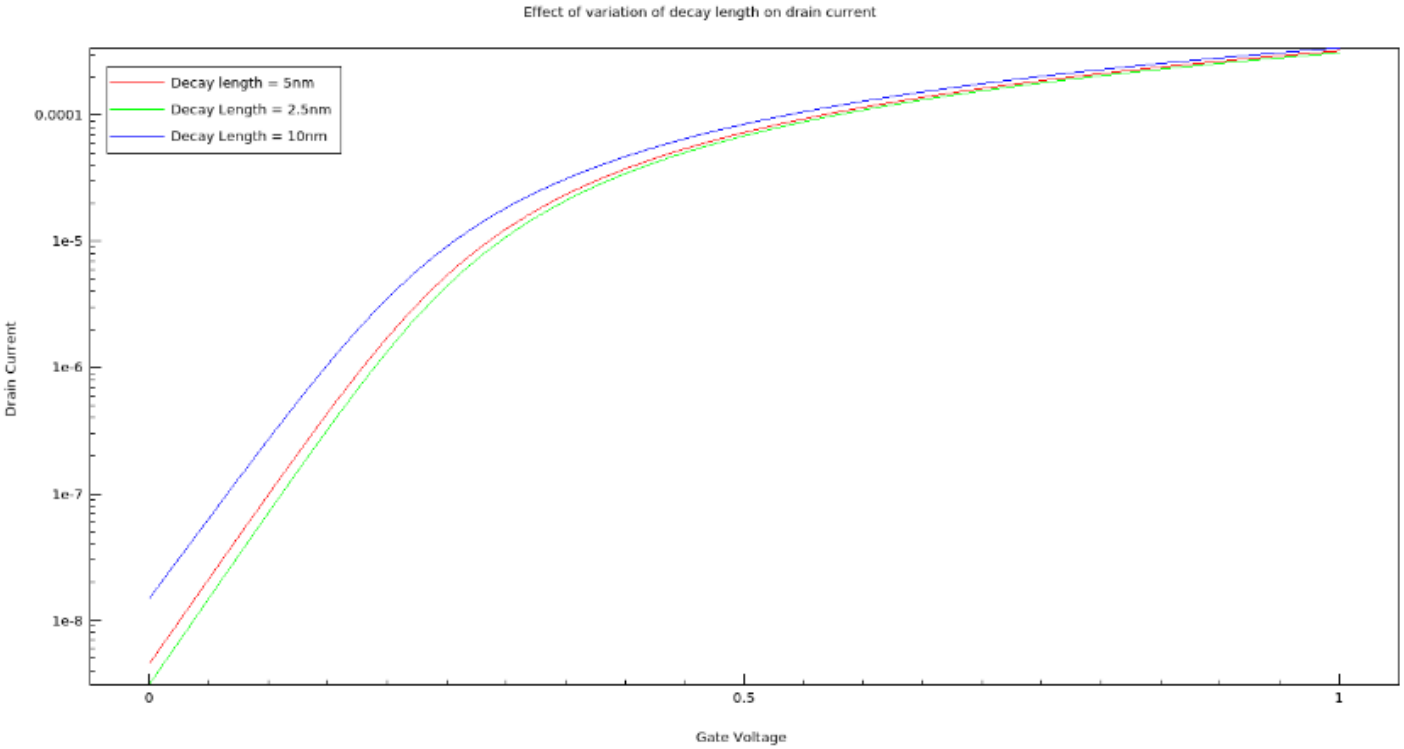
Understanding the variation of Diffusion length on Drain Current:



The profiles for different diffusion length are as shown above. As could be easily intuited, higher lateral diffusion results in more DIBL as more of the channel region is affected by the potential on the drain. Also, the threshold voltage is decreased with increasing diffusion. Furthermore, Subthreshold swing gets worse too.

However, it is significant to note that the ON current increases with an increase in lateral diffusion as channel length are reduced subsequently affecting the electrical field across the junctions too.



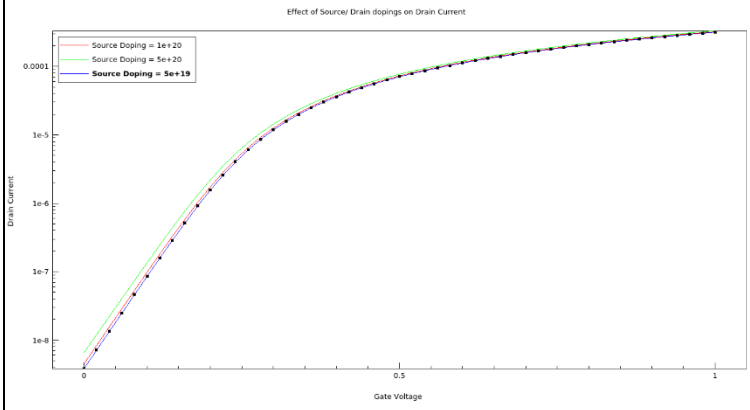


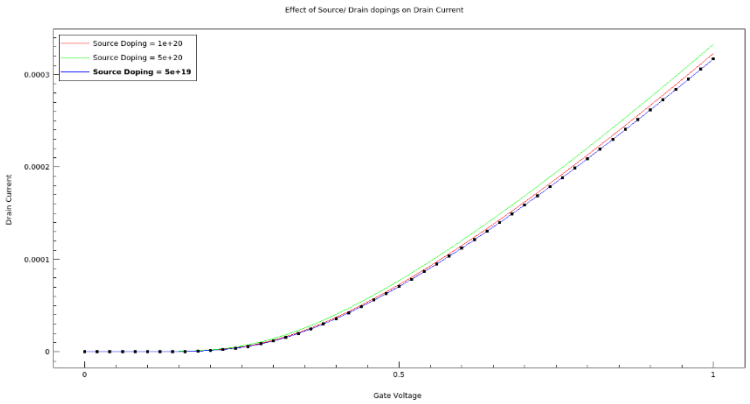
The characteristics of MOS devices based on the variation of decay length of source/drain junctions are as listed below:

	l = 2.5nm	l = 5nm	l = 10nm
I_{OFF} (Amp)	3.1×10^{-9}	4.53×10^{-9}	1.49×10^{-8}
I_{ON} (Amp)	3.11×10^{-4}	3.22×10^{-4}	3.4×10^{-4}
I_{ON}/I_{OFF}	1.003×10^{5}	7.10×10^{4}	2.28×10^{4}
DIBL (mV/V)	47.66	52.22	67.11
Subthreshold Slope	89.7	93.01	97.26

Understanding the variation of Source/ Drain doping:

Source and drain doping although do not have a powerful effect for the drain current. The associated figures of merit are listed below:





The characteristics of MOS devices based on the variation of source/drain doping is as listed below:

	S/D = 5×10^{19}	S/D = 1×10^{20}	S/D = 5×10^{20}
I_{OFF} (Amp)	3.854×10^{-9}	4.53×10^{-9}	6.575×10^{-9}
I_{ON} (Amp)	3.16×10^{-4}	3.22×10^{-4}	3.38×10^{-4}
I_{ON}/I_{OFF}	8.199×10^{5}	7.10×10^{4}	5.14×10^{4}
DIBL (mV/V)	49.8	52.22	41.10
Subthreshold Slope	90	93.01	96.6

Conclusion:

TSMC 180 nm technology allows the creation of a feature size limited by 180nm. Therefore, all the lateral dimensions that can be made with the fabrication process would have to be bigger than 180nm. Gate Oxide thickness is around 3-4 nm and junction depth to be around 50-74nm as decided by ITRS 1997 and for TSMC180 nm Oxide thickness is fixed over 4.1nm. Doping of Substrate and junctions are application-specific and have variation among the values. The ascertained voltage values for 180nm technology are around 1-1.8V.