EE32 Device Simulation Lab

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Lab 5: Design and analysis of 90-nm FD SOI using 2D process simulation

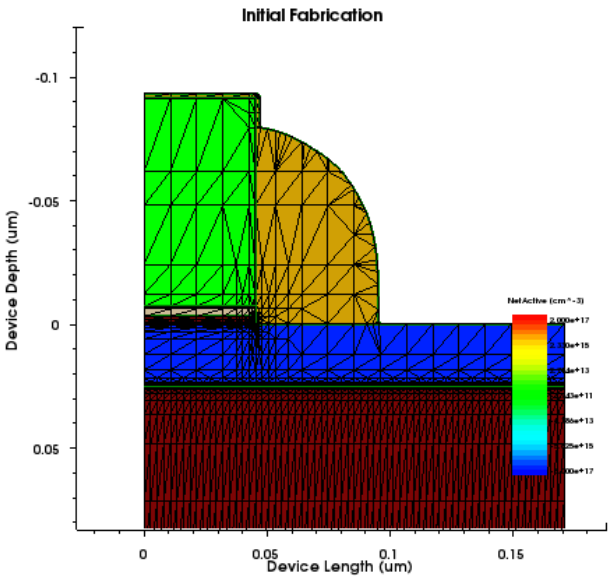
Device Specifications:

Gate Length (L_G):	90nm
Gate Oxide Thickness (T_{OX}):	3nm
Body Thickness (T_{Si}):	25nm
Box Thickness (T_{BOX}):	400nm
Spacer:	50nm
RSD Diffusion Temperature	1050° C for 1min
Add other parameters required for the design	Junction Depth = 60nm

Process Simulation:

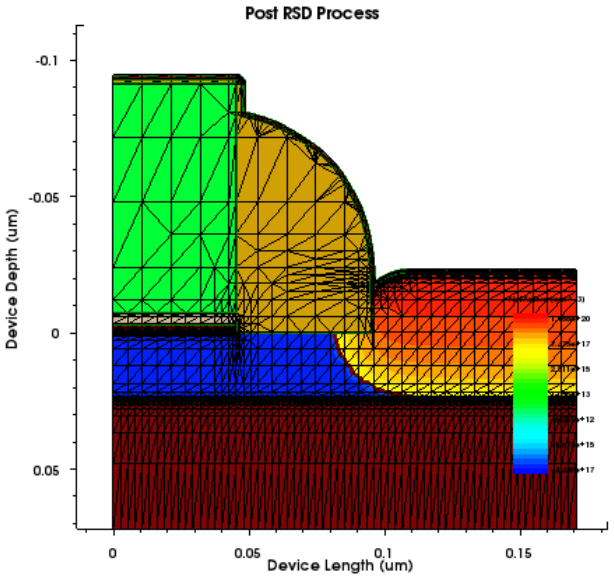
The process flow includes undoped channels, high-k ferroelectric hafnium-based dielectrics with metal gate, dual spacer for NFET and PFET, epitaxially grown strained raised source–drain (RSD) pockets, and silicidation.

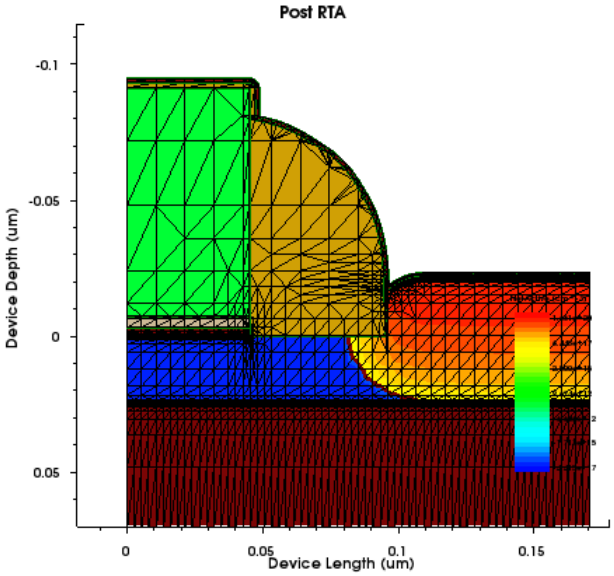
As a matter of fact in bulk technology, body-biasing is very limited due to parasitic current leakage; whereas, in FDSOI design, biasing is more efficient due to a thin buried oxide layer. Different architectures are used with back-biasing: flip wells (SLVT/LVT or low Vth) and conventional wells (RVT/HVT or high Vth) that either increase performance through forward-biasing or decrease leakage by reverse back-biasing, respectively.

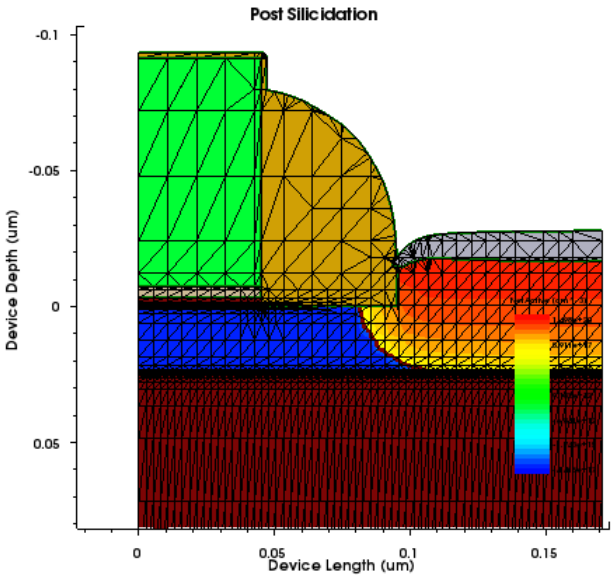


The process flow of the FDSOI MOSFET represents a generic 90-nm SOI technology node. The following key characteristics for the process flow have been chosen:

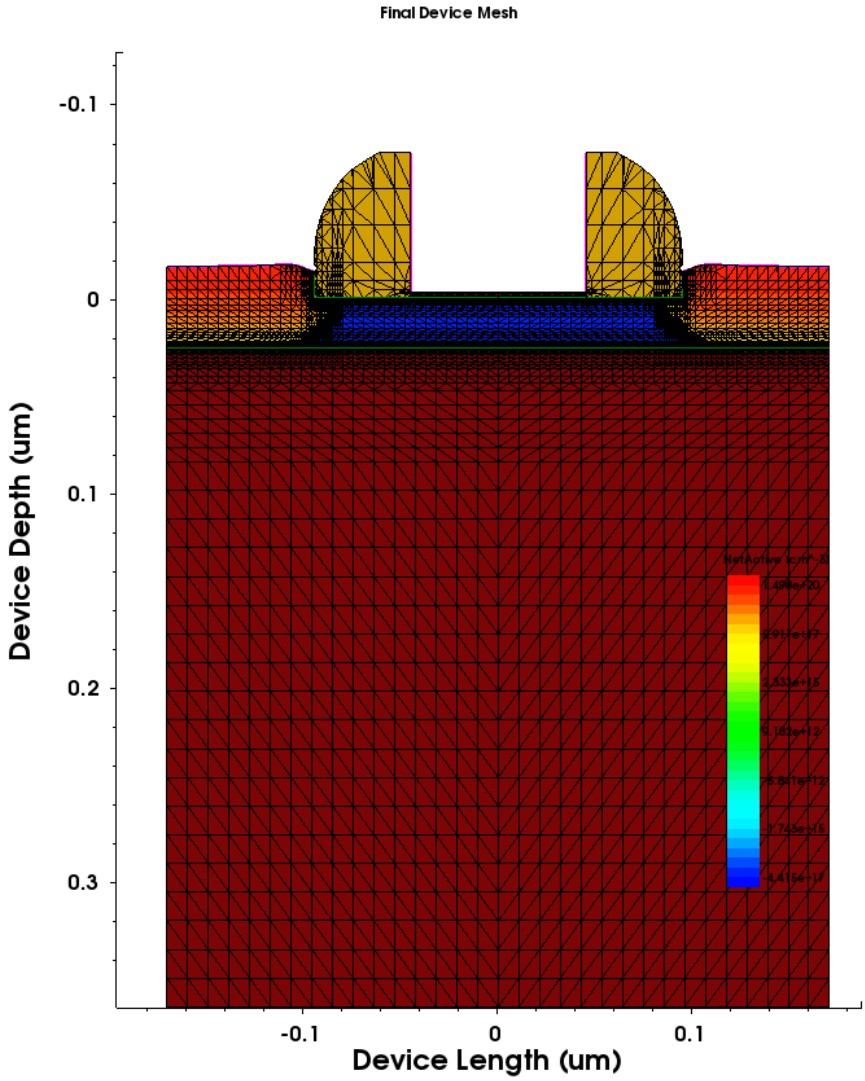
- Undoped 25 nm SOI channel formation
- Oxide and metal gate deposition
- NFET spacer formation, and *in situ* phosphorus-doped Si:C raised source–drain (RSD) epitaxial growth
- PFET spacer formation, and *in situ* boron-doped SiGe (25% Ge) RSD epitaxial growth
- Rapid thermal anneal (RTA) at 1050C
- Laser anneal for 1.0 ms and maximum temperature of 1363 C
- Nickel silicidation for contacts







The final device and the meshing designed for device simulation is as shown.

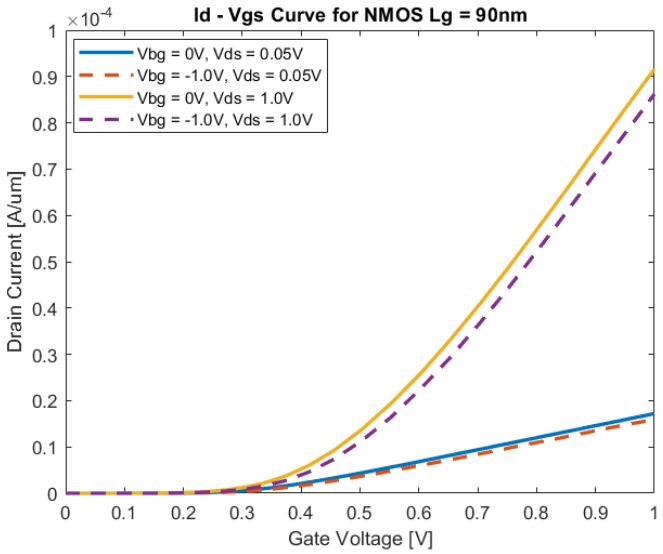


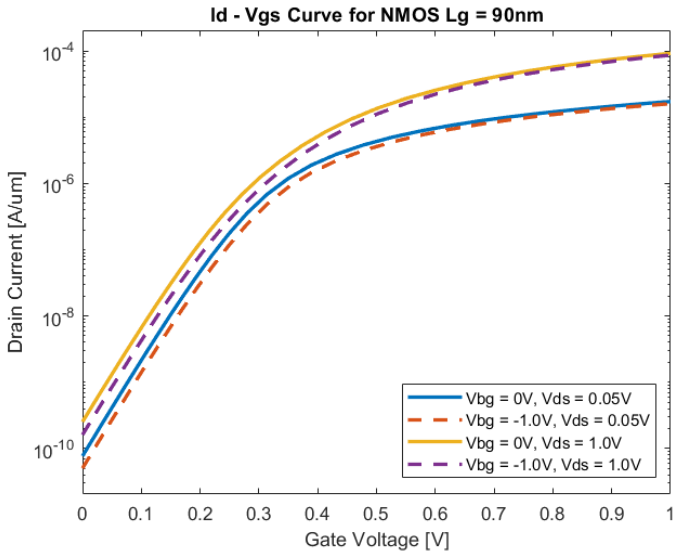
Results and Discussion:

The various parametres that can be extracted from the simulation are tabulated as bellow. The constraints for the device design have been met too.

Vbg (V)	Vtgm (V)	VtiLin (V)	IdLin (A/um)	SSlin (mV/dec)	gmLin (mho)	IdSat (A/um)	Ioff (A/um)	VtiSat (V)	SSsat (mV/dec)	gmSat (mho)	Ron (ohms)	DIBL (mV/V)	Ion/Ioff
0	0.339	0.346	1.72E-05	68.207	2.61E-05	9.16E-05	2.53E-10	0.297	69.252	1.75E-04	63027.17	51.57894737	3.62E+05
-1	0.37	0.368	1.60E-05	68.097	2.55E-05	8.62E-05	1.61E-10	0.317	69.014	1.71E-04	67196.24	53.68421053	5.35E+05

The Id-Vgs plots are as shown below:





Id-Vd achieves a variation as shown in the figure. Backgate voltage reduces the on current as well as significantly reduces the leakage current.