

Digital Logic and Design - Handwritten Style Notes

1. Half Adder

A Half Adder is a combinational circuit that adds two single-bit binary numbers (A and B). It has two outputs:

- Sum: $A \oplus B$
- Carry: $A * B$

Truth Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Used in: Basic binary addition.

2. Full Adder

A Full Adder is a digital circuit that adds three binary bits: A, B, and Cin (carry in). It produces:

- Sum = $A \oplus B \oplus C_{in}$
- Carry = $(A * B) + (B * C_{in}) + (A * C_{in})$

Truth Table:

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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Used in: Multi-bit binary adders.

3. Encoder

An Encoder is a digital circuit that converts 2^n input lines into n output lines. It performs the reverse operation of a Decoder.

Example: 4-to-2 Encoder

Inputs: D0, D1, D2, D3

Outputs: A, B

Truth Table:

D0	D1	D2	D3	A	B
0	0	0	1	1	1
0	0	1	0	1	0
0	1	0	0	0	1
1	0	0	0	0	0

Used in: Keyboards, Priority Encoders.

4. Decoder

A Decoder is a circuit that converts n input lines to 2^n output lines. It is used to activate one unique output line based on the input combination.

Example: 2-to-4 Decoder

Inputs: A, B

Outputs: Y0, Y1, Y2, Y3

Truth Table:

A	B	Outputs
0	0	Y0 = 1

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0 1 | Y1 = 1

1 0 | Y2 = 1

1 1 | Y3 = 1

Used in: Memory address decoding, I/O selection.

5. Multiplexer (MUX)

A Multiplexer selects one of many input signals and forwards it to a single output line. It uses selection lines to choose the input.

Example: 4-to-1 MUX

Inputs: I0, I1, I2, I3

Select lines: S0, S1

Output: Y

$$Y = (I0 \text{ AND } \sim S1 \text{ AND } \sim S0) + (I1 \text{ AND } \sim S1 \text{ AND } S0) + (I2 \text{ AND } S1 \text{ AND } \sim S0) + (I3 \text{ AND } S1 \text{ AND } S0)$$

Used in: Data routing, Communication systems.

6. De-Multiplexer (DEMUX)

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A De-Multiplexer takes a single input and routes it to one of several output lines. It is the reverse of a Multiplexer.

Example: 1-to-4 DEMUX

Inputs: Data (D), Select Lines (S0, S1)

Outputs: Y0, Y1, Y2, Y3

$$Y0 = D \text{ AND } \text{NOT}(S1) \text{ AND } \text{NOT}(S0)$$

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$Y1 = D \text{ AND } \text{NOT}(S1) \text{ AND } S0$

$Y2 = D \text{ AND } S1 \text{ AND } \text{NOT}(S0)$

$Y3 = D \text{ AND } S1 \text{ AND } S0$

Used in: Data distribution, Memory writing, Communication channels.