EnggTree.com

Reg. No. : E N G G T R E E . C O M

Question Paper Code : 50897

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024

Third Semester

Computer Science and Engineering

For More Visit our Website
EnggTree.com

CS 3351 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design / Computer Science and Engineering (Artificial Intelligence and Machine Learning) / Computer Science and Engineering (Cyber Security) / Computer and Communication Engineering / Artificial Intelligence and Data Science / Computer Science and Business Systems / Information Technology)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is combinational circuit?
2. Which combinational circuit is otherwise known as data selector? Why?
3. Write down the characteristic table of T flip flop.
4. Compare Mealy and Moore Models.
5. What is the difference between register addressing mode and register indirect addressing mode?
6. What is data transfer instruction? Specify any two data transfer instructions.
7. What is pipelining?
8. Differentiate: Hardwired Control and Microprogrammed Control.
9. Can a computer work without cache? Justify.
10. What is the purpose of SATA?

Downloaded from EnggTree.com

EnggTree.com

PART B — (5 × 13 = 65 marks)

11. (a) Why do we need a code conversion? Explain with the conversion of binary to gray code.

Or

(b) Identify the combinational circuit that is used to compare the relative magnitude of two binary numbers. Construct the identified circuit for comparing 2-bit binary numbers.

12. (a) Which flip flop is called as data flip flop? Explain the operation of the same with its circuit diagram, characteristic table and excitation table.

Or

(b) Which counter is called decade counter? Why? Explain the operation of the same in asynchronous mode.

13. (a) Explain Von Neumann Architecture with neat sketch.

Or

(b) Describe any five addressing modes with examples.

14. (a) Draw a simple MIPS data path with control unit and explain the execution of ALU instruction.

Or

(b) Describe the methods for avoiding the control hazards.

15. (a) Explain in detail the memory hierarchy with neat diagram.

Or

(b) Explain in detail about Direct Memory Access (DMA) with neat diagram.

PART C — (1 × 15 = 15 marks)

16. (a) Design a Mod-5 Synchronous Counter using JK flip flop.

Or

(b) Design 8 × 1 MUX. Implement the following Boolean function using 8 × 1 MUX $F(P,Q,R,S) = \sum m(0,1,3,4,8,9,15)$.

Downloaded from EnggTree.com

EnggTree.com

Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 20864

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023

Third Semester

Computer Science and Engineering

For More Visit our Website
EnggTree.com

CS 3351 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design / Computer Science and Engineering (Artificial Intelligence and Machine Learning) / Computer Science and Engineering (Cyber Security) / Computer and Communication Engineering / Artificial Intelligence and Data Science / Computer Science and Business Systems and Information Technology)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write down the sum and carry expressions for half adder.
2. How many selection inputs, data inputs and output for 16 X 1 MUX?
3. What is shift register? List its types.
4. How many flip flops are required for designing BCD counter? Justify.
5. List the functional units of a digital computer.
6. Interpret the Instruction Set Architecture.
7. What is program counter?
8. When do data hazards occur in pipelining?
9. What is memory hierarchy?
10. Differentiate write back and write through.

Downloaded from EnggTree.com

EnggTree.com

PART B — (5 × 13 = 65 marks)

11. (a) Explain full adder and full subtractor with the help of circuit diagrams.

Or

(b) Explain binary to octal decoder and octal to binary encoder with the help of circuit diagrams.

12. (a) Describe J-K and D flip flops with the help of block diagrams and characteristic tables.

Or

(b) Explain Mealy and Moore Models with the help of block diagrams.

13. (a) Explain about any four addressing modes with example.

Or

(b) Describe Instruction sequencing and branching with examples.

14. (a) Depict how instruction is being fetched and executed through the data path in the processor?

Or

www.EnggTree.com

(b) Describe data hazards and control hazards. Explain with suitable techniques, how these hazards can be mitigated?

15. (a) Explain how memory mapping techniques are useful for finding the memory blocks in cache?

Or

EnggTree.com

(b) How virtual addresses are translated into physical addresses? Explain it with the help of virtual memory organization and page translation.

PART C — (1 × 15 = 15 marks)

16. (a) Using K – Map, find the sum of products and product of sums for the given function $F = \sum_m (0,2,6,7,8,10,12,14,15)$.

Or

(b) Design a Mod – 7 synchronous counter using J – K flip flop.

Downloaded from EnggTree.com