DESIGN OF SINGLE-STAGE DIFFERENTIAL AMPLIFIER

The domain of the Project

Analog Mixed-Signal (AMS) Design

Under the guidance of

Mr. Karnati Prudhvi kumar (Silicon Design Engineer 2)

By

Mr. Billakurthi Veera Manikanta Reddy (B.Tech ECE, 4th year)

Period of the project

November 2024 to July 2025

SURE TRUST

PUTTAPARTHI, ANDHRA PRADESH

Declaration

The project titled **"Design of Single-Stage Differential Amplifier"** has been mentored by **Mr. Karnati Prudhvi kumar**, organised by SURE Trust, from November 2024 to July 2025, for the benefit of the educated unemployed rural youth for gaining hands-on experience in working on industry relevant projects that would take them closer to the prospective employer.

I Mr. **Billakurthi Veera Manikanta Reddy**, hereby declares that I have solely worked on this project under the guidance of my mentor. This project has significantly enhanced my practical knowledge and skills in the domain.

Name **Signature**

Mr. Billakurthi Veera Manikanta Reddy

Mentor **Signature**

Mr. Karnati Prudhvi kumar
Silicon Design Engineer 2— AMD

Seal and Signature

Prof. Radhakumari
Executive Director & Founder
SURE Trust

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Executive Summary

This project focuses on the design and simulation of a single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso, a widely used industry-grade AMS design tool. The main objective was to develop a high-performance analog amplifier block suitable for mixed-signal integrated circuits, meeting specific design specifications and performance criteria.

The amplifier was designed to operate within an input common-mode range (ICMR) of 0.8V to 1.6V, achieving a voltage gain of approximately 40dB and a gain-bandwidth product of 5MHz. These specifications were carefully targeted to ensure the amplifier meets the requirements for moderate-speed analog signal amplification in low-power mixed-signal applications.

Throughout the design process, various stages including biasing, transistor sizing, DC operating point analysis, AC gain simulation, and frequency response evaluation were performed. The design was verified through SPICE-level simulations to validate its performance under different operating conditions and process corners.

The key finding of this work is that a well-optimized differential amplifier using a simple single-stage topology can still deliver stable gain, wide bandwidth, and acceptable input range, making it a suitable candidate for front-end analog blocks in many AMS systems.

Introduction

Background and Context

In modern analog and mixed-signal (AMS) integrated circuit design, differential amplifiers play a crucial role as foundational building blocks. They are commonly used in operational amplifiers, analog front ends, data converters, and sensor interfaces, where high gain, noise immunity, and common-mode rejection are essential. With the continuous scaling of CMOS technology, designing analog circuits in deep submicron nodes like 90nm has become increasingly challenging. Parameters such as device mismatch, low intrinsic gain, and short-channel effects must be carefully addressed. At the same time, there is growing demand for compact, power-efficient analog blocks that can operate reliably within limited voltage headroom.

This project was initiated to explore the design of a single-stage differential amplifier using 90nm CMOS technology, aiming to strike a balance between performance, simplicity, and area efficiency. By designing and simulating the amplifier in Cadence Virtuoso, this project also provides hands-on exposure to industry-standard AMS design flow, including schematic design, biasing, transistor sizing, and SPICE-level simulation.

Problem Statement / Project Goals

In today's electronics, especially in analog and mixed-signal systems, there's a constant need for amplifiers that are not only compact and power-efficient but also capable of handling real-world signal variations with precision. One of the most fundamental and widely used components in such systems is the differential amplifier—it forms the heart of many analog building blocks like op-amps, comparators, and sensor interfaces.

With technology scaling down to 90nm and below, designing analog circuits has become more challenging. Effects like lower intrinsic gain, reduced voltage headroom, and device mismatches can significantly impact performance. This makes it important to explore how well we can still meet performance requirements using simpler, single-stage designs. The goal of this project is to design a single-stage differential amplifier using 90nm CMOS technology, targeting the following:

1. A **voltage gain of around 40 dB with a gain-bandwidth of 5 MHz**, making it well-suited for moderate-speed analog signal amplification tasks.
2. An **input common-mode range (ICMR) of 0.8V to 1.6V**, allowing flexible signal operation.

Scope

This project focuses on the design and simulation of a single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso. The design emphasizes achieving specific performance goals such as:

1. A voltage gain of approximately 40 dB
2. A gain-bandwidth product of 5 MHz
3. An input common-mode range (ICMR) between 0.8V and 1.6V

The amplifier is intended for use in analog front-end blocks, sensor interfaces, and moderate-speed mixed-signal systems. The project covers schematic design, biasing, small-signal analysis, and SPICE-level simulations, offering practical insights into analog circuit behavior at the transistor level.

Limitation

While the design meets its primary objectives, there are certain limitations to be noted:

1. The amplifier is not layout-verified, meaning parasitic effects from physical design are not considered.
2. The project focuses on a single-stage topology, which may not provide sufficient gain or output swing for all high-performance applications.
3. The design is tested only under typical process corners, without extensive PVT (Process-Voltage-Temperature) variation checks.

Innovation

1. **Technology-aware design:** The amplifier was specifically designed for the 90nm CMOS node, accounting for short-channel effects and lower intrinsic gain, which are common limitations in modern technology nodes.
2. **Performance-focused transistor sizing and biasing**: Careful adjustment of W/L ratios and bias currents was done to achieve the target gain and bandwidth without cascading multiple stages, proving that high gain (~40 dB) can still be achieved in a single-stage architecture.

Project Objectives

Project Objectives and Outcomes

1. Design and simulate a single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso, targeting a **voltage gain of 40 dB**.

   Outcome: Successfully achieved a voltage gain of 39.83 dB validating the design through SPICE-level simulations.

2. The **Gain-Bandwidth Product (GBW)** defines the frequency at which an amplifier's gain drops to 1. A target GBW of **5 MHz** was chosen to support moderate-speed analog applications. This ensures the amplifier can handle dynamic signal changes without distortion. Careful sizing and biasing were used to meet this specification.

   Outcome: The final design achieved a gain-bandwidth of 4.8 MHz, which is close to the desired value and suitable for reliable signal amplification.

3. The target **Input Common-Mode Range (ICMR)** was set between **0.8V and 1.6V** to ensure flexible signal handling.

   Outcome: The designed amplifier successfully operated within this range of 0.099 to 1.17 (V) range, maintaining stable performance and proper biasing throughout.

Deliverables

- Schematic design of a single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso.
- SPICE-level simulations including DC analysis, AC gain, frequency response, and ICMR verification.
- Performance summary showing achieved gain, gain-bandwidth, and input common-mode range.
- Documentation of design methodology, results, and analysis in the final project report..

Methodology and Results

Methods/Technology Used

1. **Cadence Virtuoso**: Used for schematic design, biasing, and circuit simulation.
2. **90nm CMOS Technology**: Target process node for designing and analyzing the amplifier.
3. **SPICE-Level Simulation (Spectre)**: Performed DC, AC, and frequency response analysis for accurate performance verification.
4. **Analog Design Techniques**: Applied small-signal analysis, transistor sizing, and current mirror biasing.
5. **Performance Evaluation**: Focused on key metrics like voltage gain, gain-bandwidth product, and ICMR.

Tools/Software Used

1. **Cadence Virtuoso** – For schematic design and analog simulation.
2. **Spectre Simulator** – For SPICE-level circuit simulations (DC, AC, transient).
3. **90nm CMOS PDK** – Process Design Kit used for technology-specific transistor modeling.
4. **ADE (Analog Design Environment)** – For setting up and running simulation testbenches.
5. **Virtuoso Visualization Tool** – For plotting and analyzing waveforms and simulation results.

Project Architecture

The architecture of this project is centered around the design of a single-stage differential amplifier using 90nm CMOS technology, built and simulated in Cadence Virtuoso. The design aims to provide high gain, wide input common-mode range (ICMR), and adequate bandwidth, making it suitable for analog front-end applications.

1. **Differential Pair (Input Stage):** At the heart of the amplifier lies a differential pair of NMOS transistors, which receive two input signals — typically a signal and its complement. This configuration allows the amplifier to amplify the difference between the two inputs while rejecting common-mode noise, a key feature in analog and mixed-signal designs.

2. **Current Source Biasing:** A current source is connected to the tail of the differential pair to provide a constant bias current. This current defines the transconductance of the input stage and ensures the amplifier operates in the saturation region, where MOSFETs behave linearly for small signals. The tail current source plays a critical role in setting the operating point and improving linearity and common-mode rejection.

3. **Output Node:** The output is taken from one side of the differential pair. It provides an amplified version of the differential input signal. This output can be fed into further analog stages such as buffers or additional gain stages, depending on the application.

A current mirror load is used at the top to convert the differential signal into a single-ended output while providing gain. The biasing circuit sets the operating point of the amplifier and ensures stable performance across the desired input range (ICMR).
This simple yet effective architecture allows the amplifier to achieve:

1. High voltage gain (close to 40 dB)
2. Operation across a wide input common-mode range (0.099V to 1.17V)
3. A moderate gain-bandwidth product (around 4.8 MHz)

The entire design was implemented and simulated in **Cadence Virtuoso**, using **SPICE-level analysis** to fine-tune and validate each component of the architecture.

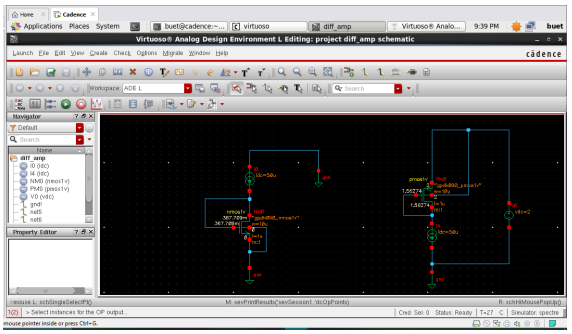

Fig-1: Circuit set-up for finding "βreff" values of nMos, pMos

In MOSFET-based analog circuit design, especially in technologies like 90nm CMOS, one of the most critical steps is determining the correct W/L ratio (width-to-length ratio) of the transistors. The W/L ratio directly influences important parameters like transconductance (gm), drain current (Id), and gain, and it must be carefully calculated to meet design specifications.
βreff = μ × Cox × (W/L)
Where: **μ** is the **carrier mobility**, **Cox** is the **oxide capacitance per unit area, W and L** are the transistor **width and length**.

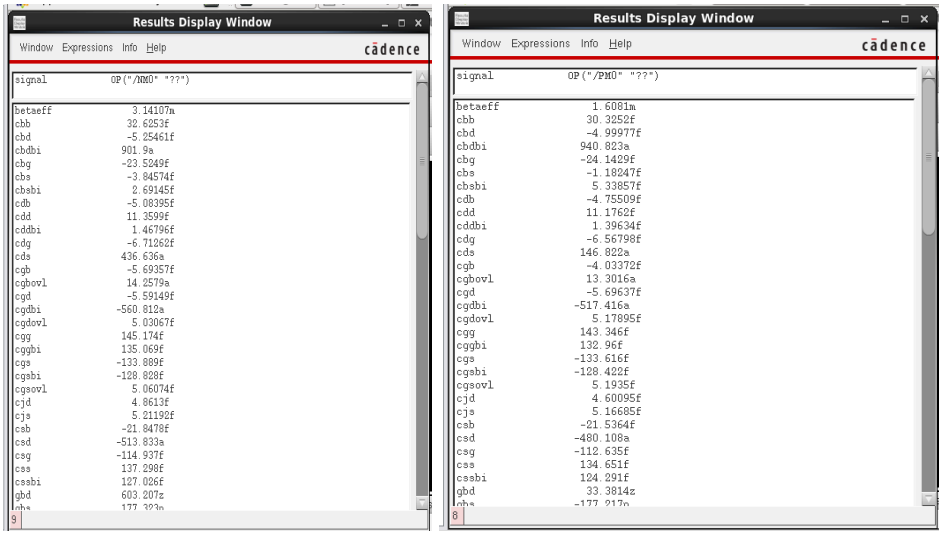

Fig-2: Above are the simulated results obtained for **βreff** in Virtuoso

Final Project and Working Screenshots

- **Differential Amplifier Setup and AC Analysis**

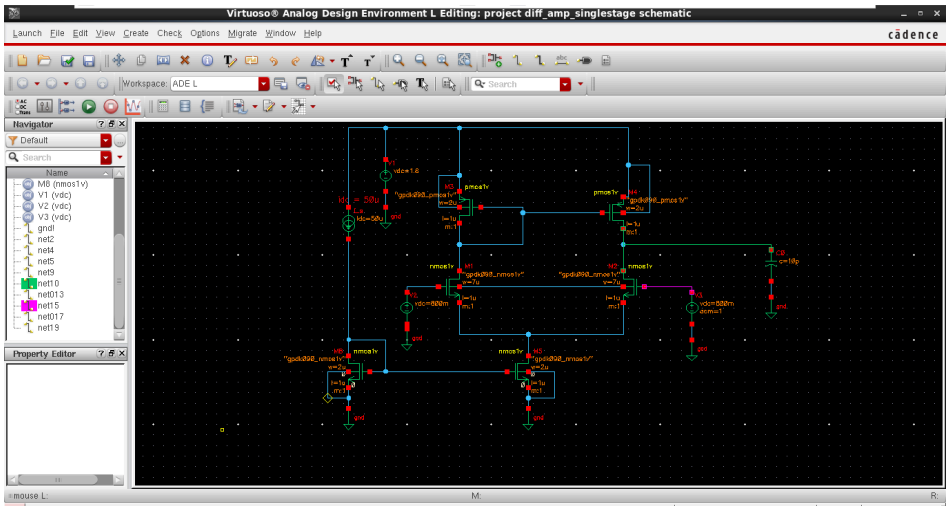

Fig-3: **Circuit connection for AC Analysis**

To analyze the frequency response and gain behavior of above designed single-stage differential amplifier circuit, an AC analysis was performed using Cadence Virtuoso. The amplifier consists of a differential pair of NMOS transistors at the input, a current mirror load using PMOS transistors, and a tail current source for biasing. A DC power supply (VDD) is provided at the top, typically set to 1.8V, as per 90nm technology standards. Proper biasing circuits were included to ensure all transistors operate in the

saturation region, which is essential for achieving linear amplification. For AC analysis, a small-signal AC voltage source was applied to one of the inputs (usually with 1V AC magnitude), while the other input with normal voltage level to establish differential operation. The output was taken from the drain of one input transistor. A suitable load was added if required to replicate real-world conditions. In ADE (Analog Design Environment), an AC analysis was set up with a frequency sweep ranging from 1 Hz to 10 MHz. The simulation plotted the AC gain (Vout/Vin) in both dB and phase across frequency. The observed voltage gain was around 39.83 dB, and the gain-bandwidth was approximately 4.8 MHz. This setup validates that the amplifier meets its design goals and performs reliably across the required frequency range.

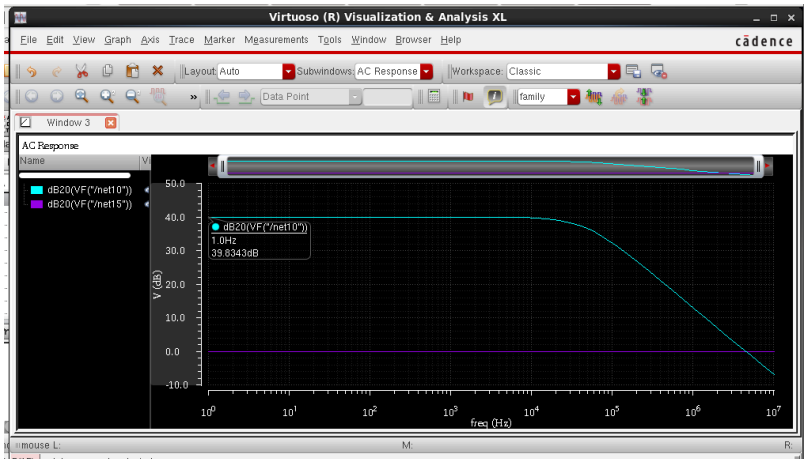

Fig-4: **Frequency Response Plot Showing Voltage Gain (dB) vs Frequency (Hz)**

- **Differential Amplifier Setup and Transient Analysis**

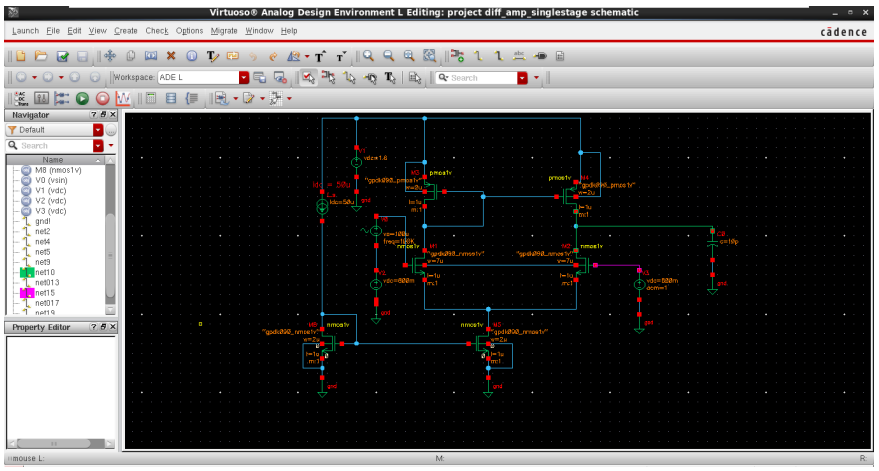

Fig-5: **Circuit connection for Time-domain analysis**

To analyze the time-domain behavior of the designed single-stage differential amplifier, a transient analysis was performed in Cadence Virtuoso. The setup involved applying an input signal to one side of the differential pair while keeping the other side at a fixed DC level. Specifically, a small AC sine wave signal was superimposed on a DC bias of 800 mV with frequency of 1KHz, which lies well within the amplifier's designed input common-mode range (ICMR) of 0.8V to 1.6V. The output was taken from one side of the current mirror load and monitored over time. The transient simulation showed an amplified version of the input sine wave, validating the amplifier's ability to handle small-signal variations effectively.

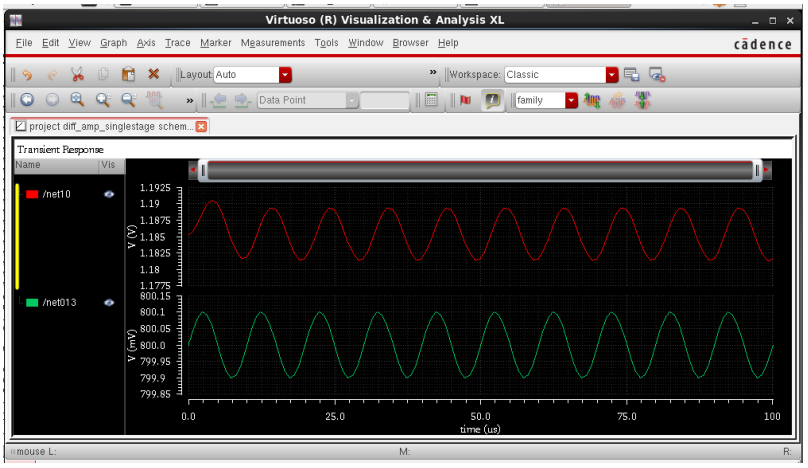

Fig-6: **Time-Domain Output Waveform Analysis**

- **ICMR Checking in Differential Amplifier Design**

To ensure proper operation of the differential amplifier across a range of input voltages, an ICMR (Input Common-Mode Range) analysis was performed. The ICMR defines the range of common-mode input voltages over which the amplifier functions correctly, with all transistors remaining in the desired region of operation(saturation region).
In this design, the ICMR was tested by sweeping the common-mode voltage applied to both inputs of the differential pair. The DC operating point and output voltage were monitored throughout the sweep to ensure that:

- The input transistors remained in saturation.
- The output stayed within an acceptable voltage swing.
- The amplifier maintained linear behavior and bias stability.

Through this simulation in Cadence Virtuoso, the amplifier was found to operate correctly within the input common-mode range of 0.099V to 1.17V, aligning with the targeted specification. This confirms that the amplifier can handle input signals across a wide range, making it suitable for various analog front-end conditions.

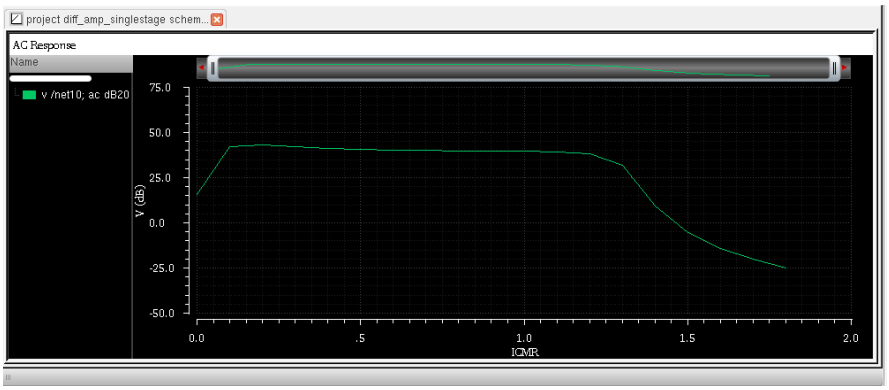

Fig-7: **Operating Region Validation through ICMR Sweep**

GitHub Link

https://github.com/Mani654/project__design-of-single-stage-differential-amplifier

Learning and Reflection

New Learning

- **Familiarity with Cadence Virtuoso Tool**

  One of the most significant learnings from this project was getting hands-on experience with the Cadence Virtuoso design environment. I learned how to build circuit schematics, set up simulations, define inputs and outputs, and interpret the simulation results using various tools within the Virtuoso suite, including ADE and Spectre simulators. This helped me understand the real-world workflow followed by professionals in analog circuit design.

- **Understanding AMS Design Concepts**

  This project really helped me build a stronger understanding of Analog and Mixed-Signal (AMS) design. Working on a differential amplifier, which is a key building block in analog circuits, gave me a practical way to apply what I've learned in theory. I got comfortable setting up and running DC, AC, and transient simulations, and I learned how each type of analysis helps reveal different parts of the circuit's behavior — like its biasing, frequency response, and time-domain performance.

- **Learning Key Analog Parameters**

  I became familiar with important performance parameters such as:

  - ICMR (Input Common-Mode Range) and how to verify it through simulation.
  - Voltage Gain and Gain-Bandwidth Product, and their role in amplifier performance.
  - Biasing techniques and W/L sizing which are crucial for proper operation of MOSFETs in analog design.

Experience

Working on this project, I learned how to carefully select and size transistors, set up proper biasing, and use simulation techniques like DC, AC, and transient analysis to evaluate circuit behavior. I became more confident in using Cadence for schematic entry, simulation setup, and waveform analysis.

I also developed a much deeper understanding of Analog and Mixed-Signal (AMS) concepts such as ICMR, gain-bandwidth product, and voltage gain, and how they are affected by design parameters. This hands-on experience taught me how to troubleshoot, optimize, and verify a circuit step-by-step.

Overall, this project helped me connect theoretical knowledge with hands-on practice. I gained confidence in using Cadence tools, developed a systematic approach to analyzing analog circuits, and understood how AMS design principles are applied in real-world projects.

Conclusion and Future Scope

Project Objectives

- To design a single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso.
- To achieve a voltage gain of approximately 40 dB.
- To maintain an Input Common-Mode Range (ICMR) from 0.8V to 1.6V.
- To attain a gain-bandwidth product (GBW) of around 5 MHz.
- To verify the amplifier's performance through DC, AC, and transient simulations.

Project Achievements

- Successfully designed and simulated the amplifier using Cadence Virtuoso.
- Achieved a voltage gain of 39.83 dB, close to the target.
- Verified an ICMR of 0.9V to 1.17V, ensuring stable operation across input range.
- Achieved a gain-bandwidth product of 4.8 MHz, suitable for mid-speed analog applications.
- Performed and analyzed DC biasing, AC frequency response, and transient behavior effectively.
- Gained hands-on experience in AMS design, tool usage, and simulation interpretation.

Conclusion

The primary objective of this project was to design and analyze a single-stage differential amplifier using 90nm CMOS technology in the Cadence Virtuoso environment. The project aimed to achieve a high voltage gain, maintain a wide input common-mode range (ICMR), and ensure sufficient bandwidth for mid-speed analog applications. Through careful transistor sizing, bias current selection, and performance tuning, the amplifier was successfully designed to operate within the desired specifications. The final design achieved a voltage gain of **39.83 dB**, an ICMR of 0.099V to 1.17V, and a gain-bandwidth of **4.8 MHz** — closely aligning with the design targets. These results were validated using SPICE-level simulations, including DC operating point analysis, AC frequency response, and transient analysis.

This project provided deep insights into Analog and Mixed-Signal (AMS) design practices, particularly in working with differential circuits. It also reinforced the importance of key analog parameters like gain, ICMR, and GBW, and how they are influenced by transistor-level design decisions. Overall, the project successfully met

its goals and served as a valuable learning opportunity in analog design methodology and tool usage.

Future scope of this project

The design and simulation of the single-stage differential amplifier using 90nm CMOS technology achieved the intended performance goals, but it also opened up various directions for further enhancement and exploration. The future scope of this project can be broadly divided into performance improvements, design extensions, and real-world integration. The following points highlight the potential future developments:

- **Cascoding for Higher Gain**

  Introducing cascode transistors in the differential pair or the load section can significantly increase the voltage gain. This helps improve output resistance and bandwidth control, making the amplifier suitable for more precise analog signal processing applications.

- **Design of Two-Stage Amplifier**

  The current single-stage design is simple and effective but has limitations in gain and output swing. Extending the amplifier to a two-stage configuration can help improve gain further and drive larger capacitive loads. Compensation networks like Miller compensation can also be explored.

- **Exploration in Other Technology Nodes**

  To study the scalability and performance consistency of the design, future work can involve implementing the same amplifier in different CMOS technology nodes such as 45nm or 180nm. This helps understand the impact of process scaling on analog performance.