Submit on LMS

- Submit the code and testbench along with snapshot of waveform.
- If you are getting an error and unable to get waveform, submit snapshot of error
- Rename the individual verilog files (.v) as: rollnumber1_filename.v

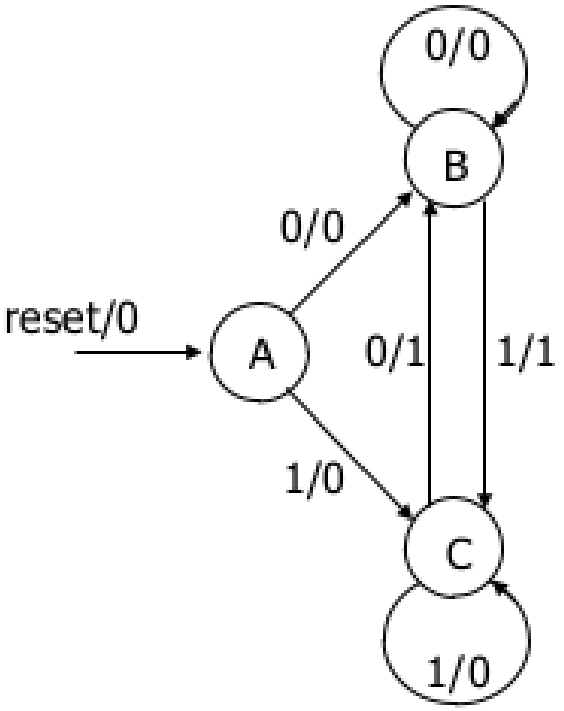
  for eg, imt< >_filename.v
- Now, upload all these files (renamed verilog, snapshot of waveforms etc) as separate files in to the midterm-link on Exam LMS
- Do not submit vcd files
- Important- DO NOT COMPRESS THESE FILES INTO ZIP/TAR. UPLOAD THE FILES INDIVIDUALLY INTO THAT LINK.
- **All codes will go through Turnitin- for plagiarism check. Codes which are similar, will get a zero for the entire assignment.**

Verilog Assignment Total 30 marks
Deadline April 29, 11.55pm

Q1: (Marks: 10 for code + 10 for testbench)

Write a verilog code to define the following FSM. Testbench should test all states and combinations

For eg- 0/0 in the FSM means, input = 0 in that state and output=0



Q2. Debug codes (5 + 5 marks)

- Two verilog files – counter and ALU, with errors, have been uploaded. You are required to debug the errors, and fix them
- Write comments in the code, at the top of the file, mentioning the error and how you fixed it.
- Upload this code with comments on LMS