EE 719 Mixed Signal VLSI Design

Project Part 4

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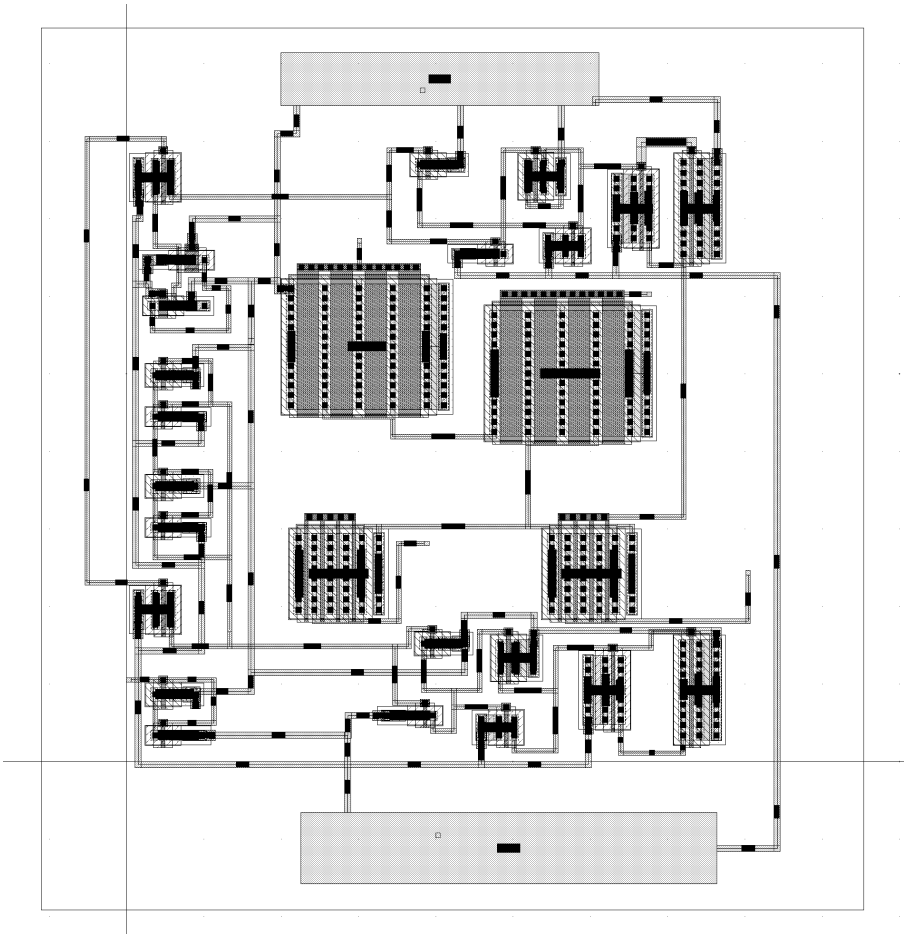

Figure 1: Layout of the Unit Cell

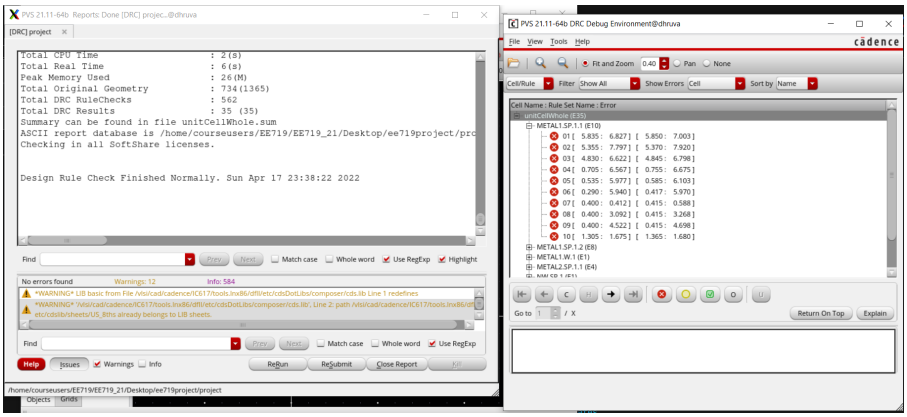

Figure 2: DRC

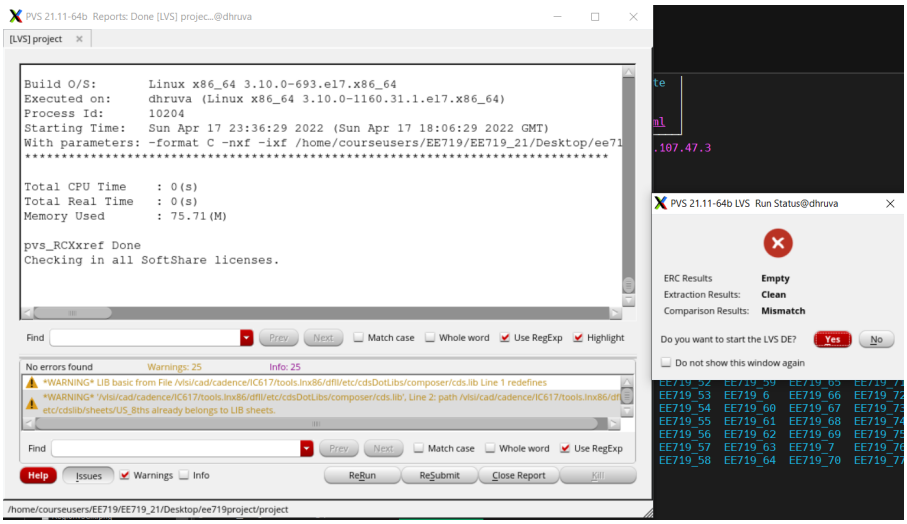

Figure 3: LVS