EE719: Mixed-Signal VLSI Design

Course Project: Part 3

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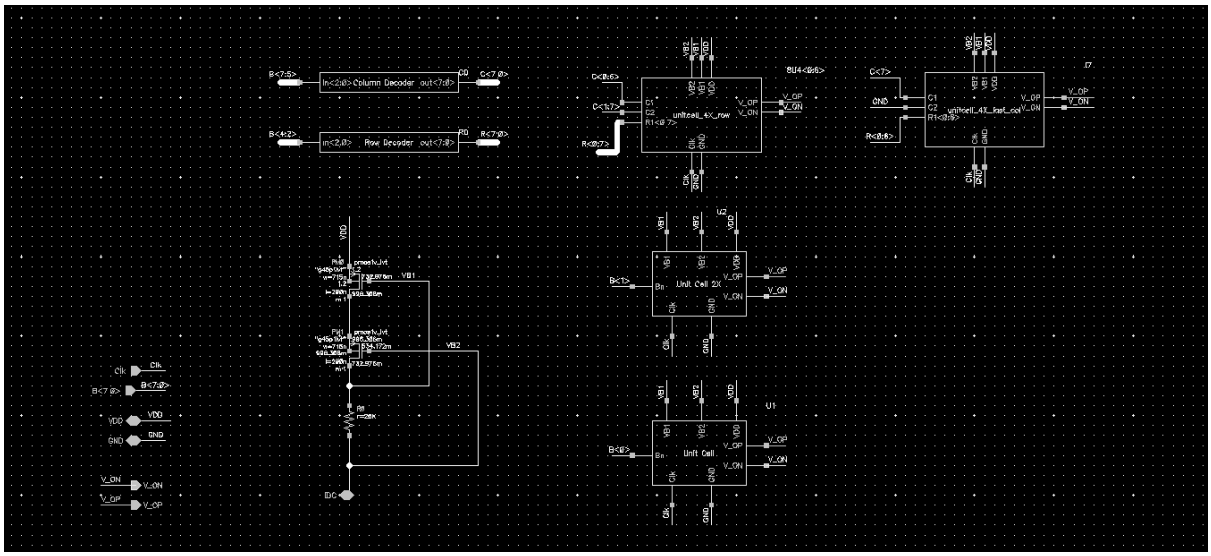
Design modification:

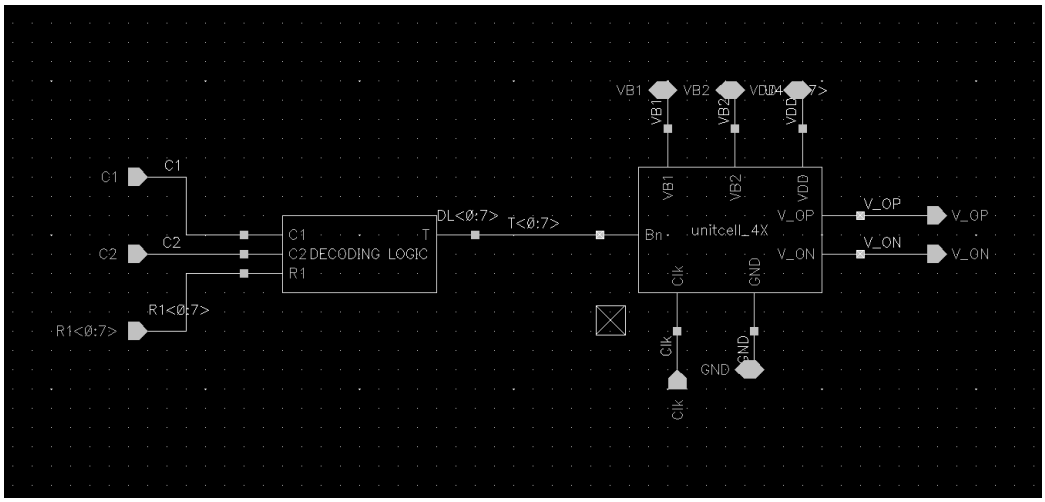
Changed the length of switching transistor MB2 from 200 nm to 600 nm to meet reqd SFDR specs

Parameter	M_{B1}	M_{B2}	M_1	M_2
Width (in nm)	4070	4070	5025	5025
Length (in nm)	200	600	50	50

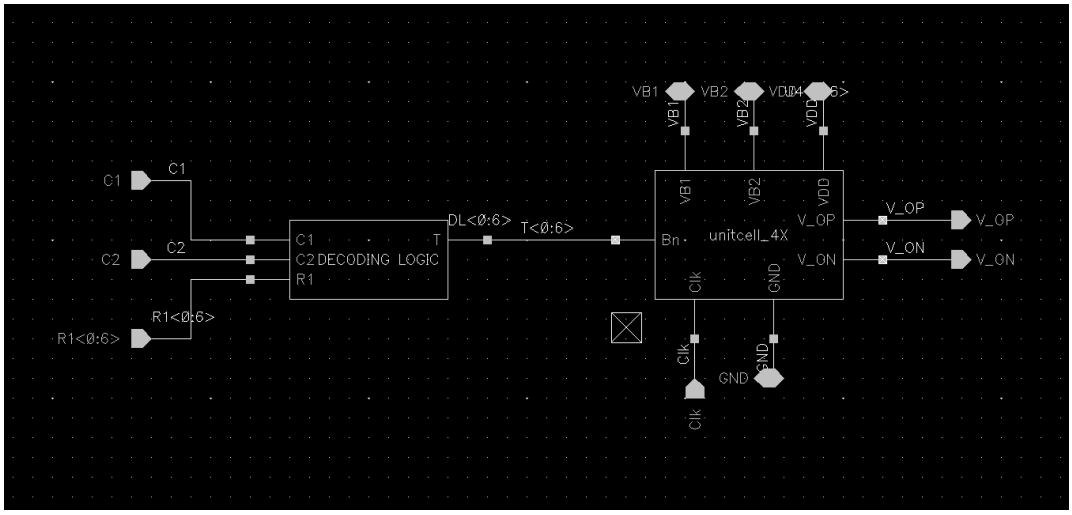
3(a)



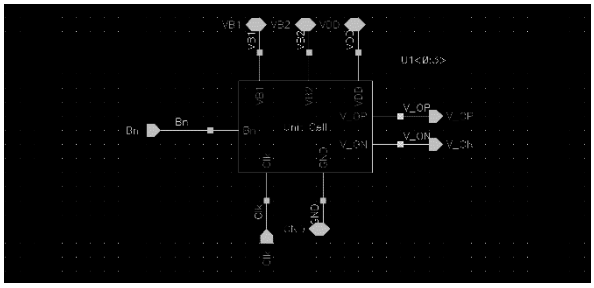
DAC schematic



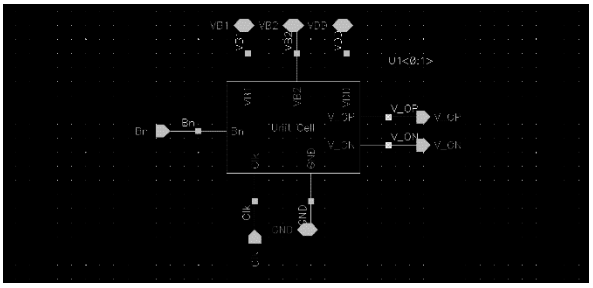
Unitcell_4X_row schematic



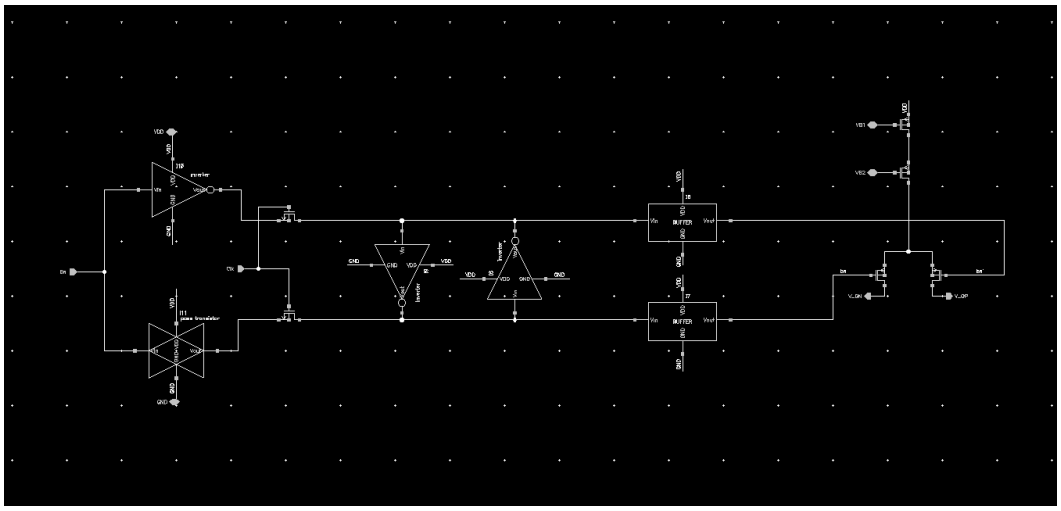
Unitcell_4X_last_col schematic



Unitcell_4X schematic



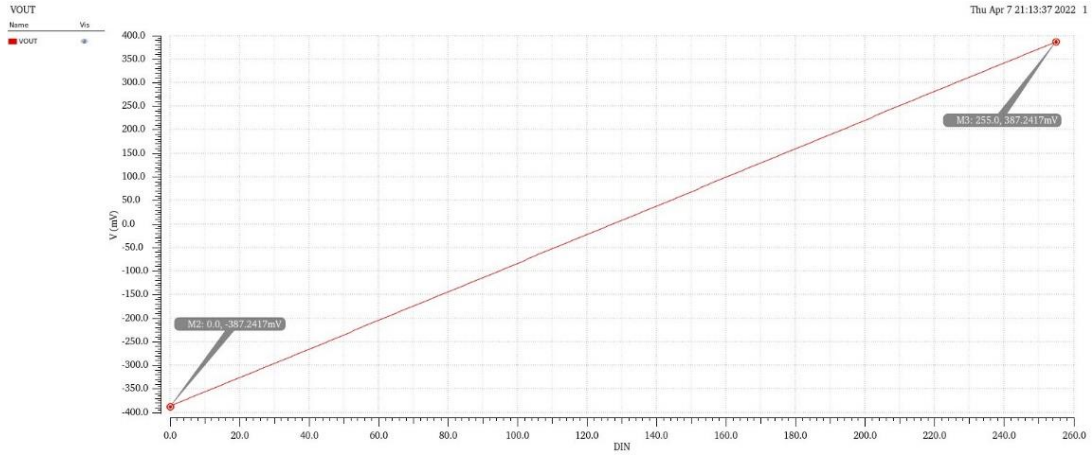
Unitcell_2X schematic



Unitcell schematic

3(b)

DC Analysis



$$Maximum\ voltage\ =\ 387.2417\ mV\ (D_{in} = 0)$$

$$Minimum\ voltage\ =\ -387.2417\ mV\ (D_{in} = 255)$$

Taking DC operating point after the design update, measured $I_{LSB} = 52.78\ uA$.

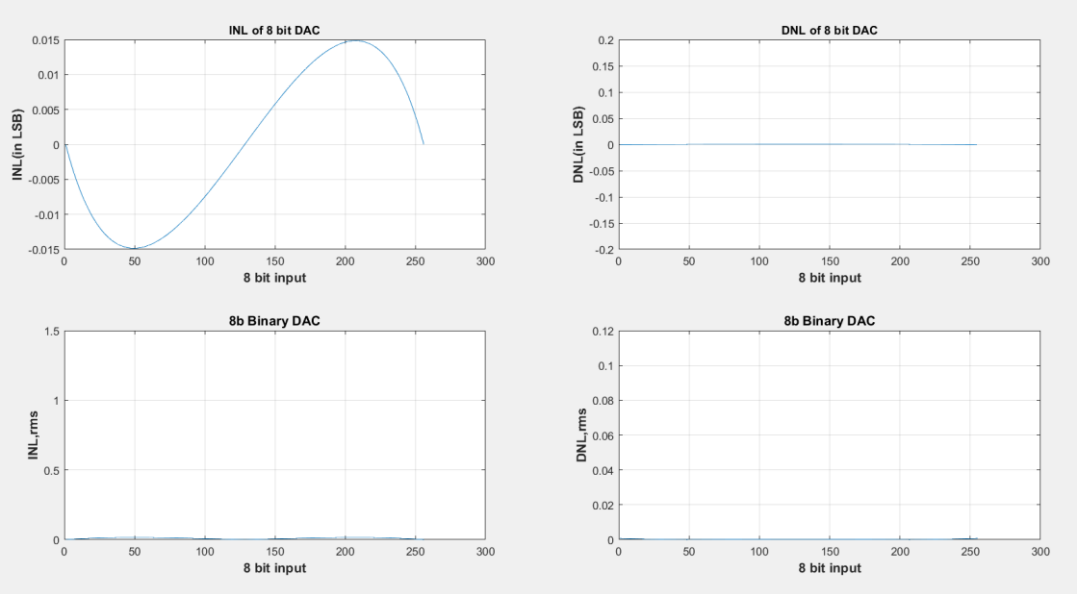
Then, the ideal voltage when $D_{in} = 0$ is $-255 * R_L * I_{LSB} = -390.3081\ mV$

$$\Rightarrow Offset\ error = V_{ideal} - V_{measured} = -390.3081 - (-387.2417) = -3.0664\ mV$$

Similarly, $Full\ scale\ error = 390.3081 - 387.2417 = 3.0664\ mV$

$$Gain\ error = \frac{V_{FS} - Full\ scale\ error}{V_{FS}} = 0.9921$$

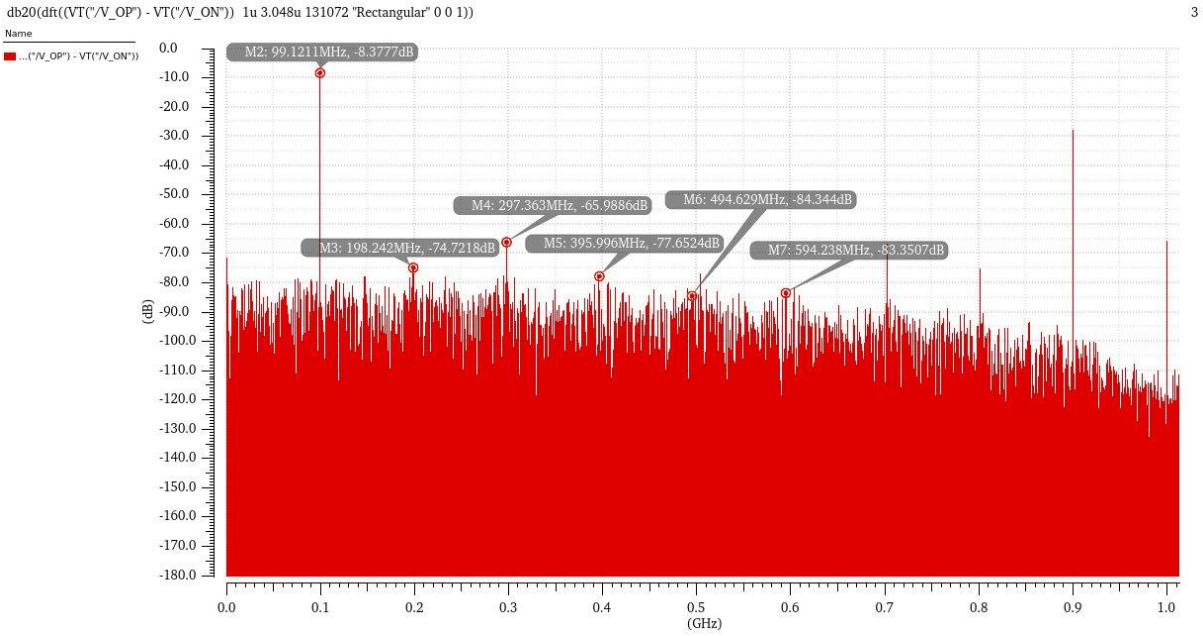
Offset Error	Full Scale Error	Gain Error
-3.0664 mV	3.0664 mV	0.9921



3(d)

M = 203; N = 2048

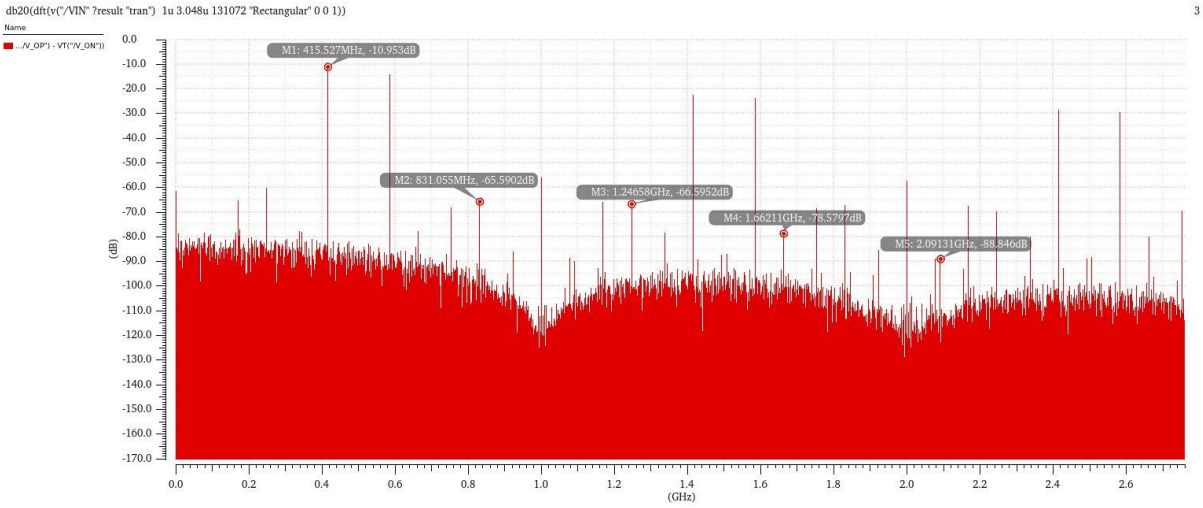
2048 point FFT spectrum for sinusoidal input = 99.121 MHz



3(d)

M = 851; N = 2048

2048 point FFT spectrum for sinusoidal input = 415.527 MHz



The capacitance of the switching transistors (MB1 and MB2) and non-linearities of the transistor and digital components present in the DAC cause the harmonics.

3(f)

f_{input}	SNDR (in dB)	SFDR (in dB)	ENOB
99.121 MHz	49.91	57.61	7.999
415.527 MHz	45.64	53.00	7.289

3(g)

Total analog power consumed = V_{DD} x 255I_{LSB}

Power consumed by digit driver can is negligible as I^2R across it is comparatively very low.

From the DC analysis of the DAC in DNL_INL_TB, we found out

$$I_{LSB} = 60.74\ uA$$

⇒ Total power consumed $= 1.2\ V * 255 * 60.74\ uA = \mathbf{18.59\ mW}$