EE719: Mixed-Signal VLSI Design
Course Project

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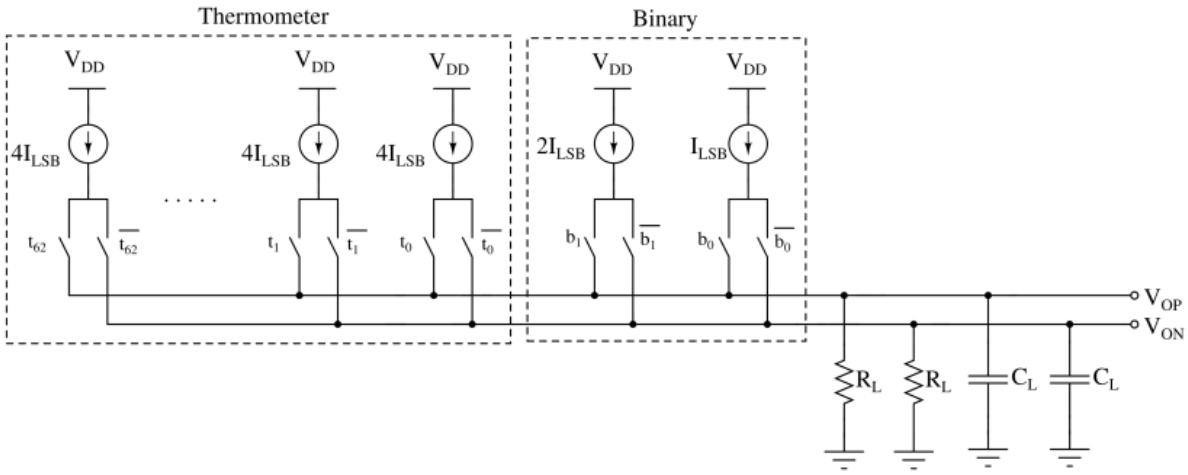
Design of unit cell Analog circuitry for the 8-bit segmented DAC

PART 1

(Made changes in values from the previous submission)

Last digit of roll no. = 4 ⇒ $R_L = 25 + 4 = 29\ \Omega$, $C_L = 1 + \frac{4}{10} = 1.4\ pF$

Calculating V_{FS}, I_{LSB}



From the 8-bit DAC circuit diagram,

$$V_{out} = V_{OP} - V_{ON}$$

$(V_{out})_{max} = 0 - 255 I_{LSB} R_L = -255 I_{LSB} R_L$, (Digital input = 0)

$(V_{out})_{min} = 255 I_{LSB} R_L - 0 = +255 I_{LSB} R_L$, (Digital input = 255)

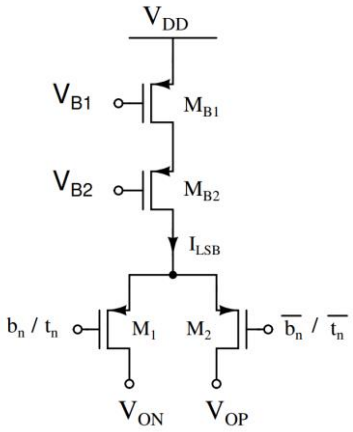
$\Rightarrow Output\ voltage\ swing = V_{FS} = (V_{out})_{max} - (V_{out})_{min} = 510 I_{LSB} R_L$

$Given, V_{FS} > 0.8\ V_{pp} \Rightarrow I_{LSB} > \frac{0.8}{510*29}$

$\Rightarrow I_{LSB} > 54.1\ \mu A$

------- (1)

Now, we can find an upper limit on I_{LSB} as follows



Switch circuit in the DAC unit cell

From the above circuit, in saturation,

$$V_{ON} \mid V_{OP} = V_{DD} - ((V_{dsat})_{M_{B1}} + (V_{dsat})_{M_{B2}} + (V_{dsat})_{M_1} \mid (V_{dsat})_{M_2})$$

Minimum possible voltage at V_{ON} or V_{OP} is $\frac{0.8V}{2} = 0.4V$ $\quad (V_{DD} = 1.2\ V)$

$$\Rightarrow 1.2\ V - \Sigma V_{dsat} > 0.4\ V$$

$$\Rightarrow \Sigma V_{dsat} < 0.8\ V$$

The overdrive voltage (or V_{dsat}) for the cascode transistors $M_{B1}\ and\ M_{B2}$ has to be between 200-300 mV and the same for the switching transistors has to be 50-100 mV

(ref. Razavi's paper)

We can choose $(V_{dsat})_{M_{B1}} = (V_{dsat})_{M_{B2}} = 200\ mV$ and $(V_{dsat})_{M_1} = (V_{dsat})_{M_2} = 90\ mV$ to satisfy the above conditions.

$$\Rightarrow \Sigma V_{dsat} = 200\ mV + 200\ mV + 90\ mV = \ 490\ mV$$

That makes $(V_{ON})_{max} = (V_{OP})_{max} = 1.2 - 0.490 = 0.710\ V$

$$\Rightarrow 255 I_{LSB} R_L < 0.710$$

$$\Rightarrow I_{LSB} < \mu A$$

---------(2)

From (1) and (2)

$$\Rightarrow 54.1\ \mu A < I_{LSB} < \ \mu A$$

I choose

$$\boxed{I_{LSB} = 57\ \mu A}$$

$$\Rightarrow V_{FS} = 510 I_{LSB} R_L$$

$$\boxed{V_{FS} = 0.843\ V}$$

Calculating W/L

$$(I_D)_{sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}V_{dsat}^2 \qquad (\mu_p C_{ox} = 140\ \frac{\mu A}{V^2})$$

For M_{B1}, M_{B2}

$$\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(0.2)^2 = 57 * 10^{-6} \Rightarrow \frac{W_1}{L_1} = 20.36$$

--------(3)

For M_1, M_2

$$\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(0.09)^2 = 57 * 10^{-6} \Rightarrow \frac{W_2}{L_2} = 100.53$$

--------(4)

Expression for INL_{max}

From Pelgrom's paper,

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{4\sigma_{V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{\sigma_\beta^2}{\beta^2}, \qquad \frac{\sigma_\beta^2}{\beta^2} \approx \frac{A_\beta^2}{WL} + S_\beta^2 D^2$$

Neglecting S_β,

$$\Rightarrow \frac{\sigma_{I_D}^2}{I_D^2} = \frac{4\sigma_{V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{A_\beta^2}{WL} = \frac{4\sigma_{V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{A_\beta^2}{WL}$$

From Razavi's paper,

$$INL_{max} = \frac{\sigma_{I_u}}{2I_u}\sqrt{2^N}\ LSB\ \ (N = 8)$$

$$\Rightarrow INL_{max} = 8\sqrt{\frac{4A_{V_{TH}}^2}{WL(V_{GS} - V_{TH})^2} + \frac{A_\beta^2}{WL}}\ \ LSB$$

$$(A_\beta = 4\%\ \mu m, \qquad A_{V_{TH}} = 4.6\ mV - \mu m)$$

Required: $INL_{max} < 1\ LSB$

$$\Rightarrow 8\sqrt{\frac{4A_{V_{TH}}^2}{W_1 L_1 (V_{GS} - V_{TH})^2} + \frac{A_\beta^2}{W_1 L_1}} < 1$$

$$\Rightarrow W_1 L_1 > 2.378\, x\, 10^{-13}\, m^2$$

From eqn (3)

$$\Rightarrow 21.43 L_1^2 > 2.378\, x\, 10^{-13}\, m^2$$

$$\Rightarrow L_1 > 105.34\, nm$$

We can take $L_1 = 200\, nm,\ W_1 = 4072\, nm$

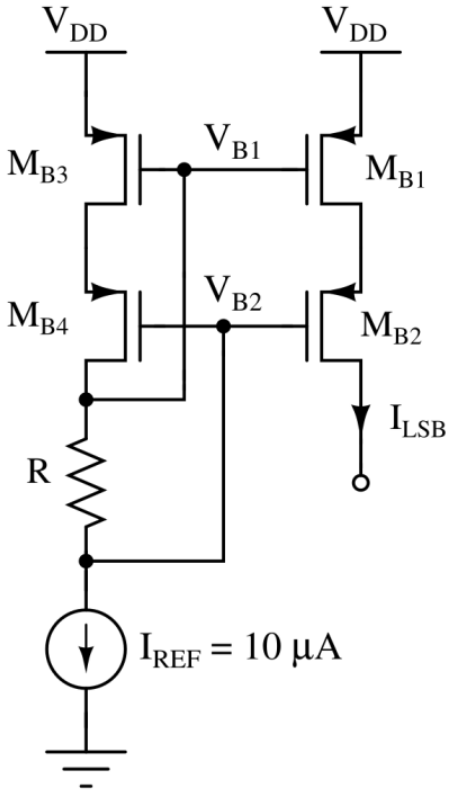
For the switching transistors, to ensure fast witching we take minimum channel length.

$$L_2 = 50\, nm$$

$$\Rightarrow W_2 = 5026.5\, nm$$

Parameter	M_{B1}	M_{B2}	M_1	M_2	V_{FS}	I_{LSB}
Width (in nm)	4070	4070	5025	5025	0.843 V	60 μA
Length (in nm)	200	200	50	50		

Part 1 (b)



$$I_{REF} = R(V_{B1} - V_{B2})$$

$$V_{B1} = V_{DD} - V_{SG1}$$

$$V_{SG1} = V_{dsat1} + V_{TH}$$

$$V_{B1} = V_{DD} - V_{dsat1} - V_{TH} \qquad \text{---- (1)}$$

$$V_{B2} = V_{DD} - V_{dsat1} - V_{SG2}$$

$$V_{SG2} = V_{dsat2} + V_{TH}$$

$$V_{B2} = V_{DD} - V_{dsat1} - V_{dsat2} - V_{TH} \qquad \text{---- (2)}$$

Using (1) and (2),

$$V_{B1} - V_{B2} = V_{dsat2} = 0.2\ V$$

$$\Rightarrow R = \frac{0.2}{10\ x\ 10^{-6}} = 20\ k\Omega$$

$$I_{REF} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}V_{dsat}^2 \Rightarrow \frac{W}{L} = 3.57$$

For better matching, we can take the lengths of M_{B3} and M_{B4} to be same as M_{B1} and M_{B2}

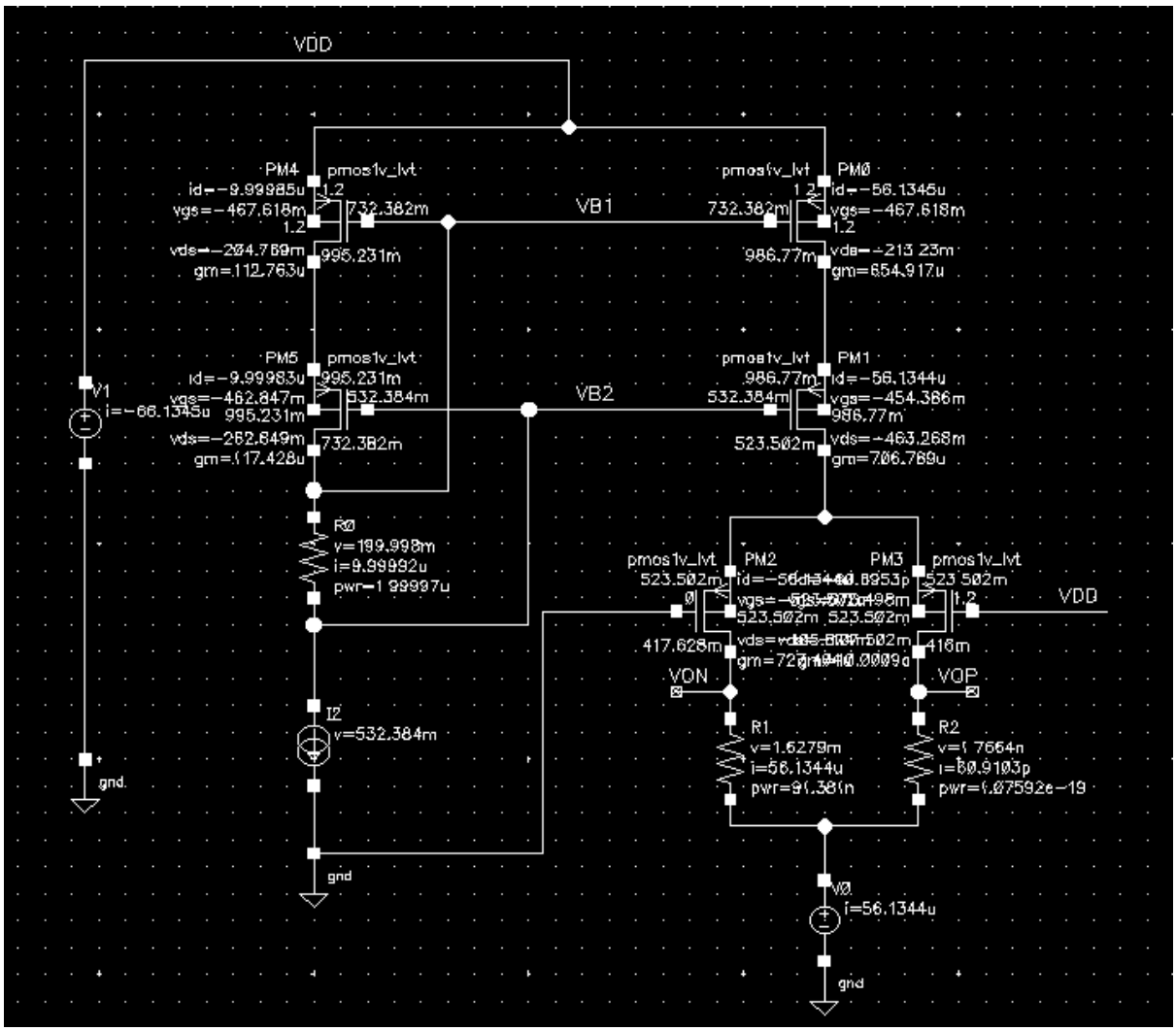
Parameter	MB3	MB4	R
Width (in nm)	715	715	20kΩ
Length (in nm)	200	200	

PART 2

2(a)

DC operating points obtained from DC analysis in Cadence

$\boldsymbol{b_n = 0}$



Annotated points from the figure

$$V_{B1} = 732.382\ mV$$

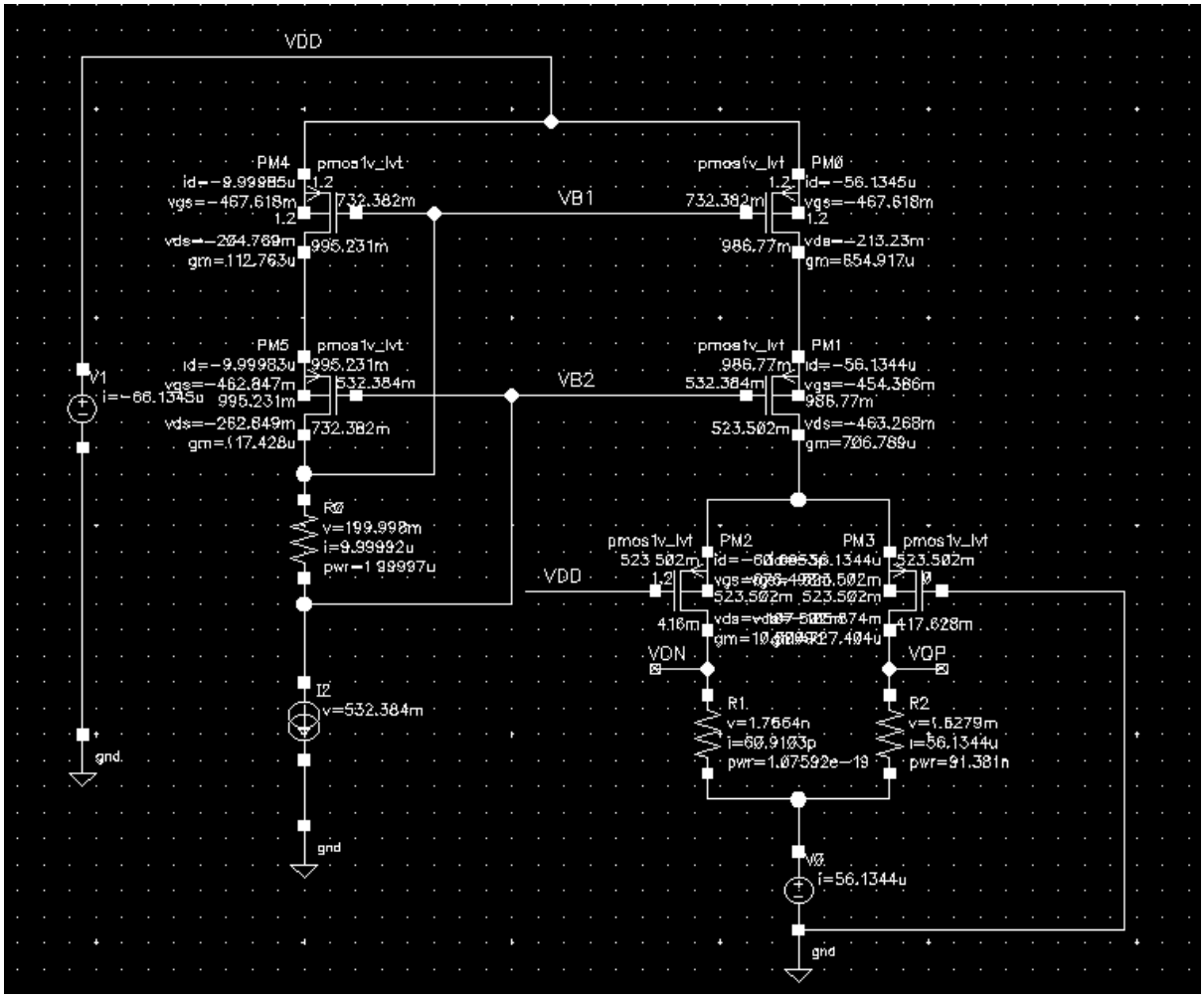
$$V_{B2} = 532.384\ mV$$

$$I_{LSB} = 56.135\ uV$$

$$V_{ON} = 417.628\ mV$$

$$V_{OP} = 416.000\ mV$$

$\boldsymbol{b_n = 1}$



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Note:

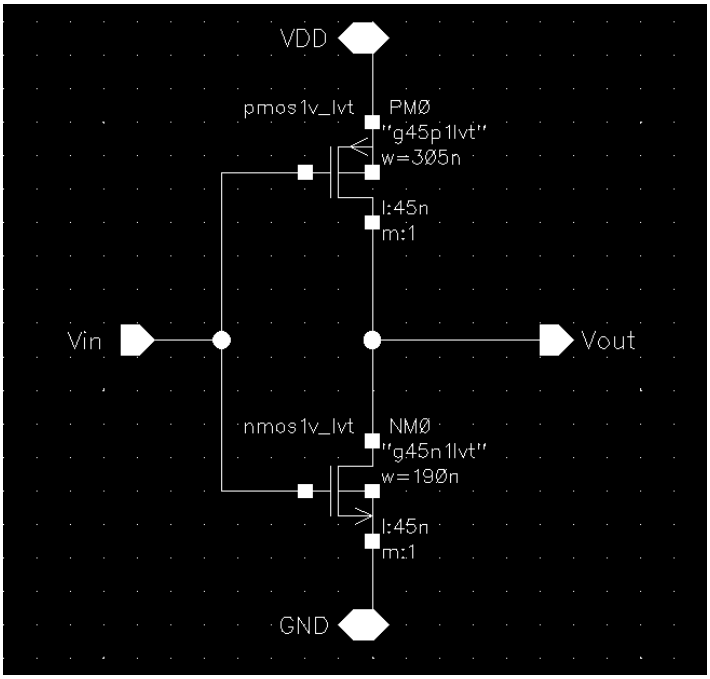
V_{FS} calculated according to this measured I_{LSB} is 830 mV whereas $V_{FS} = 843\ mV$ according to the hand calculation done in part 1.

I considered 830 mV as V_{FS} when deciding my biasing voltage of $\frac{V_{FS}}{2}$.

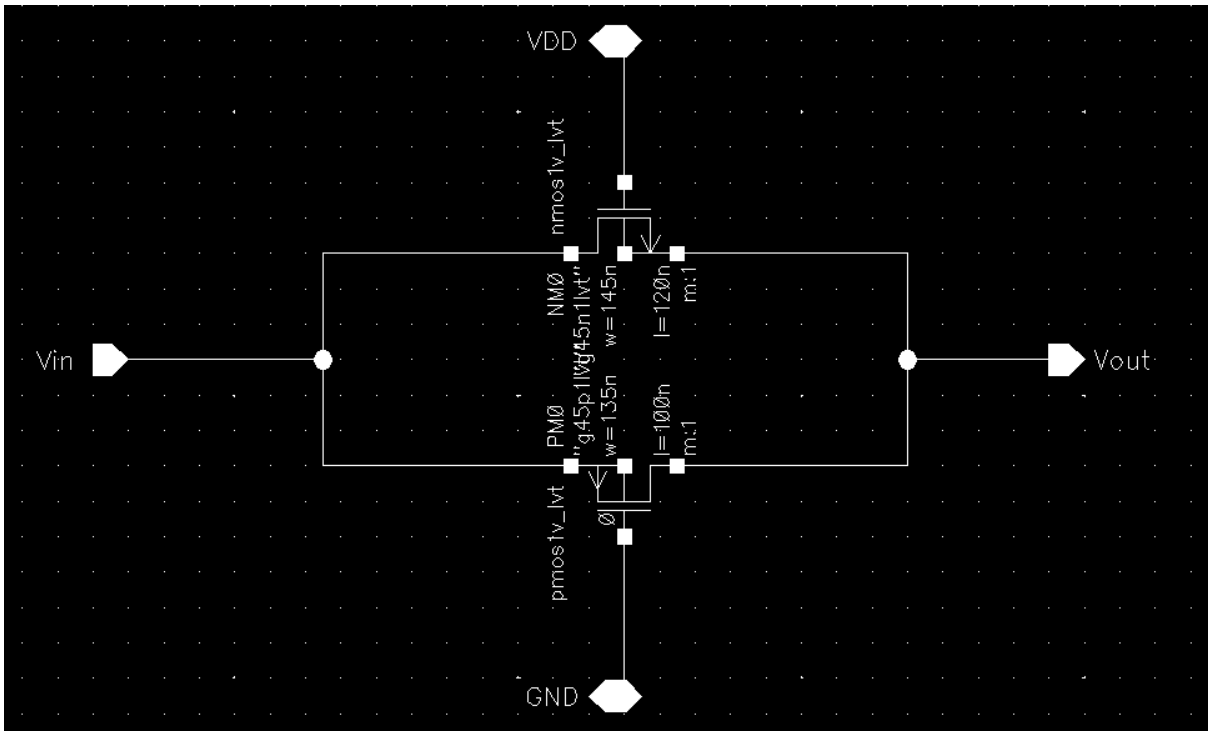
2(b)

Inverter and Pass transistor transistor sizes adjusted to have delays within 5 ps of each other.

Inverter

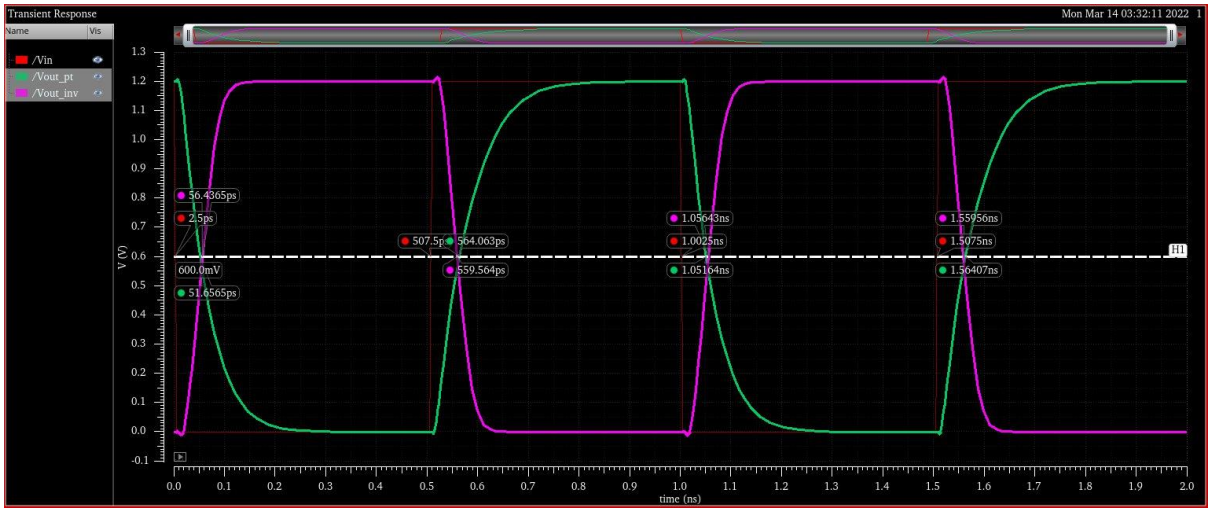


Pass transistor



Inverter: $W_p = 305\ nm, L_p = 45\ nm$; $W_n = 190\ nm, L_n = 45\ nm$

Pass transistor: $W_p = 135\ nm, L_p = 100\ nm$; $W_n = 145\ nm, L_n = 120\ nm$



Delay times

Inverter: 56.44 ps

Pass transistor: 51.66 ps

Difference in delays = 4.78 ps < 5 ps

Required specifications met

2(c)

Number of stages of the buffer can be calculated as

$$n = \frac{\ln\left(\frac{C_L}{C_i}\right)}{\ln(\beta)}$$

In our case,

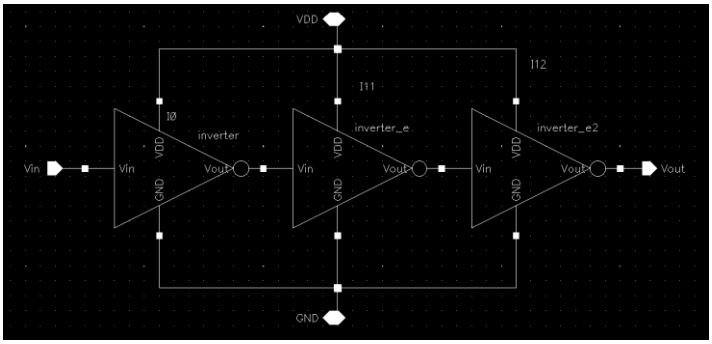
$\beta = 2.72$

$C_L = C_{gg}\ of\ M_1 = 3.505\ fF$

$C_i = C_{gg}\ of\ PMOS + NMOS\ of\ the\ inverter = (146.81 + 75.65)\ aF = 222.46\ aF$

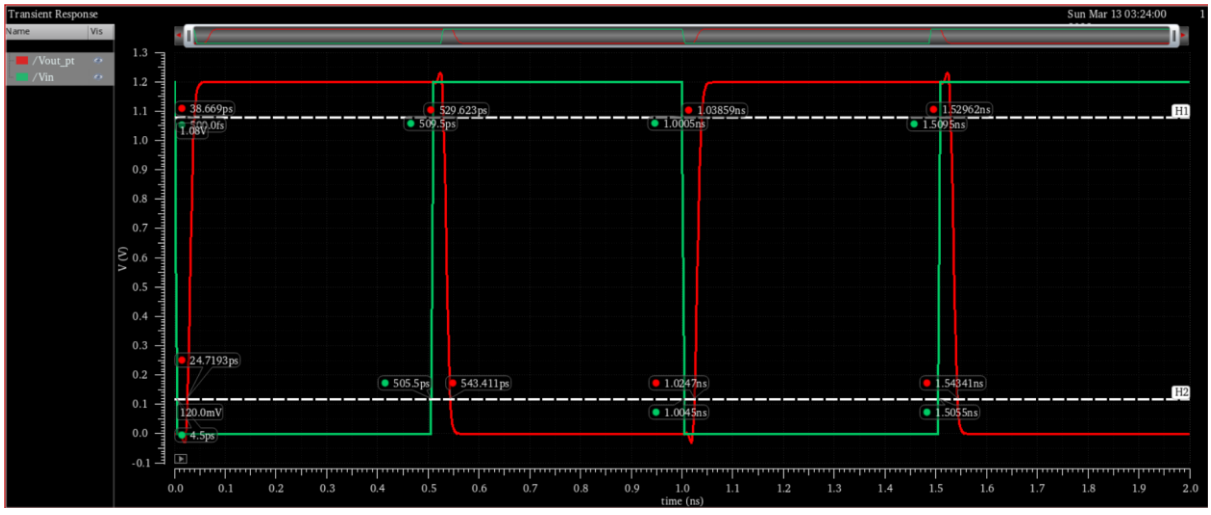
$$\Rightarrow n = 2.76$$

Therefore, we take 3 stages in our buffer and hope it works.



(all values in nm)	W_p	L_p	W_n	L_n
Stage 1	305	45	190	45
Stage 2	830	45	515	45
Stage 3	2255	45	1405	45

Transient analysis performed for 2 cycles of a 1 GHz input



In the above plot,

Rise time = Time interval between 10% and 90% of the maximum output on the rising edge

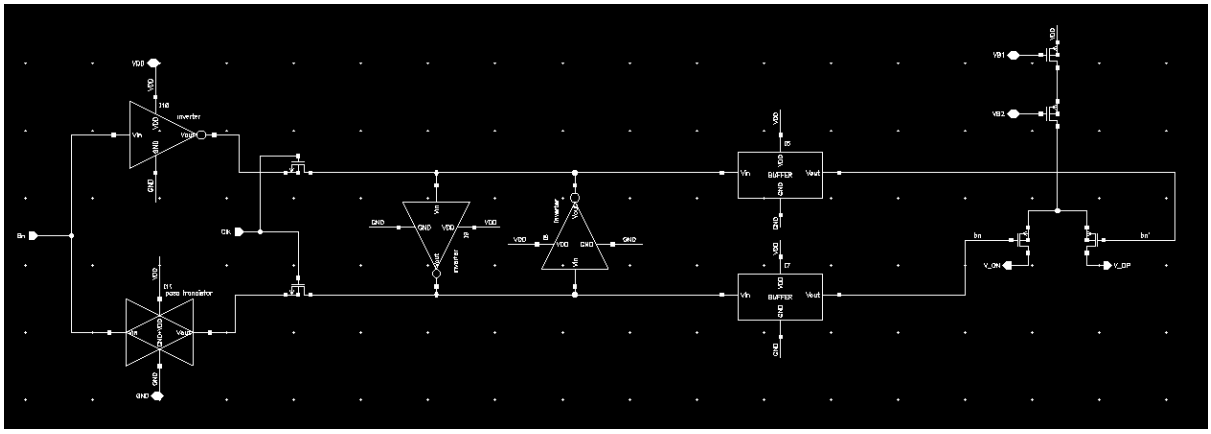
Fall time = Time interval between 90% and 10% of the maximum output on the falling edge

Accordingly,

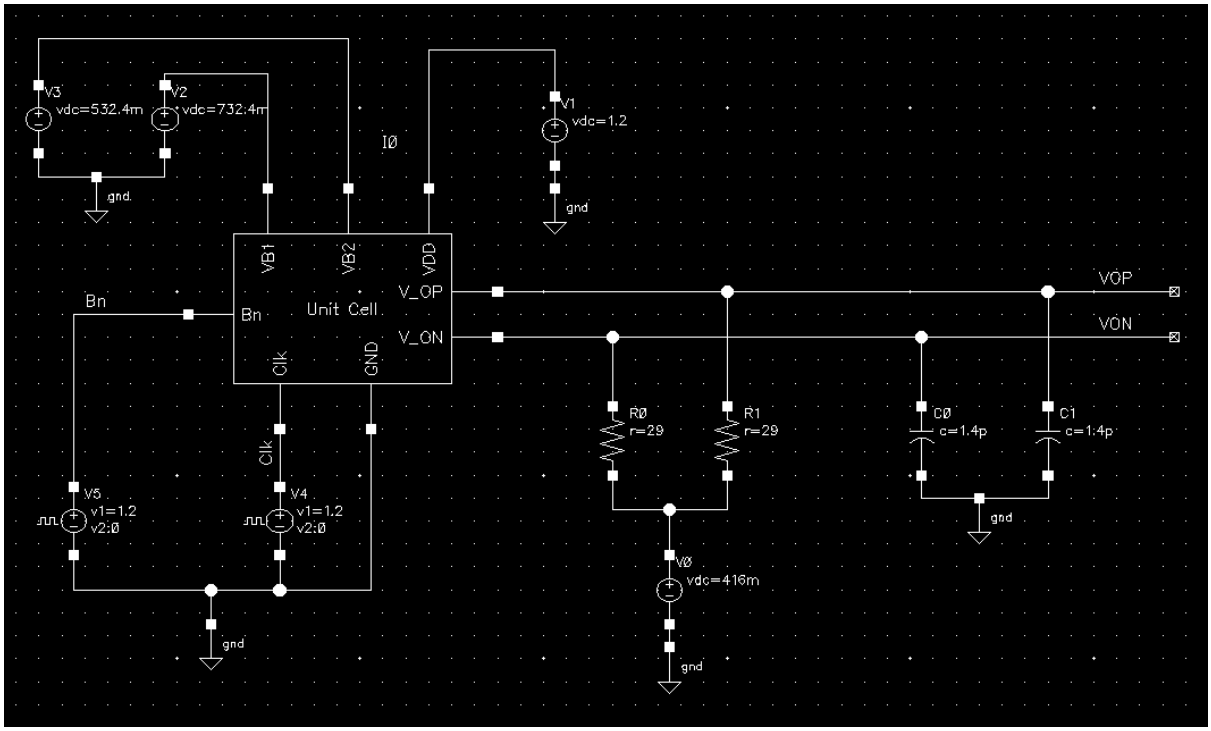
Rise time = 13.95 ps, Fall time = 13.79 ps meet our desired specifications.

2(d)

Unit cell schematic



Test bench schematic

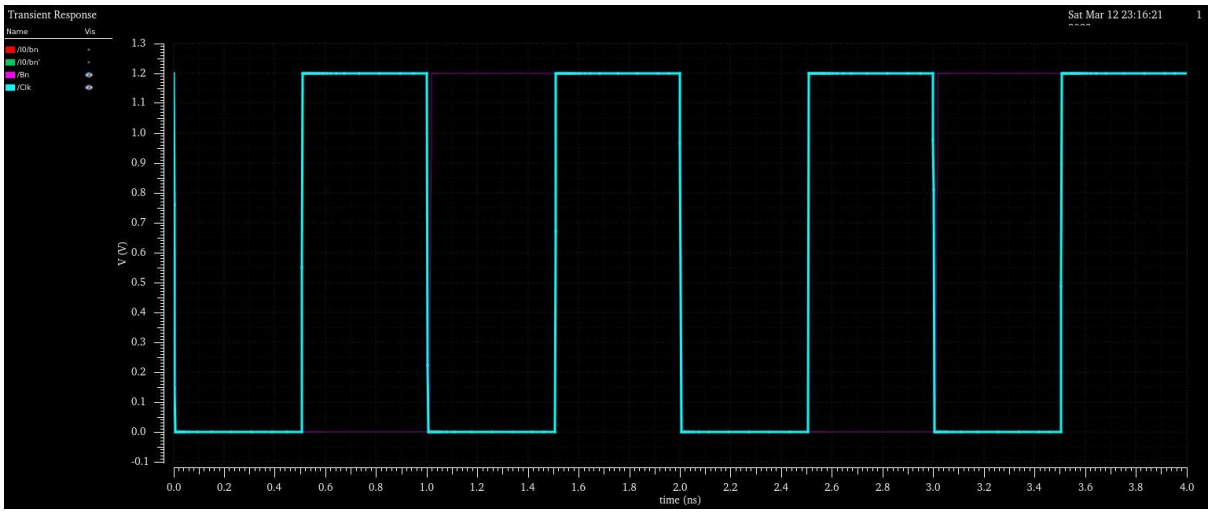


Note: $R_L = 29\ \Omega$, $C_L = 1.4\ pF$ taken according to the instructions given at the beginning.

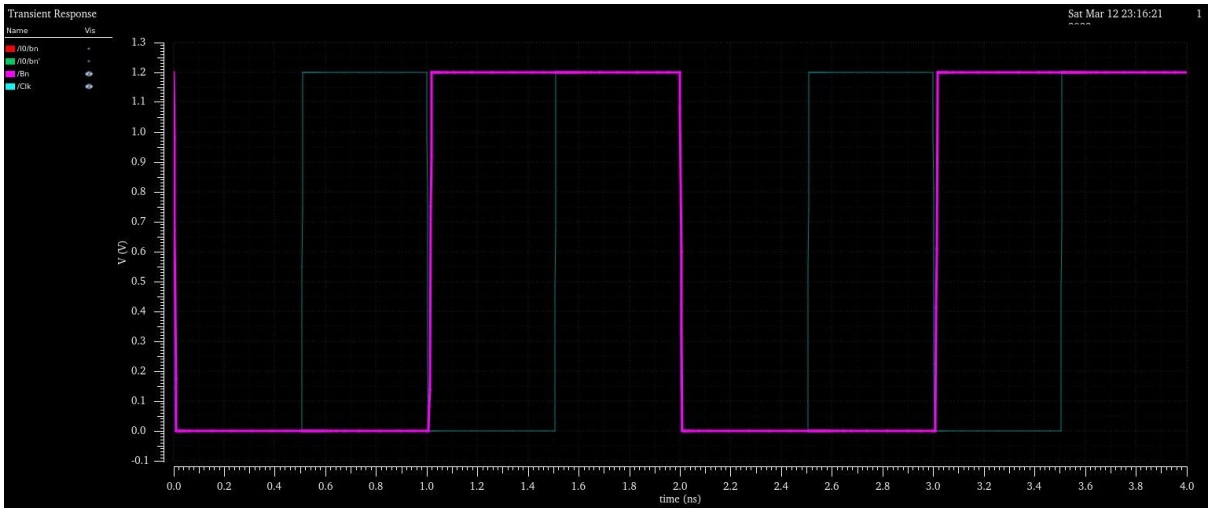
Aspect ratio of the NMOS sampling switch in the unit cell: $\frac{W}{L} = \frac{500\ nm}{45\ nm} = 11.11$

Transient analysis performed for 4 cycles of the 1 GHz clock

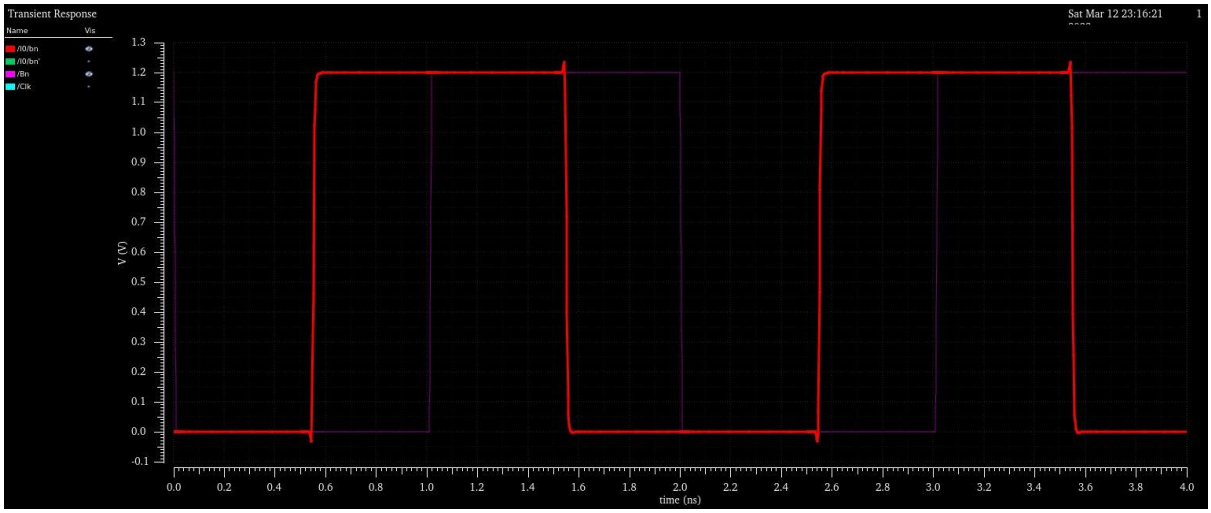
Clk



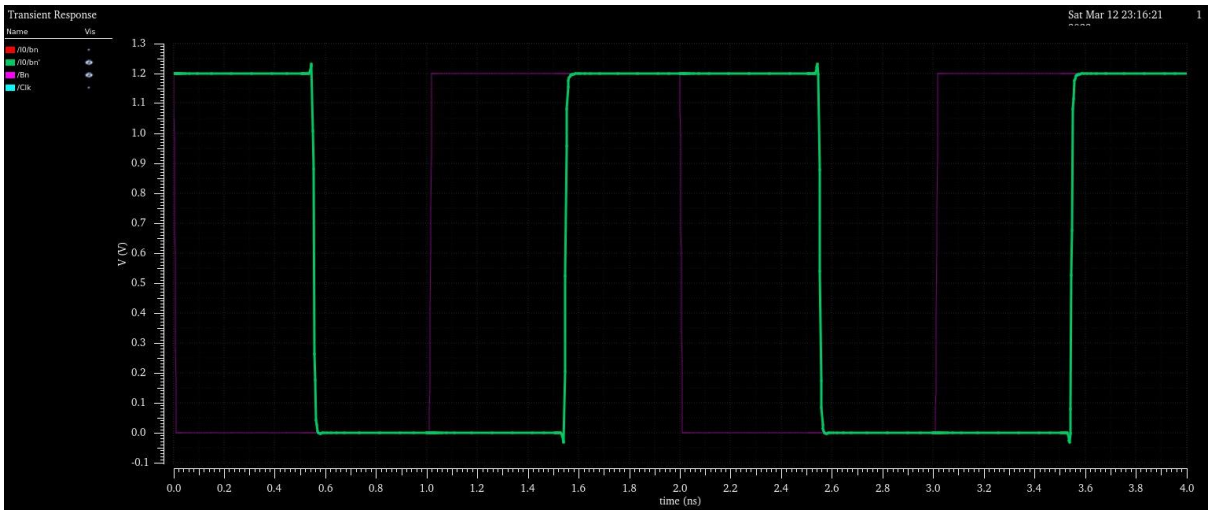
B_n



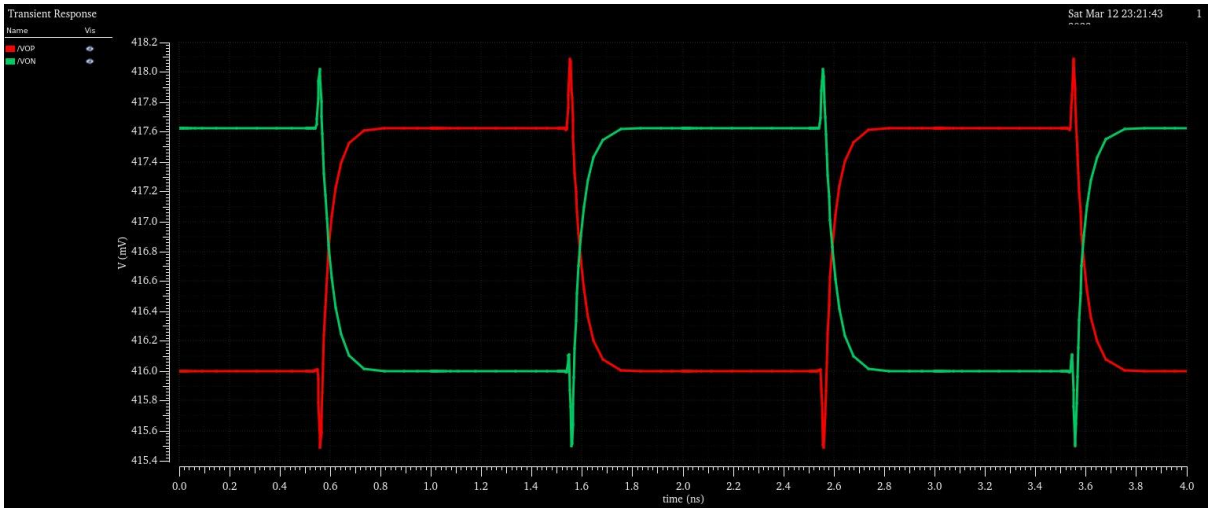
b_n



$\overline{b_n}$



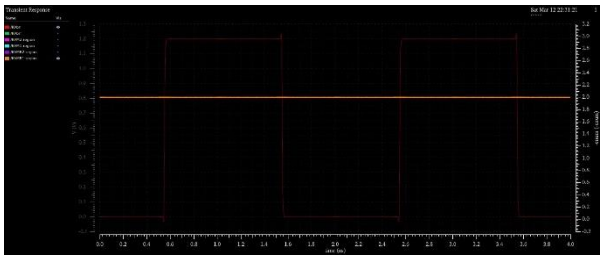
V_{OP}, V_{ON}

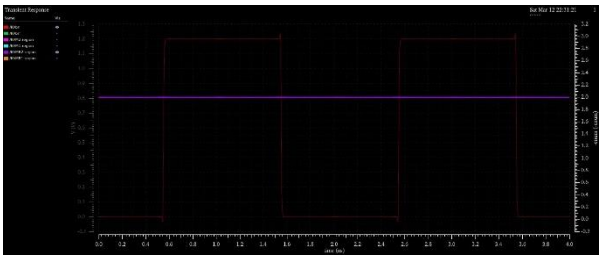


Region of operation

Current source transistors

MB1 MB2

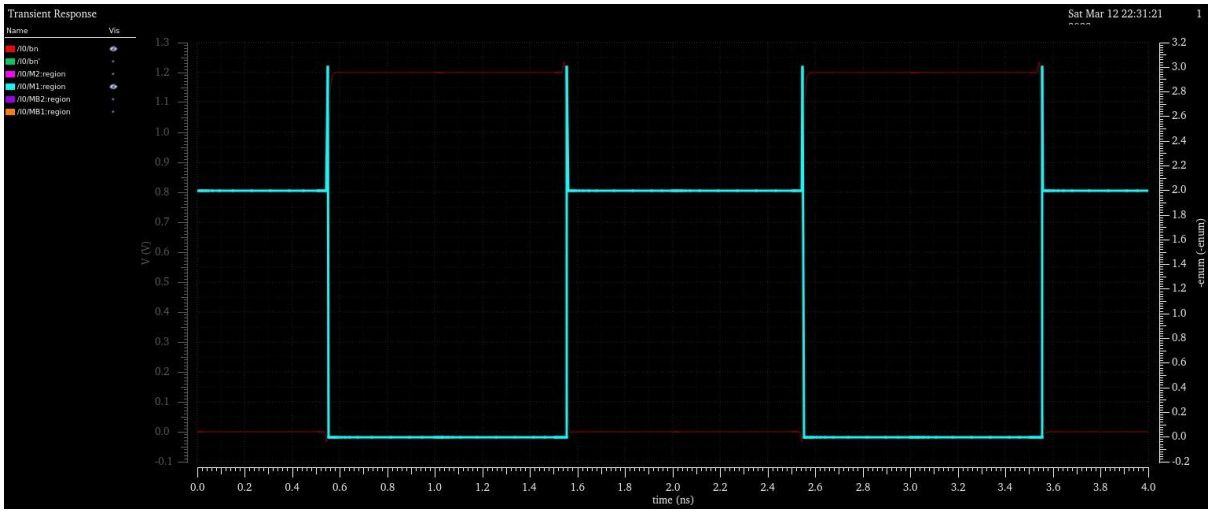




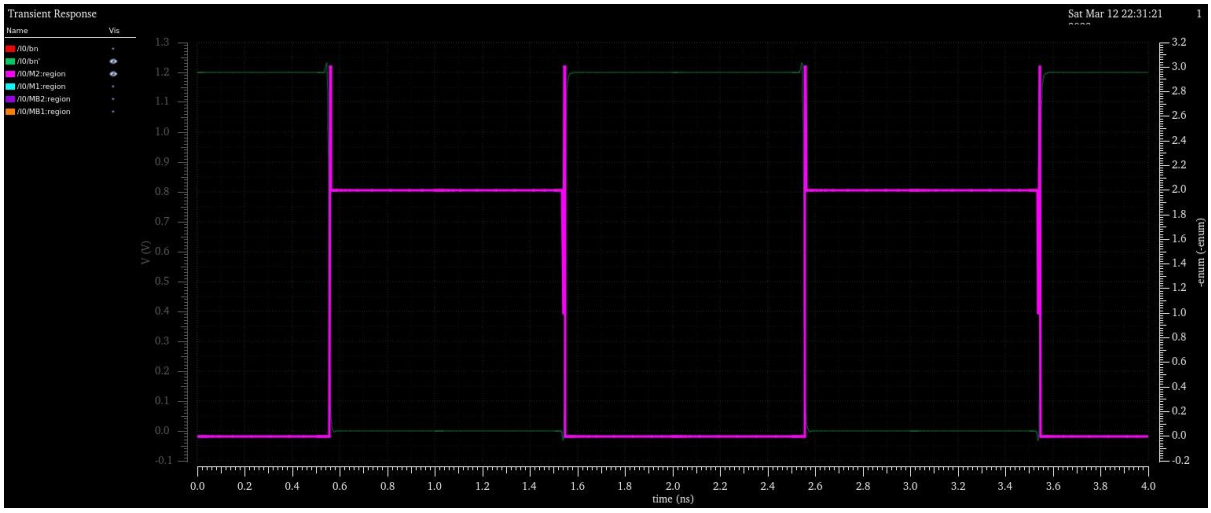
(always in saturation)

Switching transistors

M1



M2



(Switching between OFF state and Saturation)

2(e)

Working of the row-column decoder

Column decoder: Takes 3 MSB's of the digital input (Let 'n' be the value of the 3 bits in decimal) and produces a thermometer output consisting 1's as the (n+1) LSB's

Row decoder: Takes the next 3 bits of the digital input and produces a thermometer output consisting 1's as the (n) least significant bits

Decoding Logic: Thermometer cells are activated according to the logic $(C_n . R_n) + C_{n+1}$

According to this, in the DAC block diagram, all the thermometer cells in the first 'n' columns and the first 'n' cells in the (n+1)th column contribute to the output current I_{OP}.

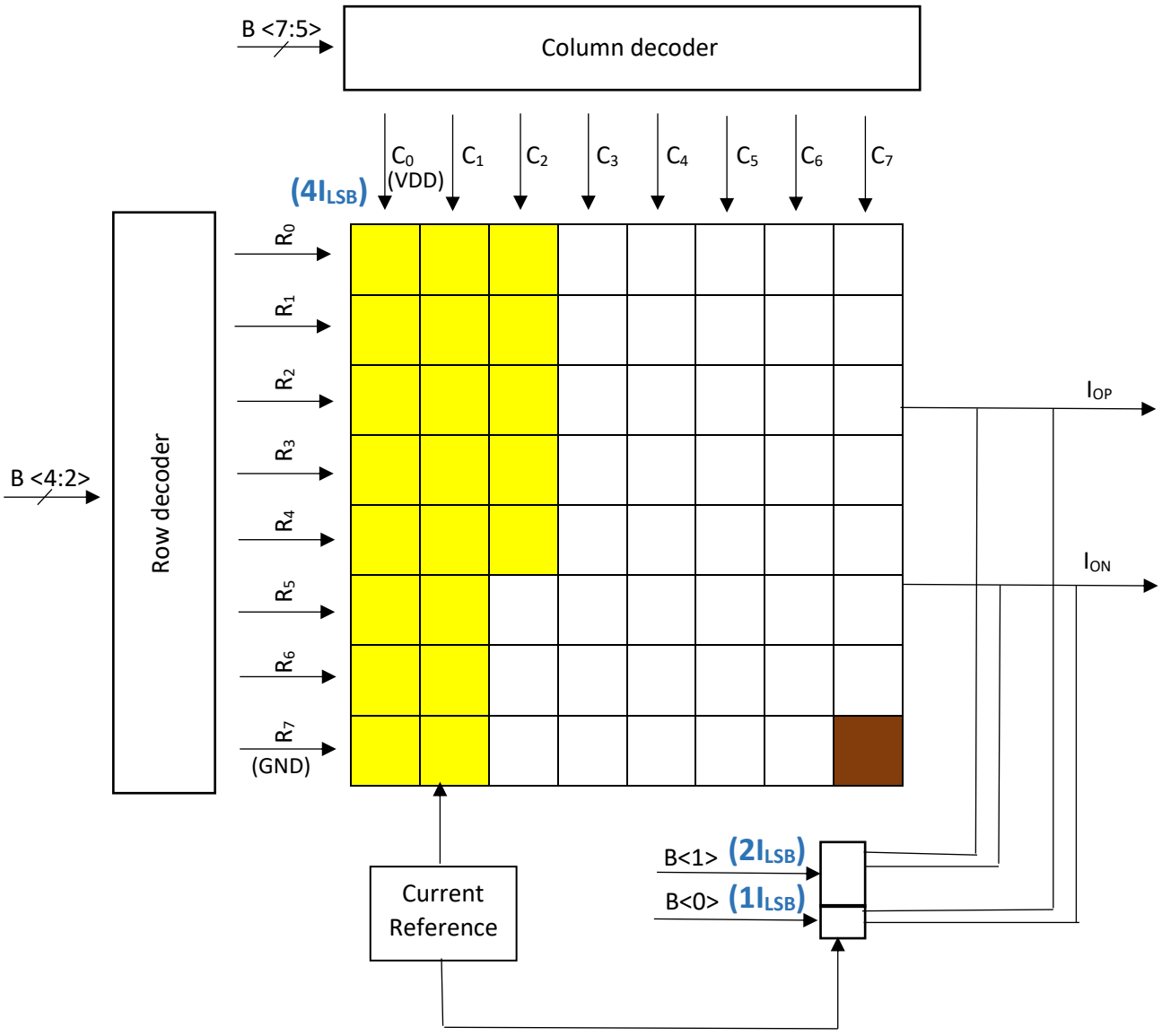
Digital code (B < 7 : 0 >): 01010100

$$B < 7:5 > = 010$$

$$\Rightarrow Column\ decoder\ output = 00000111$$

$$B < 4:2 > = 101$$

$$\Rightarrow Row\ decoder\ output = 00011111$$



Digital code (B < 7 : 0 >): 01110100

$$B < 7{:}5 > = 011$$

$$\Rightarrow Column\ decoder\ output = 00001111$$

$$B < 4{:}2 > = 101$$

$$\Rightarrow Row\ decoder\ output = 00011111$$