C009884

Sl. No. :

SASTRA UNIVERSITY

(A University established under section 3 of the UGC Act, 1956)

Thanjavur - 613 402, Tamil Nadu, India.

Cumulative Grade Sheet

M.Tech Degree Examinations 2007 - 2009

Register Number : **010940004** Name of the Candidate : **Manikandan, V**

Programme : **VLSI Design**

Course Code	Name of the Subject / Course	Semester	Credit	Grade	Month & Year of Passing
	Semester-1				
MVLD101R01	BASICS OF VLSI	1	4	C	Nov -2007
MVLD102R01	SEMICONDUCTOR PHYSICS AND PROCESSING	1	4	B	Nov -2007
MVLD103R01	MODELLING OF DIGITAL SYSTEMS USING HDL	1	4	A	Nov -2007
MVLD104E01	COMPUTER ARCHITECTURE	1	3	B	Nov -2007
MVLD105E10	DIGITAL SIGNAL PROCESSING SYSTEMS	1	3	B	Nov -2007
MVLD106R01	MODELLING LAB	1	2	S	Nov -2007
MVLD107R02	DESIGN LAB - I	1	1	B	Nov -2007
	Semester-2				
MVLD201R01	VLSI SYSTEM DESIGN AND TESTING	2	4	A	May -2008
MVLD202R01	ANALOG VLSI	2	4	A	May -2008
MVLD203R01	CAD FOR VLSI	2	3	S	May -2008
MVLD204E03	APPLICATION SPECIFIC INTEGRATED CIRCUITS	2	3	A	May -2008
MVLD205E11	EMBEDDED SYSTEMS DESIGN	2	3	S	May -2008
MVLD206R01	DESIGN LAB - II	2	1	A	May -2008
MVLD207R01	MINI PROJECT	2	2	A	May -2008
MVLD208R01	SEMINAR	2	2	A	May -2008
	Semester-3 & 4				
MVLD301R01	PROJECT WORK & VIVA VOCE	3 & 4	20	S	May -2009

Total Credits : **63** CGPA: **8.5873**

1. Semesters 1 to 4 total CGPA secured **8.5873**

FINAL RESULT: PASSED IN FIRST CLASS WITH DISTINCTION

Place : SASTRA, THANJAVUR.

Date : 12-06-2009

Controller of Examinations

CONTROLLER OF EXAMINATIONS * SASTRA UNIVERSITY * TIRUMALAISAMUDRAM THANJAVUR - 613 402.