# **CS-311 Assignment-5 Lab Report**

K.S.N Manikanta(210010050) M. Suresh (210010030)

Results:

|  |  |  |  |
| --- | --- | --- | --- |
| *Program* | *No. of instructions* | *No. of cycles* | *Throughput(IPC)* |
| descending.out | 277 | 11779 | 0.023516428 |
| evenorodd.out | 6 | 259 | 0.023166023 |
| fibonacci.out | 78 | 3581 | 0.021781625 |
| palindrome.out | 49 | 2062 | 0.023763336 |
| prime.out | 29 | 1219 | 0.023789993 |

Observations:

We can see that the number of cycles for each benchmark program has increased compared to the number of cycles we got for the pipelined processor in assignment 4. The throughput of an ideal pipelined processor is 1 whereas the throughputs(IPC) we obtained for the benchmark programs are around 0.021-0.024. The increase in the number of cycles is due to the latency of the main memory access, i.e., more number of cycles are taken to access the memory for operations like memory read in the instruction fetch stage, memory write in the memory access stage and so on.