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Hardware demonstration of stochastic p-bits for invertible logic

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Abstract

The common feature of nearly all logic and memory devices is that they make use of stable units to represent 0's and 1's. A completely different paradigm is based on three-terminal stochastic units which could be called "p-bits, where the output is a random telegraphic signal continuously fluctuating between 0 and 1 with a tunable mean. p-bits can be interconnected to receive weighted contributions from others in a network, and these weighted contributions can be chosen to not only solve problems of optimization and inference but also to implement precise Boolean functions in an inverted mode. This inverted operation of Boolean gates is particularly striking: They provide inputs consistent to a given output along with unique outputs to a given set of inputs. The existing demonstrations of accurate invertible logic are intriguing, but will these striking properties observed in computer simulations carry over to hardware implementations? This paper uses individual micro controllers to emulate p-bits, and we present results for a 4-bit ripple carry adder with 48 p-bits and a 4-bit multiplier with 46 p-bits working in inverted mode as a factorizer. Our results constitute a first step towards implementing p-bits with nano devices, like stochastic Magnetic Tunnel Junctions.

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INTRODUCTION

Contemporary logic and memory devices are largely built from standard MOS (metal-oxide-semiconductor) transistors, but the possibility of alternative devices based on new materials and phenomena for both Boolean and non-Boolean computation has been discussed extensively (see for example, [1]). The common feature of nearly all such devices is that they make use of stable and deterministic units to represent 0's and 1's. A completely different paradigm is based on three-terminal stochastic units where the output is a random telegraphic signal $m_i(t)$ that continuously fluctuates between 0 and 1 and the mean value can be tuned with an analog signal $I_i(t)$ at the input terminal. In mathematical terms

$$\mathrm{m_i(t) = sgn\Big\{ rand(-1,1) + \tanh\big(I_i(t)\big)\Big\}} \tag{1}$$

where rand(−1,+1) represents a random number uniformly distributed between −1 and +1, and τ_N is assumed large enough that memory of the last state $\mathrm{m_i(t)}$ has been lost. If the input is zero, the output $\mathrm{m_i(t, t+\tau_N)}$ takes on a value of −1 or +1 with equal probability. A negative input I_i makes negative values more likely while a positive input makes positive values more likely.

Each such unit could be called a "p-bit" with an apparent similarity to [2], and many such units can be correlated to perform useful functions by building an interconnected network where the analog input to the $\mathrm{i^{th}}$ p-bit consists of a bias $\mathrm{h_i}$ added to a weighted sum of the outputs $\mathrm{m_j(t)}$ of the other p-bits:

$$\mathrm{I_i(t+\tau_{sample}) = I_0\Big\{ h_i + \sum_j J_{ij} m_j(t)\Big\}} \tag{2}$$

We have recently shown that with a proper choice of the matrices {h} and [J], p-bit networks could be not only used to solve problems of optimization and inference [3, 4] but also to implement precise Boolean functions in an invertible mode [5, 6].

This invertible operation of Boolean gates is a particularly striking characteristic very different from standard digital gates which provide a unique output in response to a set of inputs. This is also true of a Boolean gate implemented with p-bits, but it additionally provides all the inputs that are consistent with a given output. Even when there is no unique input, the gate fluctuates among the multiple allowed inputs.

The inverse operation is made possible by the bidirectional nature of the interconnection matrix $[J]$ whereby both $\mathrm{J_{ij}}$ and $\mathrm{J_{ji}}$ are generally non-zero so that any two p-bits, say "i" and "j", influence each other, unlike standard digital logic with directed connections. A Boltzmann Machine (BM) [7] with fully bidirectional connections, (all $\mathrm{J_{ij} = J_{ji}}$) , would put inputs and outputs on an equal footing. However, a BM would normally provide approximate answers without the kind of accuracy expected from digital logic. A directed network of bidirectional BM's, on the other hand, has been shown to provide a striking combination of digital accuracy and logical invertibility.

These demonstrations of accurate invertible logic are intriguing, but they are based on purely software implementations of Eqs. (1,2) and it is natural to ask whether real hardware implementations of these equations would preserve these striking properties. This paper represents a first step in answering these questions using individual microcontrollers to emulate p-bits described by Eq. (1), while the interconnections described by Eq. (2) are implemented by another microcontroller. This approach is quite similar to [8].

While the long term goal is to develop miniature integratable devices, the hardware emulation presented here has many of its important features. The variables $m_i(t)$ and $I_i(t)$ appearing in Eqs. (1) and (2) are not symbols represented in software, but actual voltages that can be observed and measured with oscilloscopes and voltmeters. The variability in the operation of real p-bits can be included by programming each microcontroller to have a different retention time, τ_N. Interconnect delays can be included into Eq. (2) as desired.

Note that hardware implementations of Boltzmann Machines exist where Eq.(2) is implemented in dedicated hardware while Eq. (1) has been simulated off chip. Both Eq. (1,2)have have been used as basis for dedicated VLSI based hardware implementations that perform various combinatorial optimization problems [9, 10] as well as hybrid architectures in context of learning [11–16] and combinatorial optimization [17]. This work, however, is focused on invertible Boolean logic, and is configured in a way that should be isomorphic with actual hardware implementations, where each microcontroller emulates a p-bit could be replaced with a specific hardware unit, such as a stochastic magnetic tunnel junction [18, 19], as we progress.

Next we describe the approach we are using to perform a hardware emulation of Eqs. (1) and (2). We first present a 3 p-bit Boltzmann Machine implementing an AND gate in both direct and inverted modes of operation (Figs. 2,3) and evaluate the role of sampling and retention times in ensuring proper operation (Figs. 4,5). We then present results for binary adders in both direct and inverted modes (Figs. 6,7), and end with results for a 4-bit multiplier working in the inverted mode as a factorizer (Fig. 8).

METHODS

Arduino pro mini as a p-bit

A version of Eq. (1) suitable for microcontroller based emulation of a p-bit is given as

$$V_{OUT}(t) = \mathrm{sgn}\Big\{\mathrm{rand}\big(-1, 0\big) + S\big(V_{IN}(t)\big)\Big\} \tag{3}$$

where V_{OUT} and V_{IN} are the digital output and analog input voltages of the p-bit and S(x) is a sigmoidal function given by,

$$S(x) = \frac{1}{1 + e^{-2x}} \tag{4}$$

I/O characteristics: An Arduino pro mini is a 24 pin microcontroller [20] that can be programmed to emulate the behavior of Eq. (3) as shown in Algorithm 1. It has 6 dedicated analog input pins that have very high input resistances (100 MΩ) along with 6 dedicated PWM (Pulse-width modulation) output pins that have very low output resistances (100 Ω) with the ability to source 40 mA of current. This allows the Arduino to behave as a voltage controlled voltage source.

p-bit operation: The time evolution of the output voltage for a set of input voltages using an oscilloscope (Tektronix DPO7104) is shown in Fig. 1(a). As the input voltage is varied from low to high, the microcontroller generates more 1's than 0's. DC average measurements of the output voltage taken over 100 seconds are also shown in Fig. 1(b). The average voltage follows the sigmoidal function which indicates the tunable nature of the p-bit.

Retention time τ_N: Each p-bit is characterized by a retention time (τ_N) for which the output voltage is held constant. A possible physical component in the implementation of p-bits is the superparamagnet [5]:

$$\tau_N = \tau_0 \exp\left(\frac{\Delta}{kT}\right) \tag{5}$$

where τ_0 is a material dependent quantity ranging from 1 ps to 1 ns [21], Δ is the energy barrier of the nanomagnet and kT is the Boltzmann energy. For superparamagnets that are in the 10−20 kT range, the characteristic time is in the ms regime, assuming a τ_0 of 1 ns. We emulate the retention time in our p-bits using a user defined delay τ_N as shown in Algorithm 1. We later study the effect of retention time and establish some essential rules for proper operation of our interconnected p-bits.

Algorithm 1 Pseudocode for p-bit

Parameters:
Digital output V_{OUT};
Analog input V_{IN};
Repeat:
$x \leftarrow$analogRead(V_{IN}); ▷ $V_{IN} \in (0, 5\ V), x \in (0.5)$
$m \leftarrow 2x - 5$; ▷ $m \in (-5, 5)$
Bias $\leftarrow$ S(m); ▷ Bias $\in (0, 1)$ from Eq.(4)
W $\leftarrow$ rand(0, 1); ▷ W $\sim$ U(0, 1)
If(Bias > W)
  $V_{OUT} \leftarrow 1$;
Else ▷ $V_{OUT} \in \{0, 5\ V\}$
  $V_{OUT} \leftarrow 0$;
EndIf
Wait τ_N;
EndRepeat

Weight Logic using microcontroller and DAC

Fig. 2(a,b) shows a schematic and a block diagram for a 3 p-bit Boltzmann Machine that is programmed as an AND gate. The electrical wires connecting the components are not shown for clarity. The p-bits are correlated using a weight logic block that computes the input voltage of the i^{th} p-bit using the output voltages of all other p-bits in the network using

$$V_{IN}(t + \tau_{sample}) = I_0\left(h_i + \sum_j J_{ij} V_{OUT}(t)\right) \tag{6}$$

where τ_{sample} is the time interval for which the input voltages are held constant. Eq. (6) is a modified version of Eq. (2), meant to be used for our voltage controlled voltage source p-bits.

Arduino mega as weight logic: Our weight logic is implemented using an Arduino mega microcontroller in conjunction with MAXIM 5825 Digital to Analog converters [22].

The Arduino mega can read as many as 52 digital inputs and communicates with the DAC using a fast I_2C protocol. The DAC has 8 channels with each having a 10-bit resolution. A pseudocode for programming an Arduino mega to emulate Eq. (6) is given in Algorithm 2. The input voltages of the p-bits set by Eq. (6) are not constrained in general, however we limit them to the p-bit input range between 0 and 5 Volts. Note that the weight logic not only correlates the p-bits, but can also be used for monitoring and recording the state of the Boltzmann Machines. Fig. 2(c,d,e) show two possible methods for monitoring the state of the system which are,

- **Artificial nodes set through the DAC:** The microcontroller and the DAC can be used to create artificial voltage nodes that can be used to concurrently read the output of the p-bits as a single voltage. For example, in the operation of the AND gate ($A \cap B = C$), $4\times A+2\times B+C$ is evaluated and set as a voltage in Fig. 2(c) to monitor the state of the AND gate.

- **Serial logging:** The microcontroller that is part of the weight logic can also be used to log data through a serial port connection (USB). We have used this method extensively for collecting steady-state (long time) statistics for the various Boltzmann Machines that we present in this paper.

Note that even though artificial nodes can be used to monitor the correlations of p-bits, serial logging of the data is much more convenient to collect long time statistics.

Communication between the DAC and Arduino mega: The DACs use the I_2C protocol that allows the Arduino mega microcontroller to communicate with two pins SDA(Data) and SCL(Clock). When the system is first turned on, the DACs need to be initialized. This requires knowing the addresses of the individual DACs that are connected and setting a reference voltage for the DAC. We utilize at most 2 DACs within a Boltzmann Machine and the addresses for those are adjusted using two jumpers on the DAC. For example, to write a voltage of 2.5 V to channel 4 of the DAC whose address is set at "0x20", we could send the following 4 bytes over the I_2C interface: byte1 [0010000], byte2 [10110011], byte3 [10000000], byte4 [00000000]. The first byte has the address of the DAC in its 4 LSBs. The 4 MSBs of byte 2 has a command signal of writing to whichever channel is specified by the 4 LSBs of byte 2. The first 10 bits of byte 3 and 4 are the decimal equivalent of 512 which constitutes 2.5 V for a 10 bit DAC with 5V reference voltage. A library was written to internalize these operations, allowing the user to simply set voltages using a single write command that only uses the channel number and voltage for operation.

Algorithm 2 Pseudo code for weight logic

Parameters:

Analog outputs V_{IN}; ▷ The input voltages of p-bits
Digital inputs V_{OUT}; ▷ The output voltages of p-bits
Parameters [J],{h} and I_0;
$n \leftarrow$ Number of p-bits;
$k \leftarrow$ DAC terminal for word;

Repeat:

For i $\in \{1 \cdots, n\}$
  S $\leftarrow$ digitalRead(V_{OUT}[i]); ▷ $V_{OUT} \in \{0, 5V\}, S \in \{0, 1\}$
  m $\leftarrow 2S - 1$; ▷ m $\in \{-1, 1\}$
EndFor
For j $\in \{1 \cdots, n\}$
  Evaluate $I_j^{'} \leftarrow I_0\big(h_j + \sum_j J_{ij} m_j\big)$ ▷ $I_j^{'} \in (-\infty, +\infty)$
  If($I_j^{'} > 5$)
    $I_j = 5$;
  ElseIf($I_j^{'} < -5$)
    $I_j = -5$; ▷ $I_j \in (-5, +5)$
  EndIf
  $V_{IN}[j] \leftarrow 2I_j - 5$ ▷ $V_{IN} \in (0, +5V)$
  Set DAC[j] $\leftarrow V_{IN}$[j]
EndFor
Set DAC[k] $\leftarrow 4 \times V_{OUTA} + 2 \times V_{OUTB} + V_{OUTC}$ ▷ Output word
Set Serial() $\leftarrow V_{OUT}$ for all p-bits ▷ Output through the USB port
Wait τ_D ;

EndRepeat

RESULTS

AND Gate as a Boltzmann Machine

Correlated network of p-bits: Fig. 2(c) shows the output voltage of an artificial node (4×A+2×B+C) as a function of time on the oscilloscope. For the AND gate the [J] and $\{h\}$ are taken from [23]. The strength of correlation between p-bits is adjusted through the parameter I_0 in Eq. (2). I_0 can be thought as the inverse (pseudo) temperature, in the sense that as I_0 increases the p-bits get strongly correlated. When the system is uncorrelated by using a $I_0 = 0$, the 3 p-bits are independent of each other, resulting in the artificial node being uniformly distributed between 0 and 7, which can be seen from the steady state statistics for $I_0 = 0$ as shown in Fig. 2(d). However, when the system is correlated using an $I_0 = 0.8$, it locks to the states prescribed by [J] and {h} matrices, corresponding to the lines of the truth table for an AND gate which is shown by the steady-state statistics for $I_0 = 0.8$ in Fig. 2(e). Note that we have left all the inputs and outputs floating, which results in all the lines of the truth table getting highlighted as I_0 is increased. This "floating" mode of operation is a unique feature of correlated p-bits. The statistics shown in Fig. 2(d,e) have been collected through serial logging through the weight logic for up to half a million

samples.

Clamping p-bits: For Boolean computation, the p-bits need to be *clamped* to produce a given output. This is done by simply connecting the input voltage of the p-bit to either ground or 5 V. This in essence corresponds to applying a large bias, h_i, to a given p-bit according to Eq. (6). A clamped p-bit operates on the corners of the sigmoidal response shown in Fig. 1(b). Note that the input and output bits of a Boltzmann Machine are on an equal footing and can be clamped for direct and inverted operation respectively, as we discuss below.

Direct Operation: Fig. 3 shows two cases of using an AND gate for computation purposes. Fig. 3(a) shows the time evolution of output voltages of p-bits A and B being clamped to 1 on the oscilloscope. As a result, the output voltages of C mostly stay in 1 as shown. This is also confirmed by the steady state statistics shown in Fig. 3(b) which are acquired using serial logging through the weight logic.

Inverted Operation: A remarkable feature of the design is the *inverted* operation. Fig. 3(c) shows the time evolution of output voltages for A, B and C when C is clamped to 0. It can be seen that A and B follow the states prescribed by lines of the truth table of an AND gate, as shown in Fig. 3(d). This feature stems from the fact that the system places all p-bits, whether input or output, on an equal footing. It is this inverted operation that can be used to solve more complex problems such as the 4-bit factorizer presented later in this paper.

Sampling and retention time

Consider the Boltzmann Machine presented in Fig. 2. For each such network there are two major time constants:

- Retention time τ_N : Time inverval for which the output voltage is held constant by the p-bit.
- Sampling time τ_{sample} : The time interval for which the input voltages to the p-bits are held constant by the weight logic. The sampling time can be thought of as the sum of the user defined delay τ_D of Algorithm 2 and the time it takes to compute everything else in the Repeat block of Algorithm 2.

Boltzmann Law: We now study the effect of both these time constants on the operation of the system using the AND gate. For such networks of correlated p-bits, an energy functional E for the state $\{m\} = [m_i, m_j, \cdots]^T$ can be defined as [5]:

$$E(\{m\}) = -I_0\left(\sum_{i,j}\frac{1}{2}\left(J_{ij}m_i m_j\right) + \sum_i h_i m_i\right) \tag{7}$$

The Boltzmann Law accurately captures the steady state probabilities of the system to be in different states $\{m\}$ according to,

$$P(\{m\}) = \frac{\exp(-E)}{\sum_{i,j}\exp(-E)} \tag{8}$$

Sampling time distribution: Fig. 4 shows the steady state statistics of an AND gate with each of the three p-bits having $\tau_N = 200$ ms, with their sampling times τ_{sample} varying

from 1 ms to 400 ms. It can be seen from Fig. 4(a) that for extremely small τ_{sample} the behavior of the system is captured well by the Boltzmann law. However as τ_{sample} is increased to 100 ms, two incorrect states 001 and 110 stand out more. As τ_{sample} is increased to 200 ms, the system breaks down completely, with only the 001 and 110 states being highlighted. This continues for all τ_{sample} greater then 200 ms as shown by $\tau_{\text{sample}} = 400$ ms.

We observe that when the sampling time is close to the retention time ($\tau_{\text{sample}} \approx \tau_{\text{N}}$), p-bits can change their state before their input to the other p-bits are communicated, and this results in an incorrect operation. However, for fast sampling $\tau_{\text{sample}} \gg \tau_{\text{N}}$, the updating is approximately instantaneous. It is important to note that this requirement of $\tau_{\text{sample}} \gg \tau_{\text{N}}$ necessitates a fast weight logic operation in any hardware implementation of p-bits.

An essential requirement for Hopfield networks and unrestricted Boltzmann Machines is the need for sequential updating, where each p-bit is updated serially but in any random order [24, 25], as opposed to parallel updating where each p-bit is updated at once. Serial updating arises naturally in our setup since each p-bit is completely independent of each other and small phase differences that are present initially get greatly magnified as the system is run for longer periods of time, in the absence of a central clock signal. This type of updating is also known as the "asynchronous dynamic" in Hopfield networks [24].

Retention time distribution: We now investigate the behavior of an AND gate in the presence of p-bits with different retention times that would arise due to inevitable process variations in a nanoscale implementation. Fig. 5(a) shows the histogram for three different retention time configurations of the AND gate. In the most trivial case, all three p-bits have the same retention time $\tau_{\text{N}} = 200$ ms while having a sampling time $\tau_{\text{sample}} = 1$ ms. The steady state statistics for this case exhibit a good match with the Boltzmann law (Fig. 5(b)). However, this configuration is unlikely in the case of any physical system where some distribution is to be expected due to process variations.

A more realistic scenario is that of the 3 p-bits having different retention times. Fig. 5(a) shows two cases where p-bits are distributed in two sets of {137, 200, 263} ms and {50, 200, 350} ms with a spread of ±33% and ±75% around the mean value of 200 ms respectively, while maintaining very fast sampling times of $\tau_{\text{sample}} = 1$ ms. Both cases show a good match with the Boltzmann Law (Fig. 5(b)). We conclude that if the sampling time τ_{sample} is much greater than the smallest τ_{N}, the system operation is well described by the Boltzmann Law, which can be attributed to the much reduced probability of parallel updating.

Full Adder as a Boltzmann Machine

Fig. 6(a) shows a schematic of a 14 p-bit Full Adder implemented as a Boltzmann Machine. Of the 14 p-bits only 5 serve as the actual terminals of the Full Adder while the remaining 9 are auxiliary p-bits. The retention and sampling times are chosen as $\tau_{\text{N}} = 200$ ms for all the p-bits with a $\tau_{\text{sample}} = 10$ ms. However, now two DACs are needed to set the input voltages for all the p-bits since each DAC has 8-channels.

The design of [J] and {h} matrices follows the treatment presented in [5]. Direct computations can be performed by clamping p-bits as discussed earlier. Fig. 6(c,d) shows an example of 1-bit binary addition.The inputs A, B and C_{IN} have been clamped to 110 respectively, and the time evolution of output the voltages of S and C_{OUT} are shown in Fig. 6(c) which follow the states prescribed by the truth table of the Full Adder. This can also be seen from the steady state statistics shown in Fig. 6(d) which have been collected through serial logging.

Similar to the AND gate, the Full Adder implemented as a Boltzmann Machine can also be operated in inverted mode. The time evolution of the the inputs A, B and C_{IN} are shown in Fig. 5(e) when the outputs S and C_{OUT} are clamped to 0 and 1 respectively. The inputs A, B and C_{IN} follow the three prescribed states of the Full Adder truth table which is also confirmed by the steady state statistics shown in Fig. 6(f).

Directed Networks of Boltzmann Machines

To build more complex systems, one possible approach is to design the entire system as a single Boltzmann Machine, but the reversible nature of the Boltzmann Machines can hinder in the correct operation of such systems [5]. A more practical alternative is to interconnect simpler Boltzmann Machines with *directed* connections to build up more complex systems such as a 4-bit Ripple Carry Adder (RCA) (Fig.7(a)) or a 4-bit multiplier/factorizer (Fig.8(a)).

Directed Connections: Separate Boltzmann Machines can be connected in a *directed* fashion such that the connections between the two are not reciprocal $J_{ij} \neq J_{ji}$. In hardware, this corresponds to disconnecting the input voltage of p-bit "i" from its native weight logic and connecting to it the output voltage of p-bit "j" from a different Boltzmann Machine so that $J_{ij} = 1$ and $J_{ji} = 0$. Consider the case of a 4-bit adder that is built using a Half Adder and 3 Full Adders. In this case there are 3 directed connections as shown in Fig. 7(a). Each connection takes the output voltage of C_{OUT} of the $(n-1)^{th}$ adder and connects it to the input terminal of C_{IN} of the n^{th} adder. Due to this connection scheme, no information can flow from the n^{th} adder to the $(n-1)^{th}$ adder, which makes the system no longer bidirectional. However, as noted in [5], bidirectional connections of adders hinders proper operation of a n-bit adder. Also note that since the connection from one Boltzmann Machine to another is an electrical connection, the strength of the correlation between the two machines is at most 1 ($J_{ji} = 1$).

4-bit Adder: We next demonstrate the correct operation of a 4-bit RCA comprised of 48 p-bits each having different τ_N as shown in the inset of Fig. 7(d). The values of τ_N are normally distributed around an average of 200 ms with a minimum of 137 ms to a maximum of 263 ms. 4-bit binary addition is performed by clamping the input p-bits of each adder, as demonstrated by the time evolution of the sum shown in Fig. 7(c) with A=10 and B=13 resulting in the sum being 23 when converted to decimal.

Inverted mode: A more remarkable case is that of the sum bits of each of the adders being clamped to S=23, with A and B left floating. In this case, A and B fluctuate among 8 possible integer combinations that satisfy A+B=23. Note that since A and B are 4-digit binary numbers, not all integer combinations can be probed by the system, for example A=22 and B=1. This can be seen from the histogram presented in Fig. 7(f). Although there are 8 peaks in the histogram, the height of each peak is not the same since statistics presented in Fig. 7(f) are not exactly steady state. With 48 p-bits in the system, the number of samples needed for steady state statistics is prohibitively large.

4-bit multiplier/factorizer: In this final example, we show how a standard digital multiplier built out of AND gates and Full Adders can be operated in reverse to function as a factorizer as shown in Fig. 8, similar to what was proposed in [26] in the different context of memcomputing. Implementation of practically useful factorizers usually requires dedicated algorithms, here our purpose is simply to illustrate the remarkable invertibility of directed networks of p-bits.

The block diagram of a digital multiplier is shown in Fig. 8(b). The individual bits of A and B are first multiplied to produce A_1B_1, A_2B_1, A_1B_2 and A_2B_2 which are then added together to produce the product S. To convert this multiplier to a factorizer, we reverse the directed connections from the AND gates to the adders, while keeping the original directed connections of the Full Adders from the LSB to the MSB.

The output voltages from the A_X and B_X (where X is the n^{th} Full Adder) are now sent as inputs to the output p-bits of the 4 AND gates. The 4 AND gates used here are part of one Boltzmann Machine instead of 4 separate Boltzmann Machines. This is because some inputs of the AND gates need to be the clones of each other as they go to different gates. For example, in Fig. 8(b), A_1 is a common input for the two right most AND gates, while A_2 is a common input for the two left most AND gates. The retention and sampling times are chosen as $\tau_N = 200$ ms for all the p-bits with a $\tau_{sample} = 100$ ms.

Fig. 8(c) shows the time evolution of output voltages of A_1, B_1, A_2 and B_2 using an oscilloscope when the sum of the adder is clamped to 6. This results in the input p-bits of the AND gates producing the correct factors of 3×2 and 2×3. This can also be seen by the statistics of the input p-bits of the AND gate as shown in Fig. 8(e). As previously, the heights of both peaks are not the same due to the statistics not being exactly steady state. The results are collected through serial logging via the Boltzmann Machine for the AND gates. For comparison, we also show the statistics for an uncorrelated factorizer where 16 combinations are equally probable as shown in Fig. 8(d).

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AUTHOR CONTRIBUTIONS STATEMENT

All authors (A.Z.P, L.A.G, K.Y.C and S.D.) participated in conducting the experiments, analyzing the results, reviewing, and writing the manuscript.

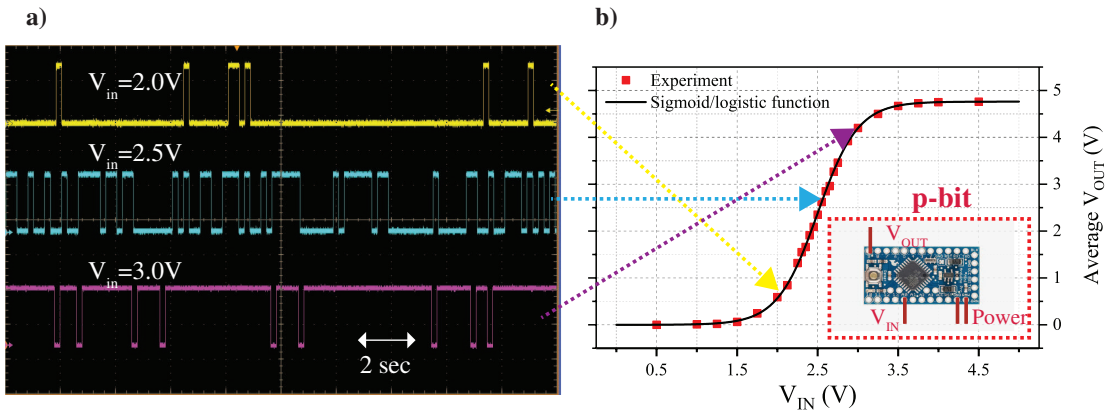


FIG. 1: **p-bit emulated using Arduino microcontroller:** Eq. (1) is emulated using the Arduino mini pro microcontroller as detailed in Algorithm 1. The microcontroller shown in the inset of (b) has dedicated analog input and digital output pins. The time evolution of the output voltages of p-bits is shown in (a) using a Tektronix DPO7104 oscilloscope. The p-bits produce more 1's than 0's as the input voltage is increased, demonstrating the tunable nature of the p-bit. Each of the red markers shown in (b) is a DC average measurement taken for a 100 second interval of the output voltage for a given input voltage. The average output voltages follows the sigmoidal function of Eq. (4).

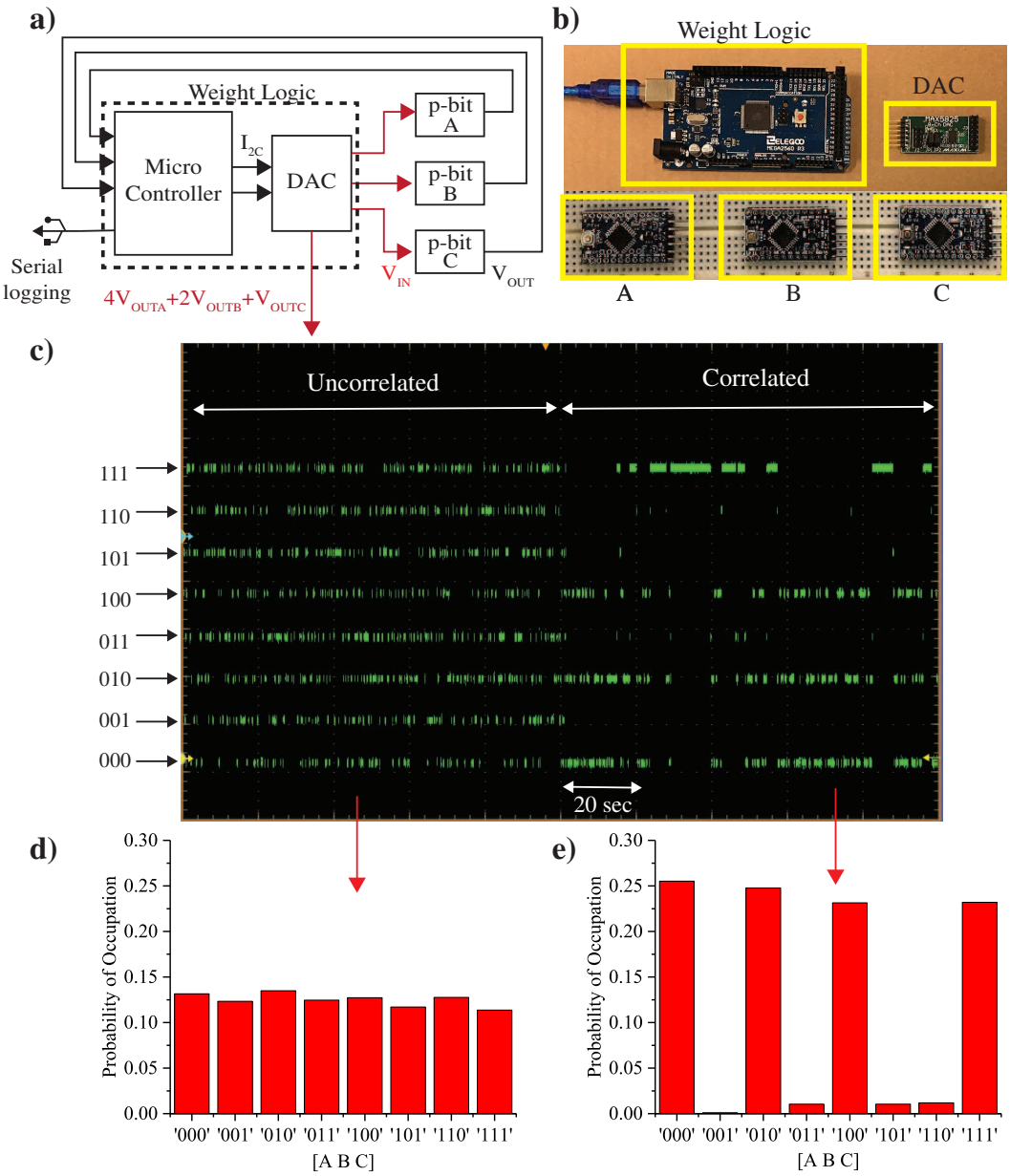


FIG. 2: **AND gate constructed from 3 p-bits:** The block diagram and the schematic of an AND gate constructed using 3 p-bits are shown in (a) and (b). The electrical wires connecting the components are not shown for clarity. A weight logic block is used to correlate the p-bits as detailed in Algorithm 2. The output voltages of the 3 p-bits A, B and C are combined to form an artificial node 4×A+2×B+C, which is set using the DAC and is used to monitor the state of the system as shown in (c). As the system is left uncorrelated, it goes through all possible 8 states of the artificial node with approximately equal probability. When the system is correlated using an $I_0 = 0.8$, it visits the lines of the truth table with approximately equal probability. This is also seen by the steady-state statistics of the two cases presented in (d) and (e).

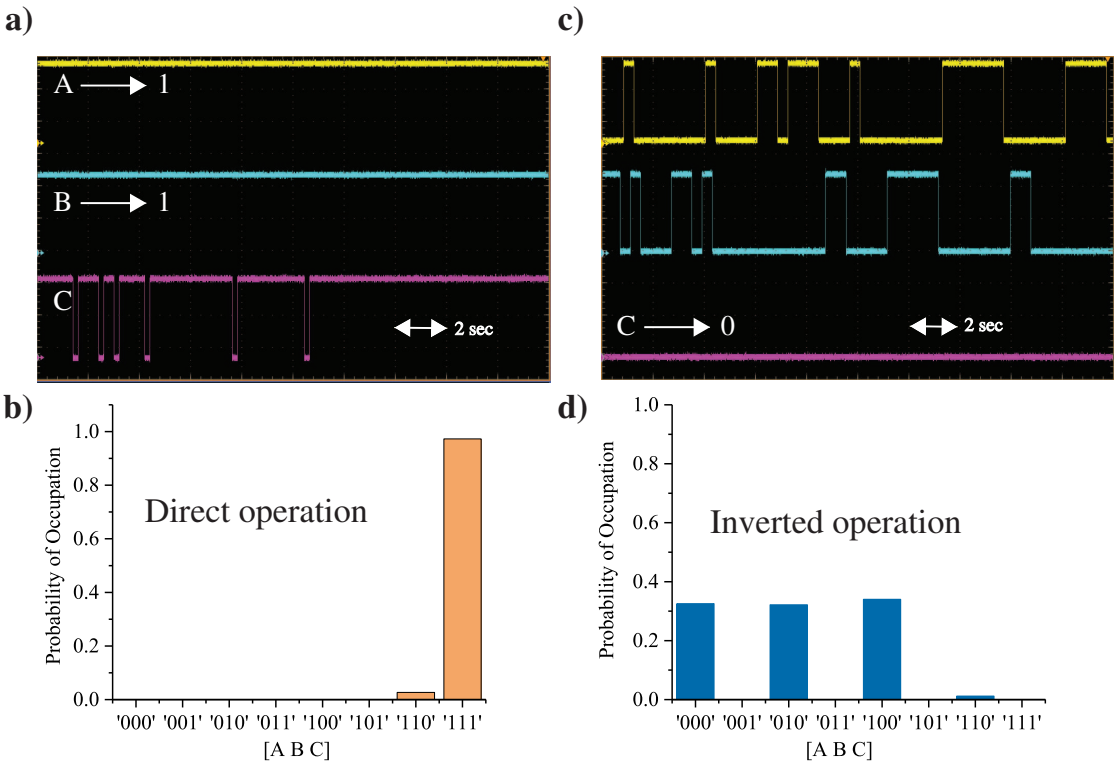


FIG. 3: **Direct and Inverted operation:** (a) shows the time evolution of the output voltages of A, B and C on an oscilloscope. When A and B are clamped to 1, C mostly stays at 1 as shown in (a) and in the steady-state histogram shown in (b). (c) Remarkably, the system can operate in the inverted mode: When C is clamped to 0, the inputs A and B fluctuate between 00, 01 and 10, consistent for a C=0, with approximately equal probability as shown in the steady-state histogram in (d).

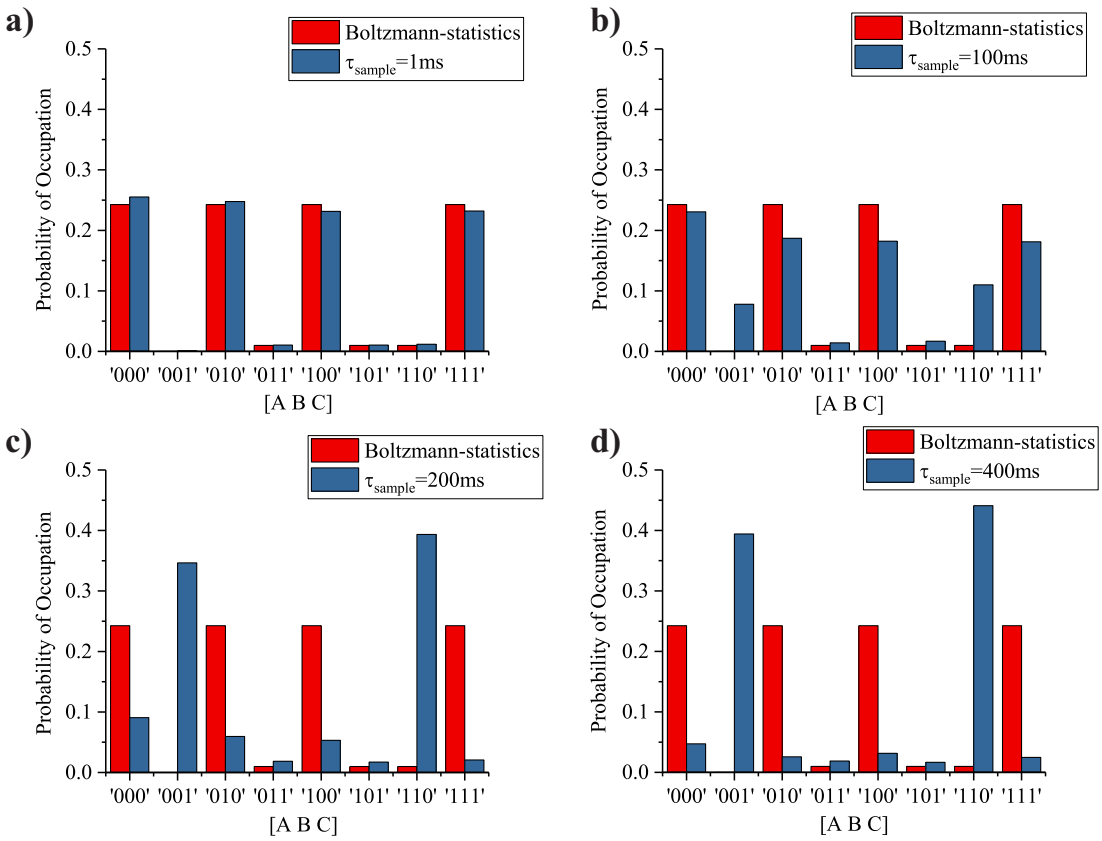


FIG. 4: **Sampling time:** The sampling time τ_{sample} is systematically varied from 1 ms to 400 ms while maintaining a constant retention time of $\tau_{\text{N}} = 200$ ms for each of the 3 p-bits. This is done by changing the user defined delay τ_{D} in Algorithm 2. When $\tau_{\text{sample}} = 1$ ms, sampling is done much faster than the p-bit retention time and for this case steady-state statistics are well-described by the Boltzmann Law. As τ_{sample} is increased to 100 ms becoming comparable to the retention time of p-bits, two erroneous states 001 and 110 get highlighted more. When τ_{sample} is further increased to 200 ms the system completely breaks down. This trend repeates for τ_{sample}=400 ms.

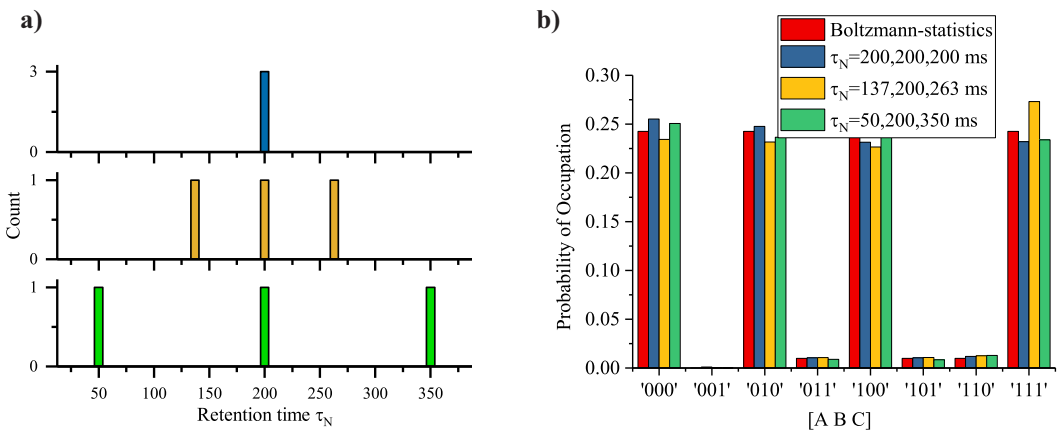
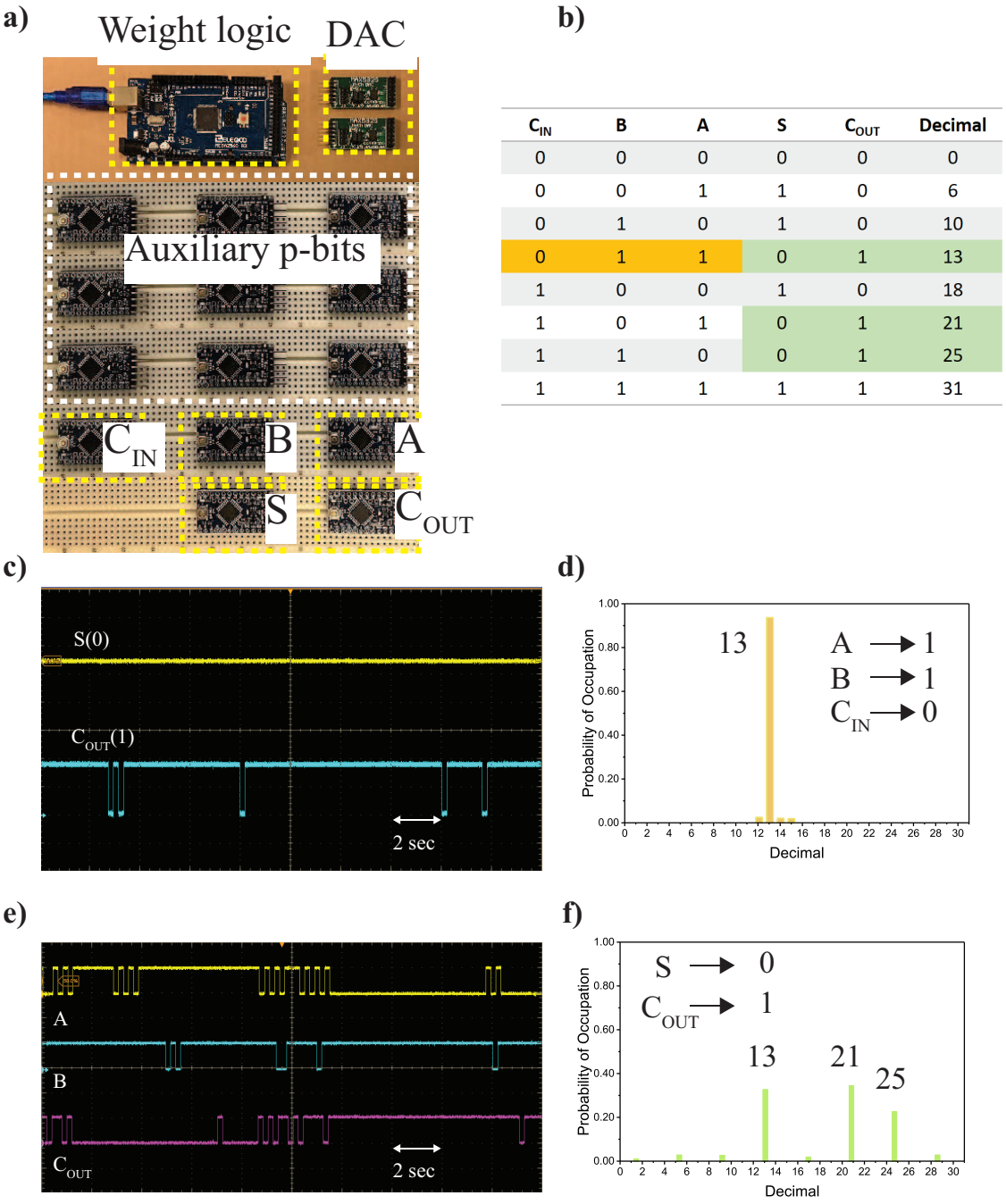


FIG. 5: **p-bit retention time τ_N:** The retention time τ_N of the p-bits is varied while maintaining a sampling time $\tau_{sample} = 1$ ms. This can be done by changing the variable τ_N defined in Algorithm 1. In the most trivial case all 3 p-bits have the same $\tau_N = 200$ ms, while in the other two they are distributed over the mean as shown in histogram of τ_N in (a) with a spread of $\pm 33\%$ and $\pm 75\%$. The steady-state statistics for each of the 3 cases shown in (b) are good matches with Boltzmann Law. This shows that as long as τ_{sample} is much greater than τ_N the system functions properly.



C_{IN}	B	A	S	C_{OUT}	Decimal
0	0	0	0	0	0
0	0	1	1	0	6
0	1	0	1	0	10
0	1	1	0	1	13
1	0	0	1	0	18
1	0	1	0	1	21
1	1	0	0	1	25
1	1	1	1	1	31

FIG. 6: **Full Adder:** A Full Adder is implemented using 14 p-bits as shown in (a) along with its truth table in (b). The electrical wires connecting the components are not shown for clarity. (c) When the inputs A, B and C_{IN} are clamped to 1,1 and 0 respectively, the Full Adder performs binary addition which can be seen from the time evolution of S and C_{OUT} on the osilloscope. (d) The steady-state statistics acquired through serial logging are shown in (d). Since the Full Adder is bidirectional similar to the AND gate, the outputs C_{OUT} and S can be clamped to 1 and 0 respectively, that cause the inputs A, B and C_{IN} fluctuate among three states consistent with lines in the truth table as shown in (e) and (f).

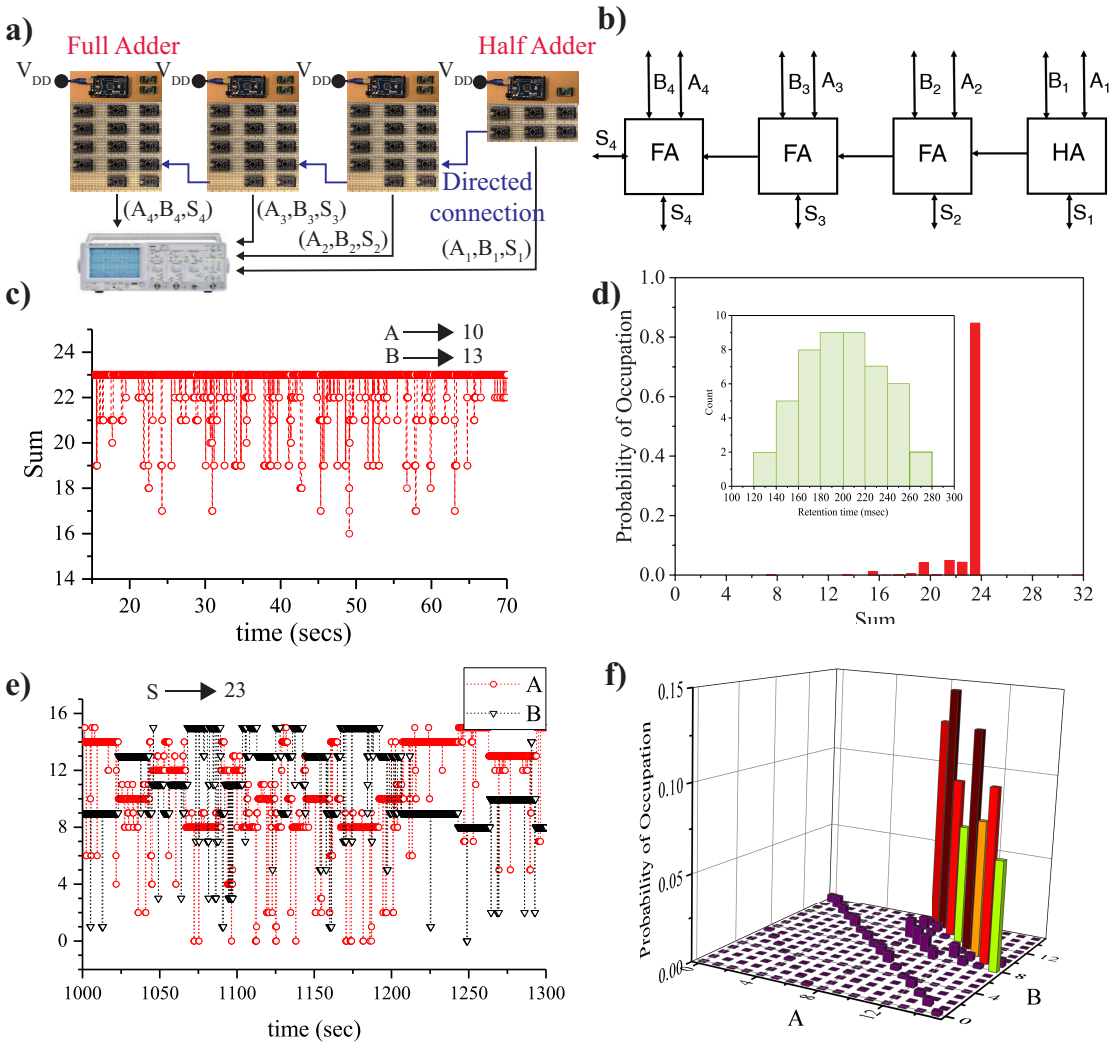


FIG. 7: **4-bit Ripple Carry Adder (RCA)**: A 4-bit adder is implemented using 3 Full Adders and a Half Adder. A schematic and a block diagram are shown in (a) and (b). We assign each p-bit a separate retention time τ_N, with a normal distribution shown in the inset. (c-d) When the inputs are clamped to A = 10 to B = 13 the output S is 23. (e-f) In the inverted mode the output S is clamped to 23, resulting in A and B going through all 8 combinations (that can be probed by 4-digit binary inputs A and B) of producing A+B=S=23.

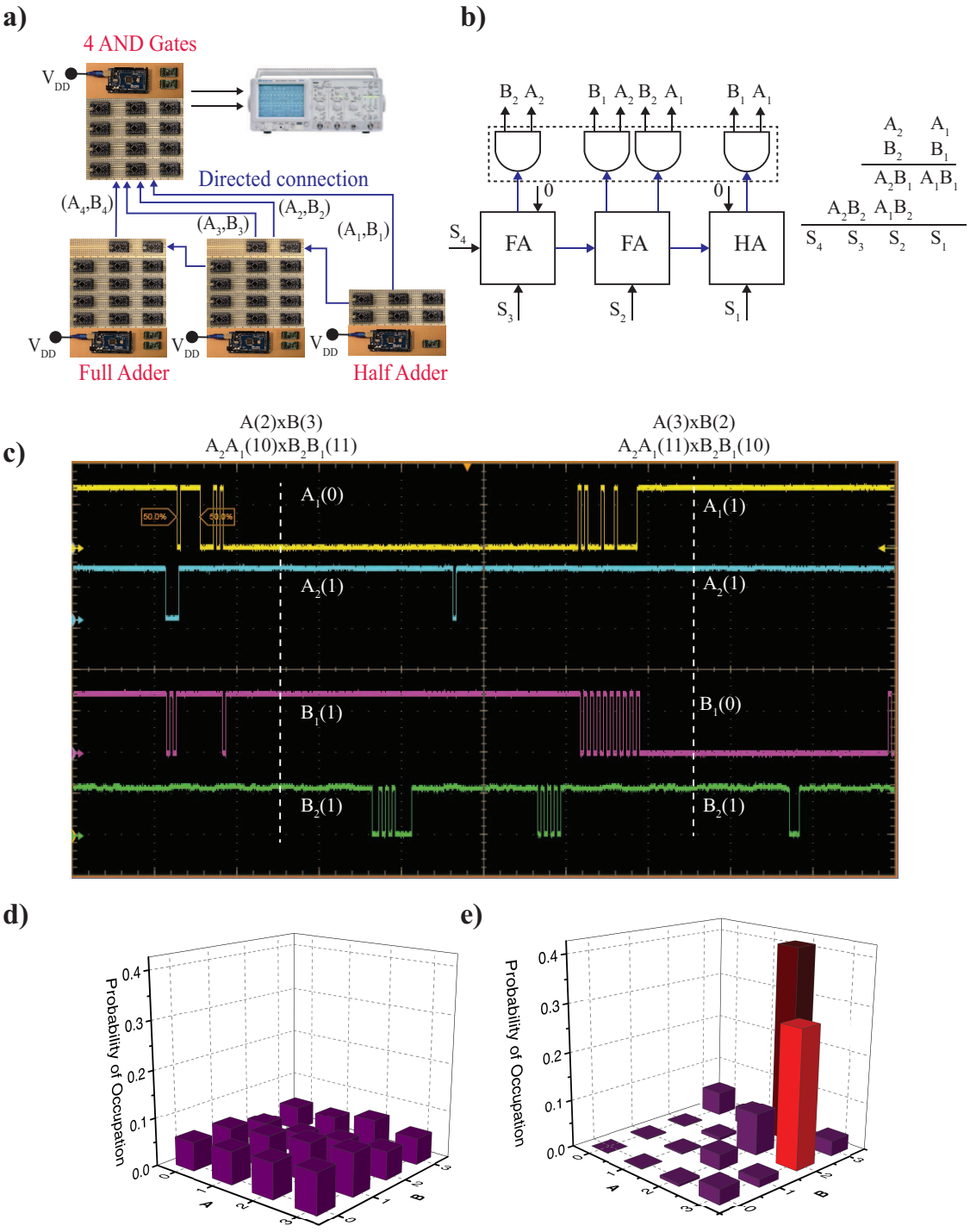


FIG. 8: **4-bit multiplier/factorizer**: A 4-bit multiplier constructed out of 3 Full Adders and 4 AND gates working in inverted mode operates as factorizer. A schematic and a block diagram are shown in (a) and (b). (c) When the sum of the 4-bit adder (product of the multiplier) is clamped to 6, the inputs A and B fluctuate between decimal 2 and 3 with approximately equal probability for the correlated system (e). For the uncorrelated system (f), the inputs fluctuate randomly among 16 possible decimal numbers.