A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations

Tadashi Shibata, *Member, IEEE,* and Tadahiro Ohmi, *Member, IEEE*

***Abstract*—A new functional MOS transistor has been proposed which works more intelligently than a mere switching device. The functional transistor calculates weighted sum of all input signals at the gate level, and controls the "on" and "off" of the transistor based on the result of such a weighted sum operation. Since the function is quite analogous to that of biological neurons, the device is named a neuron MOSFET or neuMOS (vMOS) in short. The device is composed of a floating gate and multiples of input gates that are capacitively interacting with the floating gate. As the gate-level sum operation is performed in a voltage mode utilizing the capacitive coupling effect, essentially no power dissipation occurs in the calculation, making the device ideal for ULSI implementation. The basic characteristics of neuron MOSFET's as well as of simple circuit blocks are analyzed based on a simple transistor model and experiments. Making use of its very powerful function, a number of interesting circuit applications have been explored. neuMOS inverters and neuron circuits, variable-threshold transistors and inverters, linear resistors, and neuMOS source-follower circuits and single-gate D/A converters are described. The concept of *a Soft Hardware Logic Circuit* implemented by neuMOS transistors is also proposed. The circuit exhibits a very interesting feature that the logical function of the circuit is arbitrarily altered by external signals without any changes in the hardware configuration.**

I. Introduction

OVER the past decades, we have experienced a phenomenal growth of the silicon integrated circuits technology. Due to the remarkable progress in the microfabrication techniques, the physical dimensions of transistors have been continuously scaled down. As a result, the number of transistors or functions implemented on a chip have been ever-increasing. It has been almost quadrupled every three years approximately following Moore's prediction in 1975 [1]. Although the scaling approach [2]–[5] has been so successful so far in enhancing the capabilities of silicon chips, a number of severe limitations are now being encountered in terms of material properties, performances of miniaturized devices, and design of ULSI (Ultra Large Scale Integration) circuits and systems.

The electric field strength in Si or in SiO_2 in scaled-down devices, for instance, is now approaching the limit of intrinsic material properties, presenting several reliability issues such as the time-dependent breakdown of thin gate oxide films [6] and hot-electron instabilities of short-channel MOSFET's [7]. Further difficulties are encountered in the interconnect-related technologies. Since ULSI logic circuits require long and entangled interconnections among a huge number of transistors on a chip, signal propagation delays and crosstalk errors in extremely close-packed interconnect structure impose severe limitations on the circuit performance [8]. Large current densities required for driving circuits at high speeds accelerates interconnect failures due to electromigration. All these difficulties, we believe, originate from the fact that sophisticated functions of ULSI systems are realized solely depending on a very primitive function of a transistor, i.e., the current switching function, and that the enhancement in the function of a system is only pursued by simply increasing the number of transistors integrated on a chip. What we are proposing in this paper is the enhancement in the basic function of a single transistor.

A new functional MOS transistor proposed in this paper behaves much more intelligently than a mere switching transistor does. The transistor can calculate the weighted sum of all input signals at the gate level, and controls the "on" and "off" of the transistor based on the result of such a weighted sum calculation [9], [10]. Since the function is quite analogous to that of a biological neuron [11], the new transistor is called "a neuron MOSFET" or neuMOS (abbreviated as νMOS) in short. The neuron MOSFET is, of course, most suitable to use in constructing neural networks [12]. However, a number of interesting applications have been exploited in digital circuits (binary or multivalued) as well as in analog circuits.

Application to ULSI implementation of multiple-valued logic will be one of the most interesting and promising ones. Multiple-valued ULSI's have a potential advantage over their binary counterparts in that they can provide a means of increasing data processing capability per unit area with a reduced number of interconnections [13]–[15]. This has been demonstrated by new hardware algorithms and their implementation by NMOS [16] and CMOS [17], [18] integrated circuits. In this work [17], however, the weighted sum calculation, the most essential operation,

Manuscript received June 11, 1991; revised November 5, 1991. This work was partially supported by the Ministry of Education, Science and Culture of Japan under Grant-in-Aid for Scientific Research 02402032. Part of this work was carried out in the Super Clean Room of the Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University. The review of this paper was arranged by Associate Editor S. Furukawa.

The authors are with the Department of Electronic Engineering, Faculty of Engineering, Tohoku University, Aza-Aoba, Aramaki, Aobaku, Sendai 980, Japan.

IEEE Log Number 9107573.

was carried out by wired summation of currents each bearing multivalued information. Such current mode calculation certainly increases the power dissipation. Since the νMOS performs the sum operation by a voltage mode utilizing a capacitive coupling effect, essentially no current flows except for the charging and discharging currents. This very low power nature of νMOS is most essential for realizing high-density integration. It is demonstrated in [19] that a MOSFET having an externally adjustable threshold voltage is quite essential for implementing a highly parallel AI processor based on multivalued logic. An SOS MOS transistor applied with a variable substrate bias voltage was employed for the variable-threshold transistor in their work [19]. Such a variable threshold transistor, however, can be implemented much simpler using a νMOS transistor.

Some of other interesting applications of νMOS include: a single device D/A converter; an A/D flash converter implemented with a much lower number of transistors; a *Soft-Hardware-Logic Circuit* in which the logical functions of the circuit can be arbitrarily altered by external signals using the same hardware configuration.

The purpose of this paper is to present the basic idea and characteristics of the functional MOS transistor (neuron MOSFET) and its circuit applications based on model analysis and experiment. In Section II, the basic structure of the device is described and the device characteristics and applications to simple circuits are analyzed based on a simple MOSFET model. The fabrication of νMOS transistors using a double-polysilicon n-channel MOS process and the measurement results are presented in Sections III and IV, respectively. The design of *a Soft Hardware Logic Circuit* is briefly described in Section V in order to demonstrate the versatile features of νMOS in circuit applications. In Section VI, concluding remarks are presented.

II. Basic Structure and Operation of the Functional MOS Transistors

The basic structure of the functional MOS transistor (a neuron MOSFET) is illustrated in Fig. 1(a). It is an n-channel MOS transistor having a gate electrode which is electrically floating. n input gates are capacitively coupled to the floating gate. The terminal voltages and various capacitive coupling coefficients are defined in Fig. 1(b), where ϕ_F is the floating-gate potential, V_1, V_2, $\cdots$, V_n are the input signal voltages, C_1, C_2, $\cdots$, C_n the capacitive coupling coefficients between the floating gate and each of the input gates, C_0 is the capacitive coupling coefficient between the floating gate and the substrate, and Q_0, Q_1, Q_2, $\cdots$, Q_n are the stored charges in each of the capacitors. A symbol representing the device is given in Fig. 1(c).

Let Q_F denote the net charge in the floating gate, which is calculated as

$$Q_F = Q_0 + \sum_{i=1}^{n} (-Q_i) = \sum_{i=0}^{n} C_i(\phi_F - V_i) = \phi_F \sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i. \quad (1)$$

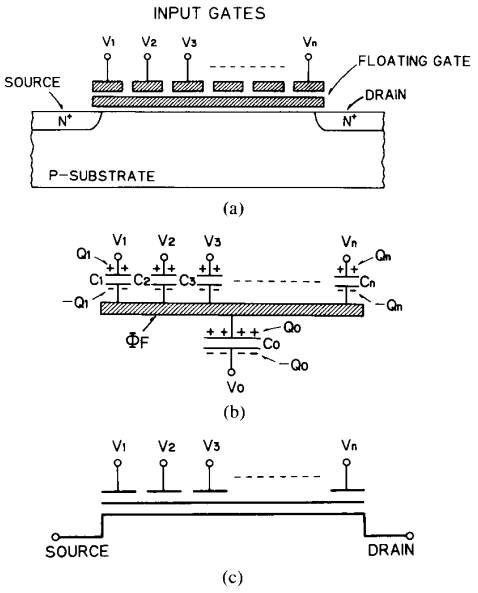


Fig. 1. (a) Conceptual drawing of the basic structure of the functional MOS transistor (neuron MOSFET). The structure is fully compatible to short-channel devices since the coupling capacitor in a real device is formed on field oxide. (See Figs. 4(a) and 8.) (b) Relationship among terminal voltages and capacitance coupling coefficients. (c) The symbol representing the device.

It is assumed that no charge injection occurs during device operation. Then Q_F is equal to the initial charge in the floating gate, which is assumed to be zero at the moment for simplicity. Such assumptions do not prevent generality of the analysis in the following, as is discussed later in this section. All voltages are measured with respect to the ground, and the substrate and source are both grounded; namely, $V_S = V_0 = 0$. Here V_S and V_0 denote the source and substrate potentials, respectively. Then (1) reduces to

$$\phi_F = \frac{C_1 V_1 + C_2 V_2 + \cdots + C_n V_n}{C_{\mathrm{TOT}}} \quad (2)$$

where

$$C_{\mathrm{TOT}} = \sum_{i=0}^{n} C_i.$$

The effect of nonzero substrate potential ($V_0 \neq 0$) will be discussed later in this section.

One of the most important features of this functional device is clearly expressed in (2), which states that the floating-gate potential ϕ_F is determined as a linear sum of all input signals weighted by the capacitive coupling coefficients. The voltage signals are directly added at the gate level without any power dissipation. This voltage-mode summation is the most attractive feature of the capacitive coupling technique as compared to the wired sum of currents [17] in terms of reducing the power dissipation.

Such a capacitive coupling technique using a similar device structure was first implemented in a dual-control-gate EEPROM cell in which two input gates with the same

capacitive coupling coefficients are equipped to control the floating-gate potential [20], [21]. Only when both of the input gates are biased at a programming voltage, the floating-gate potential becomes high enough to cause Fowler–Nordheim tunneling via tunnel oxide for injecting electrons into the floating gate. When either one or both of the two input gates are grounded, injection does not occur, thus realizing selective writing/erasing of a cell in the matrix of cell array. In the present functional MOSFET, however, a number of input gates are interacting with the floating gate via different capacitive coupling coefficients and the potential of the floating gate controls the formation of the channel underneath the gate oxide, i.e., the "on" and "off" of the MOS transistor.

The value of ϕ_F is uniquely determined by (2) provided that all capacitive coupling coefficients are not changing during device operation. Among all C_i's, only C_0 can vary depending on the operating condition of the transistor. However, it can be reasonably well approximated by the gate oxide capacitance when the device is on and the channel is formed, the case of interest in the study of device operation. As long as the channel is formed, the value of C_0 does not vary appreciably and can be regarded as a constant.

Here we would like to introduce a parameter γ which is defined as

$$\gamma \equiv \frac{C_1 + C_2 + \cdots + C_n}{C_{\mathrm{TOT}}} = \frac{C_{\mathrm{TOT}} - C_0}{C_{\mathrm{TOT}}}. \tag{3}$$

γV_{DD} represents the maximum floating-gate voltage obtained as all input gates are at V_{DD}. Since the value is the voltage gain of the floating gate as a result of its capacitive coupling to all of the input gates, γ is called the floating-gate gain factor, one of the key design parameters of the device and circuits.

Let V_{TH}^* be the threshold voltage of the transistor as seen from the floating gate. Then the transistor turns on at the condition of $\phi_F > V_{\mathrm{TH}}^*$, namely

$$\frac{C_1 V_1 + C_2 V_2 + \cdots + C_n V_n}{C_{\mathrm{TOT}}} > V_{\mathrm{TH}}^*. \tag{4}$$

This relationship presents the other important feature of the device, the threshold operation. When the linear weighted sum of all input signals exceeds a certain threshold value V_{TH}^*, the transistor turns on. The behavior of the transistor very well resembles that of a biological neuron if the turn-on of the transistor is correlated to the firing of a neuron [11]. In this respect, we call the new functional MOS transistor a "neuron MOSFET" or a neuMOS in short. Hereafter in this paper, the device is called neuMOS or is abbreviated as νMOS.

The learning function of neural networks, the most important feature of the circuit, however, originates not from the threshold operation of a neuron but from the weight (w_i) that changes with time to optimize the strength of connections for establishing desired responses of a system for problem solving. Such a variable weight connection is called a synapse. However, in the νMOS such weights are fixed because they are determined by the capacitive coupling coefficient of the input gate to the floating gate (C_i/C_{TOT}). In order to build neural network systems using νMOS transistors, all input gates of a νMOS must have an identical capacitive coupling coefficient, and a synapse circuit must be provided to each input gate for variable weight connection. We have proposed a synapse circuit constructed using νMOS transistors, as well, which is free from stand-by power dissipation [12]. The synapse circuit is most appropriate to construct neural networks by combination with artificial neurons implemented by νMOS transistors.

In the following, the most basic applications of νMOS transistors to circuits are presented. Subsection A describes a variable-threshold transistor in which the threshold voltage is arbitrarily altered by an external signal. The implementation of a linear resistor with an adjustable resistance is presented in Subsection B. In Subsection C, a νMOS inverter, one of the most important νMOS circuits, is described. The circuit output changes its state from high to low when the linear weighted sum of all input signals exceeds a certain threshold value. In Subsection D, a circuit which directly outputs the results of weighted sum calculation is presented. Although these circuits are all very simple and primitive, the circuits described in Subsections A, C, and D are particularly important as key components in construction of more complicated and sophisticated νMOS logic circuits and systems.

A. Variable Threshold Transistor

The relation (4) is rearranged for V_1 as

$$V_1 > \frac{C_{\mathrm{TOT}}}{C_1} V_{\mathrm{TH}}^* - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n. \tag{5}$$

If an n-input-gate νMOS is regarded as a single-input-gate MOSFET where gate 1 is the only signal input gate and the other gates are for threshold control, then the threshold voltages of the MOSFET as seen from gate 1 is given by

$$V_{\mathrm{TH}}^{(1)} = \frac{C_{\mathrm{TOT}}}{C_1} V_{\mathrm{TH}}^* - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n. \tag{6}$$

It is obvious that $V_{\mathrm{TH}}^{(1)}$ is determined as a function of control signals $V_2, V_3, \cdots, V_n$.

Consider the simplest case of a two-input-gate νMOS with $C_1 = C_2$, then

$$V_{\mathrm{TH}}^{(1)} = \frac{C_{\mathrm{TOT}}}{C_1} V_{\mathrm{TH}}^* - V_2. \tag{7}$$

Thus the threshold voltage of the MOSFET is controlled by an analog signal V_2. The experimental verification of this relation is presented later in Fig. 10. If the values of coupling capacitances are designed as $C_1 = (1/2)\gamma C_{\mathrm{TOT}}$, $C_a = (1/3)\gamma C_{\mathrm{TOT}}$, and $C_b = (1/6)\gamma C_{\mathrm{TOT}}$ in a three-input-gate νMOS (γ: the floating-gate gain factor defined in (3)), gate 1 threshold (the threshold voltage as seen from gate 1) is controlled by the binary digital signals V_a and

V_b as in the following:

$$V_{TH}^{(1)} = \frac{C_{TOT}}{C_1} V_{TH}^* - \frac{1}{3}(2V_a + V_b). \quad (8)$$

If $(C_{TOT}/C_1)V_{TH}^*$ is taken equal to V_{DD}, i.e., $V_{TH}^* = (1/2)\gamma V_{DD}$, $V_{TH}^{(1)}$ changes as V_{DD}, $(2/3)V_{DD}$, $(1/3)V_{DD}$, and 0 according to $(V_a, V_b) = (0, 0)$, $(0, 1)$, $(1, 0)$, and $(1, 1)$, respectively. Here "1" stands for the input voltage at V_{DD}. These examples here are only the simplest cases demonstrating the principles of variable-threshold transistors implemented by νMOS. A variety of threshold controls is possible by changing the coupling capacitances and the number of control signal inputs.

So far the net charge in the floating gate Q_F has been assumed to be zero. All equations given in this paper are applicable to the cases of nonzero Q_F by just replacing V_{TH}^* by $V_{TH}^* - Q_F/C_{TOT}$. If charge transfer is allowed to occur among the floating gate and some other gates, as in the case of EEPROM cells, this will provide another means of threshold change with its memory function, resulting in further interesting applications such as learning capabilities of synapses [12]. However, in the present paper it is assumed that Q_F does not change during device operation since it is most essential in establishing the reliable operation of νMOS circuits to be described in this paper. In this respect, the employment of the single integrated device structure, as shown later in Fig. 8, is quite essential for realizing capacitive coupling and control of the floating-gate potential. This is because the polysilicon floating gate entirely covered by thermal oxide exhibits an excellent charge retention characteristics, allowing no charge loss or gain due to leakage currents induced during the circuit operation. It is quite difficult to achieve long-term stability of the floating-gate charge using single-gate MOSFET's and externally connected capacitors.

The transconductance of a νMOS transistor as seen from gate 1 is given by

$$g_m^{(1)} = \frac{\partial I_D}{\partial V_1} = \frac{\partial I_D}{\partial \phi_F} \cdot \frac{\partial \phi_F}{\partial V_1} = \frac{C_1}{C_{TOT}} g_m^*$$

where g_m^* denotes the transconductance as seen from the floating gate.

B. Linear Resistor

One of the most primitive νMOS applications, a linear resistor, is described in the following. A MOS transistor is usually used as a resistor either by connecting its gate to the drain or by supplying a constant bias to the gate. However, it exhibits a strong nonlinearity in its current voltage characteristics as exemplified in Fig. 2(a). In order to circumvent the problem, a dual-input-gate νMOS connected as in Fig. 2(b) is proposed. As a result of the competing effects of the constant bias V_1 and the increasing bias V_2 following the drain voltage, it is expected that the convex upward and downward I–V curves in Fig. 2(a) would be somehow averaged to yield a linear relationship. The I–V characteristics of the νMOS under the linear-parabolic regime are obtained by substituting $(w_1 V_1 + w_2 V_2)$ to the gate–source voltage in a simple transistor equation as

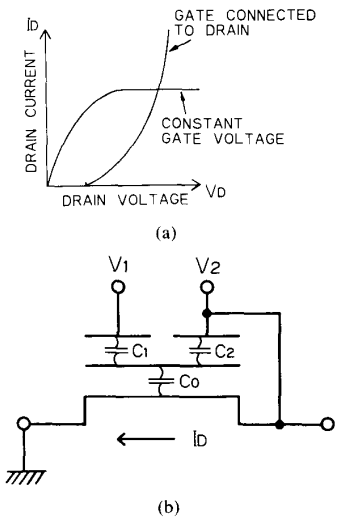


Fig. 2. (a) Current-voltage characteristics of conventional MOSFET's used as resistors. (b) A linear resistor implemented by a two-input gate νMOS by connecting gate 2 to the drain.

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[\left(w_1 V_1 - V_{TH}^*\right)V_D + \left(w_2 - \frac{1}{2}\right)V_D^2\right]. \quad (9)$$

Here V_D, I_D are the drain voltage and current, μ_n the surface electron mobility, C_{OX} the gate oxide capacitance per unit area, W and L the channel width and length, $w_1 = C_1/C_{TOT}$ and $w_2 = C_2/C_{TOT}$. If we take $w_2 = 1/2$, the parabolic term in (9) disappears and a linear relationship is obtained. When the drain voltage increases and satisfies

$$V_D > \frac{w_1}{1 - w_2} V_1 - \frac{1}{1 - w_2} V_{TH}^*$$

the transistor operates in the saturation regime, and the current is given by

$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}\left[(w_1 V_1 - V_{TH}^*) + w_2 V_D\right]^2.$$

The V_D^2 term again appears, but the coefficient is reduced by a factor $w_2^2 (= 1/4)$, thus improving the linearity. Although the discussion here is only valid within the framework of the simple transistor model, it is shown by experiments (in Fig. 14) that nearly linear I–V characteristics are obtained by optimizing the w_1/w_2 ratio.

C. νMOS Inverter

If an inverter circuit is built using a neuron MOSFET and a resistor as shown in Fig. 3(a), the output of the circuit would be that in Fig. 3(b). The output is low when the linear weighted sum of input voltages $\Sigma_{i=1}^n w_i V_i$ is below the floating-gate threshold, and the output becomes high when the sum is larger than the threshold. Here w_i stands for C_i/C_{TOT}. The characteristics are exactly those

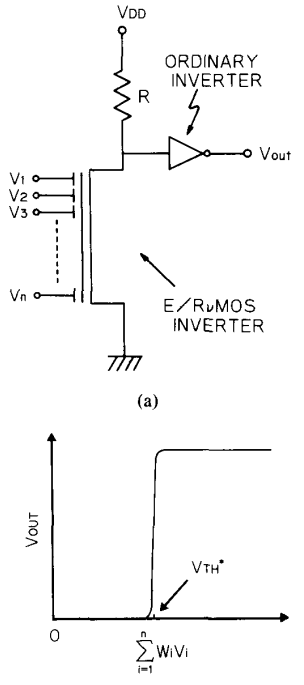


Fig. 3. (a) An n-channel neuron circuit constructed with an n-channel νMOS, resistor, and an ordinary inverter and (b) its typical output characteristics, where $W_i \equiv C_i/C_{\text{TOT}}$.

expected for an artificial neuron [11]. Thus the neuron function can be implemented using such a simple circuit configuration.

Since essentially no dc current flows in the voltage-mode summation, the power dissipation in a neuron circuit shown in Fig. 3(a) mostly occurs in the inverter. In order to suppress the power dissipation as well as to enhance the speed performance, a ratioless-type inverter must be constructed using νMOS transistors. Namely, the employment of CMOS configuration is quite essential. A possible layout and the cross section of a complementary νMOS inverter are depicted in Fig. 4, along with its symbol representation. The n- and p-channel devices are called n-channel νMOS and p-channel νMOS, respectively, and the n-νMOS and p-νMOS both share the same floating gate in the C-νMOS inverter.

The switching threshold voltage of the inverter as seen from the floating gate, V^*_{INV}, is defined as a voltage at which the inverter output becomes $V_{DD}/2$. It is given by

$$V^*_{\text{INV}} = \frac{V_{DD} + \sqrt{\beta_R}\, V^*_{T_n} + V^*_{T_p}}{\sqrt{\beta_R} + 1} \tag{10}$$

where $V^*_{T_n}$ and $V^*_{T_p}$ are the n- and p-channel νMOS threshold voltages as seen from the floating gate, respectively. β_R is the beta ratio

$$\beta_R \equiv \frac{\beta_n}{\beta_P} = \frac{(W/L)_n \mu_n}{(W/L)_p \mu_p} \tag{11}$$

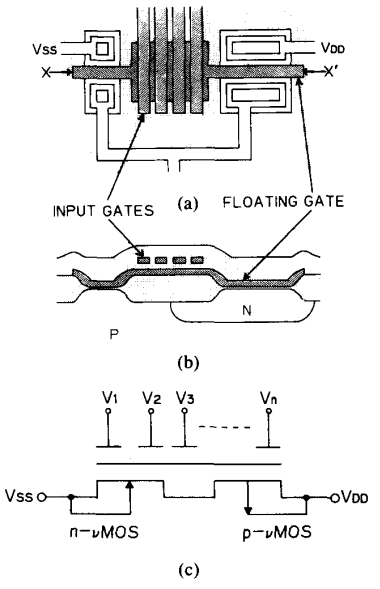


Fig. 4. Complementary νMOS inverter circuit: schematics of (a) possible pattern layout, (b) cross section at X–X', and (c) symbol representation.

where subscripts n and p refer to n- and p-channel, respectively, μ_n and μ_p are the surface mobilities of electrons and holes, respectively. If $\beta_R = 1$, (10) reduces to

$$V^*_{\text{INV}} = \frac{1}{2} V_{DD} + \frac{V^*_{T_n} + V^*_{T_p}}{2}. \tag{12}$$

Here a comment is made on the effect of the substrate potential which has been so far assumed to be zero. The assumption is not valid for the p-νMOS transistor in the inverter configuration because the n-well is biased to V_{DD}. Therefore, corrections need to be made in (2) as follows:

$$\phi_F = \frac{\sum_{i=1}^{n} C_i V_i + C_{0p} V_{DD}}{C_{\text{TOT}}}$$

where C_{0p} is the substrate capacitance of a p-νMOS which can be approximated by the gate oxide capacitance, provided that the p-νMOS is on. Then the basic relation (4) must be revised as

$$\frac{C_1 V_1 + C_2 V_2 + \cdots + C_n V_n}{C_{\text{TOT}}} > V^*_{\text{INV}} - \frac{C_{0p}}{C_{\text{TOT}}} V_{DD}. \tag{4'}$$

Equation (6) that has been derived for the threshold voltage of a variable-threshold transistor can be made applicable to the switching threshold of a C-νMOS inverter by just replacing V^*_{TH} by $V^*_{\text{INV}} - (C_{0p}/C_{\text{TOT}})V_{DD}$. The C-$\nu$MOS inverter threshold as seen from gate 1 is given by

$$V^{(1)}_{\text{INV}} = \frac{C_{\text{TOT}}}{C_1}\left(V^*_{\text{INV}} - \frac{C_{0p}}{C_{\text{TOT}}} V_{DD}\right) - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n.$$

For a two-input gate C-νMOS inverter having identical capacitive coupling coefficients, the switching threshold as seen from gate 1 is given by

$$V_{\mathrm{INV}}^{(1)} = \frac{C_{\mathrm{TOT}}}{C_1}\left(V_{\mathrm{INV}}^{*} - \frac{C_{0p}}{C_{\mathrm{TOT}}} V_{DD}\right) - V_2 \qquad (7')$$

and it reduces to $V_{\mathrm{INV}}^{(1)} = V_{DD} - V_2$ if the value of V_{INV}^{*} is taken as

$$V_{\mathrm{INV}}^{*} - \frac{C_{0p}}{C_{\mathrm{TOT}}} V_{DD} = \frac{1}{2}\gamma V_{DD}. \qquad (13)$$

The threshold as seen from gate 1 for the three-input-gate C-νMOS inverter shown in Fig. 5 is given by

$$V_{\mathrm{INV}}^{(1)} = V_{DD} - \tfrac{1}{3}(2V_a + V_b) \qquad (14)$$

provided V_{INV}^{*} is given by (13). Therefore, $V_{\mathrm{INV}}^{(1)}$ changes as a function of the binary digital control signals V_a and V_b in exactly the same manner as $V_{\mathrm{TH}}^{(1)}$ in (8). Such a variable-threshold inverter is one of the most important key components in construction of the so-called *Soft Hardware Logic Circuit* to be discussed later in Section V.

From (12) and (13), we obtain

$$V_{T_n}^{*} + V_{T_p}^{*} = (\gamma - 1 + 2C_{0p}/C_{\mathrm{TOT}})V_{DD}$$
$$= \frac{C_{0p} - C_{0n}}{C_{\mathrm{TOT}}} V_{DD} \qquad (15)$$

where C_{0p} and C_{0n} denote the gate oxide capacitances of p-νMOS and n-νMOS transistors, respectively. Equation (13) yields the standard setting of V_{INV}^{*} for C-νMOS inverters and (15) specifies the condition to determine the floating-gate threshold voltages for n- and p-νMOS transistors provided $\beta_R = 1$.

D. νMOS Source-Follower Circuit

We have shown that the input signals to a νMOS transistor are summed over with multiplication factors specified by each capacitive coupling coefficient of the respective gate. Therefore, if the floating-gate potential is directly read out as an output voltage, a variety of analog calculations can be performed very simply. This is possible by employing the well-known source-follower circuitry.

Consider a source-follower circuit composed of an n-input-gate n-channel νMOS transistor and a load resistor shown in Fig. 6. If the resistance R is much larger than the on-resistance of the νMOS transistor, the V_{OUT} is given by

$$V_{\mathrm{OUT}} = \phi_F - V_{\mathrm{TH}}^{*}.$$

If the threshold is selected as $V_{\mathrm{TH}}^{*} = 0$, then $V_{\mathrm{OUT}} = \phi_F$. One of the most useful applications of this circuit configuration is a single-device D/A converter, in which the coupling capacitances are designed as $C_i \propto 2^{i-1}$ ($i = 1, 2, 3, \cdots, n$). Then the output voltage is expressed as

$$V_{\mathrm{OUT}} = \frac{\gamma V_{DD}}{2^n - 1}(X_1 + 2X_2 + \cdots + 2^{n-1}X_n) \qquad (16)$$

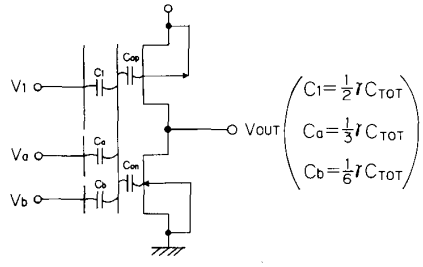


Fig. 5. Variable-threshold C-νMOS inverter where V_1 is the input terminal, and V_a and V_b are the control signal inputs. The inverter switching threshold voltage changes as V_{DD}, $(2/3)V_{DD}$, $(1/3)V_{DD}$, and 0 according to $(V_a, V_b) = (0, 0)$, $(0, 1)$, $(1, 0)$, and $(1, 1)$, respectively.

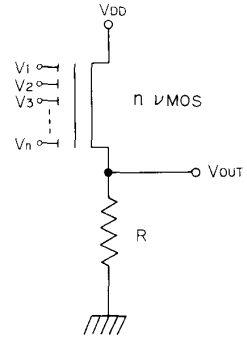


Fig. 6. A source-follower circuit composed of an n-channel νMOS and a load resistor R.

where γ is the floating-gate gain factor and $X_1, X_2, \cdots, X_n$ are binary digital signals, i.e., $V_i = X_i V_{DD}$ and $X_i = 0$ or 1. The output voltage is proportional to an analog value represented by n-bit binary signal inputs. Thus a D/A converter circuit can be very simply constructed. The results of experiments are given later in Fig. 15.

The speed performance of the circuit is limited by the time required for discharging the output node capacitance through the load resistor R. Therefore, the resistance must be reduced to enhance the response. However, it in turn reduces the voltage gain of the circuit, resulting in degraded noise margins. Moreover, the circuit dissipates a stand-by power of V_{OUT}^2/R which is further increased by the reduction in R.

The complementary n- and p-νMOSFET configuration circuit for reading out ϕ_F is demonstrated in Fig. 7. The circuit is basically a source-follower circuit of an n-channel νMOS transistor where a p-channel νMOS is utilized as an active load. The circuit looks like a C-νMOS inverter, but the positions of n- and p-channel devices are interchanged. Such an upside-down complementary νMOS circuit exhibits very interesting features and is called a reciprocal C-νMOS transfer amplifier or simply C-νMOS source-follower. In the charging cycle of the output node, the p-νMOS turns off and serves as an infinitely large load resistor, thus yielding a voltage gain of unity. While in the discharging cycle, the p-νMOS turns on and accelerates discharging. In addition, both n- and

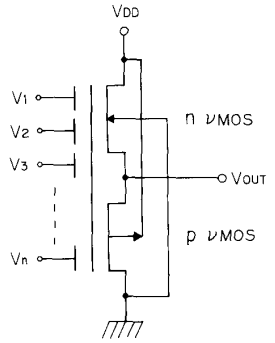


Fig. 7. A complementary νMOS source-follower circuit in which a p-channel νMOS acts as an active load and both n- and p-νMOSFET's share the same floating gate. The circuit is called a reciprocal C-νMOS transfer amplifier.

p-νMOSFET's can be made to operate under a nearly cut-off condition when the circuit is holding a constant voltage level. Thus the power dissipation can be minimized. Therefore, we can expect that high-speed performance is achieved without degrading the voltage gain at relatively low power dissipation.

However, the following issues must be taken into account in the design of power dissipation. The charging of a capacitance load through an enhancement-mode NMOS is a relatively slow process as usually encountered in the turn-off of E/E inverters. In order to enhance the speed performance, as well as to increase the stability and noise margins of νMOS circuit operation, νMOS source-followers must conduct stand-by current to maintain the multi-valued output level. Consequently, the magnitude of the current, and hence the power dissipation, need to be determined as a tradeoff among these issues.

The detailed analysis of C-νMOS source-follower circuit operation as well as the derivation of the quantitative relationship between V_{OUT} and ϕ_F will be described in a separate publication.

III. Experimentation

In order to perform feasibility studies on νMOS transistors and circuits the following experiments were conducted.

νMOS transistors with varying configurations were fabricated by Tohoku University standard double-polysilicon n-channel MOS process. Typical process parameters were: the gate oxide thickness underneath the floating gate varied as 200–500 Å; the interpoly oxide thickness ranging from 500 to 1000 Å; the arsenic-implanted source and drain junction depths of 0.25 μm. Tapered sidewall spacers were formed by depositing CVD SiO_2 followed by RIE at the periphery of the floating gates in order to define accurate control-gate to floating-gate overlap areas as well as to facilitate the directional etching of the second poly. Photomicrographs of fabricated test neuron MOSFET's are shown in Fig. 8 as examples. Detailed description of fabrication process issues will be presented elsewhere. In these test νMOS transistors, the C_0/C_{TOT} ratio

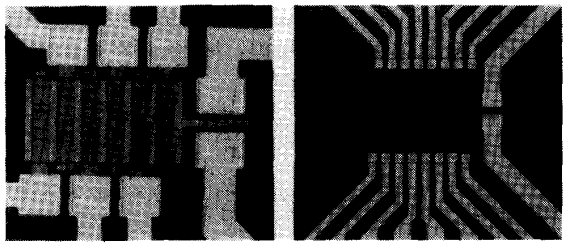


Fig. 8. Photomicrographs of 6-input (left) and 16-input (right) neuron MOSFET's fabricated by Tohoku University Standard Double-Polysilicon NMOS Process.

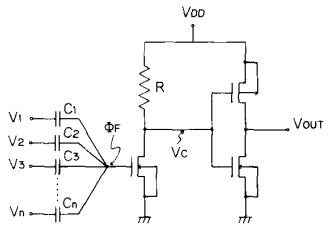


Fig. 9. An n-channel neuron circuit composed of discrete components which has been utilized in the experiment. ϕ_F is the floating-gate potential and V_C the input to the CMOS inverter.

was designed typically in the range of 0.2–0.1 or γ = 0.8–0.9.

The basic structures of νMOS transistors were also constructed using discrete components. Single polysilicon-gate NMOS transistors were directly probed on a wafer and several coupling capacitors were externally connected to the gate electrode. The circuit configuration used in the experiment is depicted in Fig. 9. A 40-kΩ resistor was used as a load to form the E/R configuration νMOS inverter in the first stage. The CMOS inverter in the second stage was composed of discrete NMOS and PMOS transistors. This two-stage inverter circuit corresponds to the n-channel neuron circuit shown in Fig. 3(a). External capacitors of a few thousands picofarads were used as coupling capacitances, and their values were measured at 100 kHz using an *LCR* meter (HP 4284). Since the gate oxide capacitance of the NMOS used for this measurement was 0.52 pF ((L/W) = 15 μm/50 μm, T_{OX} = 500 Å), γ = 1 approximately holds.

IV. Results and Discussion

Fig. 10 shows the measured current–voltage characteristics of a two-input-gate νMOS transistor fabricated by the double-polysilicon process. One of the input gates was used as a gate terminal and the other was used as a threshold-control terminal to which control voltages from +5 to −5 V were applied. The apparent threshold voltage as seen from the input gate is arbitrarily changed by a control signal. For this device, $C_1 = C_2 = 0.518$ pF and $C_0 = 0.086$ pF (therefore, $\gamma = 0.92$) as calculated from the designed pattern dimensions and oxide thicknesses. V_{TH}^* was measured to be 0.60 V. The calculated values of $V_{TH}^{(1)}$ using (7) and these parameters almost exactly coincide with the experimental results.

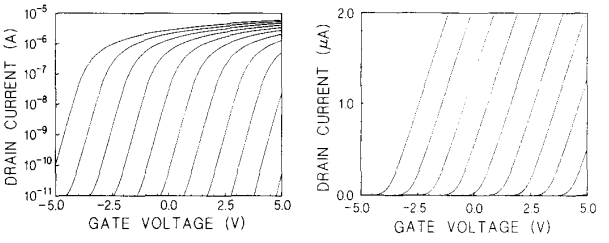


Fig. 10. Measured drain current–gate voltage characteristics of a variable-threshold transistor. One of the input gates of a 2-input νMOS was used as a gate terminal and the other was used as a threshold control terminal to which control voltages from +5 to −5 V were applied (from left to right).

The results of measurement on the circuit shown in Fig. 9 are given in Fig. 11. Fig. 11(a) represents the transfer characteristics of the CMOS inverter in the second stage of the circuit and Fig. 11(b) the transfer characteristics of the E/R νMOS inverter in the first stage. The overall characteristics of the entire circuit, i.e., the n-channel neuron circuit is also given in Fig. 11(c). The switching threshold voltage of the CMOS inverter is 1.88 V. The input voltage to the E/R inverter that yields the inverter output (V_C) of 1.88 V is 2.24 V. In the circuit composed of these two inverters, the output V_{OUT} changes its logical state from 0 to 1 or *vice versa* at an input voltage of 2.24 V, which is the threshold voltage of the νMOS inverter as seen from the floating gate. Namely, $V^*_{INV} = 2.24$ V.

In order to demonstrate an example of neuron operations of the circuit, an eight-input-gate neuron MOSFET was constructed by connecting eight capacitors with identical capacitance values (1300–1400 pF). The results are shown in Fig. 12(a). In this experiment, an input voltage changing from 0 to 5 V was applied simultaneously to some of the eight input gates, while the rest of the gates were grounded. In the figure, the abscissa represents the common input voltage V_{IN} and N is the number of gates to which the common input voltage was applied. For values of N smaller than 3, the output is always low. The circuit outputs a high level when N is larger than 4, and the switching threshold for the low-to-high transition decreases with an increase in N. The behavior is easily understood in terms of (4), which reduces in this case to

$$(1/8)N \times V_{IN} > V^*_{INV} = 2.24. \qquad (17)$$

This allows the circuit to output a high level. For $N \leqq 3$, it is required that $V_{IN} > 5$. Therefore, only low levels are obtained. For $N \geqq 4$, the minimum value of V_{IN} that satisfies (17), i.e., the switching threshold, is calculated as 4.48, 3.58, 2.99, 2.56, or 2.24 V for $N = 4$, 5, 6, 7, or 8, respectively. These values are in excellent agreement with the experimental results: 4.37, 3.50, 2.99, 2.55, and 2.20 V (for $N = 4$–8) determined as a value giving a half V_{DD} output.

The variation of the νMOS inverter (the E/R inverter) output is shown in Fig. 12(b). The common input voltage that gives the output of 1.88 V (the threshold voltage of the CMOS inverter) is also in excellent agreement with the above values. It is seen from the curves in Fig. 12(b),

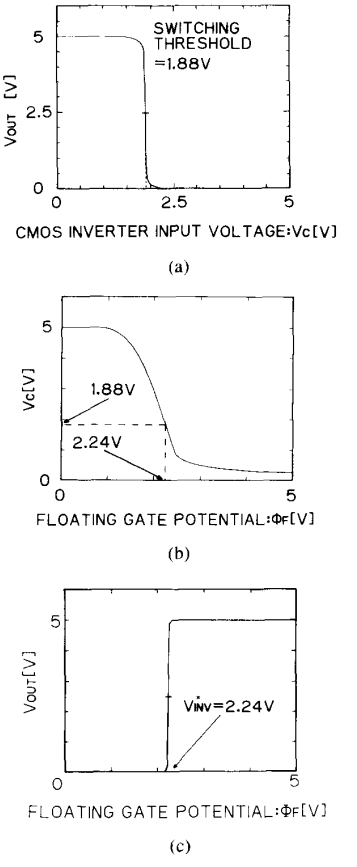


Fig. 11. Measured transfer characteristics of the circuits represented in Fig. 9. (a) Transfer characteristics of the CMOS inverter in the second stage. (b) Transfer characteristics of E/R νMOS inverter in the first stage. (c) Overall characteristics of the entire circuit, i.e., the n-channel neuron circuit.

that as the total capacitive coupling coefficient of the common input gate decreases (i.e., the value of N decreases), the slope of the E/R inverter output versus V_{IN} becomes very gradual. However, a very steep output characteristics is obtained at the output of the CMOS inverter. This is due to the very large voltage gain of the CMOS inverter. This fact suggests that similar very steep characteristics will be obtained if complementary νMOS inverter configuration, as shown in Fig. 4, is employed instead of the E/R νMOS inverter. Nevertheless, the gain of each input, as given by $g_m^{(1)}$ in Section II-A, will be reduced and noise margin or resistance to upsets will be lower than in binary logic. The employment of E/R νMOS inverter in this example is only for demonstration purposes, and CMOS configuration should be usually employed in the real circuit design. The data in Fig. 12 clearly demonstrate the neuron circuit in Fig. 9 functions exactly as the artificial neuron model works in that it outputs 1 when the weighted sum of inputs exceeds a certain threshold value and outputs zero otherwise.

An example of a variable-threshold inverter controlled by binary digital signals 0 or V_{DD} in which the coupling

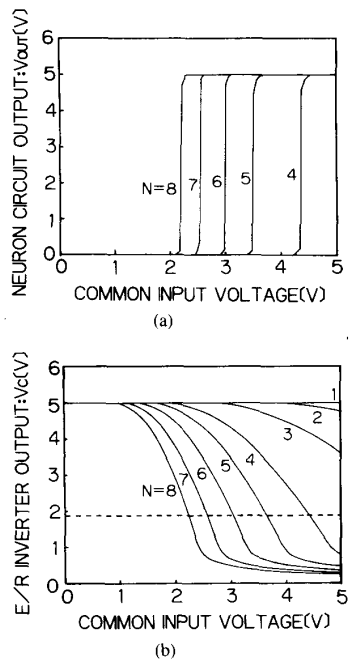


Fig. 12. (a) Output characteristics of the neuron circuit (shown in Fig. 9) having eight input gates of identical coupling capacitances. N indicates the number of gates to which the common input voltage is applied with remaining gates being grounded. (b) E/R inverter output as a function of common input voltage.

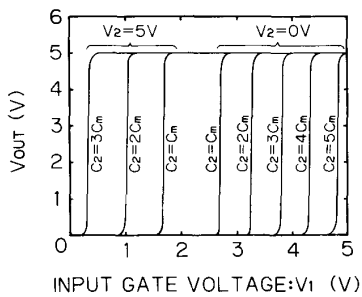


Fig. 13. A neuron circuit with two-input gate E/R νMOS inverter at the input stage. The input gate capacitance C_1 = 10.8 nF and the control gate capacitance C_2 is varied as a multiple of C_m (= 2500 ± 200 pF) as indicated in the figure.

capacitances are varied is shown in Fig. 13. Here the data are shown as the output characteristics of the neuron circuit shown in Fig. 9. It is clearly indicated that the threshold voltage for the neuron to be fired is controlled by changing the coupling strength (the capacitance value), again demonstrating the characteristics of the neuron function.

The application of a νMOS transistor as a linear resistor is demonstrated in Fig. 14. Here the drain characteristics of a νMOS connected as shown in Fig. 2(b) is shown as a function of the ratio of C_2/C_1. It is very interesting to see that as the ratio is reduced, the characteristics show a gradual transition from the well-known gate-drain-connected E-mode transistor characteristics in Fig. 14(a) to

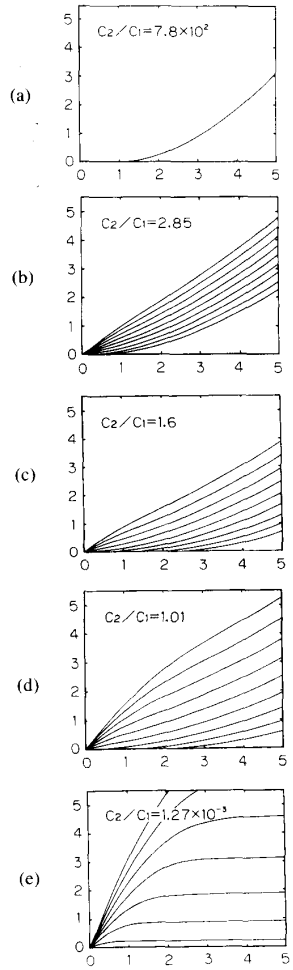
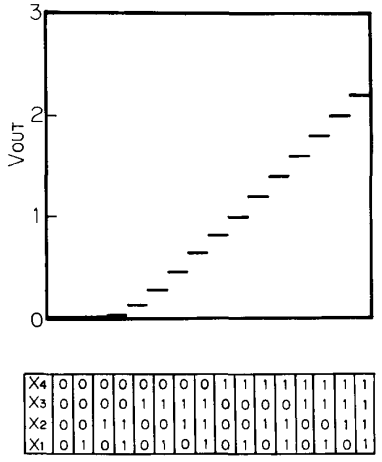


Fig. 14. Two-input gate νMOS transistor connected to form a linear variable resistor as shown in Fig. 2(b). The drain current-voltage characteristics are shown for various C_2/C_1 ratios. The ordinate and abscissa scales represent I_D (mA) and V_D, respectively.

the typical MOS characteristics in Fig. 14(e) via intermediate characteristics in Fig. 14(b), (c), and (d). Fairly reasonable linear resistor characteristics are observed at intermediate stages where the resistance value is controlled by the input voltage V_1. The theory based on the simple transistor model predicts perfect linearity will be obtained for $C_1/C_2 = 1$ in the liner-parabolic region. However, this is not exactly the case in the experimental data shown here. This is due to the lack of accuracy in the simple transistor model we used for the analysis.

Finally, the output characteristics of a νMOS source-follower circuit implemented by a four-input-gate n-νMOS and a load resistor of 40 kΩ is shown in Fig. 15. The output voltage increases in proportion to the analog value represented by the 4-b binary input. The offset seen on the abscissa is due to the threshold voltage of the NMOS (0.94 V). For input signals greater than 4(= 0100), the floating gate voltage exceeds the threshold, yielding non-



X4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
X3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
X2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
X1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Fig. 15. The output characteristics of an n-channel νMOS transistor source-follower circuit with four input gates, where C_1 = 183 pF, C_2 = 359 pF, C_3 = 713 pF, and C_4 = 1405 pF.

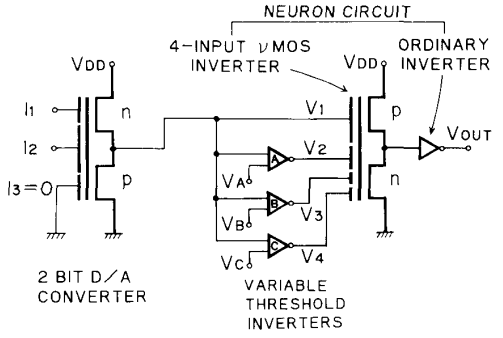


Fig. 16. An example of a *Soft Hardware Logic Circuit* implemented by νMOS transistors. The circuit can represent 16 different logic functions by just changing the control signals V_A, V_B, and V_C.

zero output. This offset can be easily avoided either by adjusting the threshold of the device or giving a positive bias to the floating gate by attaching an extra control gate with a constant positive input voltage. The latter method, however, reduces the gain of the circuit by the increase in C_{TOT}, i.e., the reduction in γ (see (16)). In order to obtain the desired output characteristics, the employment of C-νMOS source-follower configuration is preferred.

V. Application to *Soft Hardware Logic Circuit* Implementation

In order to demonstrate the versatile feature of a νMOS transistor in circuit applications, the implementation of a *Soft Hardware Logic Circuit* is briefly discussed. This is a circuit whose logical function can be altered arbitrarily by external signals without any modifications in its hardware configuration.

An example is shown in Fig. 16 in which the circuit diagram of a *Soft Hardware Logic Circuit* for two binary digital inputs is given. The circuit is composed of a 2-b D/A converter at the input stage and a 4-input-gate neuron circuit at the output stage. Three inverters A, B, and C in the intermediate stage are variable-threshold C-νMOS inverters whose inversion thresholds are given by $V_{DD} - V_A$, etc., i.e., their values are controlled by external signals V_A, V_B, and V_C, respectively. The 4-input C-νMOS inverter is designed as: $C_1 = (1/2)\gamma C_{TOT}$; $C_2 = (1/4)\gamma C_{TOT}$; $C_3 = C_4 = (1/8)\gamma C_{TOT}$; $V_{Tn}^* + V_{Tp}^* = 0$; $\beta_R = 1$ (then, $V_I^* = \gamma V_{DD}/2$).

Two binary digital variables, I_1 and I_2, are converted to a four-level variable by the D/A converter according to the relation

$$V_1 = V_{DD}(\tfrac{1}{4} X_1 + \tfrac{1}{2} X_2) + \tfrac{1}{8} V_{DD}.$$

The four-level signal (V_1) is directly led to the input gate of the four-input νMOS inverter having the largest coupling capacitance and determines the "on" and "off" of the inverter. The threshold of this inverter is controlled by the output voltages of the intermediate inverters. The outputs of these inverters, V_2, V_3, and V_4, take values of either 0 or V_{DD} depending on the four-level signal (V_1) and the control signals V_A, V_B, and V_C, respectively. The output of the entire circuit V_{OUT} alternates between 0 or 1 (V_{DD}) according to V_1. The most important characteristics of this circuit is that the values of V_1 at which 1 appears at V_{OUT} is arbitrarily selected by the combination of V_A, V_B, and V_C. When the 2-b binary-input variable is correlated to the four-level signal, any Boolean function can be generated. This is what is meant by Soft Hardware Logic. The circuit in Fig. 16 can represent any sixteen logic functions for 2-b binary inputs by just changing the control signals. The circuit becomes, for instance, exclusive-OR, exclusive-NOR, OR, and AND circuits for (V_A, V_B, V_C) = (1/4, 1/4, 1), (3/4, 3/4, 0), (0, 0, 1), and (1, 1, 0), respectively. Here 1, 1/4, etc., represent V_{DD} and $V_{DD}/4$, respectively. More detailed description of the circuit operation and the generalized design methodology for *Soft Hardware Logic Circuits* for a larger number of inputs will be presented in a forthcoming paper [22].

It should be noted here that the *Soft Hardware Logic Circuit* shown in Fig. 16, if the input-stage D/A converter is removed, is the implementation of a universal literal function for a multiple-valued radix-4 system in the terminology of multiple-valued logic [14]. Its functional form can be arbitrarily altered by external signals. This is one of the numerous examples of νMOS applications to multivalued logic implementation.

VI. Conclusions

A new type of MOS device called a neuron MOSFET has been described which functions more intelligently than the conventional MOS and bipolar transistors that are working as only switching devices in digital integrated circuits. The device has a very simple structure consisting

of a floating gate and a number of signal input gates. One of the most essential aspects of the function of the device is the weighted sum calculations of all input signals performed at the floating-gate level. Since this calculation is carried out in a voltage mode utilizing the capacitive coupling effect, no current flows except for the charging and discharging currents of coupling capacitors, thus showing superiority over the current-mode summation technique. Its low power nature is one of the most attractive features of the device for ULSI implementation. Another essential aspect of the device function is the threshold operation of the device, i.e., the control of the "on" and "off" of the transistor based on the result of the weighted sum calculation. Thus the essential part of the artificial neuron function has been realized for the first time in a single transistor level. Basic applications of the νMOS transistor such as neuron circuits, variable threshold transistors and inverters, linear resistors, source-follower circuits, and single-gate D/A converters are presented and analyzed in detail to furnish sufficient bases for circuit design. The validity of the analyses has been verified by experiments using n-channel νMOS transistors fabricated by a double-polysilicon NMOS process or those composed of discrete MOS transistors and externally connected coupling capacitors. Also, the concept of a *Soft Hardware Logic Circuit* has been introduced as one of the most exciting applications of the νMOS transistor. We believe the concept is very important in construction of new logic circuit architectures for future ULSI's including multiple-valued logic architecture.

Finally, it is pointed out that no special technologies are requested in the fabrication of νMOS integrated circuits. Standard CMOS processes with double-polysilicon gate technology are sufficient. For ultra large scale integration of νMOS circuits, however, the accuracy of the voltage level at the floating gate is most essential in the operation of νMOS transistors and circuits, which is primarily determined by the lithographic accuracy of capacitor pattern delineation. Great progress in the microfabrication technologies will be utilized in enhancing the pattern dimensional accuracy. We would like to propose an alternative direction of future technological development of ULSI's where very high patterning accuracy is achieved while keeping the minimum device dimensions at a moderate level. This would lessen a number of difficulties arising from the smallness of device structures. The penalty of decreased packing density will be well compensated for because the νMOS transistor introduced here carries out much more jobs than the conventional switching transistors do. The noise-free manufacturing [23] we are developing based on Ultra Clean Technologies [24], [25] will further enhance the performance and capability of ULSI νMOS circuits and systems.

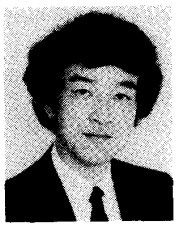
Acknowledgment

The authors wish to thank T. Yamashita, K. Kotani, and K. Yamada for their assistance in the experiment.

References

[1] G. Moore, in *IEDM Tech. Dig.*, 1975, p. 11.
[2] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassouse, and A. R. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 5, pp. 256–268, 1974.
[3] J. R. Brews, W. Fichtner, E. H. Nicollian, and S. M. Sze, "Generalized guide to MOSFET miniaturization," *IEEE Electron Devices Lett.*, vol. EDL-1, no. 1, pp. 2–4, 1980.
[4] T. Shibata, K. Hieda, M. Sato, M. Konaka, R. L. M. Dang, and H. Iizuka, "An optimally designed process for submicrometer MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-29, no. 4, pp. 531–535, 1982.
[5] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. ED-31, no. 4, pp. 452–462, 1984.
[6] K. Yamabe and K. Taniguch, "Time-dependent dielectric breakdown of thin thermally grown SiO_2 films," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 423–428, 1985.
[7] T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster, and H. N. Yu, "1-μm MOSFET VLSI technology: Part IV—Hot-electron design constraints," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 346–353, 1979.
[8] T. Ohmi, S. Imai, and T. Hashimoto, "VLSI interconnects for ultra high speed signal propagation," in *Proc. 5th Int. IEEE VLSI Multilevel Interconnection Conf.* (Santa Clara, CA, June 1988), pp. 261–267.
[9] T. Ohmi, M. Miyawaki, and T. Shibata, "High-performance devices and functional intelligent devices in deep-submicron era," in *Ext. Abstracts, 8th Int. Workshop on Future Electron Devices* (Kochi, Japan, Mar. 1990), pp. 137–142.
[10] T. Shibata and T. Ohmi, "An intelligent MOS transistor featuring gate-level weighted sum and threshold operations," in *IEDM Tech. Dig.*, 1991, pp. 919–922.
[11] W. S. McCulloch and W. Pitts, "A logical calculus of the ideas immanent in nervous activity," *Bull. Math. Biophys.*, vol. 5, p. 115, 1943.
[12] T. Shibata and T. Ohmi, "A self-learning neural network LSI using neuron MOSFET's," in *Dig. Tech. Papers, 1992 Symp. on VLSI Technology* (Seattle, WA, June 1992, to be published).
[13] K. C. Smith, "The prospects for multivalued logic systems," *IEEE Trans. Comput.*, vol. C-26, no. 9, pp. 619–634, Sept. 1981.
[14] K. C. Smith, "Multiple-valued logic: A tutorial and appreciation," *Computer*, pp. 17–27, Apr. 1988.
[15] D. Etiemble and M. Israel, "Comparison of binary and multivalued ICs according to VLSI criteria," *Computer*, pp. 28–42, Apr. 1988.
[16] M. Kameyama, T. Hanyu, and T. Higuchi, "Design and implementation of quaternary NMOS integrated circuits for pipelined image processing," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 1, pp. 20–27, Feb. 1987.
[17] S. Kawahito, M. Kameyama, and T. Higuchi, "VLSI-oriented bidirectional current-mode arithmetic circuits based on the radix-4 signed-digit number system," in *Proc. 1986 Int. Symp. on Multiple-Valued Logic* (Blacksburg, VA, May, 1986), pp. 70–77.
[18] M. Kameyama, S. Kawahito, and T. Higuchi, "A multiplier chip with Multiple-valued bidirectional current-mode logic circuits," *Computer*, pp. 43–56, Apr. 1988.
[19] T. Hanyu and T. Higuchi, "Design of a highly parallel AI processor using new multiple-valued MOS devices," in *Proc. 18th Int. Symp. on Multiple-Valued Logic* (Palma De Mallorca, Spain, May, 1988), pp. 300–306.
[20] M. Wada, K. Hieda, T. Shibata, and H. Iizuka, "A new EEPROM cell with dual control gate structure," in *Dig. Tech. Papers, 1983 Symp. on VLSI Technology*, Sept. 1983, pp. 114–115.
[21] K. Hieda, M. Wada, T. Shibata, and H. Iizuka, "Optimum design of dual-control gate cell for high-density EEPROM's," *IEEE Trans. Electron Devices*, vol. ED-32, no. 9, pp. 1776–1780, 1985.
[22] T. Shibata and T. Ohmi, "Implementing binary logic circuits using neuron MOS transistors," to be submitted to *IEEE Trans. Electron Devices.*
[23] T. Ohmi, "Future trends and applications of ultra clean technology," in *IEDM Tech. Dig.*, 1989, pp. 49–52.
[24] T. Ohmi, N. Mikoshiba, and K. Tsubouchi, "Super clean room system-ultra clean technology for submicron LSI fabrication," in S.

Broydo and C. M. Osburn, Eds., *ULSI Science and Technology/1987* (PV87-11) Pennington, NJ: Electrochem. Soc. 1987, pp. 761–785.
[25] R. W. Keeley and T. H. Cheyney, Eds., *The Ohmi Papers—Challenges to Ultimate Cleanliness for Semiconductor Processing* (A Canon Communications, Inc. Pub., Santa Monica, CA, 1990).



Tadashi Shibata (M'79) was born in Hyogo, Japan, on September 30, 1948. He received the B.S. degree in electronic engineering and the M.S. degree in material science both from Osaka University, Osaka, Japan, and the Ph.D. degree from the University of Tokyo, Tokyo, Japan, in 1971, 1973, and 1984, respectively.

From 1974 to 1986, he was with Toshiba Corporation, where he worked as a researcher on the R&D of device and processing technologies for ULSI's. He was engaged in the development of microprocessors, EEPROM's and DRAM's, especially in the process integration and the research of advanced processing technologies for their fabrication. From 1984 to 1986, he worked as a production engineer at one of the most advanced manufacturing lines of Toshiba. During the period of 1978 to 1980, he was a Visiting Research Associate at Stanford Electronics Laboratories, Stanford University, Stanford, CA, where he studied laser beam processing of electronic materials including silicide, polysilicon, and superconducting materials. Since 1986, he has been Associate Professor at the Department of Electronic Engineering, Tohoku University, Sendai, Japan. He is now engaged in the research and development of ultraclean technologies. His main interest is in the area of low-temperature processing utilizing very-low-energy ion bombardment for the promotion of processes as well as in the development of the ultraclean ion implantation technology to form defect-free ultrashallow junctions by low-temperature annealing. He is currently working on the research of advanced device structures and their circuit and system applications.

Dr. Shibata is a member of Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, and the IEEE Electron Devices Society.

Tadahiro Ohmi (M'81) was born in Tokyo, Japan, on January 10, 1939. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, in 1961, 1963, and 1966, respectively.

Prior to 1972, he served as a Research Associate in the Department of Electronics of Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multivalley diffusion, and frequency limitation of negative differential mobility due to an electron transfer in the multivalleys, high-field transport in semiconductors such as unified theory of space-charge dynamics in negative differential mobility materials, Bloch oscillation induced negative mobility, and Bloch oscillators, and dynamics in injection lasers. He is currently a Professor in the Department of Electronics, Faculty of Engineering, Tohoku University, Sendai, Japan. He is currently engaged in researches on high-performance ULSI such as ultrahigh-speed ULSI: current overshoot transistor LSI, HBT LSI, and SOI on metal substrate, base store image sensor (BASIS), and high-speed flat-panal display, as well as advanced semiconductor process technologies, i.e., ultraclean technologies such as high-quality oxidation, high-quality metallization due to low kinetic energy particle bombardment, very low temperature Si epitaxy with simultaneous doping capability due to low kinetic energy particle bombardment, crystallinity control film growth technologies from single crystal, grain-size-controlled polysilicon and amorphous due to low kinetic energy particle bombardment, *in situ* wafer surface cleaning technologies due to low kinetic energy particle bombardment, highly selective CVD, highly selective RIE, high-quality ion implantations with low-temperature annealing capability, etc., based on the new concept supported by newly developed ultraclean gas supply system, ultrahigh vacuum compatible reaction chamber having self-cleaning function, ultraclean wafer surface cleaning technology, etc. His research activities are as follows: 260 original papers and 190 patent applications. He received the Ichimura Award in 1979, the Teshima Award in 1987, the Inoue Harushige Award in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, and the Okochi Memorial Technology Prize in 1991. He serves as the President of the Institute of Basic Semiconductor Technology Development (Ultra Clean Society).

Dr. Ohmi is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electrical Engineers of Japan, the Japan Society of Applied Physics, and the ECS, and the IEEE Electron Devices Society.