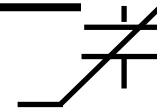


Typical Performance of Packaged “AB” Capacitors

Joe T. Evans, Jr.
Radiant Technologies, Inc.
August 29, 2008



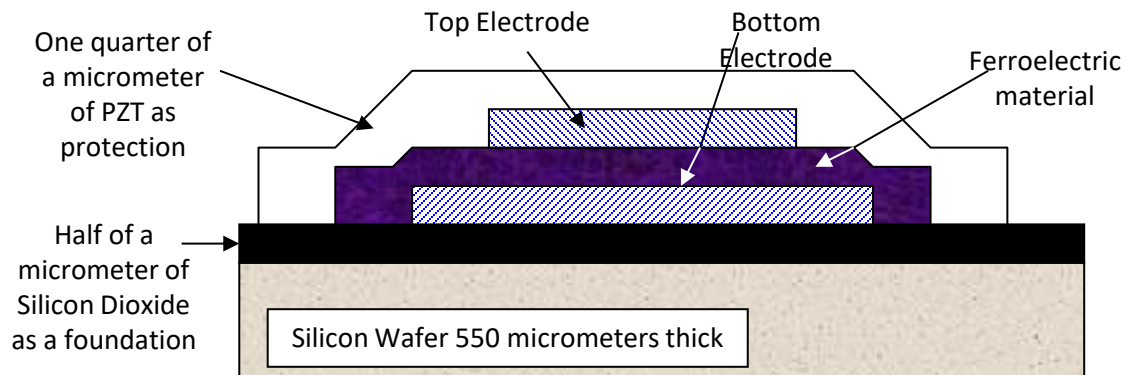


Introduction

- The Type AB capacitors were designed to demonstrate all of the performance and reliability properties found in most ferroelectric capacitors, including fatigue and imprint.
- The data plotted in the following pages came from one dataset: “typical type ab performance 07_07_08.dst” which can be downloaded from www.ferrodevices.com/components2.html. Vision can be downloaded from www.ferrodevices.com/tdownload.html.
- The data shown in this document represents a cross-section of the types of tests that may be executed on ferroelectric capacitors.

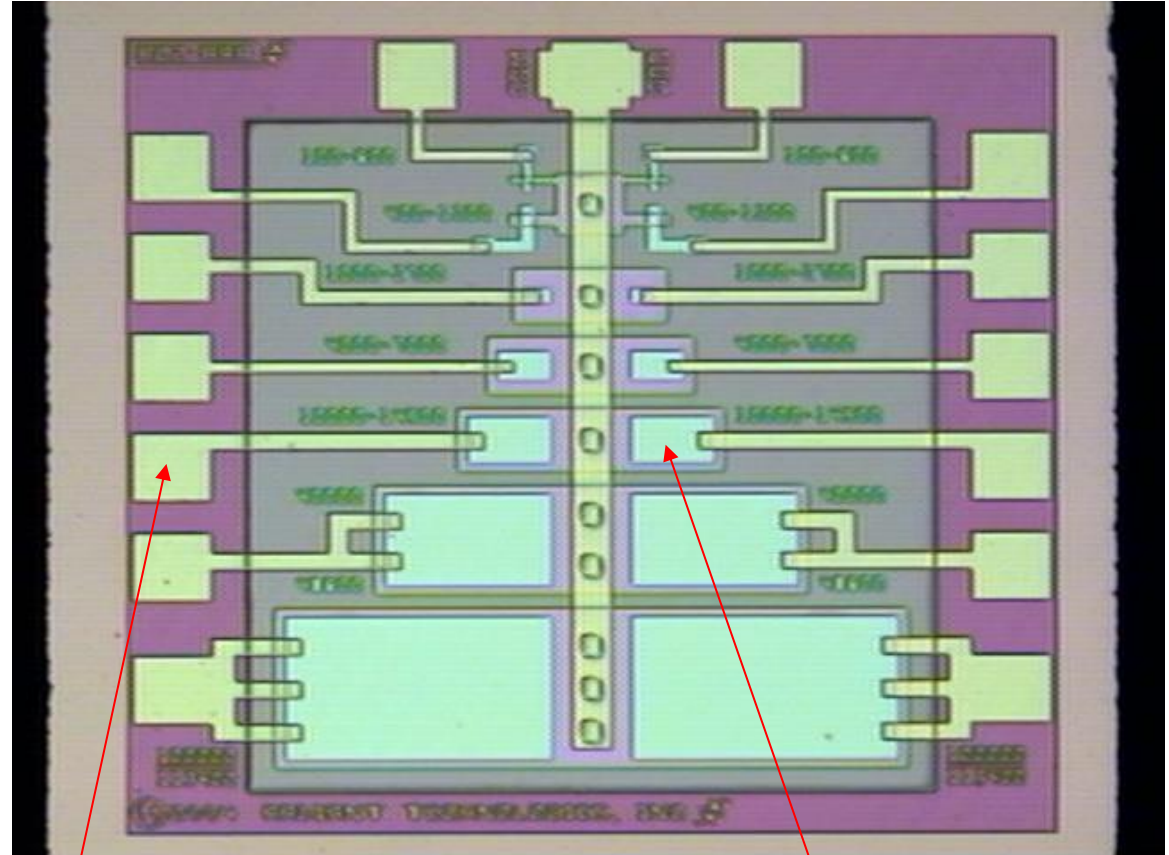
Description of Samples

- Capacitor Structure (from bottom to top):
 - 5000Å silicon dioxide on <100> silicon
 - 400Å titanium dioxide
 - 1500Å polycrystalline <111> & <200> platinum bottom electrode
 - 2550Å 20/80 MOD PZT deposited in seven layers
 - 1000Å polycrystalline platinum top electrode
 - 2200Å 20/80 PZT passivation topped by 400Å titanium dioxide
 - Metal interconnect using 200Å chromium & 5000Å gold



Description of Samples

The $400\mu^2$ and $100\mu^2$ capacitors are “cross” type devices with the top electrode contact to the side of the capacitor. The larger capacitors are “plate” capacitors where the top electrode is fully enclosed by the bottom electrode and the top electrode contact is over the active capacitor area.

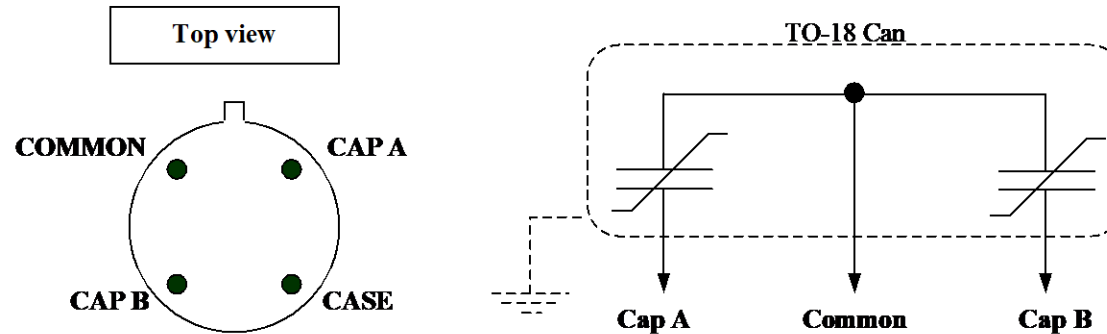


Contact Pad in Gold

10,000 square micron capacitor

Packaging

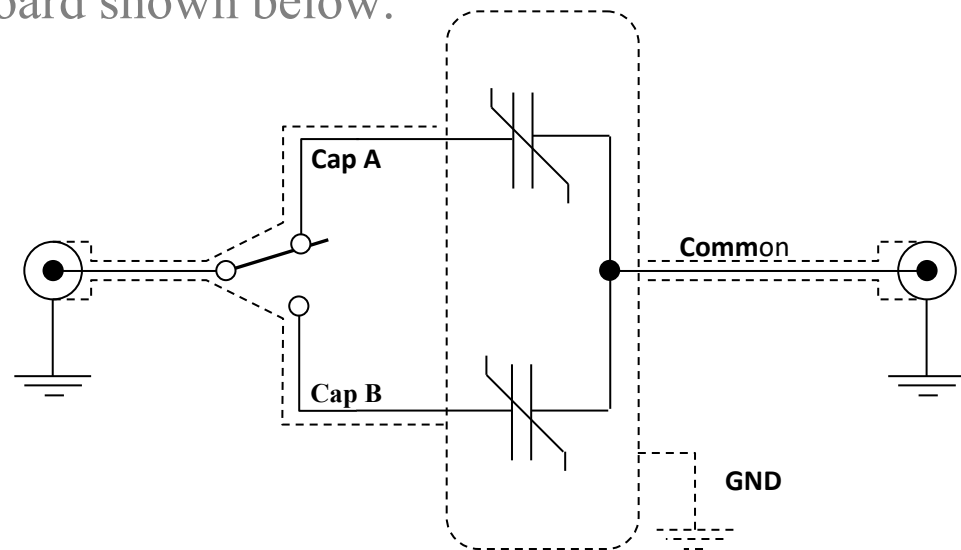
- The capacitors are bonded into TO-18 transistor type cans with four leads.



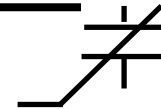
- See the document “Ferroelectric Component Technical Description - RC2-AAA” for more information

Socket Board

- Most test data were collected from a single “AB” capacitor mounted on the TO-18 Socket Board shown below.

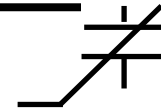


- Data at temperature was collected from unpackaged die on a semiconductor probe station with a hot chuck.



Recovery

- As has been reported in the past, a DC bias applied to a ferroelectric capacitor can reverse some imprint effects.
- The “AB” capacitors are capable of withstanding long periods at 9V across their 2550Å of thickness.
- Imprint effects may be almost 100% reversed using the recovery procedure recommended below.
- A significant amount of fatigue effects may also be reversed using the same recovery procedure.
- Recommended Recovery Procedure:
 - 9V 1Hz square wave for 100 seconds at room temperature. Longer periods may be executed if necessary.



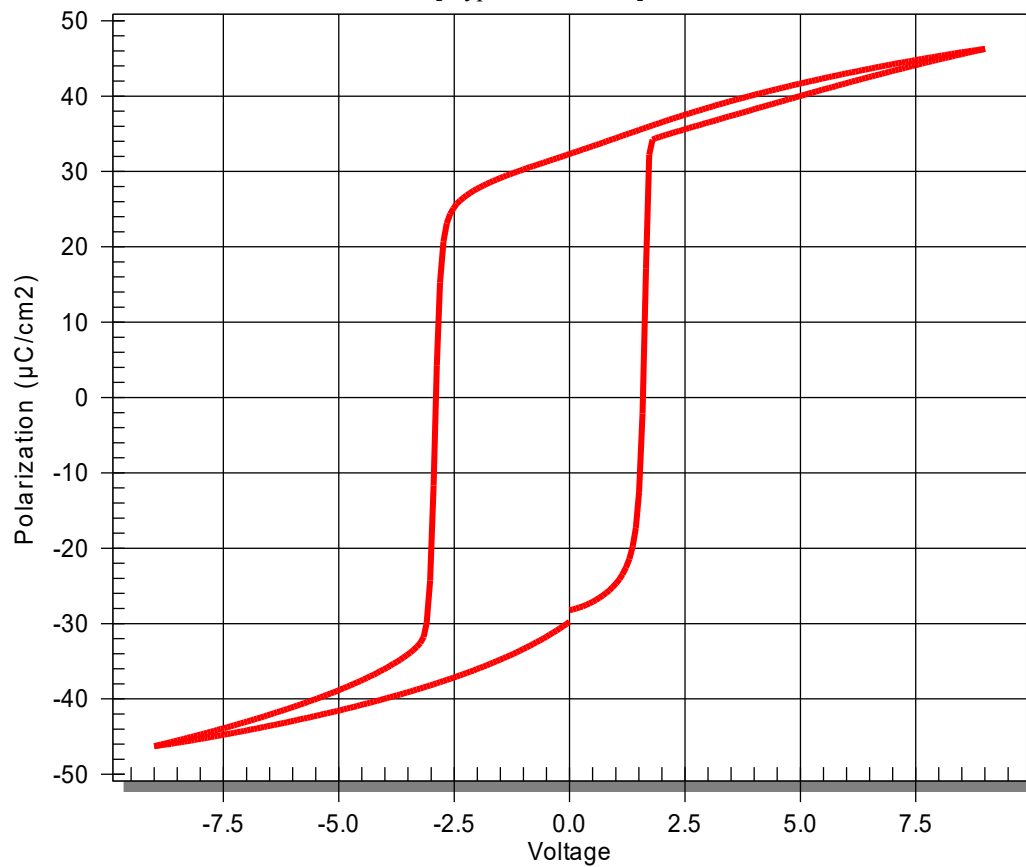
Typical Performance

- Typical performance data for the $400\mu^2$ “AB” packaged part are plotted on the following pages.
- All test data were taken on a Precision LC or Precision Premier II.
 - All plots were formatted using plotting tools in Vision and then copied directly into this presentation.
- The dataset containing the plotted data may be found at www.ferrodevices.com/components2.html.

Before Recovery

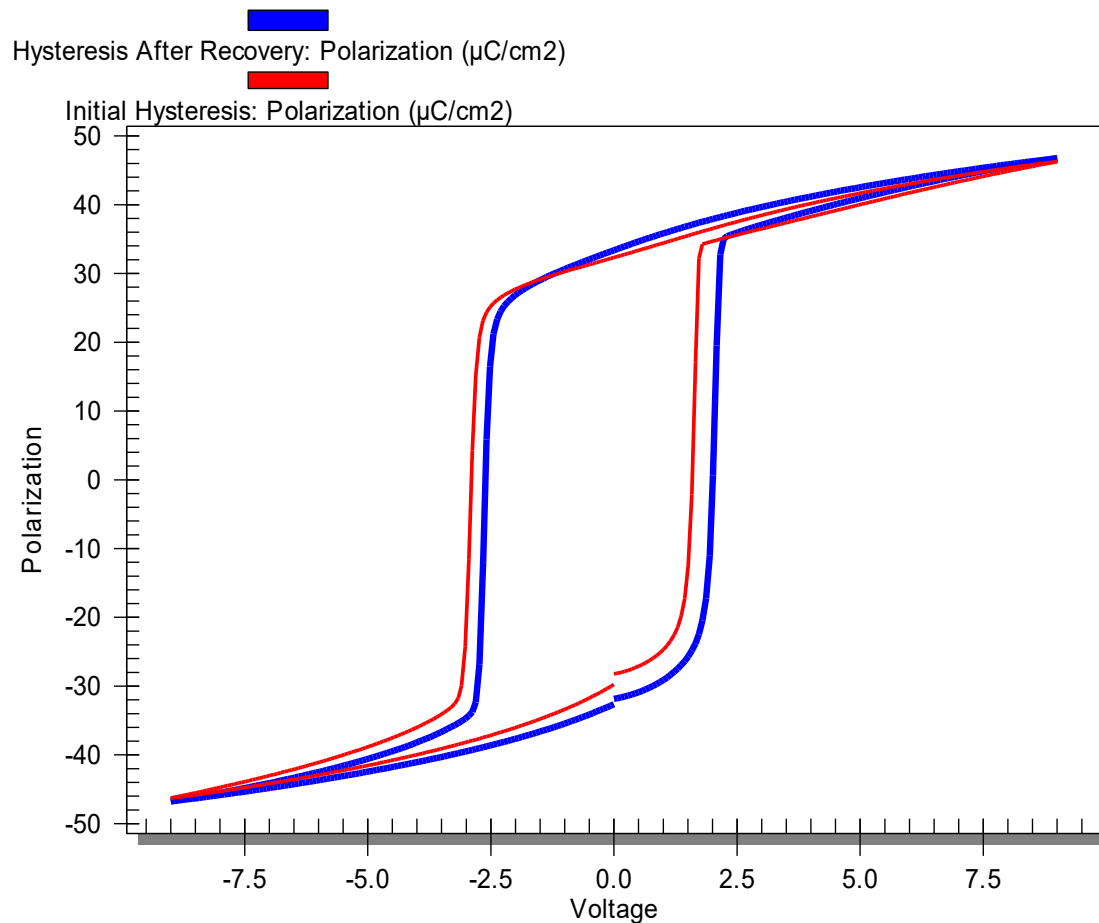
(10ms Period)

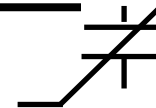
Hysteresis Before Recovery
[Type AB WHITE]



After 100 Second Recovery (10ms Period)

Hysteresis Before and After Recovery
[Type AB WHITE]



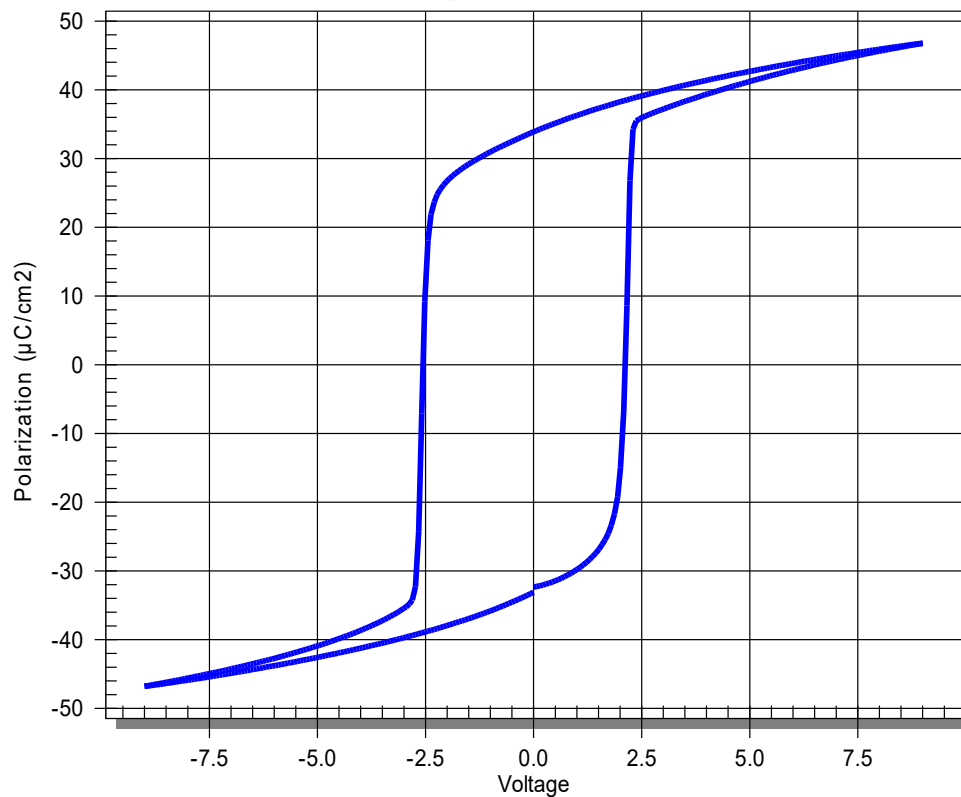


Longer Recovery

(5 minutes, room temperature)

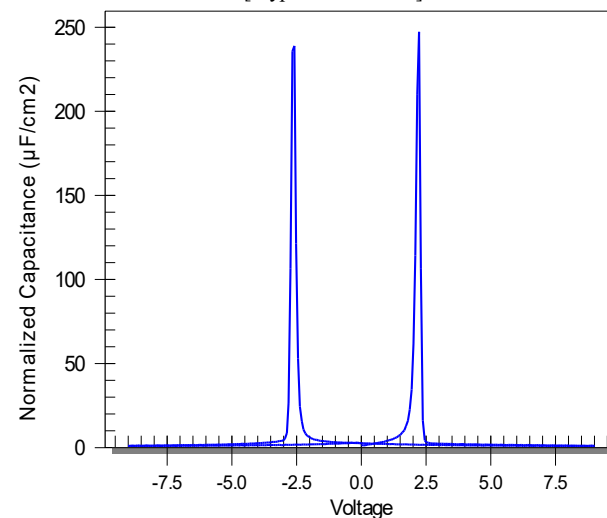
After 5 Minutes Total Recovery

[Type AB WHITE]



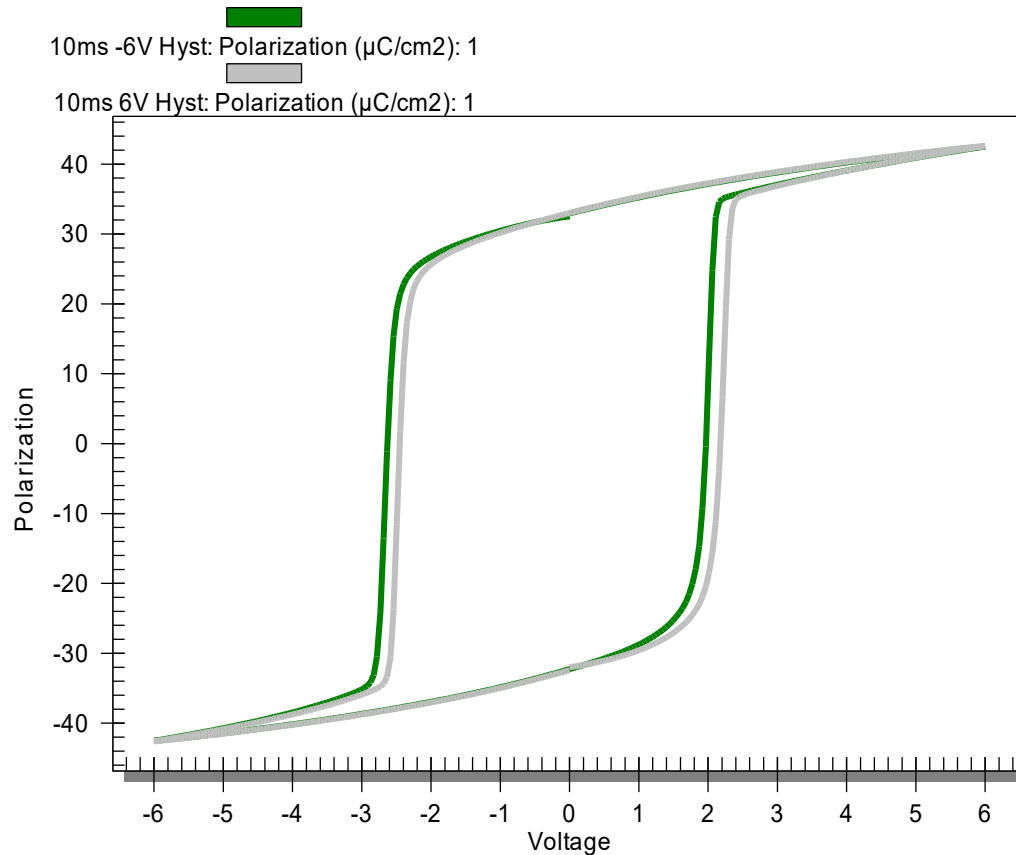
Normalized CV of Recovered Capacitor

[Type AB WHITE]



Opposing Hysteresis Loops

Opposing 6V Loops
[Type AB WHITE]

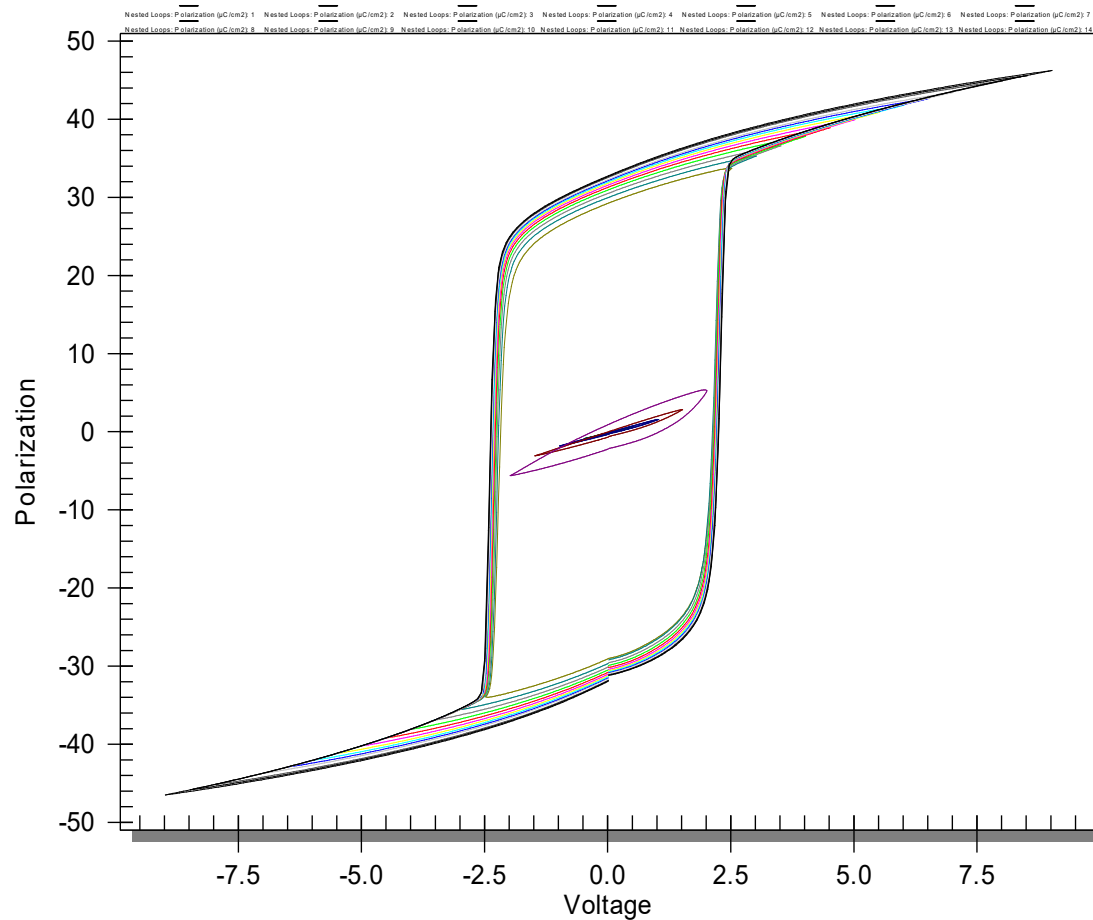


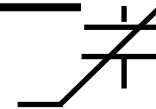
The 20/80 PZT slides back and forth depending on the value of its remanent polarization before the loop starts. Other compositions do not have this effect to such a magnitude.

Nested Hysteresis Loops

(10ms Period)

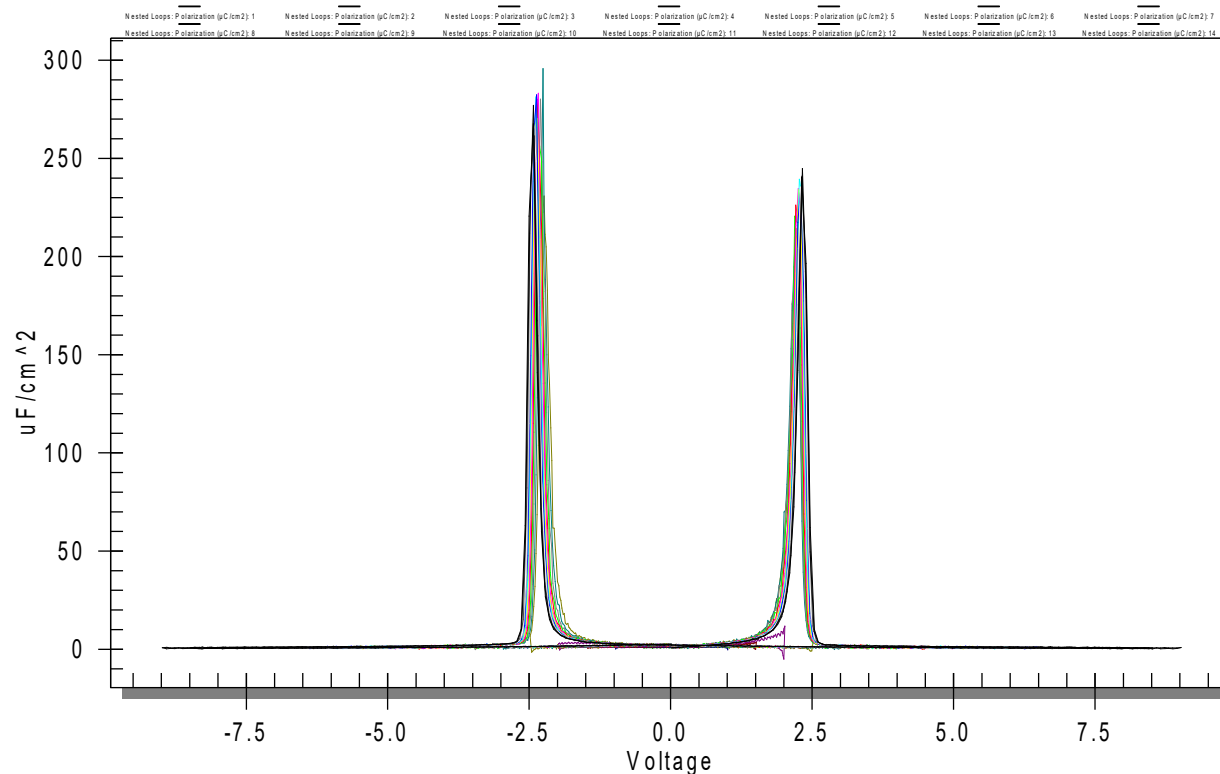
Hysteresis Loop vs Voltage
[Type AB WHITE, 10ms period]



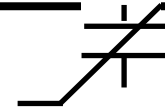


Nested nCV Loops

nCV vs Voltage
[Type AB WHITE, 10ms Period]

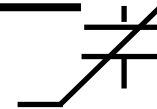


The normalized CV is the mathematical derivative of a hysteresis loop. It has the units of capacitance per unit area and represents the instantaneous capacitance of the capacitor at each point in the loop. The plot above is the derivative of the nested hysteresis loops on the previous page.

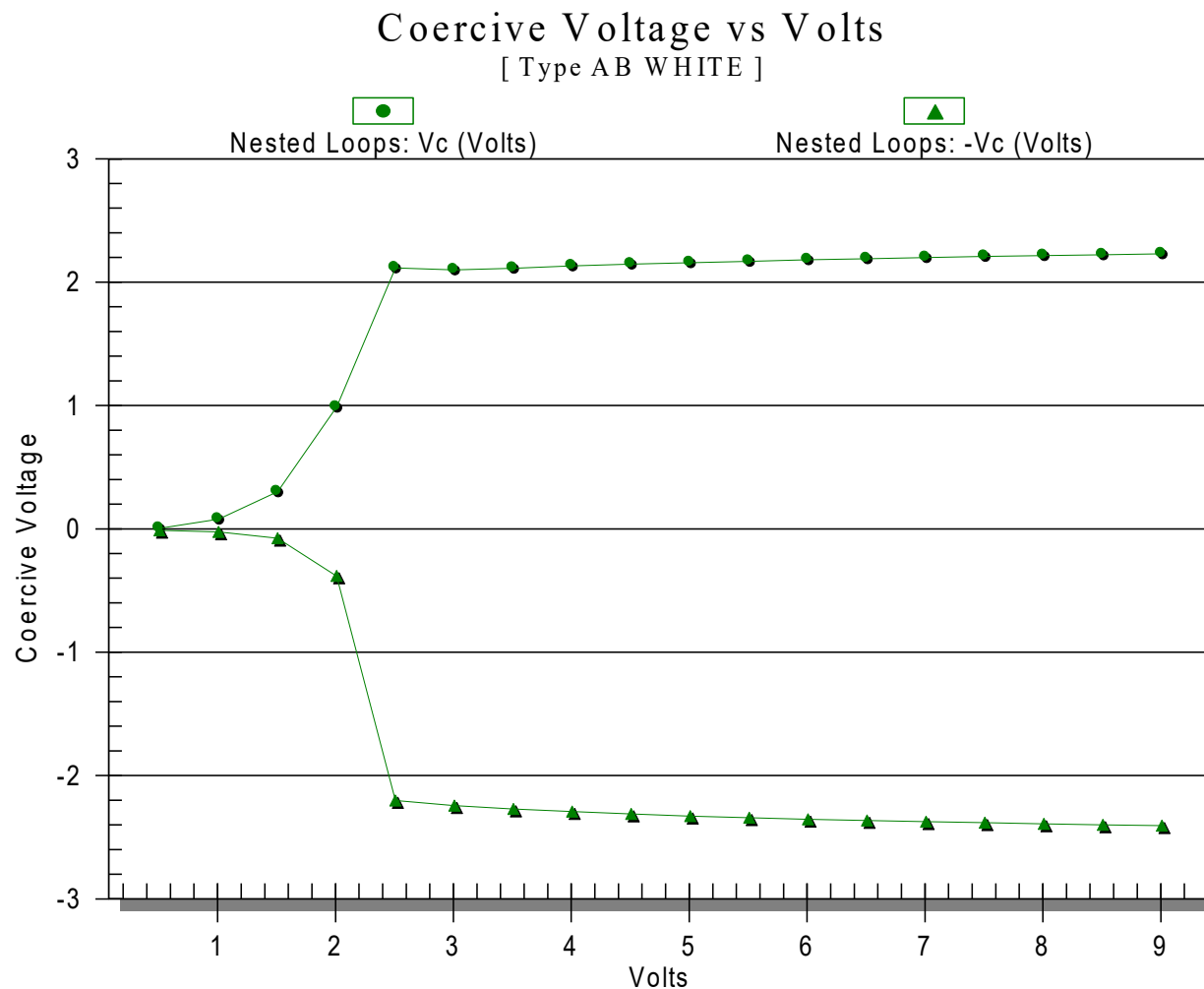


Capturing Data During Loops

- The Vision data management software which controls the Radiant testers is capable of executing measurement tasks in a loop while changing one or more parameters in each loop.
- The Vision Library provides data filters which may be inserted in a loop to read and then plot the measurement results as a function of the loop parameters.
- The parameters plotted on the next few pages were captured in this manner during the same test execution that captured the nested loops plotted on the previous pages.

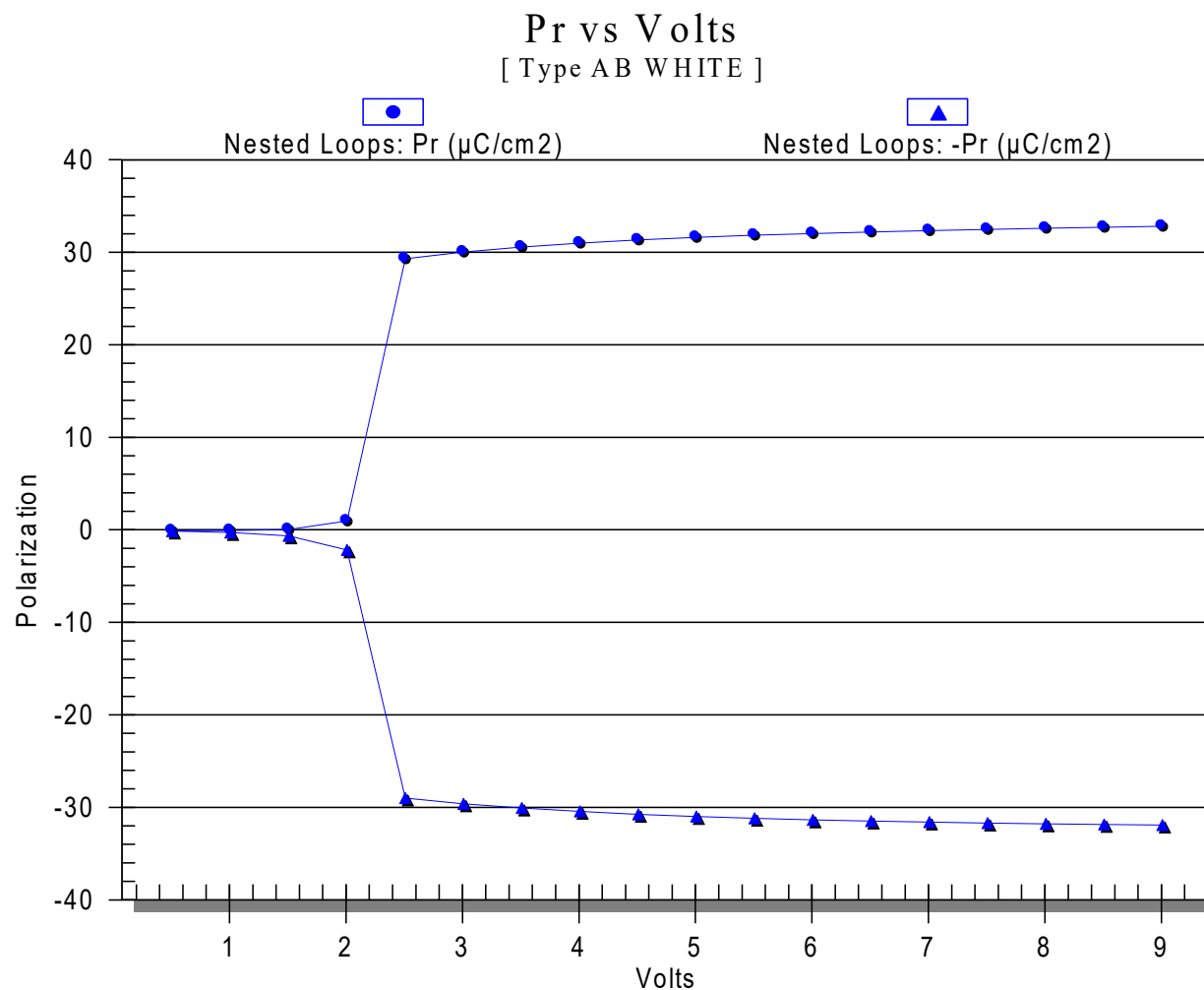


Hysteresis Coercive Voltage vs Volts



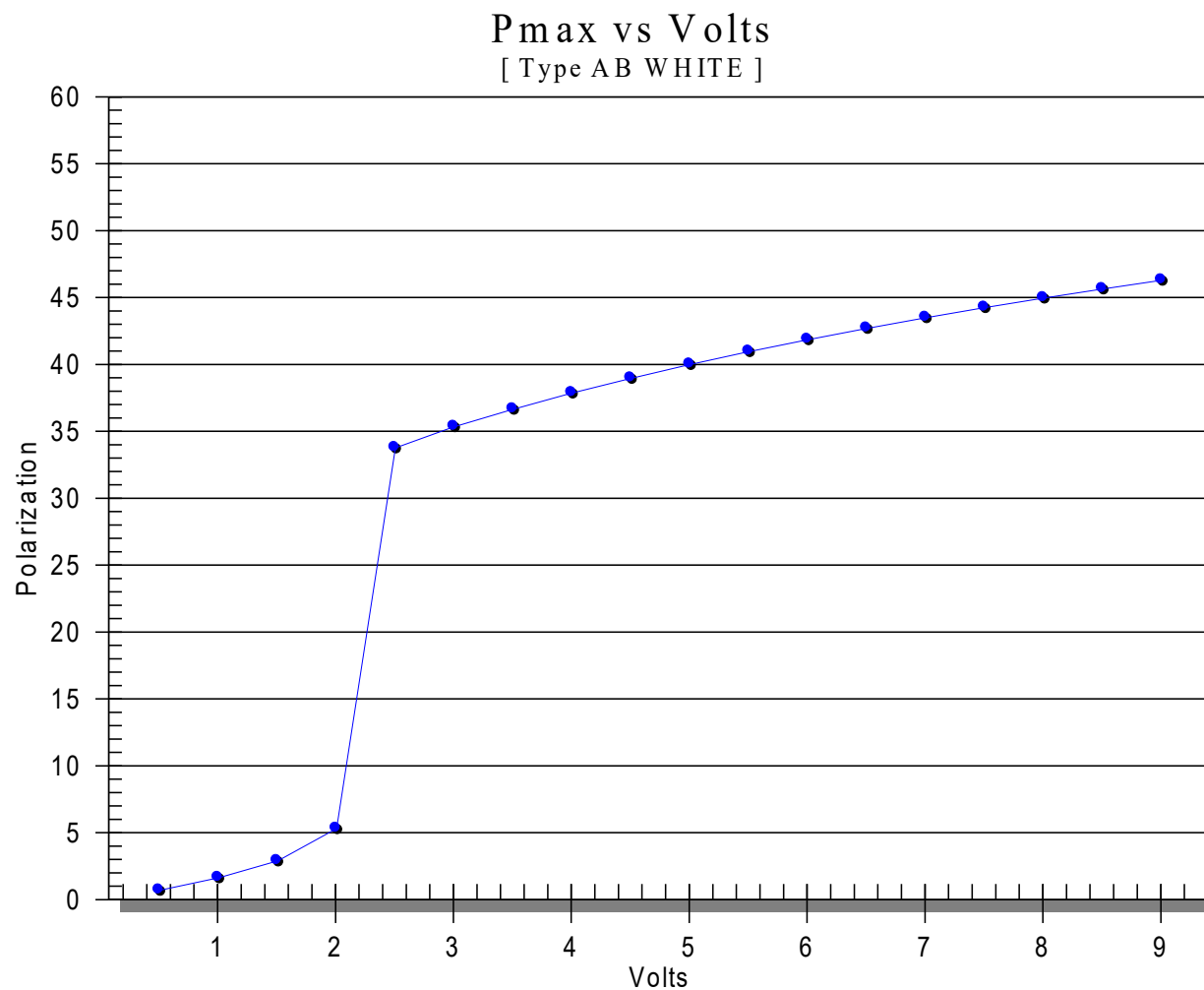


Hysteresis Pr vs Volts





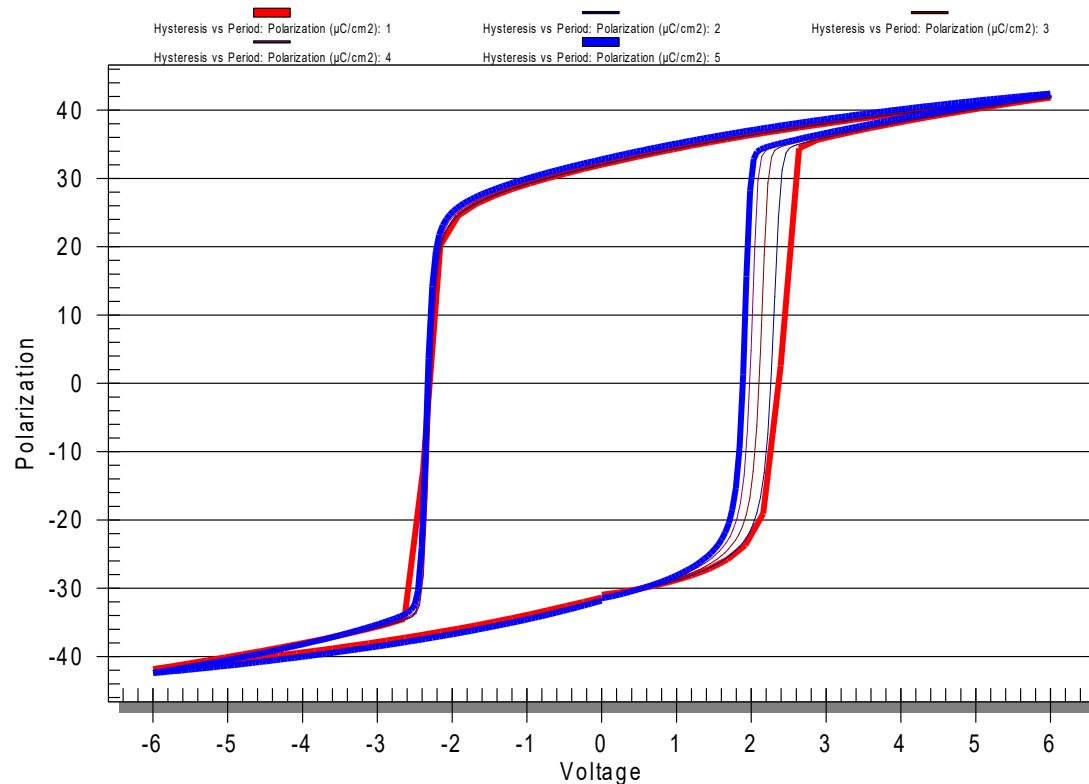
Hysteresis Pmax vs Volts



Hysteresis vs Period

6V Hysteresis vs Period 1ms->10s

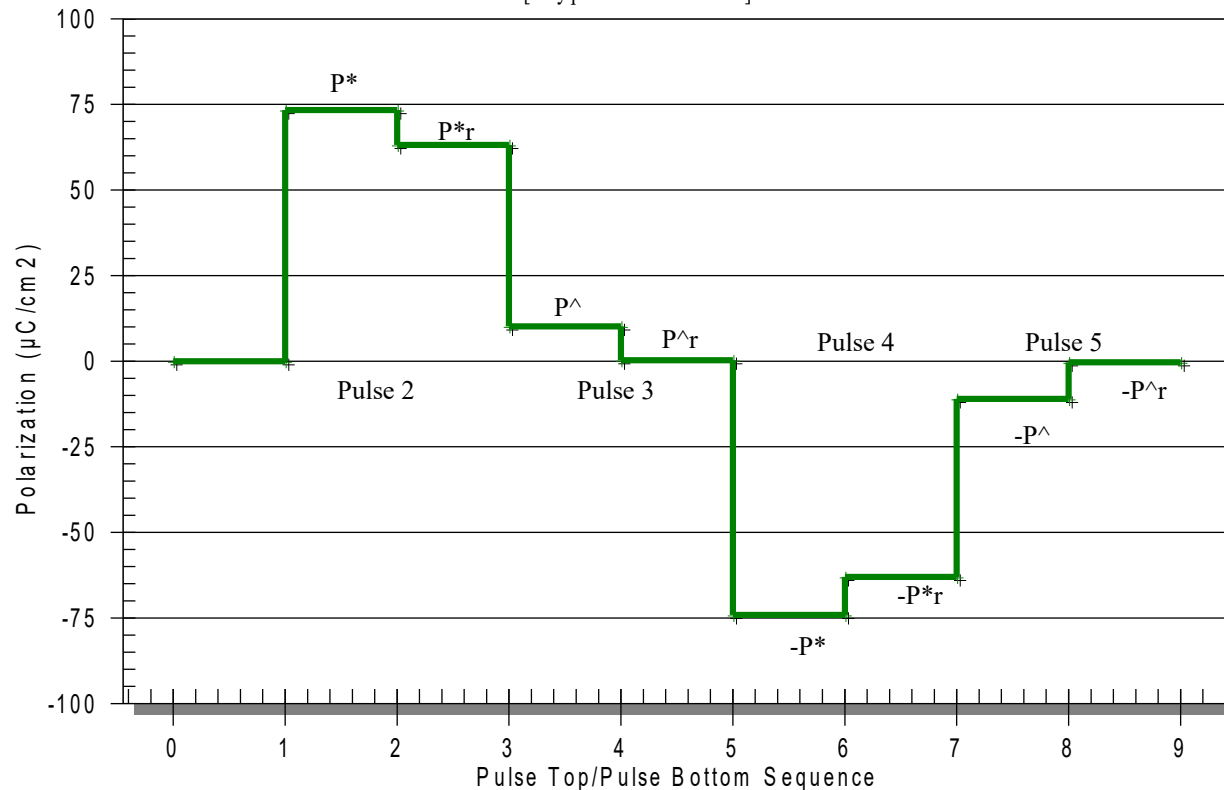
[Type AB WHITE]



As the period of the hysteresis test gets longer, the hysteresis loop gets more square with a lower coercive voltage. The **red loop** had a 1ms period. The **blue loop** had a 10 second period.

Standard PUND Results

6 V 1 m s PUND
[Type AB WHITE]



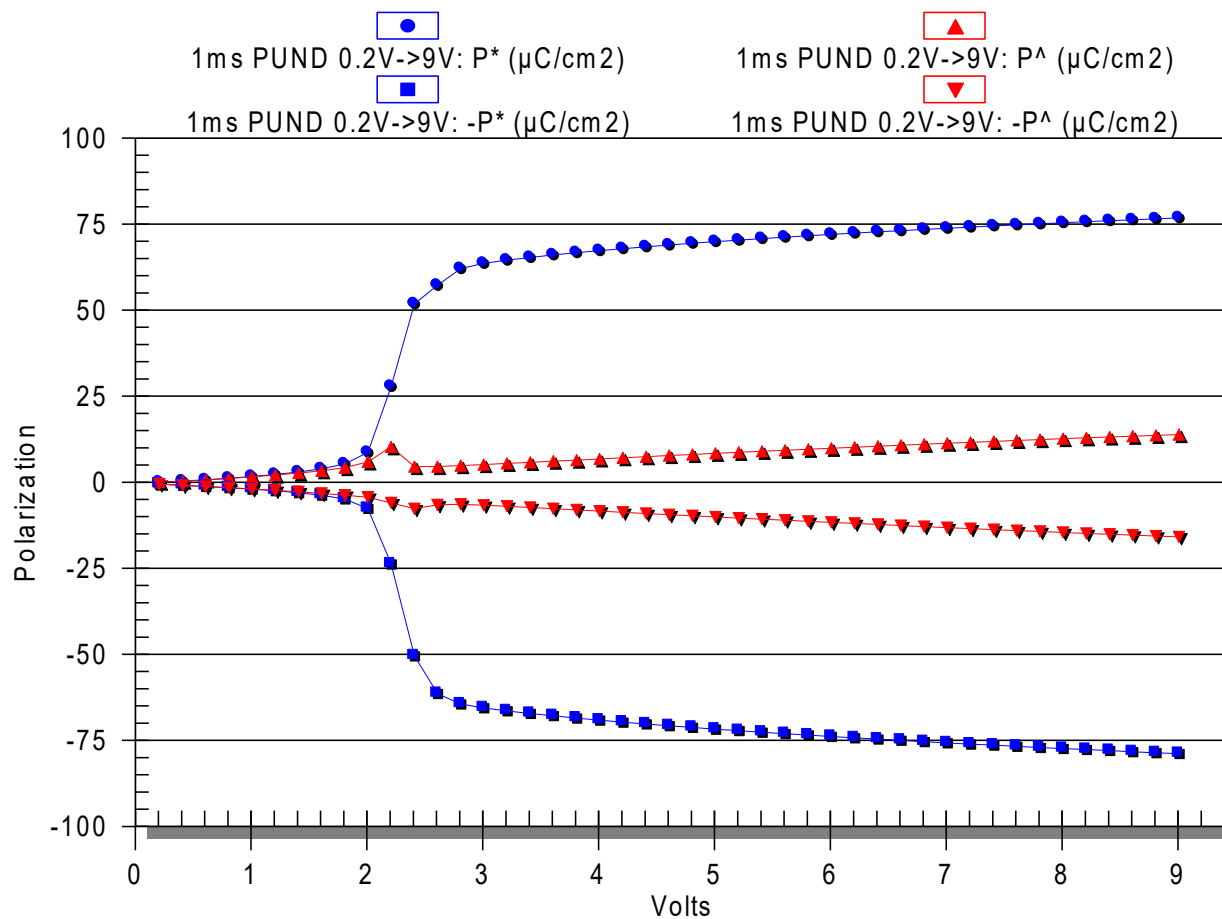
The PUND test consists of five pulses where one polarization measurement is made at the top of each pulse and one at the bottom of each pulse. The first pulse presets the remanent polarization. The next four measure it. The PUND test simulates ferroelectric RAM operation and is a quick way to measure remanent polarization.

PUND vs Voltage

($\pm P^*$ vs $\pm P^\wedge$ at 1ms Pulsewidth)

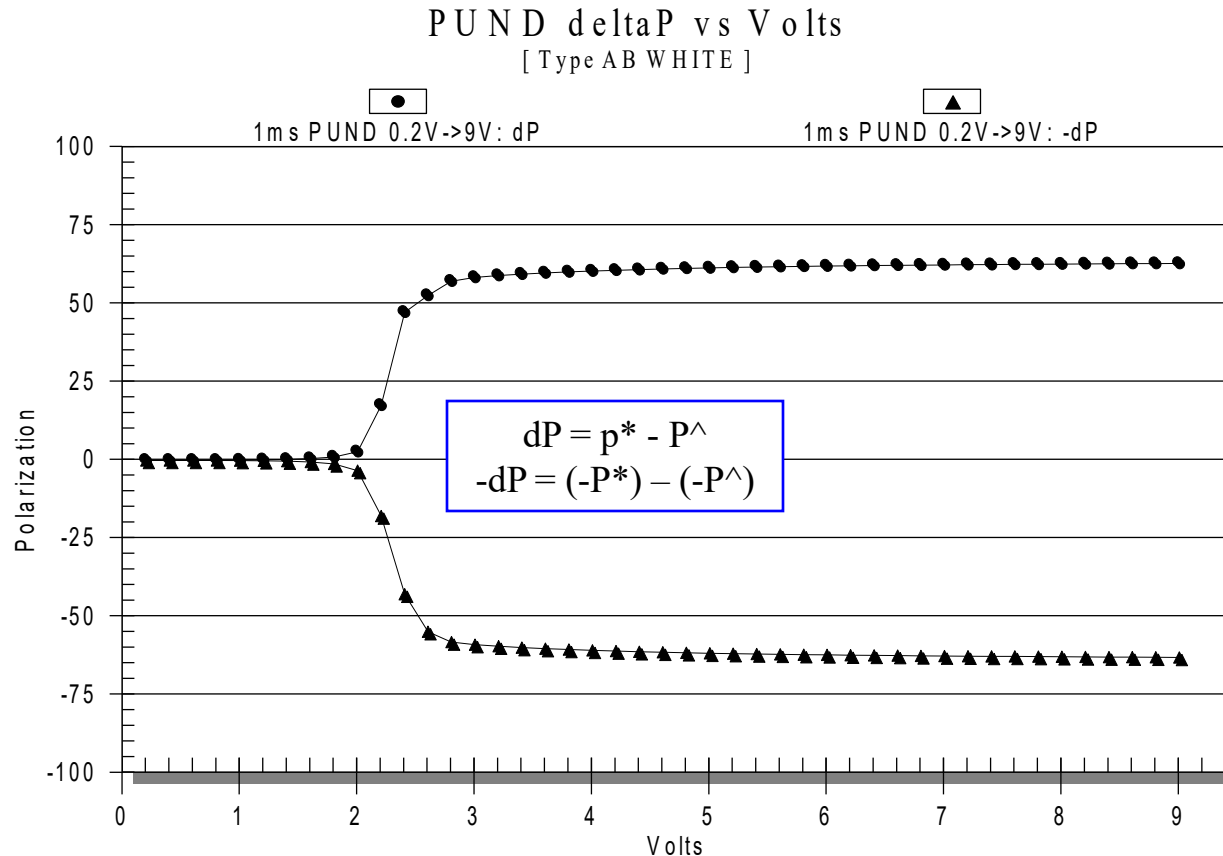
PUND P^*/P^\wedge vs Volts

[Type AB WHITE]



PUND vs Voltage

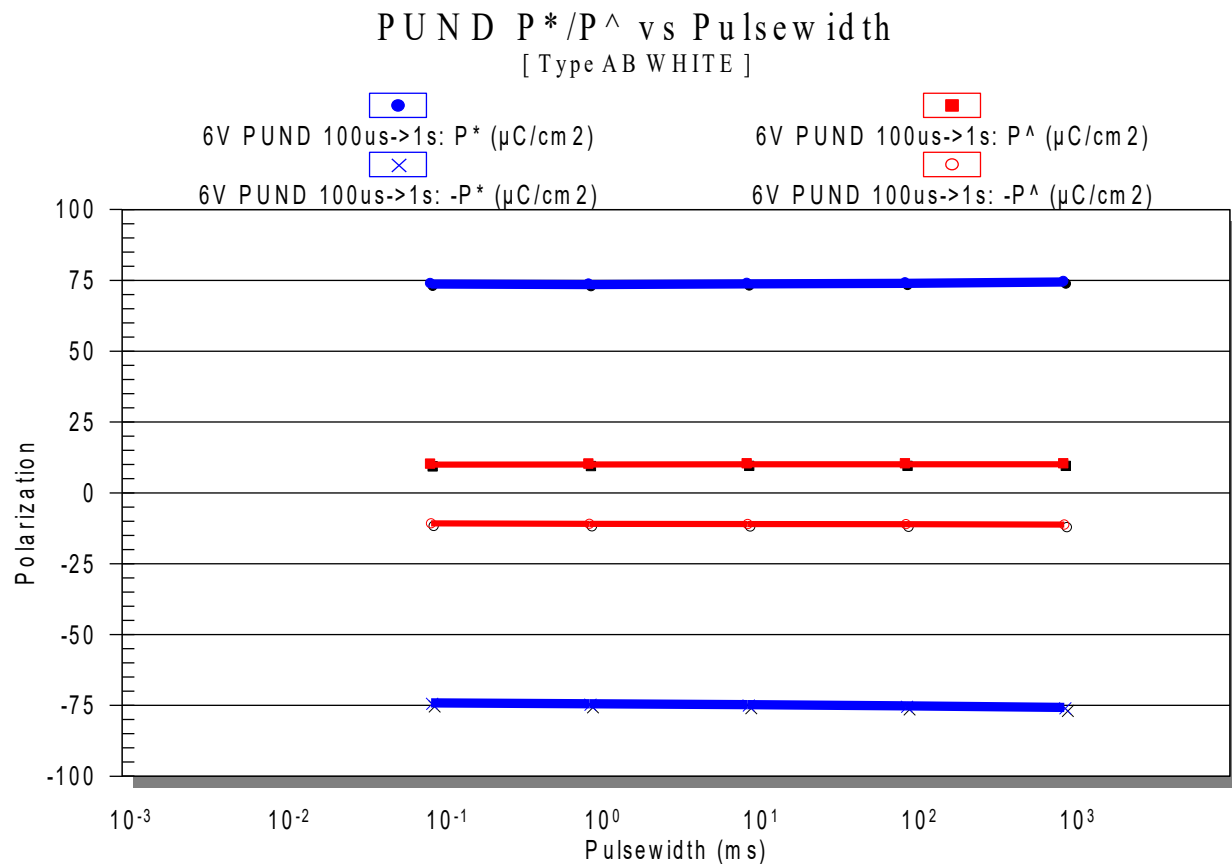
($\pm dP$ at 1ms Pulsewidth)



The “deltaP” value is the difference in polarization generated by a switching pulse and the following non-switching pulse of the PUND test. It is the remanent portion of the hysteresis loop and is two times the value of the switchable spontaneous polarization.

PUND vs Pulsewidth

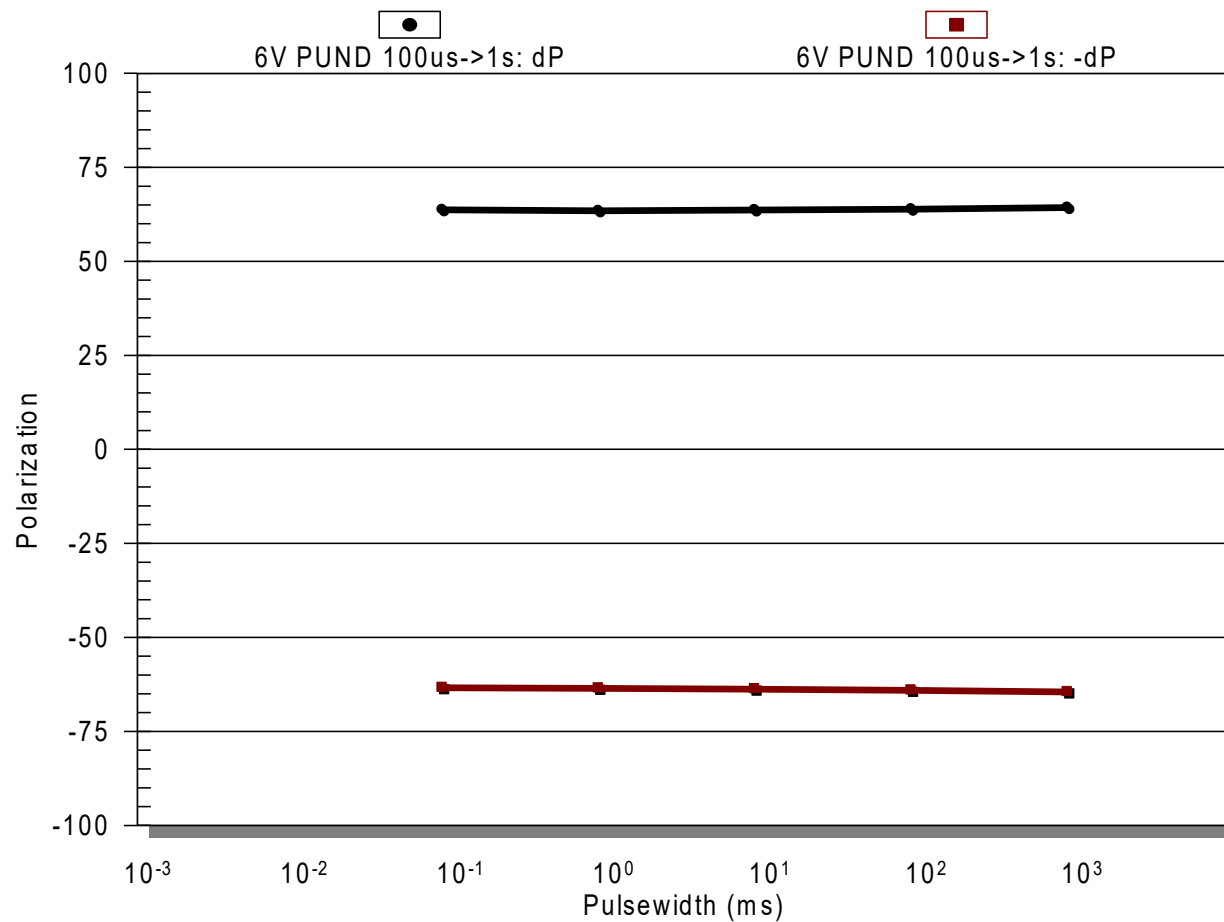
($\pm P^*$ vs $\pm P^\wedge$ at 6V)

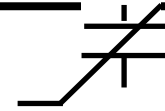


PUND vs Pulsewidth

($\pm dP$ at 6V)

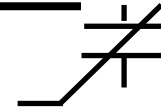
PUND deltaP vs Pulsewidth
[Type AB WHITE]





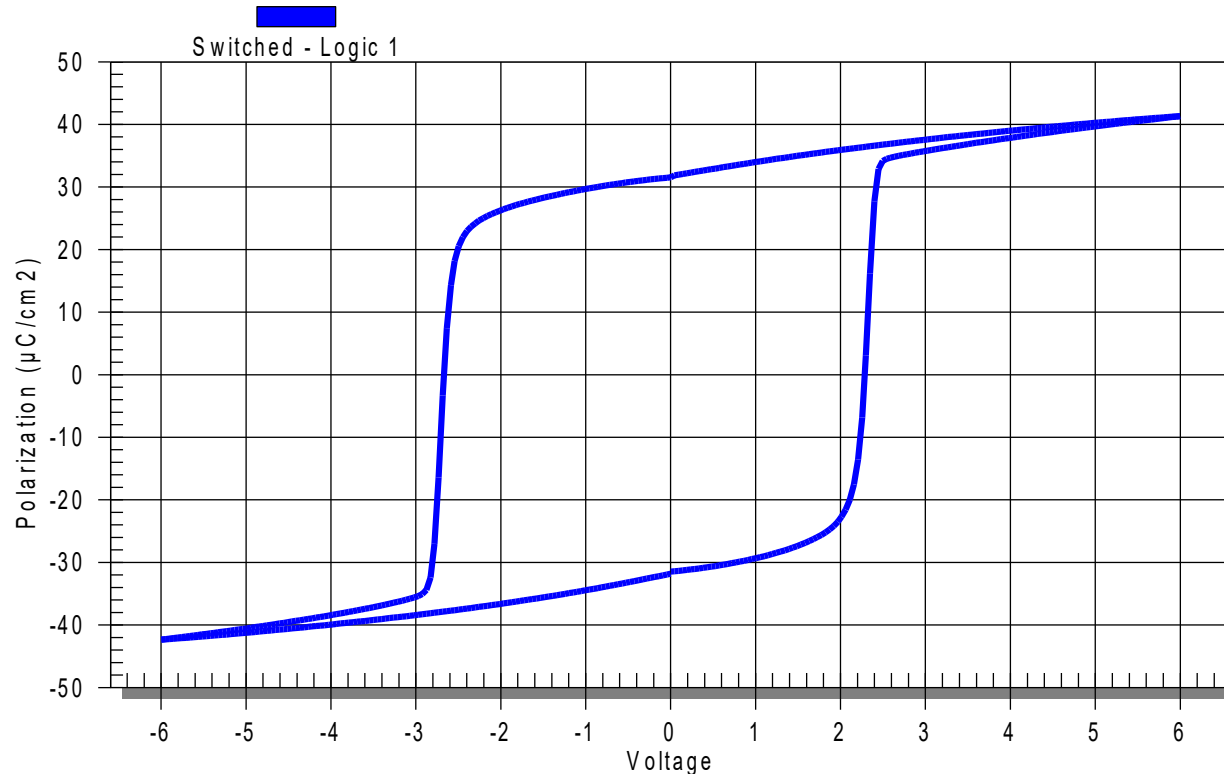
Measuring the Remanent Hysteresis Loop

- The PUND test can be executed with half-hysteresis loops instead of pulses.
- The half-hysteresis loops can be subtracted from each other to produce the remanent hysteresis loop, which is the switching loop for the remanent polarization in the capacitor.
- Measuring the remanent hysteresis loop eliminates the contribution by the dielectric and paraelectric effects as well as resistive leakage.
- The Remanent Hysteresis Task in Vision performs this measurement under automatic control.

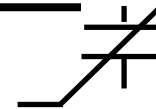


Switching Half-Loops

Switching Half-Loops
[Type AB WHITE]

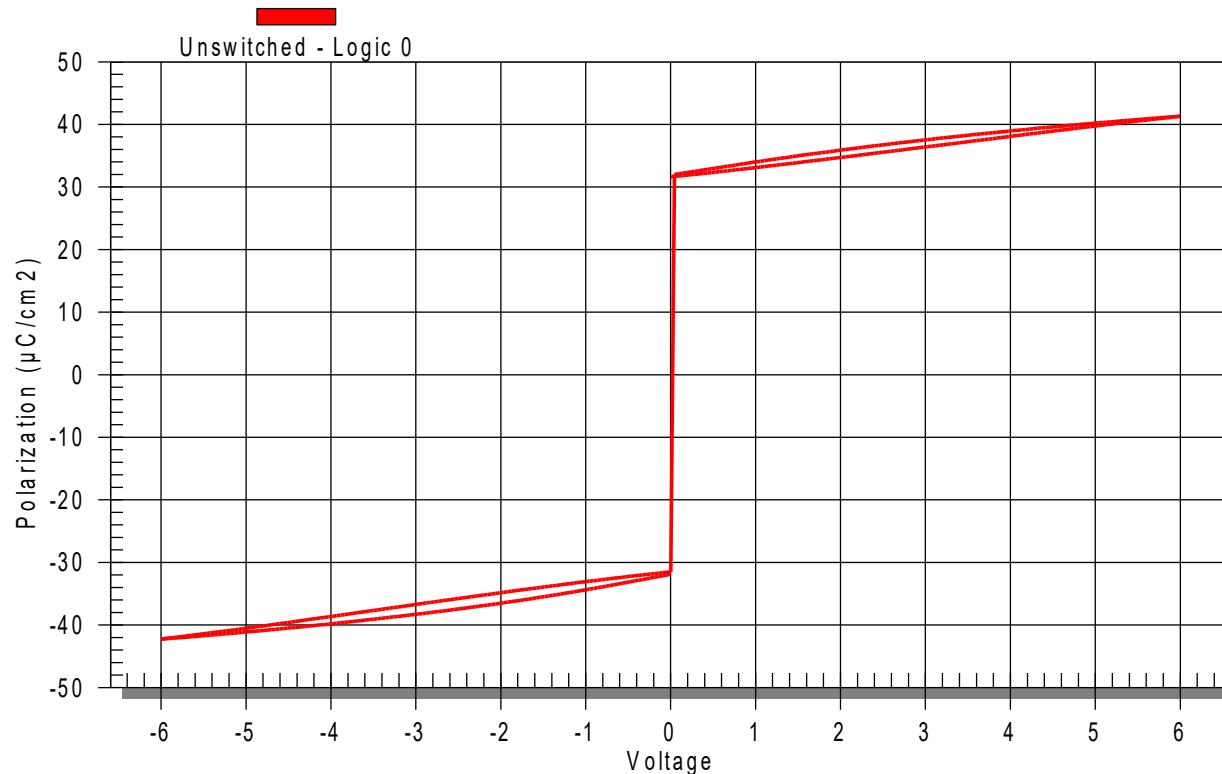


The two plots above are the two switching half-loops measured after preset half-loops in the opposite direction. The measurement above appears to be a single loop but it is actually the positive and negative measurements plotted against each other by aligning each with the origin.

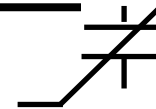


Non-switching Half-Loops

Switching Half-Loops
[Type AB WHITE]

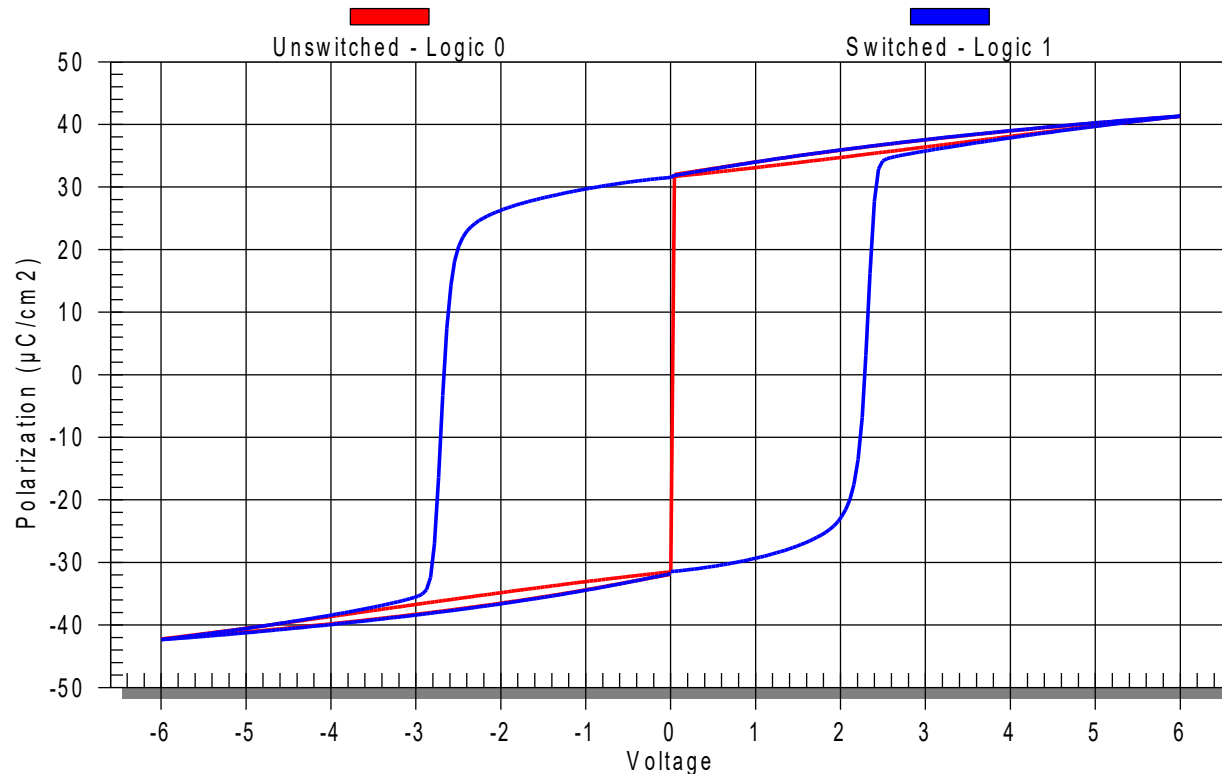


The non-switching half loops are plotted above so they line up with their respective switching half-loops.



Switching vs Non-switching

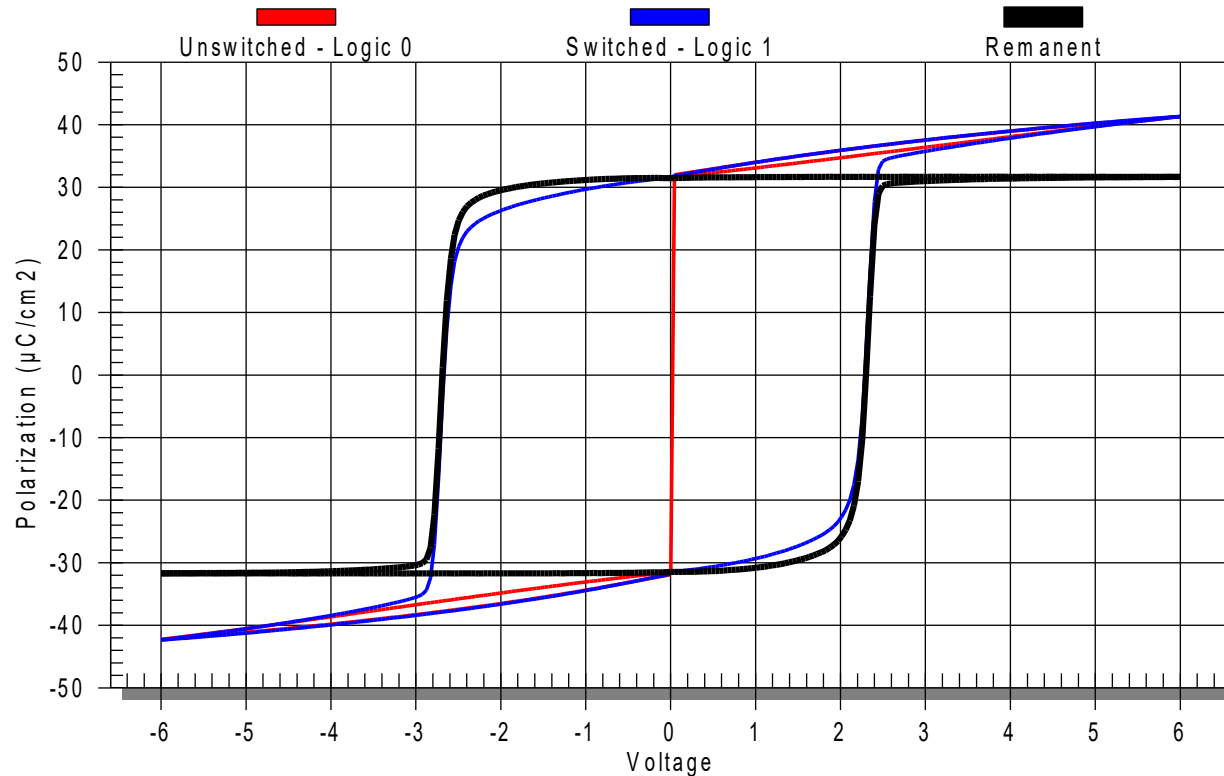
Switching Half-Loops
[Type AB WHITE]



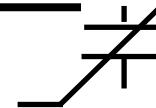
Note how the shape of the return trace of the non-switching loops matches that of the switching loops.

Remanent Hysteresis Loop

Switching Half-Loops
[Type AB WHITE]

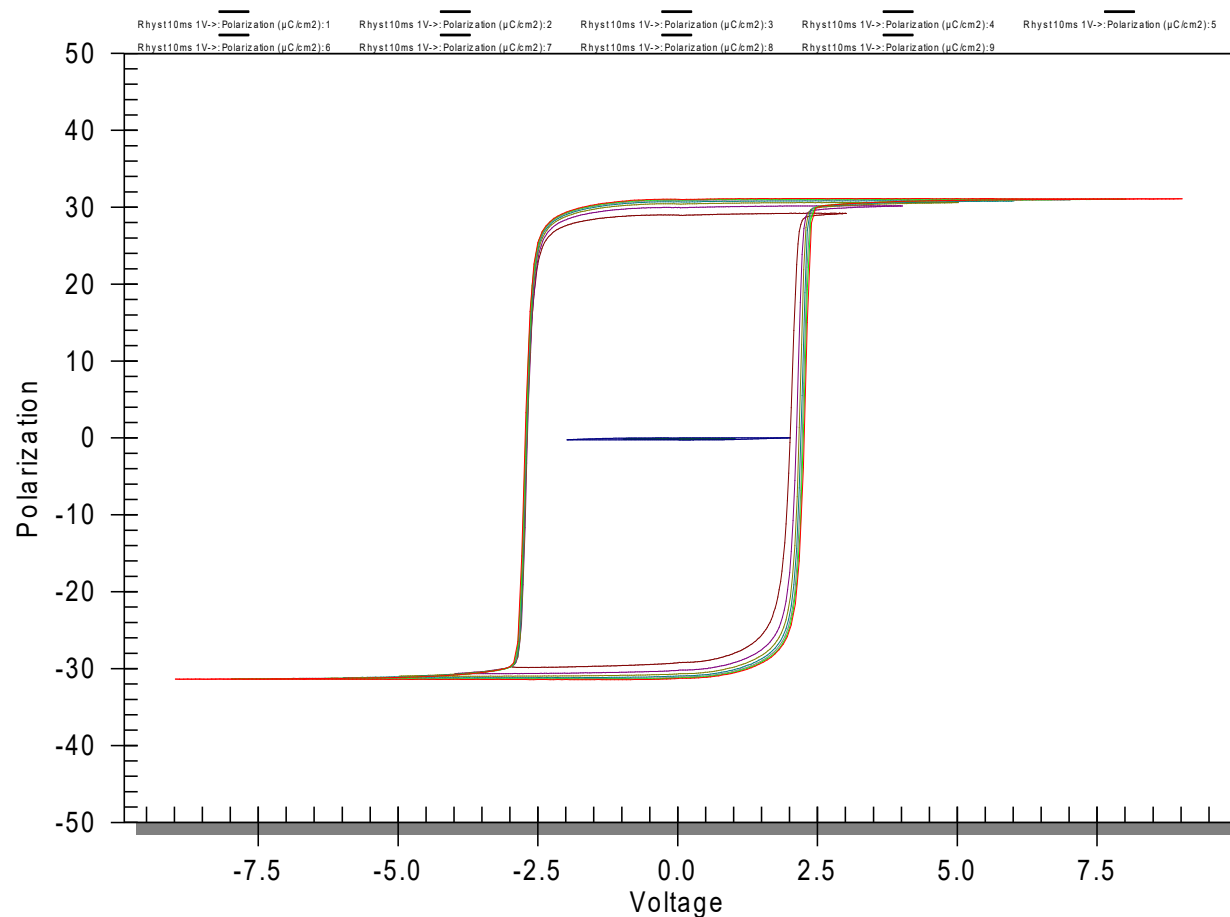


Subtracting the respective non-switching half-loops from their associated switching loops gives the remanent hysteresis loop. The remanent polarization value of the remanent hysteresis loop can also be plotted against voltage and frequency.



Nested Remanent Hysteresis Loops (10ms)

Rhyst vs Volts
[Type AB WHITE]

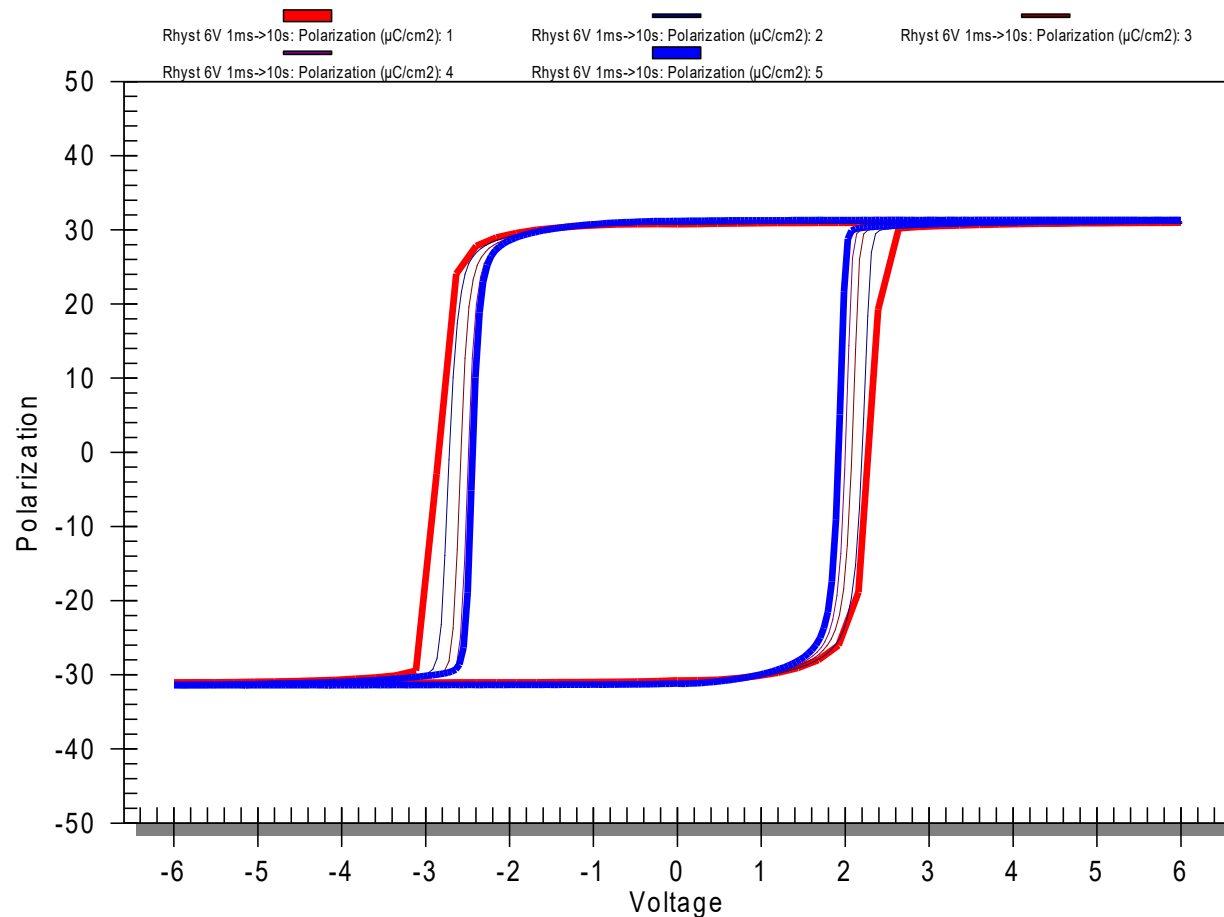


Remanent Hysteresis vs Period

(6V from 1ms to 10s)

Rhyst vs Period

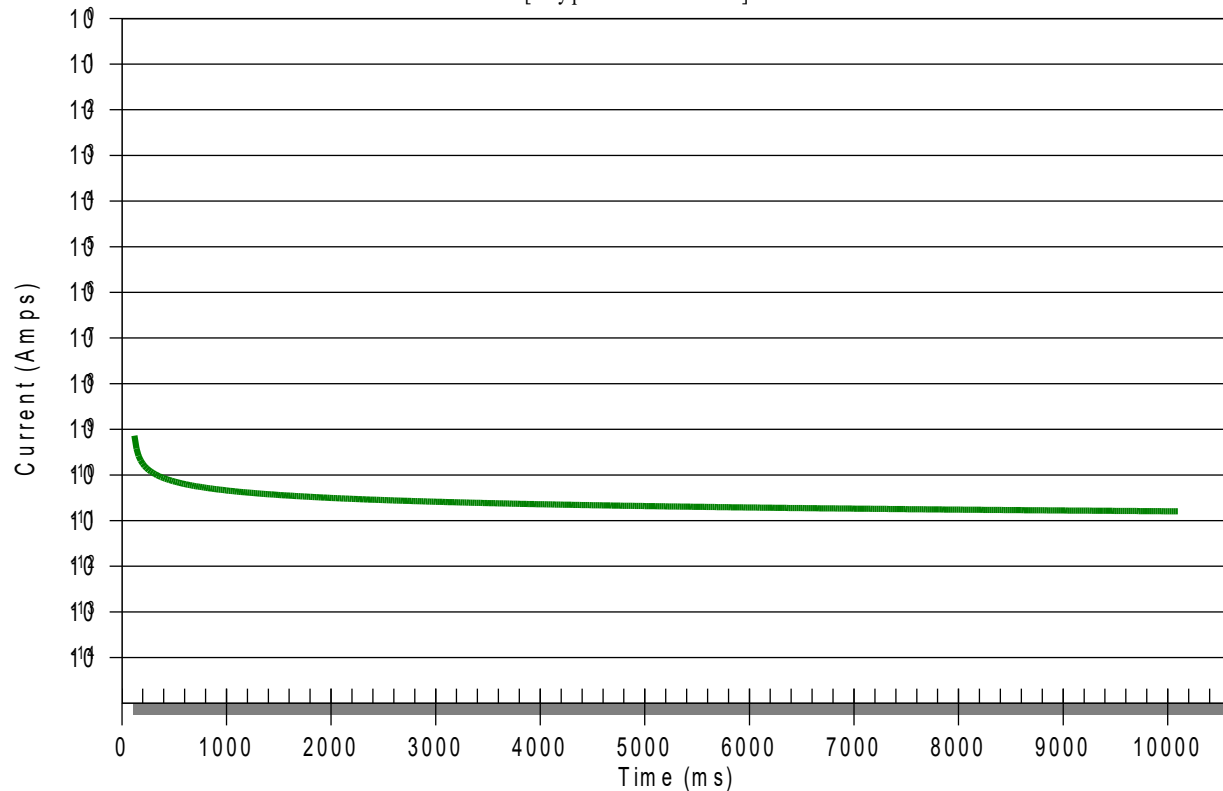
[Type AB WHITE]



Leakage Through Capacitor

(100ms Soak - 10s Integration)

DC Leakage in Amps @ 9V
[Type Ab WHITE]

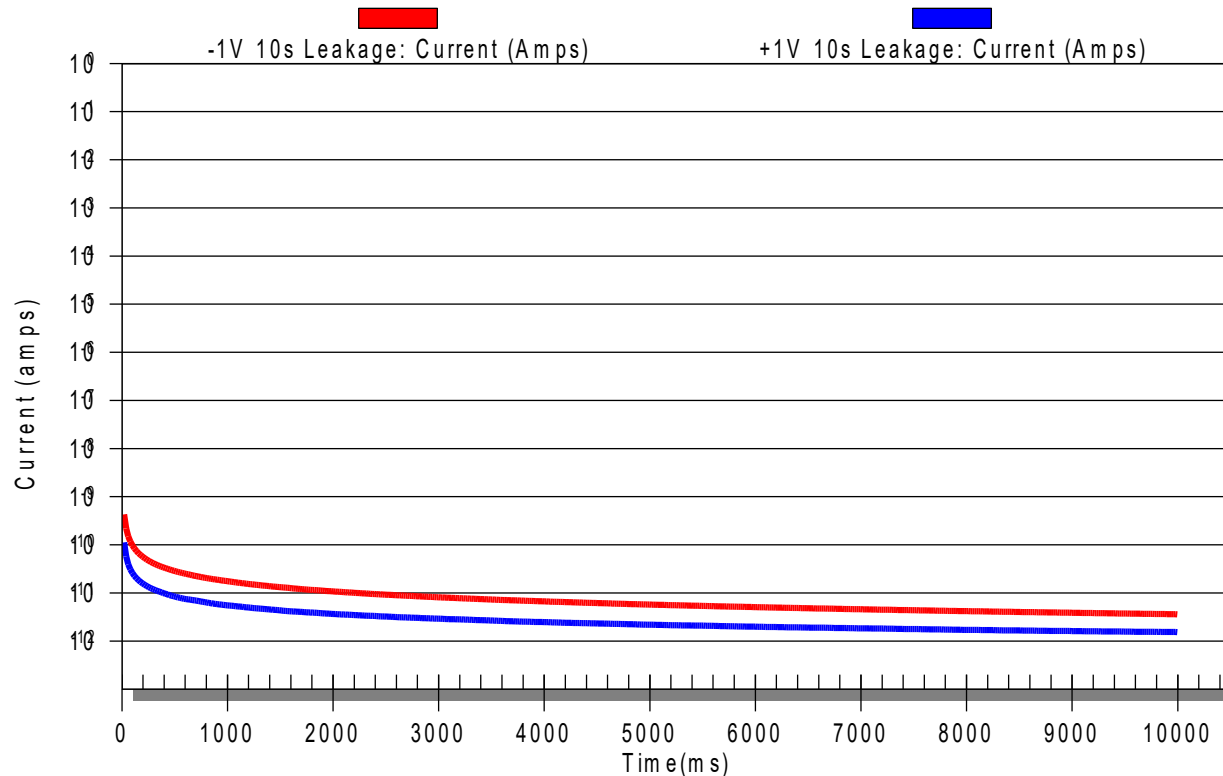


The leakage through the capacitor is measured by applying a fixed voltage across the capacitor and integrating over time the charge that passes through the capacitor. Normally, for PZT capacitors, the leakage decreases as the length of DC stress increases.

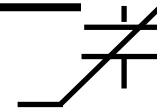
Remanent Polarization vs Leakage

(100ms Soak - 10s Integration)

Leakage @ 1 V With and Against +9 V Remanent State
[Type AB WHITE]



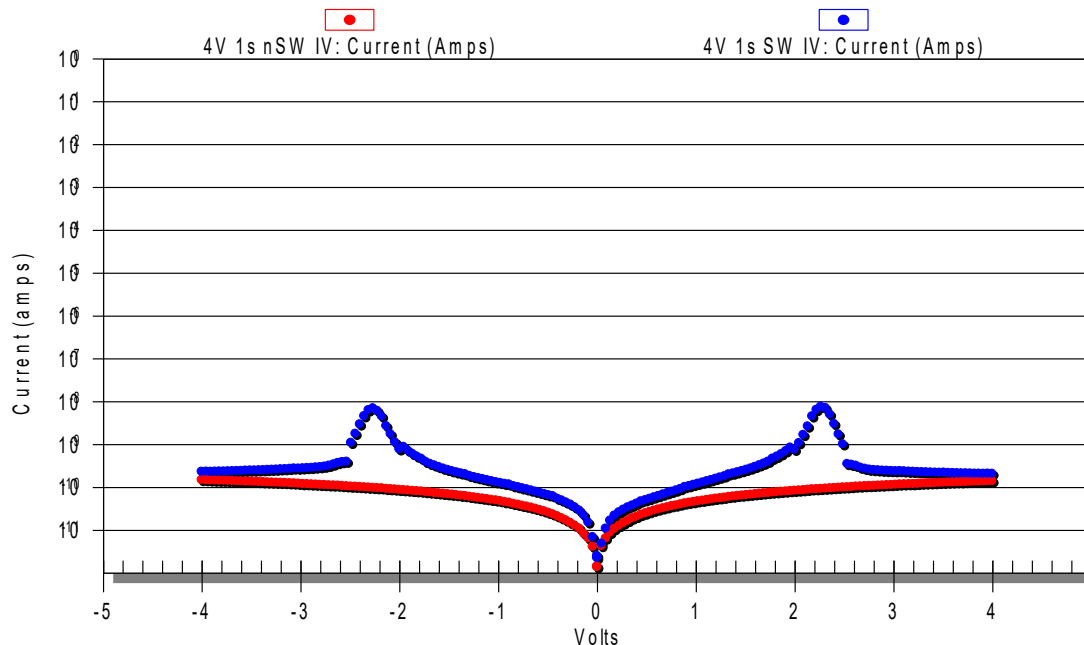
The state of the remanent polarization affects the leakage through the PZT capacitor. The two leakage measurements above were taken with opposite DC Bias but with the remanent polarization in the same direction for both measurements.



Current vs Voltage

(100ms Soak - 1s Integration)

Switched vs Unswitched 1s IV
[Radiant Type AB BLUE]

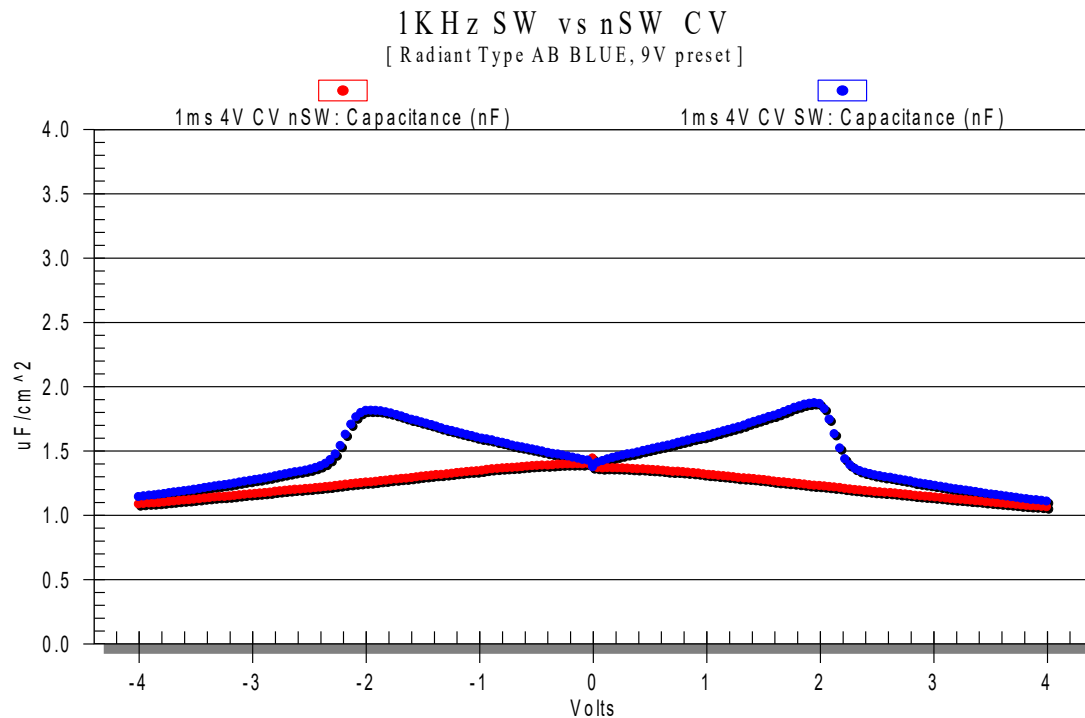


The Type AB BLUE capacitor is the same composition and has the same thickness as the WHITE capacitor. The BLUE has an area of 100,000 cm², ten times larger than the WHITE. The large area increases the net current through the device during leakage tests.

The current leakage of the capacitor can be plotted as a function of DC bias as well as the remanent polarization direction over a range of DC bias values. There are two IV measurements plotted above: 1) switching and 2) non-switching. Note the hump in the leakage for the “switching” measurement as the test voltage approaches the coercive voltage of the hysteresis loop. Leakage is highest at the coercive voltage.

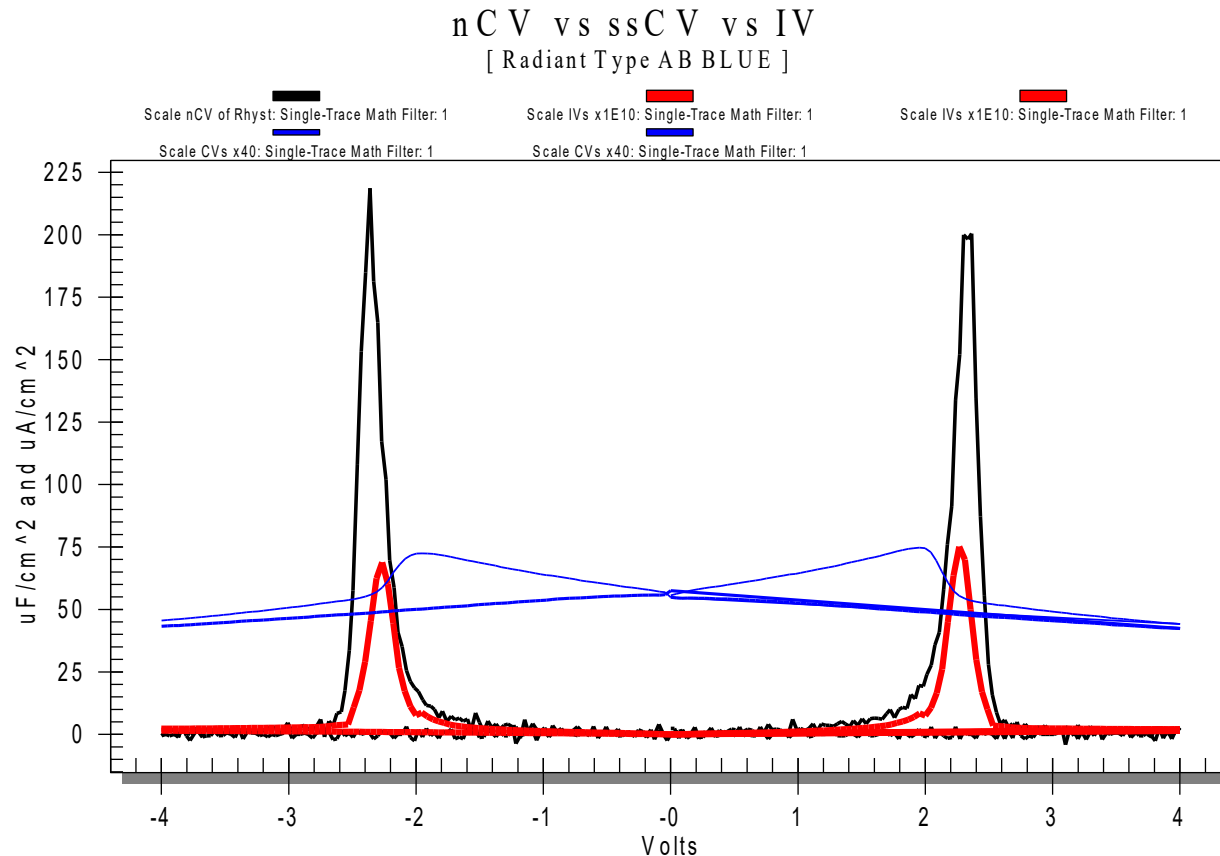
Small Signal Capacitance vs Voltage

(100ms Soak – 1kHz Test)



The small signal capacitance test evaluates the capacitance of the sample using voltage amplitudes so small that the remanent polarization is not changed by the test. Like the IV test, the small signal capacitance test can be executed over a range of voltages and it too is affected by the remanent polarization.

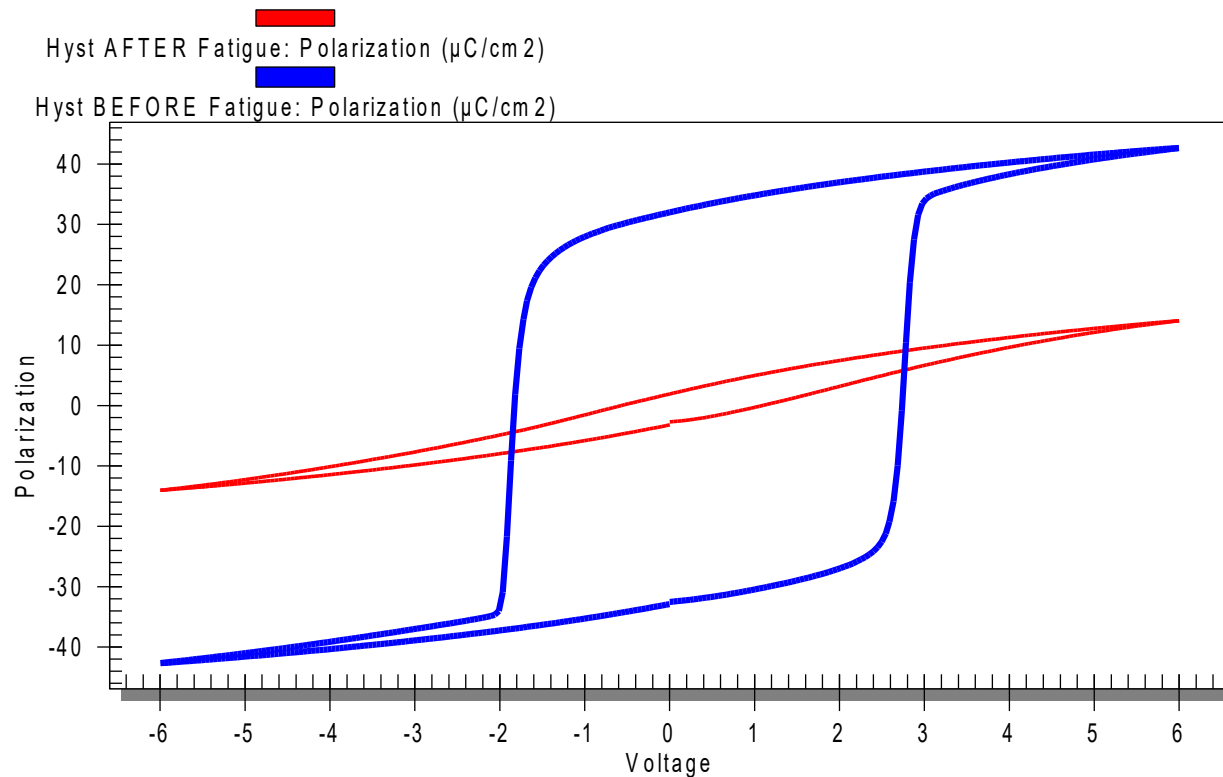
IV vs Capacitance vs Hysteresis



By re-scaling each of the measurements and plotting them together on the same graph, the relationship between the leakage vs voltage, the small signal capacitance vs voltage, and the nCV of the remanent polarization vs voltage may be examined. Interesting!

Fatigue

Hysteresis BEFORE and AFTER Fatigue
[Radiant Type AB WHITE]

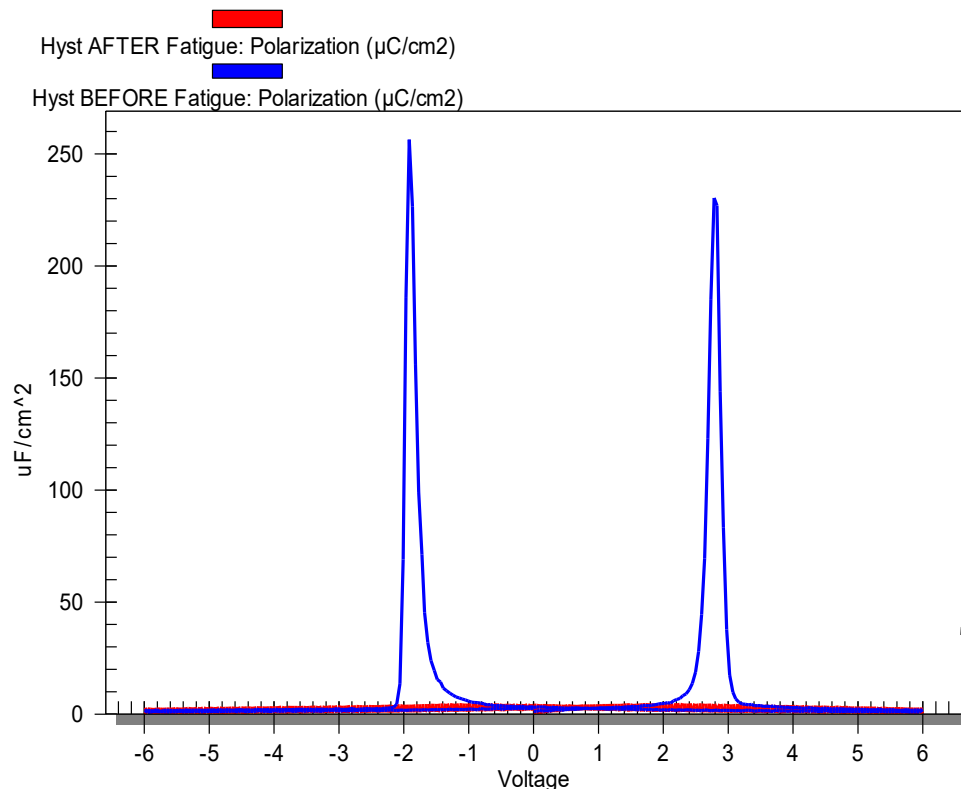


Fatigue is defined as the loss of polarization from repeated cycling of the capacitor around its loop. Experience indicates that the domains must switch direction for fatigue to occur. Fatigue does not occur with mono-polar pulsing where remanent polarization does not switch (non-switching half-loops). The 20/80 PZT of the Type AB capacitors fatigues strongly.

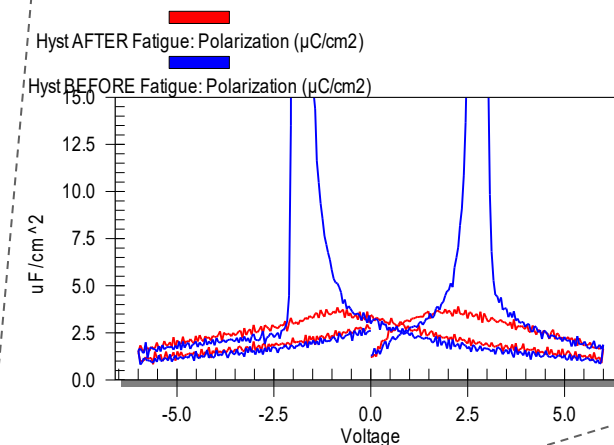
Fatigue



nCV BEFORE and AFTER Fatigue
[Radiant Type AB WHITE]



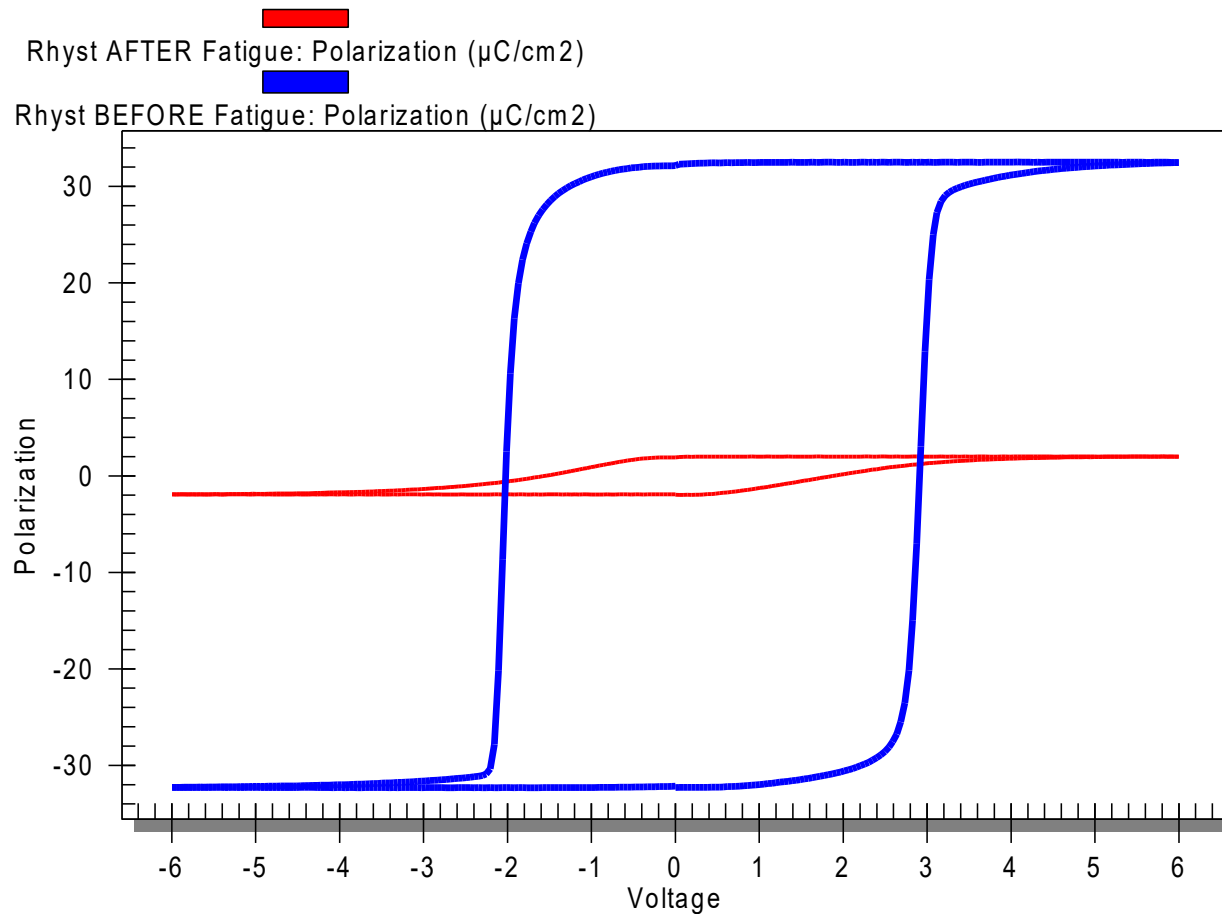
nCV BEFORE and AFTER Fatigue
[Radiant Type AB WHITE]



From the nCV of the hysteresis loop before and after fatigue, it appears that the switching peak evaporated as the fatigue progressed. The expanded view on the right indicates that the linear capacitance and leakage, already small before the test began, changed little.

Fatigue

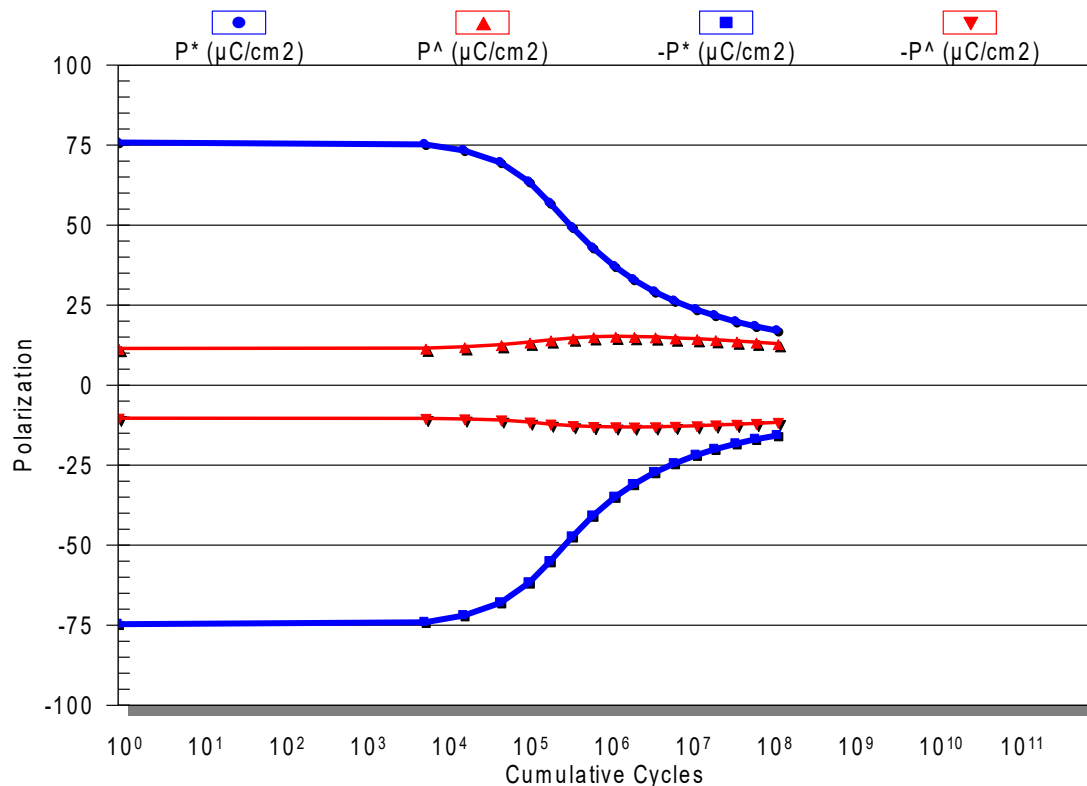
Rhyst BEFORE and AFTER Fatigue
[Radiant Type AB WHITE]



The remanent hysteresis before and after fatigue indicates that remanent polarization decreased substantially but some still exists after fatigue.

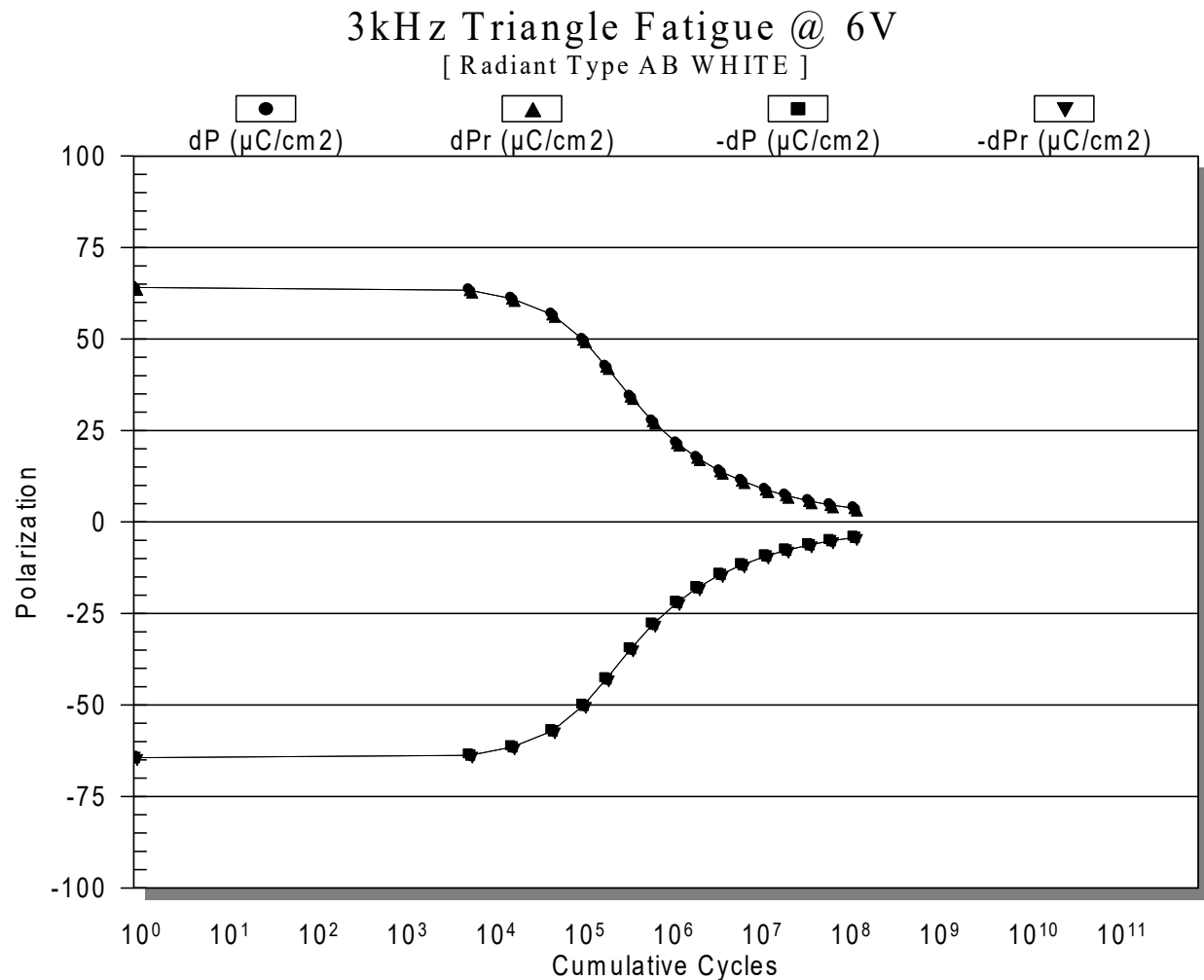
Fatigue

3 kHz Triangle Fatigue @ 6 V
[Radiant Type AB WHITE]



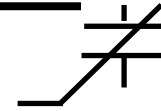
The classic fatigue test monitors the PUND values as a function of cycles. This capacitor was cycled with a 3kHz triangle wave at 6V to produce the fatigue effect. Notice that the non-switching parameters $\pm P^{\wedge}$ did not change much while the switching parameters $\pm P^*$ changed quite a bit. It is primarily the remanent polarization that fatigues.

Fatigue

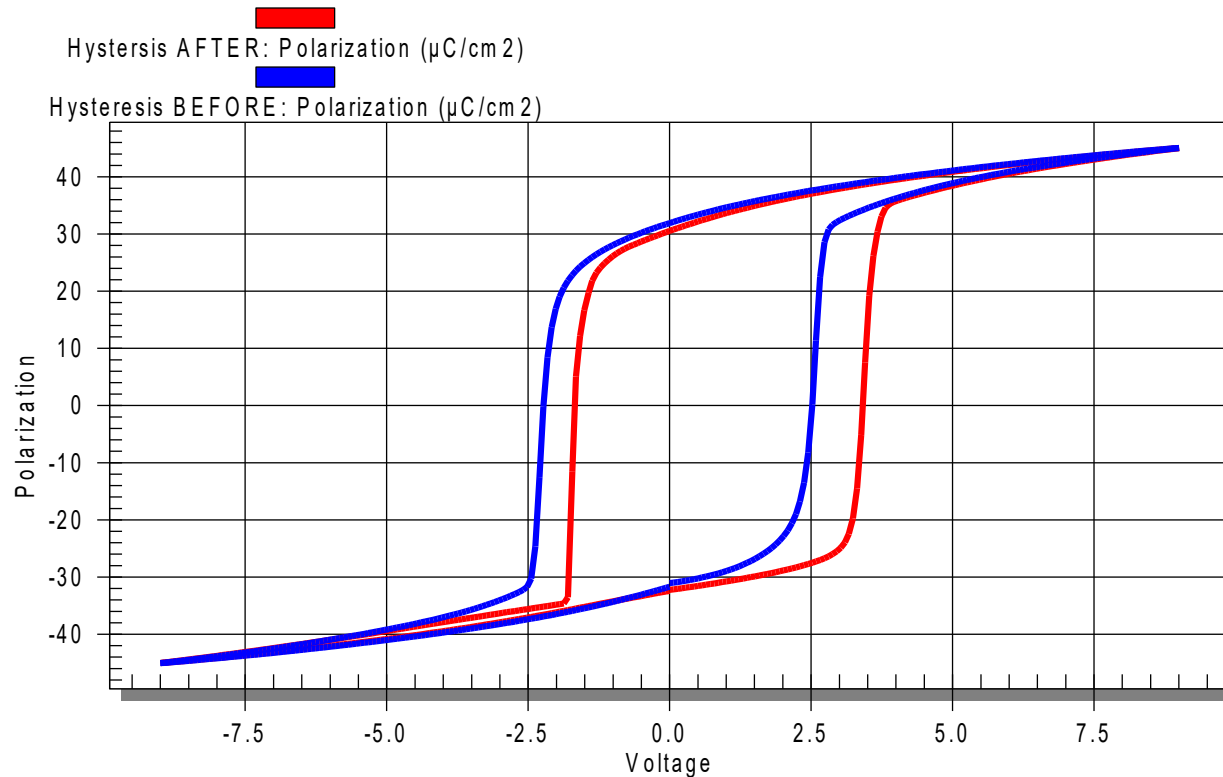


It is primarily the remanent polarization that fatigues.

Imprint

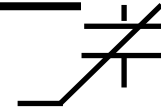


Hysteresis Before and After 155°C Imprint
[Type AB WHITE Unpackaged Die]

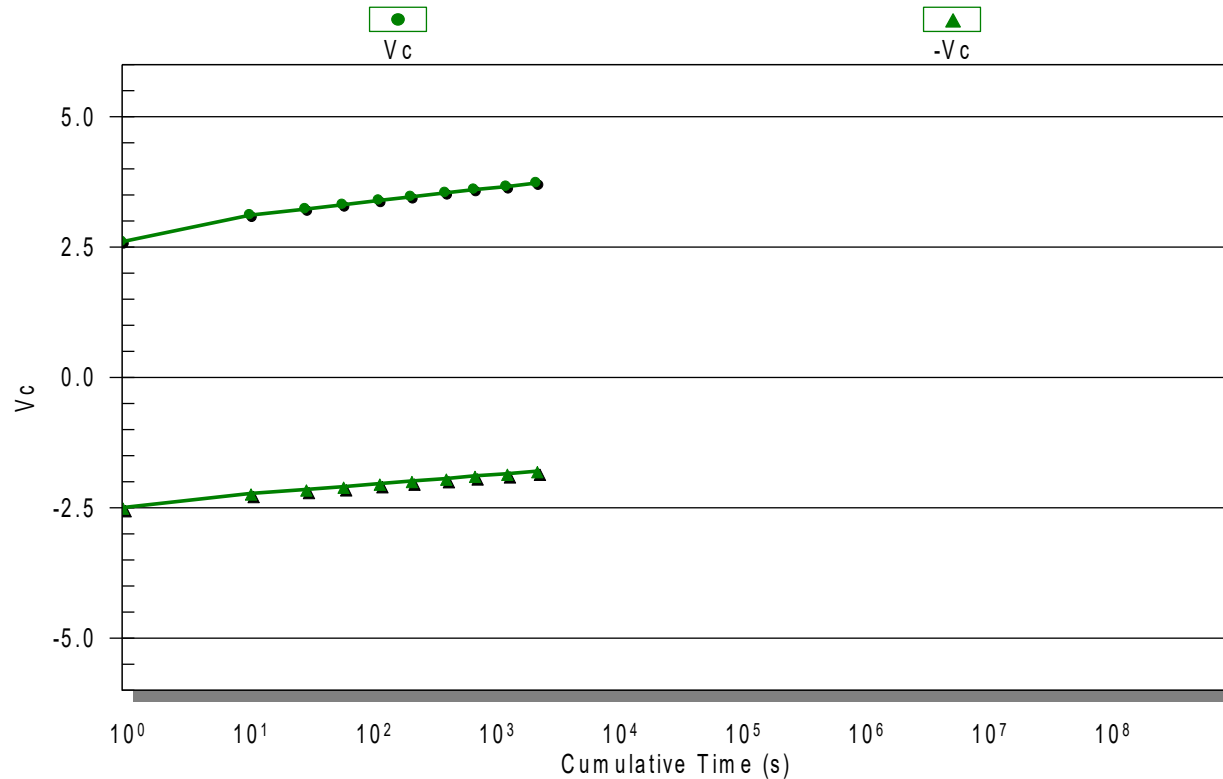


Imprint is a reliability issue with memory capacitors. Its primary mechanism is the gradual growth of an internal DC bias over time that shifts the hysteresis loop horizontally on the voltage axis. It is accelerated by temperature. The capacitor above saw 2300 seconds at 155°C between the blue loop and the red loop.

Imprint

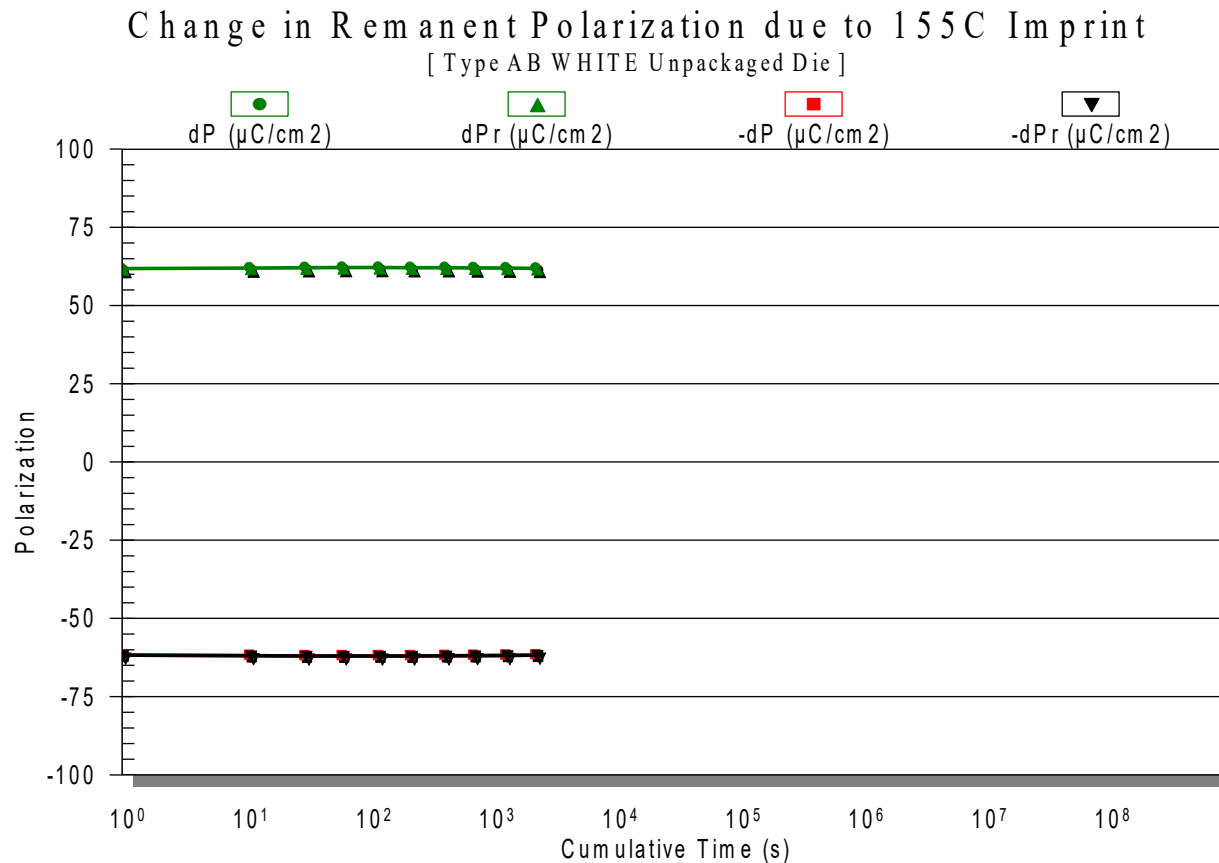


Coercive Voltage Shift due to 155°C Imprint
[Type AB WHITE Unpackaged Die]



1×10^9 seconds is equal to 30 years. $1 \times 10^{8.5}$ seconds equals 10 years. The imprint drift occurs constantly as long as the capacitor remains in the same remanent polarization state. In the data above, the capacitor was in the “down” state during the 155°C imprint periods.

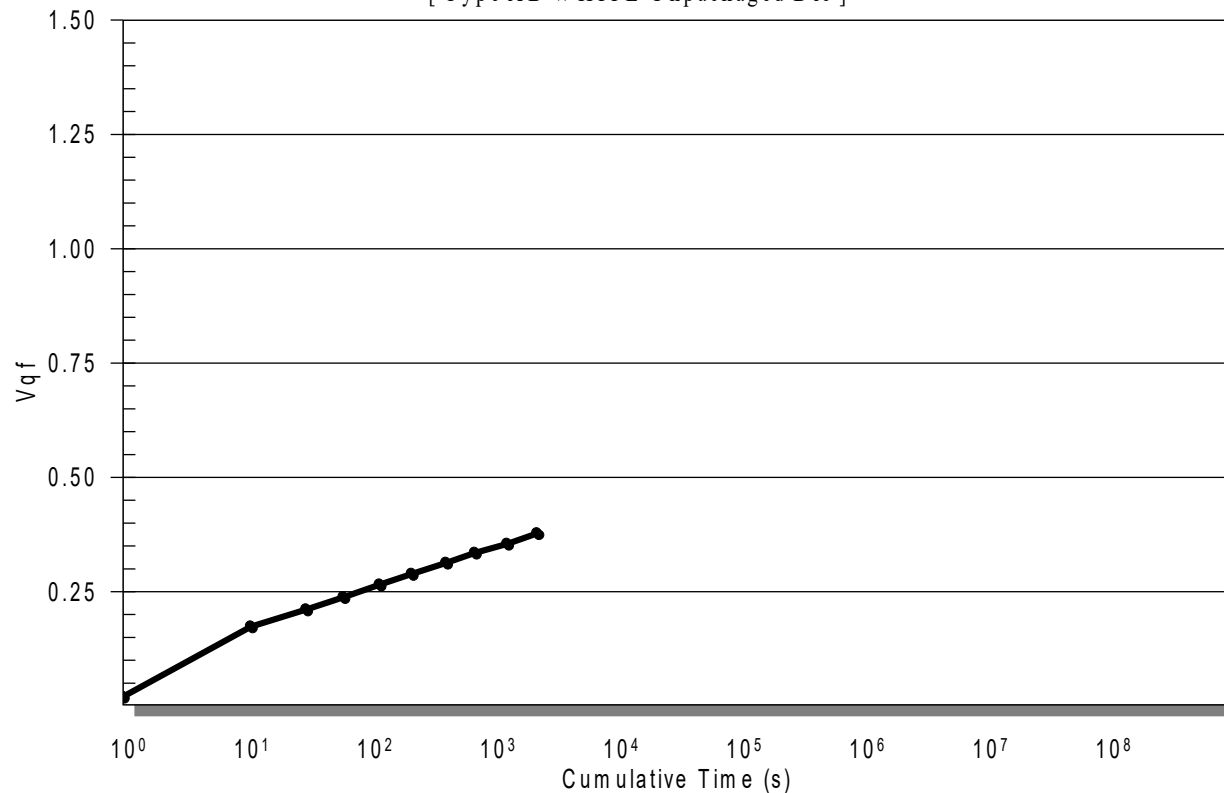
Imprint



Despite the fact that the capacitor has shifted almost a full volt to the right, the remanent polarization of the capacitor, measured periodically during the imprint period, shows no degradation. Nevertheless, once the hysteresis shifts far enough, the remanent polarization will begin to degrade.

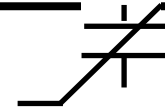
Imprint

Figure of Merit vs Time
[Type AB WHITE Unpackaged Die]

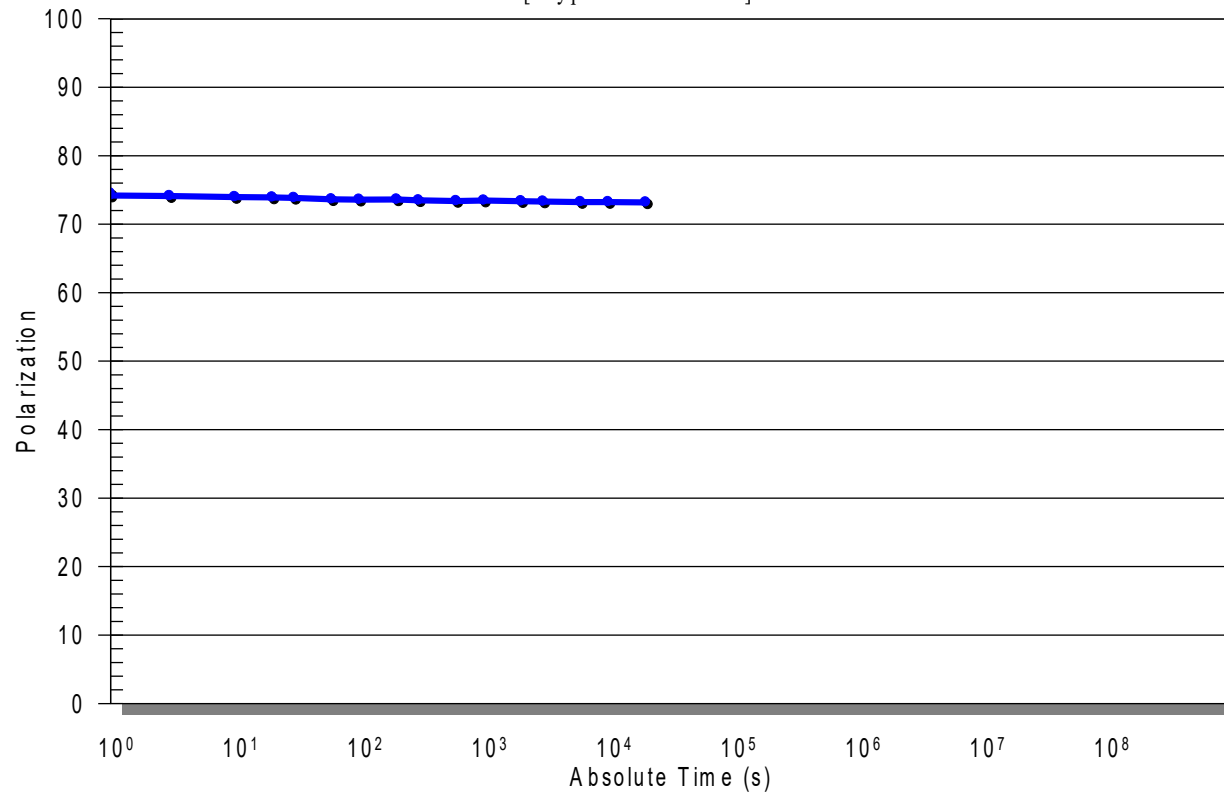


The Imprint Figure of Merit is defined by Radiant as the voltage shift divided by the initial, unimprinted coercive voltage. When the hysteresis loop translates the distance of one coercive voltage (i.e. FOM = 1), FeRAM type memories using such a capacitor will begin to fail. At that point, the written data becomes permanently “imprinted” in the memory. Accordingly, the capacitor above will just imprint in 30 years at 155C.

Retention



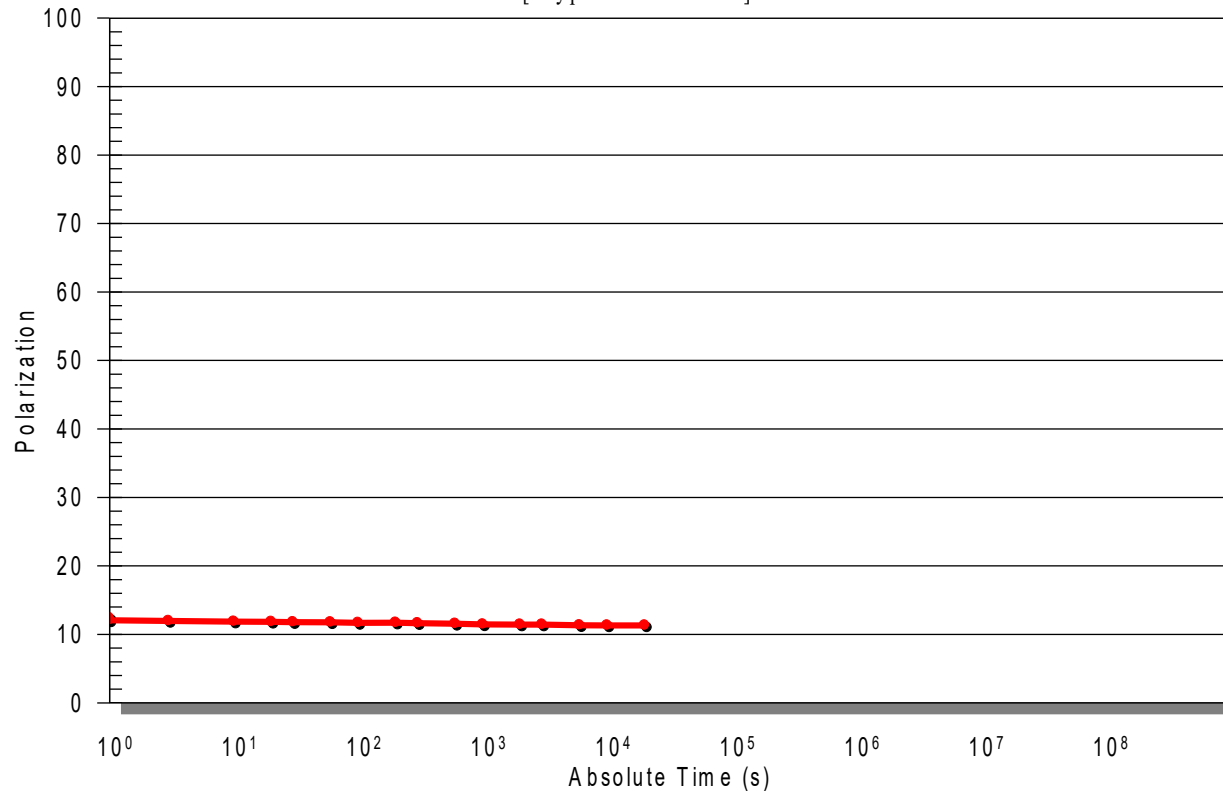
Capacitor A Retention of Switched State
[Type AB WHITE]



Retention is a simple test: apply a write pulse, wait for the retention time, and apply a read pulse. Repeat for longer periods. In the test plotted above, the capacitor retained the “down” state so that it switched up each time it was read.

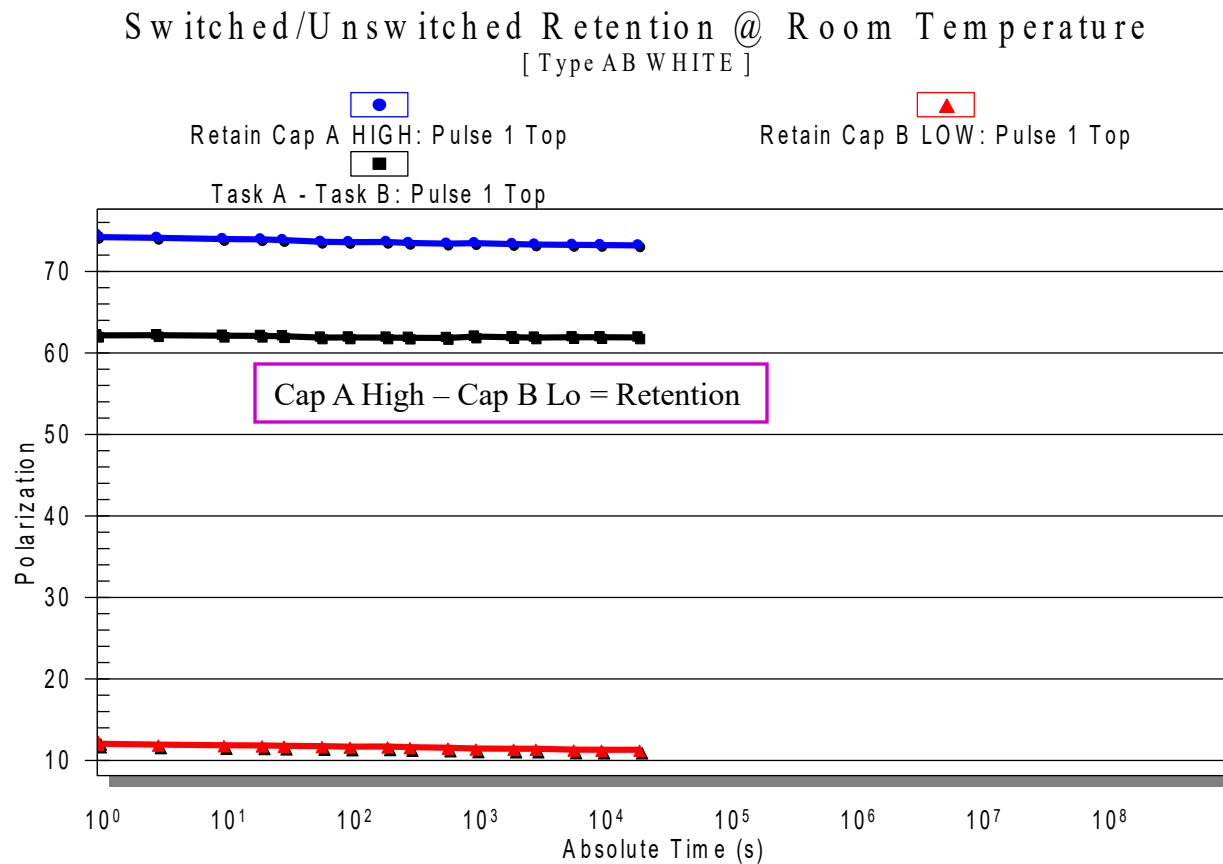
Retention

Capacitor B Retention of Non-switched State
[Type AB WHITE]

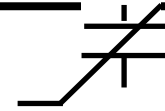


Retention is a complex test because imprint occurs during the measurement. The stored state determines the direction of imprint which shifts in opposite directions for opposite states. Retention *cannot* be measured by running sequential retention tests in opposite states on the same capacitor. The second test would start from an imprinted condition! Retention of opposing states must be measured on two new, identical capacitors.

Retention



The high and low states can be subtracted to see the trend of the retained state over the useful life of the memory.



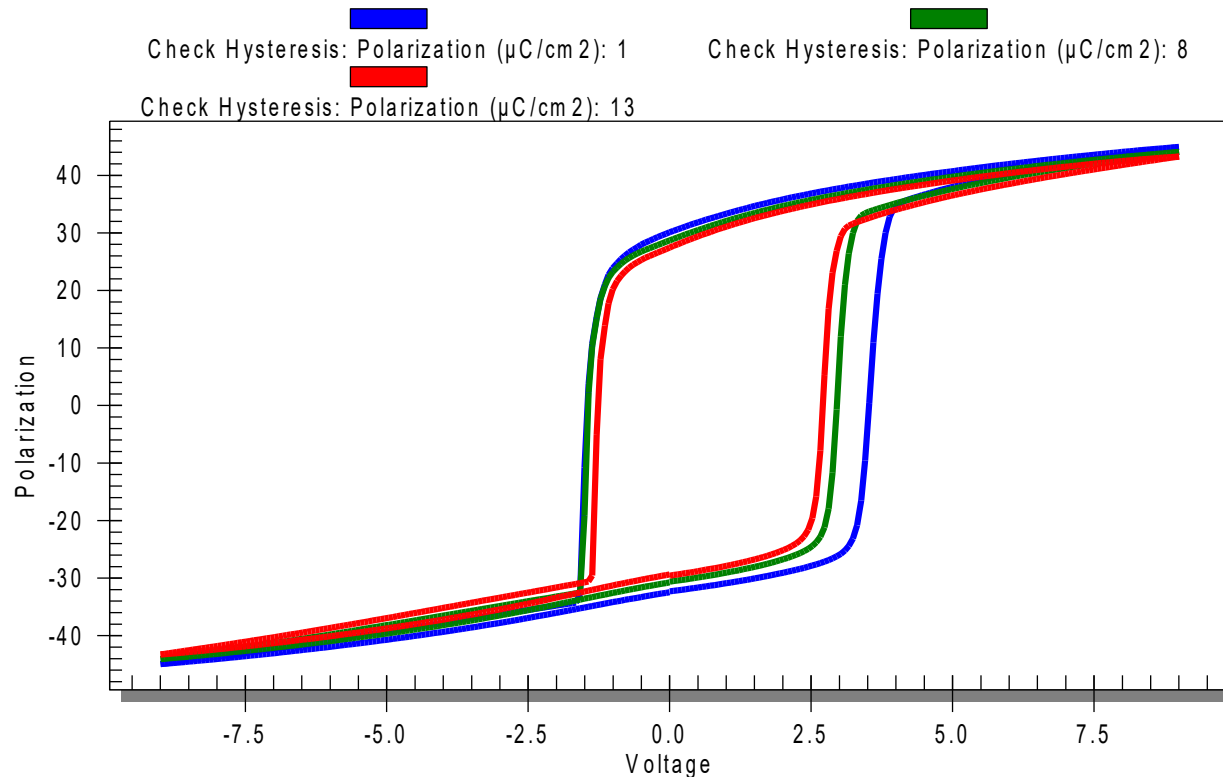
Capacitor Parameters vs Temperature

- The previous measurements in this document demonstrate the multitude of parameters that define device performance.
- Most of these parameters vary with temperature.
- In the next section of this document, the same properties, hysteresis, PUND, leakage, etc., will be plotted as a function of temperature.
- All of the temperature-based measurements were conducted with individual dice on the hot chuck of a semiconductor probe station.

Hysteresis vs Temperature

(10ms Period, 9V)

Hysteresis vs Temperature
[Type AB WHITE die]



Blue = 30°C

Green = 100°C

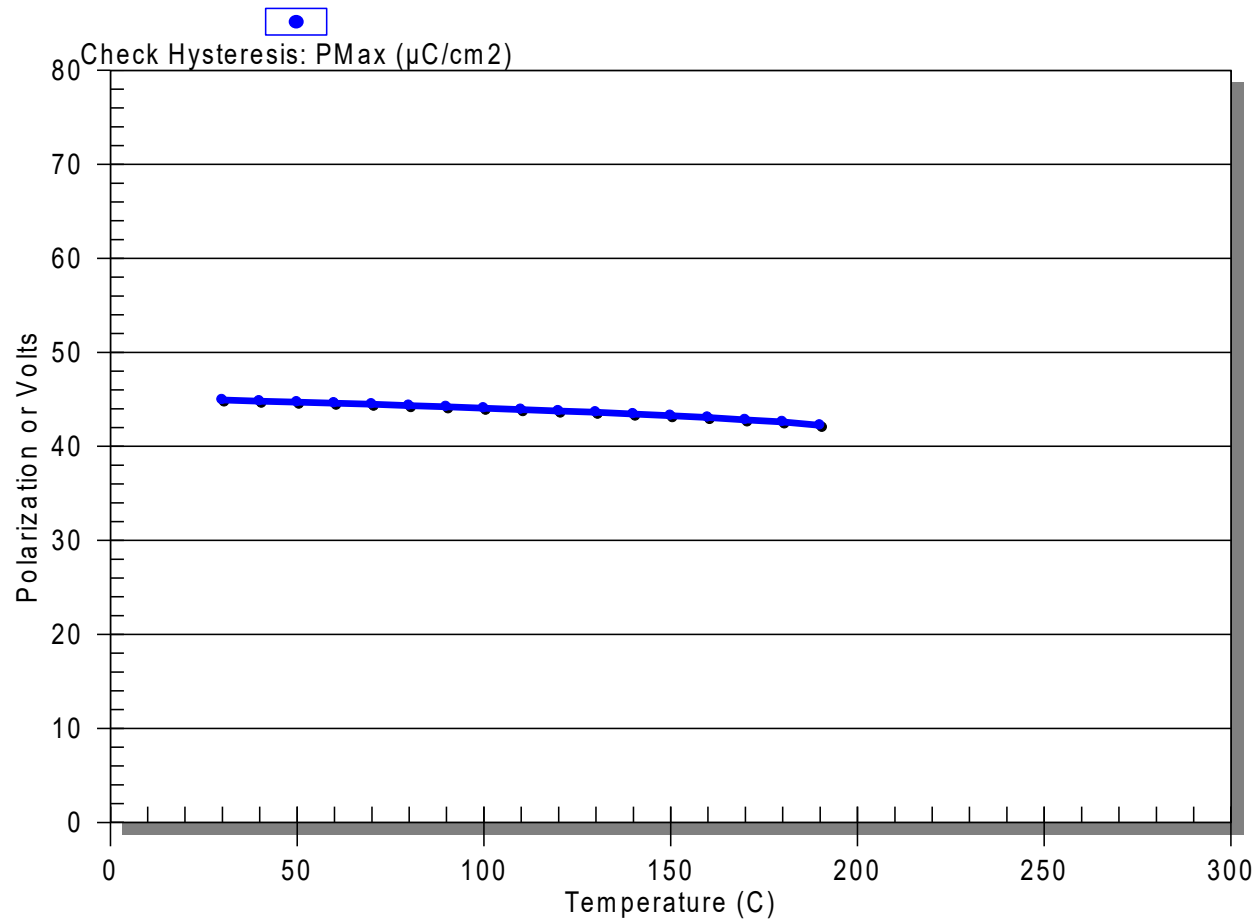
Red = 150°C

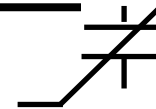
Note the offset hysteresis loop due to imprint. The capacitor being tested was intentionally imprinted for an hour prior to this test so it would not move during the test.

Pmax vs Temperature

(10ms Period, 9V)

Pmax vs Temperature
[Type AB WHITE die]

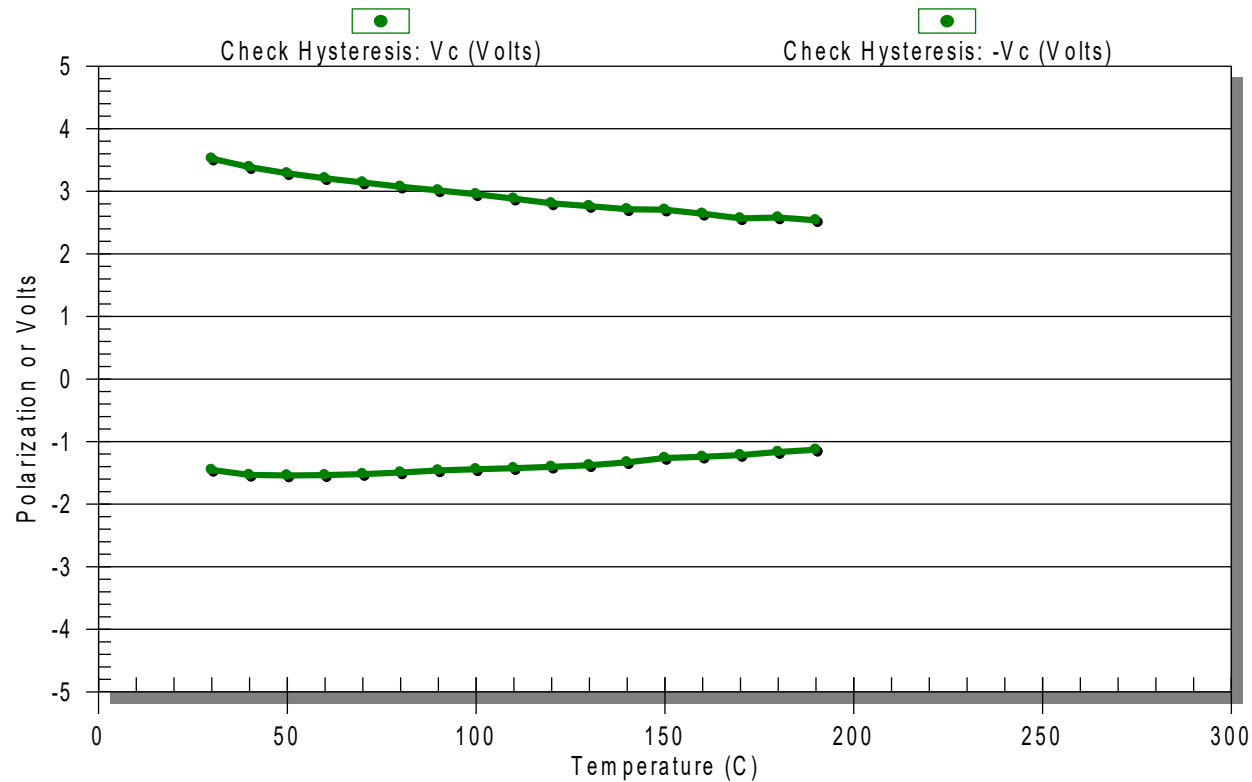




V_c vs Temperature

(10ms Period, 9V)

P_{max} vs Temperature
[Type AB WHITE die]

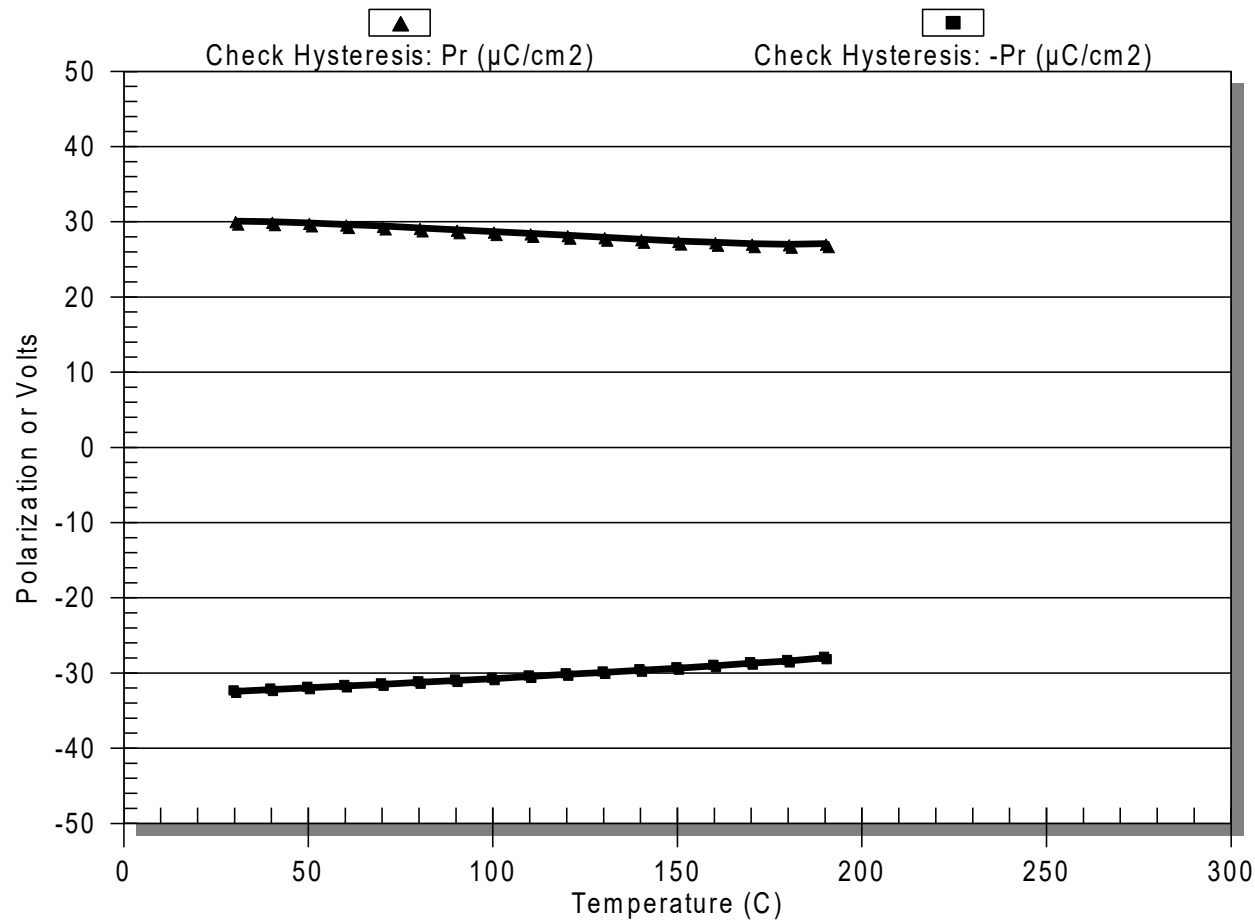


The $\pm V_c$ values are asymmetrical from the beginning because of the initial imprint condition of the sample.

$\pm Pr$ vs Temperature

(10ms Period, 9V)

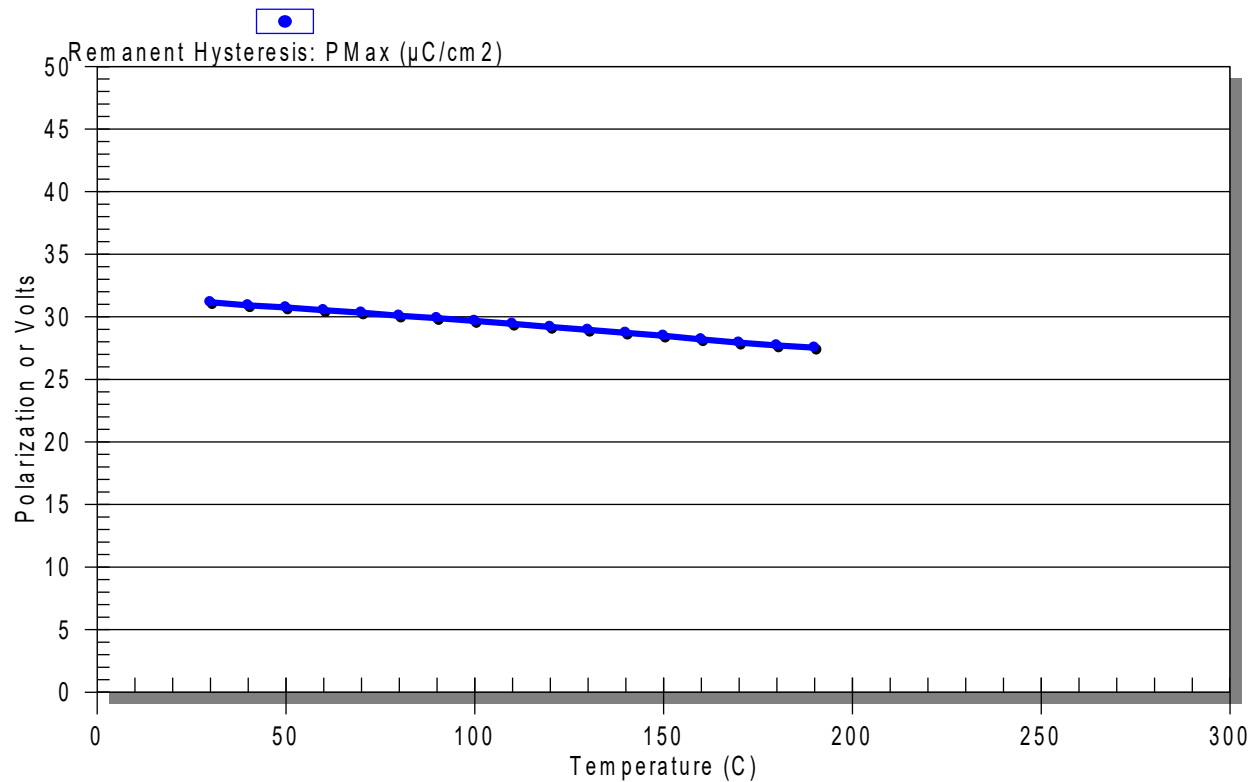
Pmax vs Temperature
[Type AB WHITE die]



Remanent Hysteresis vs Temperature

(10ms Period, 9V)

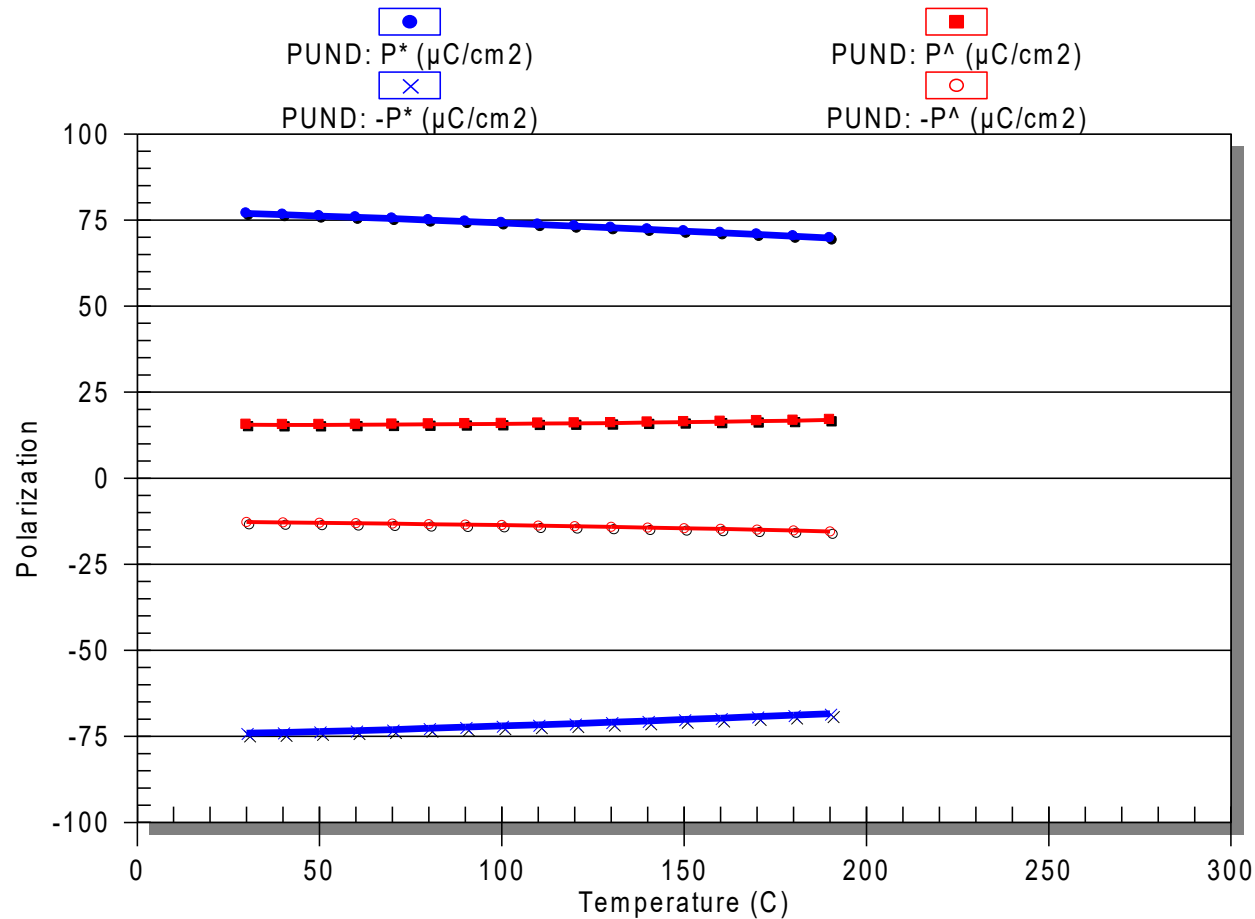
Remanent Hysteresis Parameters vs Temperature
[Type AB WHITE die]



PUND vs Temperature

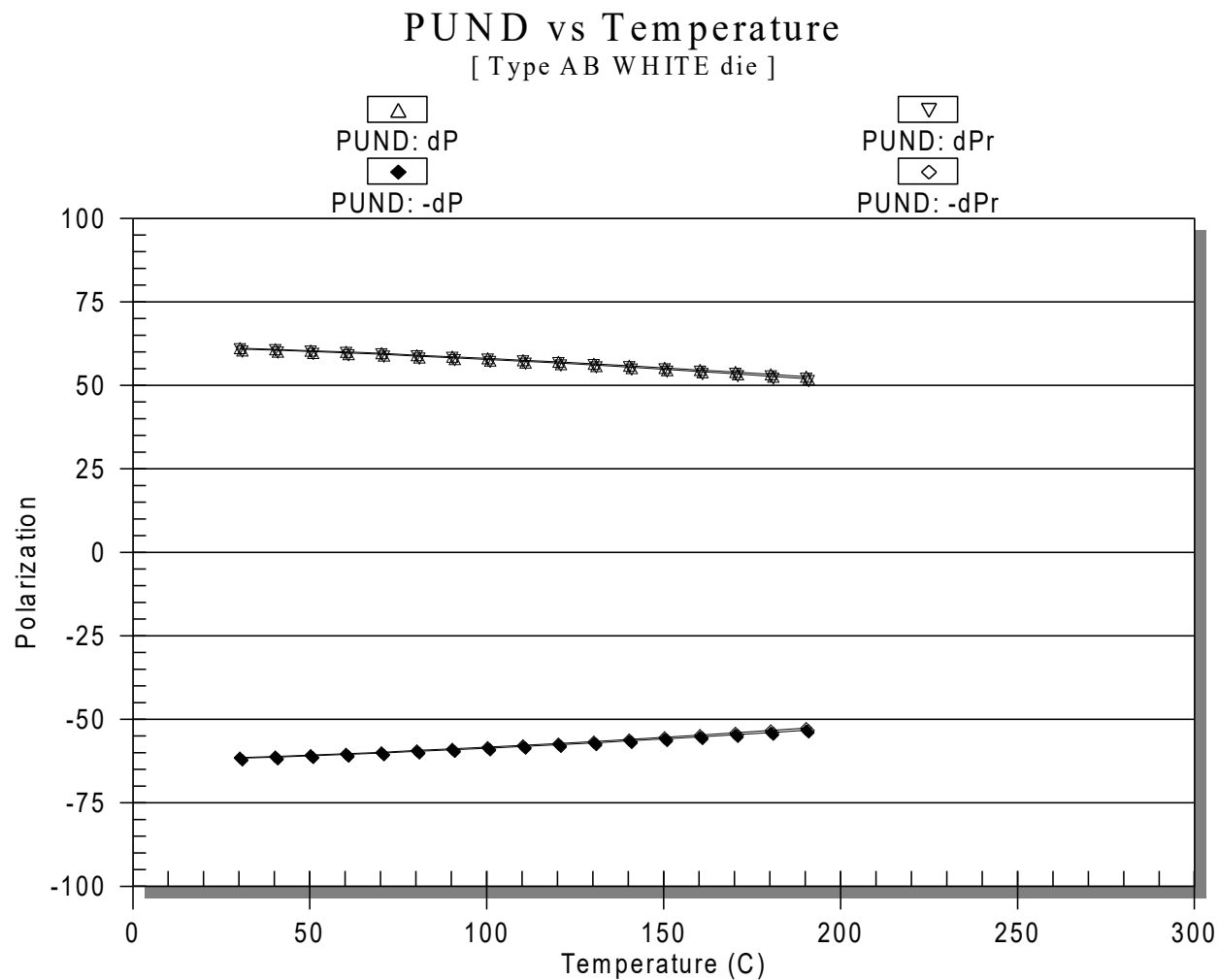
(1ms Period, 9V)

PUND vs Temperature
[Type AB WHITE die]



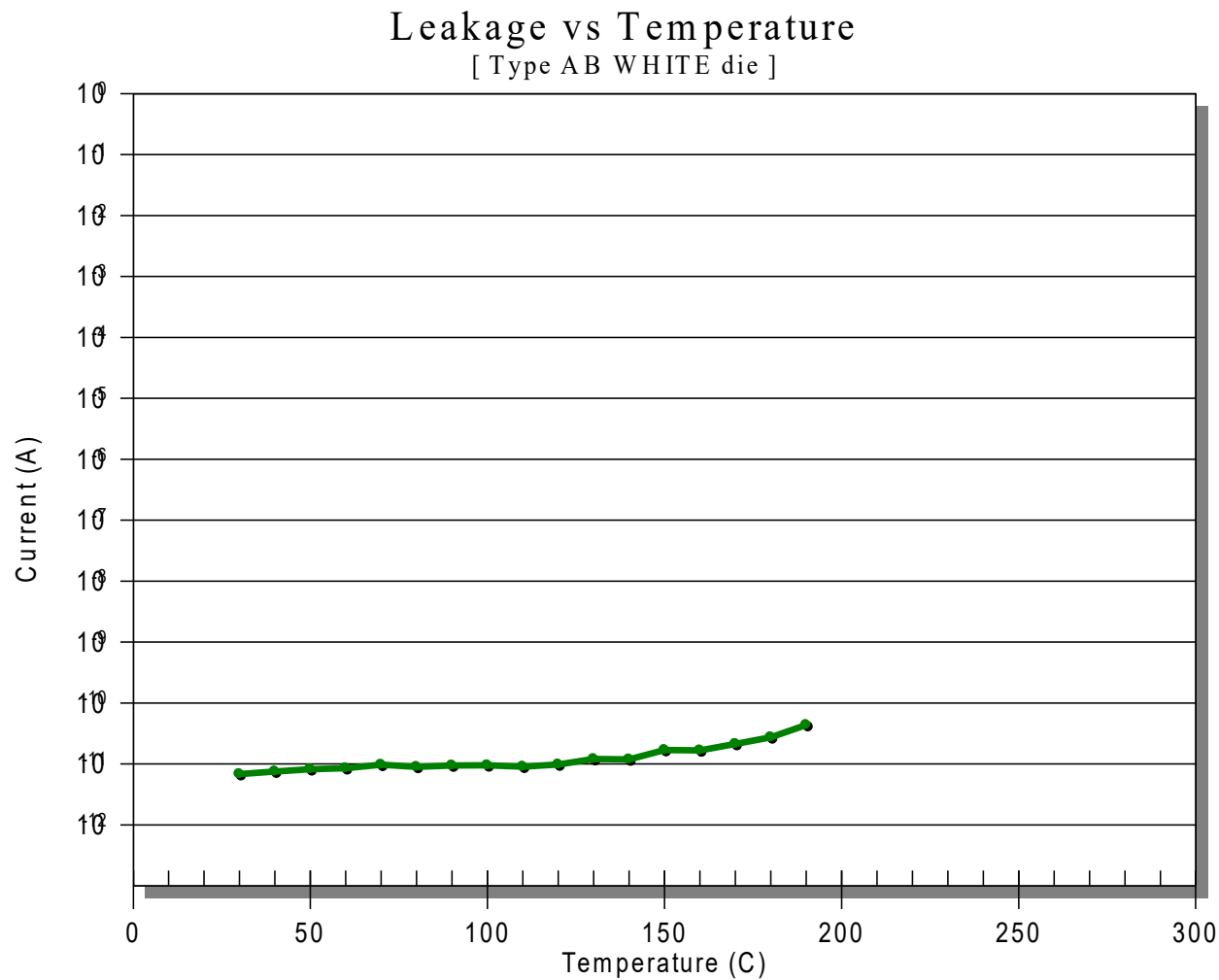
PUND vs Temperature

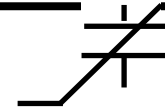
(1ms Period, 9V)



Leakage vs Temperature

(1ms Period, 9V)



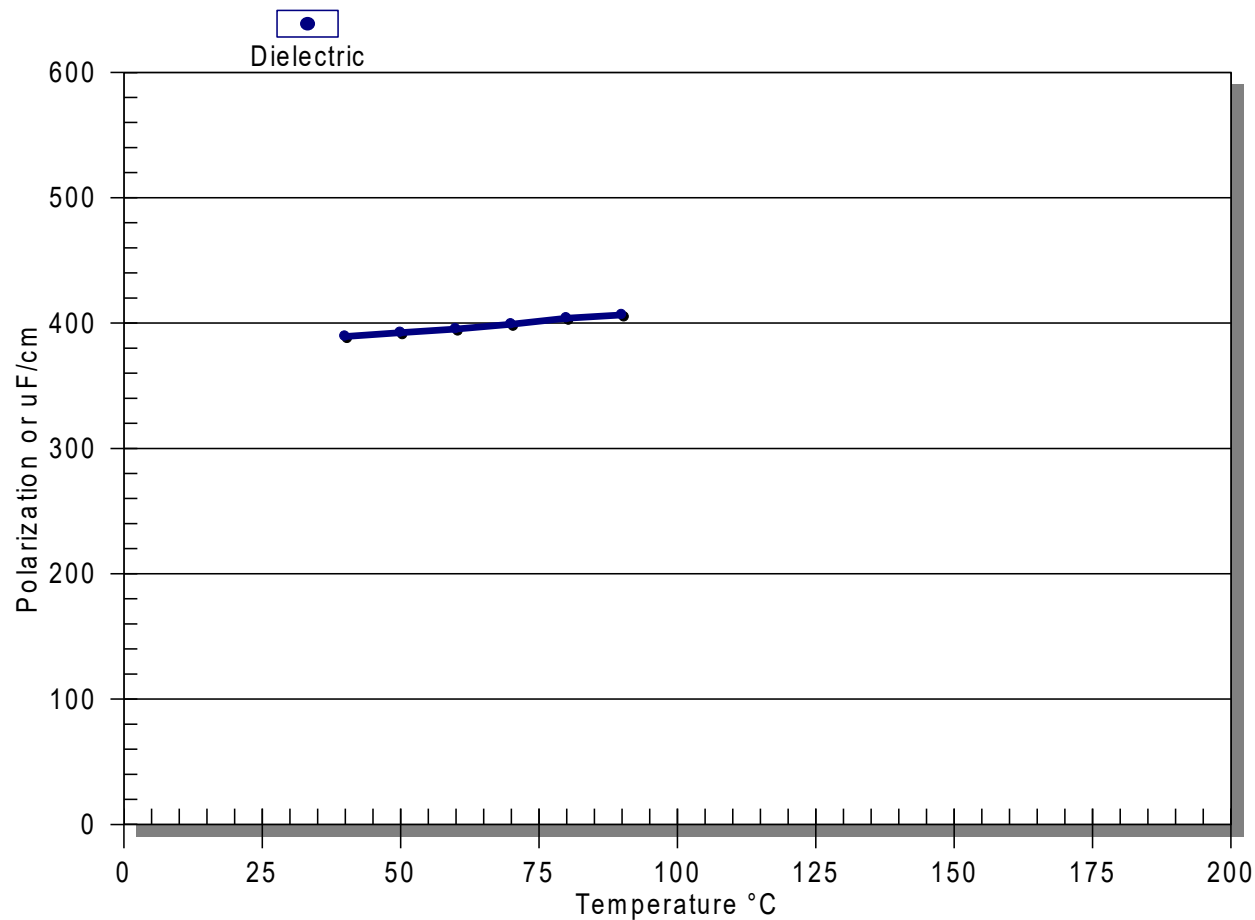


Pyroelectric Coefficients

- Vision has one task, Chamber, that will measure the pseudo-static true and false pyroelectric properties of a capacitor.
- The true pyroelectric coefficient is the change in remanent polarization (Remanent Hysteresis or PUND) with temperature.
- The false pyroelectric coefficient is the change in the dielectric constant (Small Signal Capacitance) with temperature.
- The Chamber task stabilizes the sample at each temperature in the profile and measures the remanent polarization and the small signal capacitance.

Dielectric Constant vs Temperature

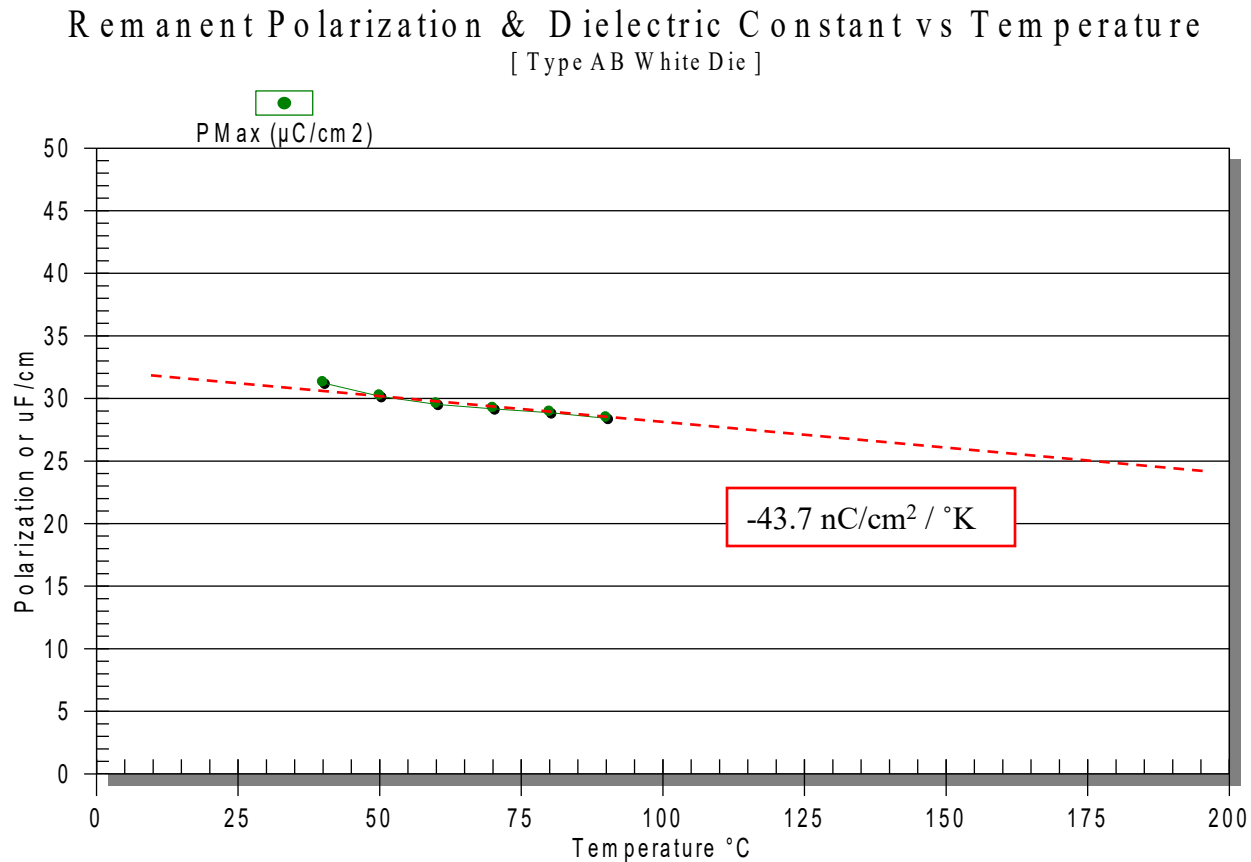
Remanent Polarization & Dielectric Constant vs Temperature
[Type AB White Die]



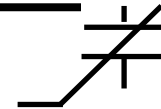
The dielectric constant usually increases with increasing temperature.

Remanent Polarization vs Temperature

(1ms Period, 9V)



The remanent polarization usually decreases with increasing temperature. The slope of the decrease is the true pyroelectric coefficient for that material.



Conclusion

- There are a multitude of performance parameters for ferroelectric capacitors.
- A capacitor's performance will vary according to its composition, electrodes, and fabrication process flow.
- The data plotted in this document are contained in a single dataset: "typical type ab performance 07_07_08.dst" which can be downloaded from www.ferrodevices.com/components2.html.
- For those without a Radiant tester, Vision can be downloaded from www.ferrodevices.com/tdownload.html. After installing Vision, you can open datasets and plot the data they contain.
- Please contact Radiant by e-mail with any questions or to ask our opinion of your own measurements. Remember to send us the dataset in question with the e-mail.