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TI Precision Designs: Verified Design

5% Error, 0.5-4.5 V Input, +/-2 A Output, Bridge-Tied-Load (BTL) Voltage-to-Current (V-I) Converter

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA569	Product Folder
REF5025	Product Folder

Circuit Description

This bridge-tied load (BTL) voltage-to-current (V-I) converter circuit creates a bidirectional current source used to drive a floating load from a single-ended source. The circuit makes use of an internal output current monitor circuit (IMON) in a specialty power amplifier. The V-I transfer function is accomplished by using the IMON current as the feedback for the first amplifier. The second amplifier inverts the output of the first amp to achieve the BTL operation which doubles the voltage swing and slew rate across the load, and allows for a bidirectional output from a single-ended power supply.

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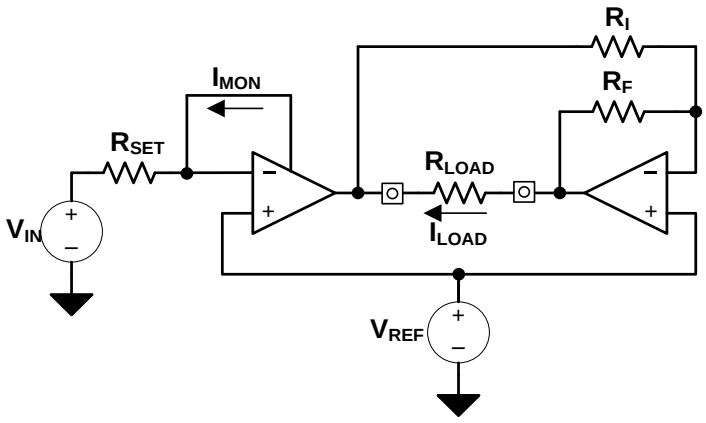

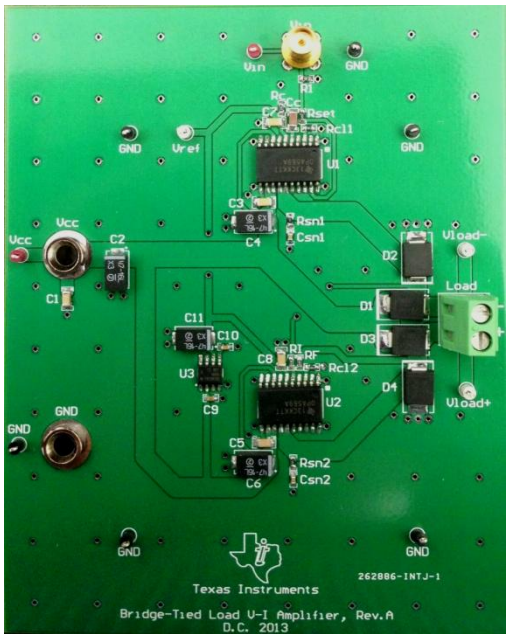

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V dc
- Input: 0.5 - 4.5 V dc, zero-scale output at 2.5 V dc
- Output: +/-2 A dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulated, and Measured Performance

	Goals	Simulated	Measured
Offset (%FSR)	1	0.033	0.0125
Gain Error (%FSR)	5	1.825	4.55
Load Compliance (V)	4.5	4.698	4.724

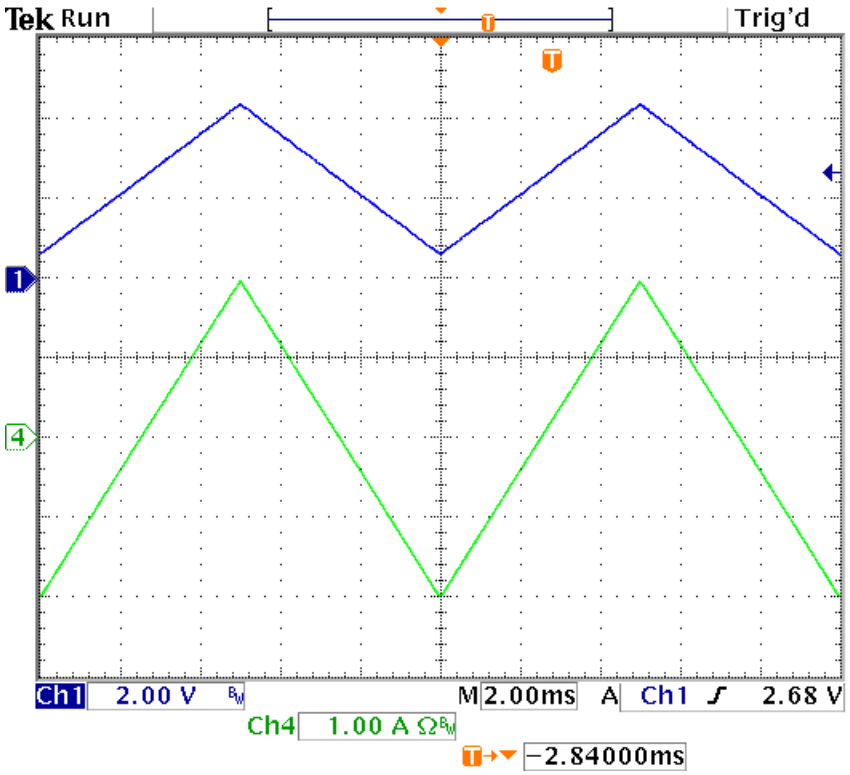

Figure 1: Measured Transfer Function

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, the reference voltage, V_{REF}, the current sensing resistor, R_{SET}, and the properties of the I_{MON} current monitor in the op-amp.

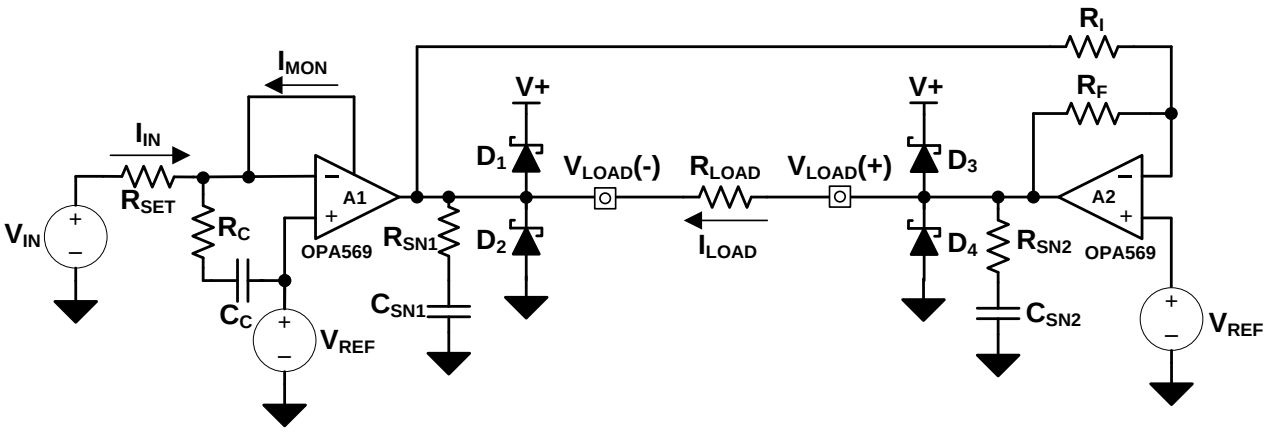

Figure 2: Complete Circuit Schematic

The transfer function for this design is defined in Equation 1.

$$I_{LOAD} = \frac{(V_{IN} - V_{REF})}{R_{SET}} \times 475 \quad (1)$$

2.1 Circuit Design

The first amplifier controls the current flowing through the load by using the I_{MON} current as feedback to the inverting terminal as opposed to standard resistive feedback from the output. The transfer function is based on cancelling the input current, I_{IN}, with the I_{MON} current to keep voltage on the inverting terminal equivalent to V_{REF}. Since the I_{MON} current is directly related to the output current of the amplifier, I_{LOAD}, the output current can be controlled by changing the input current to the circuit.

V_{REF} was selected to be +2.5 V to bias the circuit to mid-supply in order to get equal output swings in both the positive and negative directions. By applying V_{REF} to the non-inverting terminal of the OPA569, negative feedback will set the voltage at its inverting terminal to be +2.5 V as well. Applying an input voltage to the circuit other than +2.5 V will therefore cause an input current to flow into the summing node at the inverting input based on the value of R_{SET}.

$$I_{IN} = \frac{(V_{IN} - 2.5\,V)}{R_{SET}} \quad (2)$$

The I_{MON} circuit creates a 1:475 bidirectional copy of the output current delivered to the load. Having this circuit internal to the OPA569 eliminates the need for a series current sensing resistor in the design and increases the overall efficiency of the circuit. The relationship between the I_{MON} circuit and load current is shown in the equation below.

$$I_{MON} = -\frac{I_{LOAD}}{475} \quad (3)$$

Kirchhoff's current law states that the sum of currents that flow into a common node must be equivalent to the sum of the currents flowing out of the node. Therefore, I_{IN} and I_{MON} flow in different directions and must be equal and opposite.

$$I_{IN} = -I_{MON} \tag{4}$$

Replacing terms in the equation above yields the equation below.

$$\frac{(V_{IN} - 2.5\,V)}{R_{SET}} = \frac{I_{LOAD}}{475} \tag{5}$$

Solving for I_{LOAD} yields the transfer function of the design.

$$I_{LOAD} = \frac{(V_{IN} - V_{REF})}{R_{SET}} \times 475 \tag{6}$$

R_{SET} can be solved for using the ideal full-scale current and the full-scale input voltage. Solving for I_{LOAD} yields the transfer function of the design.

$$R_{SET} = \frac{(4.5\,V - 2.5\,V)}{2\,A} \times 475 \tag{7}$$

$$R_{SET} = 475\,\Omega \tag{8}$$

The OPA569 device also features a current limit function which limits the max output current, I_{LIMIT}, from exceeding the maximum desired value. The I_{LIMIT} value for the amplifiers is controlled by appropriately setting the current limit resistors, R_{CL1} and R_{CL2}. The current limit should not turn on during normal operation and should be set safely outside of the desired output current span. To limit the output current of the amplifiers to 2.1 A, follow the equation provided in the OPA569 datasheet.

$$I_{LIMIT} = 2.1A = 9800 \times \left(\frac{1.18\,V}{R_{CL}}\right) \tag{9}$$

$$R_{CL1} = R_{CL2} = 5.49\,k\Omega \tag{10}$$

3 Component Selection

3.1 Operational Amplifier

To enable the V-I transfer function described in this design, the power amplifier needs to include an internal output current monitor, eliminating most power amplifier options. The OPA569 power amplifier is a high-current device that is capable of driving a wide variety of loads with an output current over 2 A. It is optimized for low-voltage, single or dual-supply operation with rail-to-rail swing on both the input and output. The OPA569 is unity-gain stable, has low dc errors, and does not have any of the phase inversion problems commonly found in other power amplifiers. The OPA569 was chosen for this design because it includes the I_{MON} circuit with +/-3% accuracy which meets or exceeds the performance requirements for this design.

3.2 Voltage Reference Selection Can be avoid??

A +2.5 V reference voltage was applied to this circuit to accommodate for a bi-directional output with a single-supply. Along with the need for reference voltage accuracy, key considerations were made to ensure that the solution would also provide a low level of noise and temperature drift. The REF5025 was chosen for this design to exceed these key specifications.

3.3 Output Protection Diode Selection

Reactive and other electromotive force (EMF) generating loads can cause the output voltage to exceed the supply voltage, VCC, and potentially damage the circuit. This scenario can be avoided by clamping the output terminal voltage to the power supplies through the use of Schottky rectifier diodes. To protect the OPA569 from damage, a 3 A or greater continuous rating is needed. The 30BQ015 Schottky rectifier diode was chosen for this design to meet this specification and protect the circuit from damage.

3.4 Output Snubber Network (R_{SN}, C_{SN})

Designs that directly drive reactive loads will also benefit from an R-C snubber network placed directly on the output of the amplifiers. The values used in the design are standard values and may need to be modified based on the load.

3.5 Loop Compensation Components (R_C, C_C)

Compensation components R_C and C_C provide a high frequency path for currents to flow to the reference voltage at the non-inverting input. These components help dampen the response and should be included in the design. The values were obtained experimentally during simulation and then modified based on lab testing.

3.6 Passive Component Selection

The critical passive component for this design is the resistor that is part of the transfer function, R_{SET}. To meet the gain error design goal of 5% FSR, the tolerance of this resistor was chosen to be 1%.

Other passive components in this design may be selected for 1% or greater as they will not directly affect the transfer function of this design.

4 Simulation

The TINA-TI™ schematic shown in Figure 3 includes the circuit values obtained in the design process.

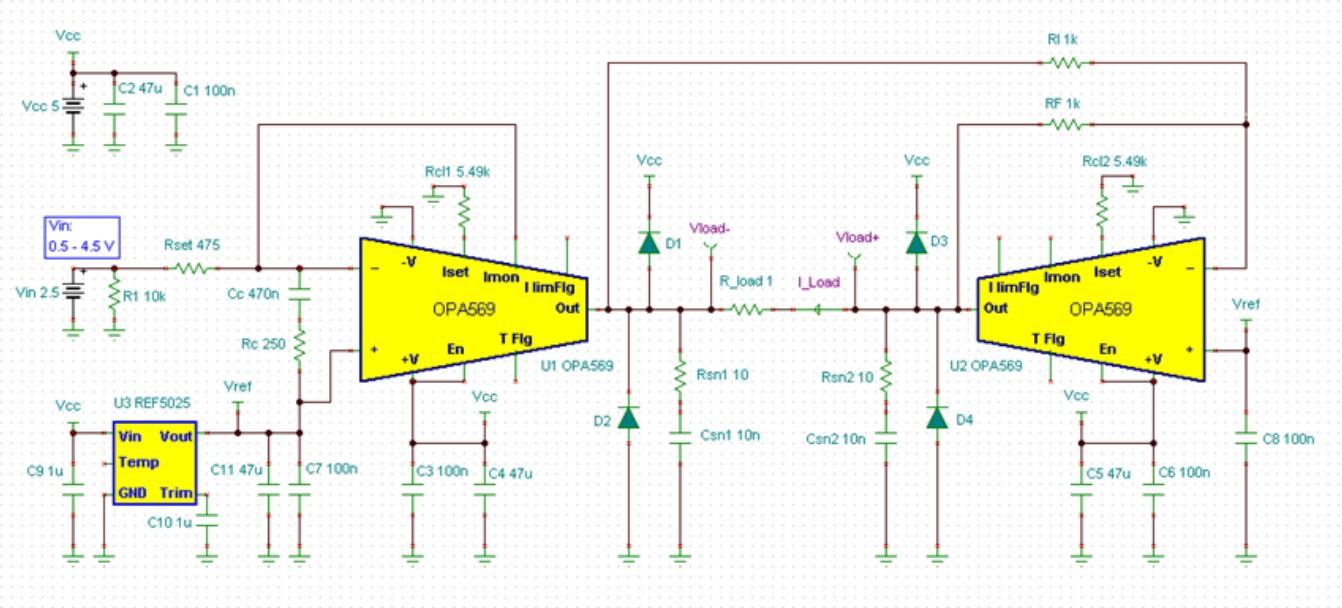

Figure 3: TINA-TI™ Simulation Schematic

4.1 DC Transfer Function

The dc transfer function simulation results of the circuit in Figure 3 are shown in Table 2 and Figure 4. The results can be used to reference the voltage or current at a given node as a function of the input voltage.

Table 2: Simulated DC Transfer Function Performance

Measurement	Simulated Results
Negative Full-Scale Current (A)	-1.981
Positive Full-Scale Current (A)	1.949
Zero-Scale Current m(A)	-1.333

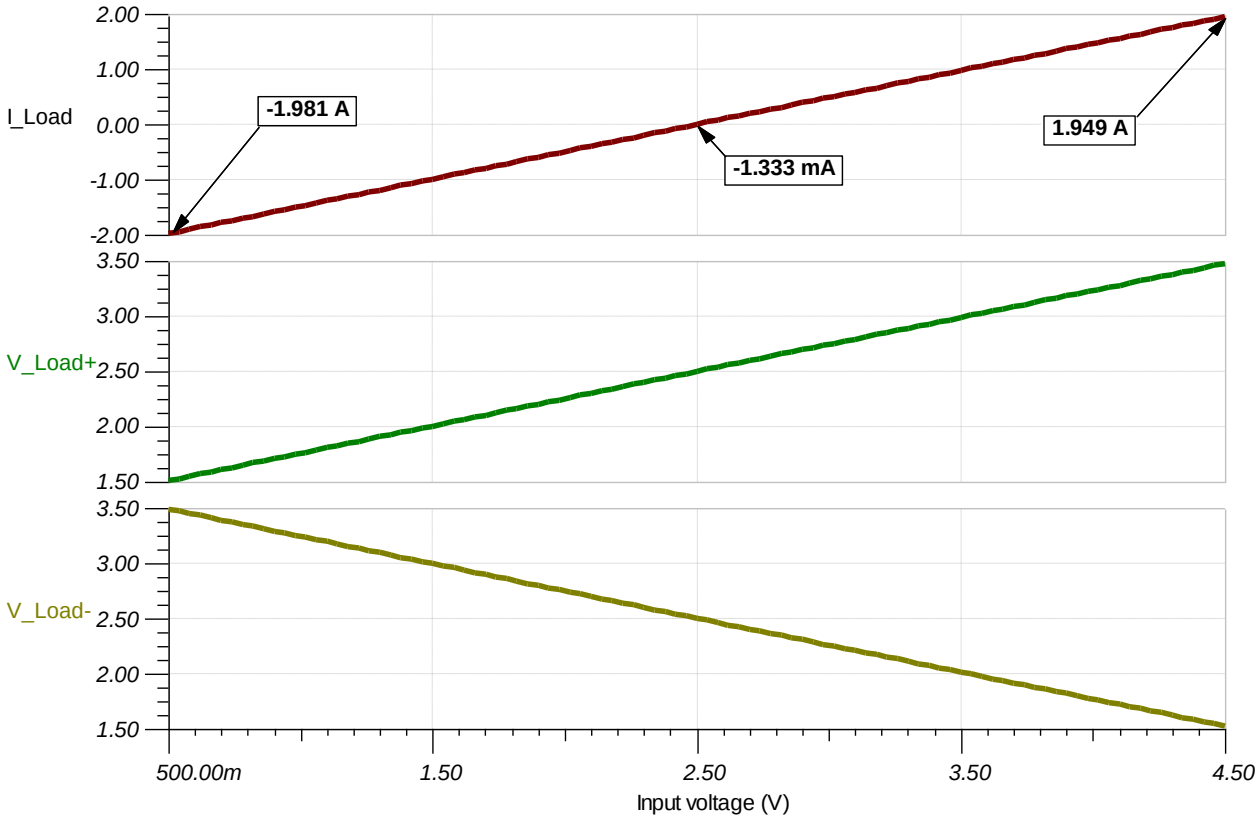

Figure 4: TINA-TI™ – DC Transfer Characteristic

The simulation results in Figure 4 were obtained using ideal passive components which reduces errors in the circuit to only the performance of the op-amps. More realistic simulation results can be obtained by running a Monte-Carlo simulation which will take into account the tolerance of the passive components.

Figure 5 displays the results of a ten iteration Monte-Carlo dc sweep performed after entering the actual passive component tolerances. The averaged statistical results of the Monte-Carlo simulation are summarized in Table 3.

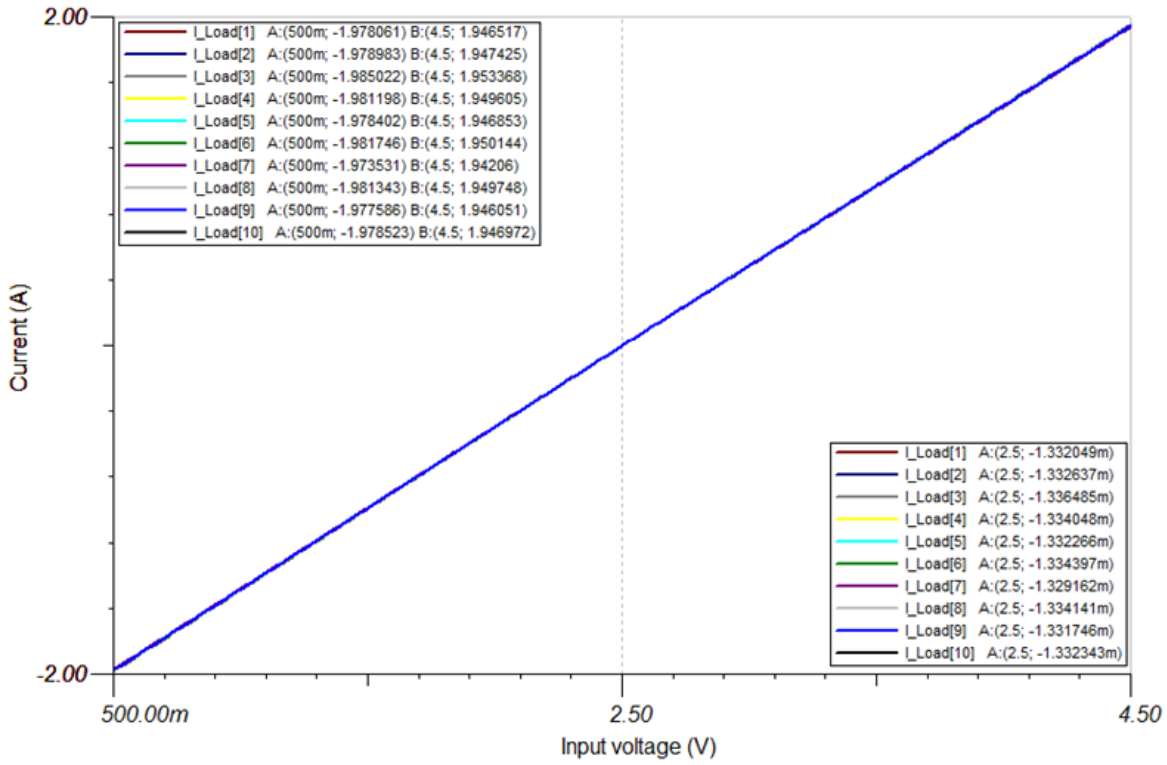

Figure 5: TINA-TI™ - Monte-Carlo Simulation of I_{LOAD}

Table 3: Average Monte-Carlo DC Transfer Results

Measurement	Results
Zero-Scale Current (mA)	-1.333
Positive Full-Scale Current (A)	1.948
Negative Full-Scale Current (A)	-1.979
Full-Scale Current (A)	3.927
Full-Scale Current Standard Deviation (σ) (mA)	6.11

The total system gain error from the ideal component sweep was determined using the following equation:

$$\text{Gain Error}(\%) = \frac{\left|\left(I_{LOAD}(\text{Ideal\_max}) - I_{LOAD}(\text{Ideal\_min})\right) - \left(I_{LOAD}(\text{max}) - I_{LOAD}(\text{min})\right)\right|}{\left(I_{LOAD}(\text{Ideal\_max}) - I_{LOAD}(\text{Ideal\_min})\right)} \times 100 \quad (11)$$

The positive and negative gain errors were calculated using similar equations using the ideal positive and negative spans (2A).

The standard deviation of the Monte Carlo sweep was very low revealing that the tolerance of the R_{SET} resistor was not too critical and most of the final system error will be due to the +/-3% typical accuracy of the I_{MON} circuit.

4.2 Step Response

The step response of the design is shown in Figure 6. The results show that the output settles to the proper value with little overshoot and ringing, indicating a stable design. The stable response was obtained by manipulating the compensation components, R_C and C_C.

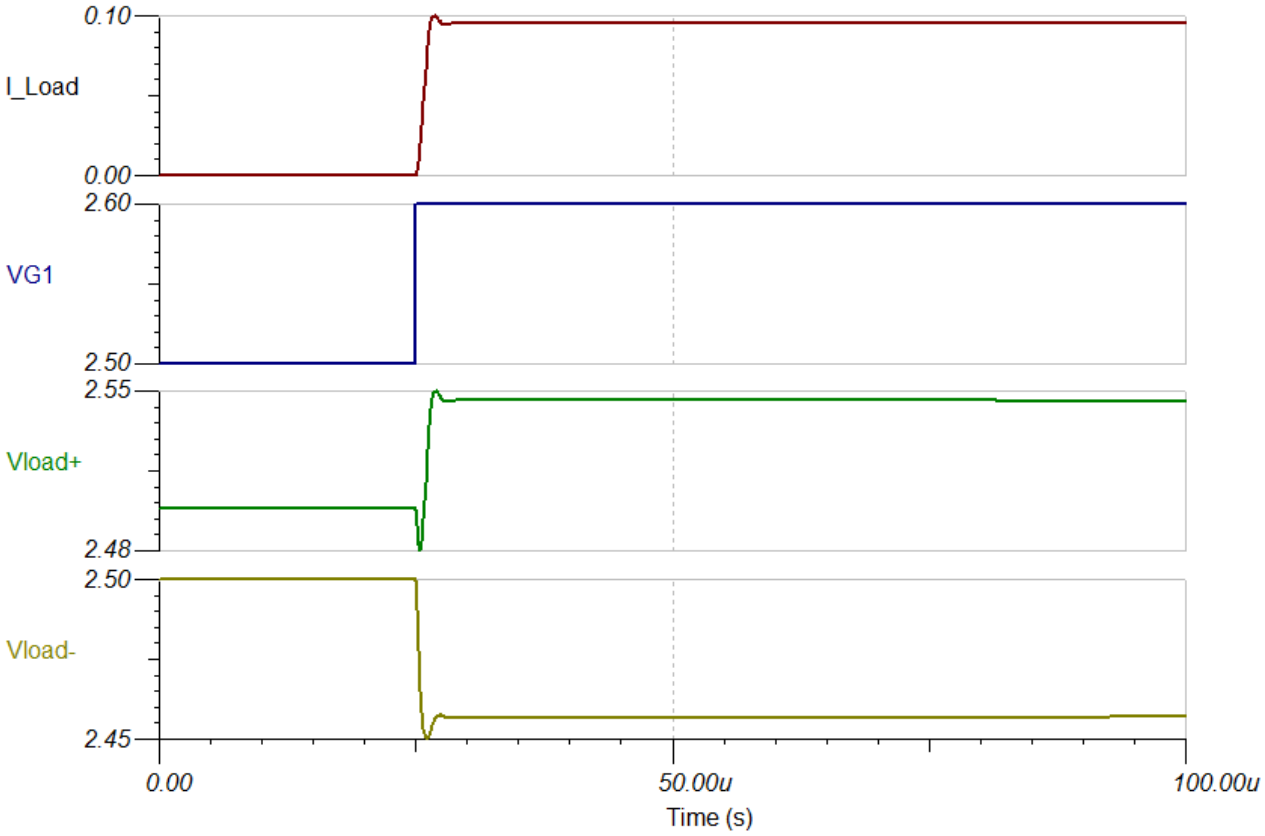

Figure 6: TINA-TI™ – Small-Signal Step Response

4.3 Compliance Voltage

To test the maximum compliance voltage and load resistance, the output was set to positive full-scale maximum current, and the load resistor, R_{LOAD}, was swept from 0 Ω - 5 Ω. The results are shown in Figure 7. The output compliance voltage was found to be 4.698 V and the maximum output resistance was 2.36 Ω.

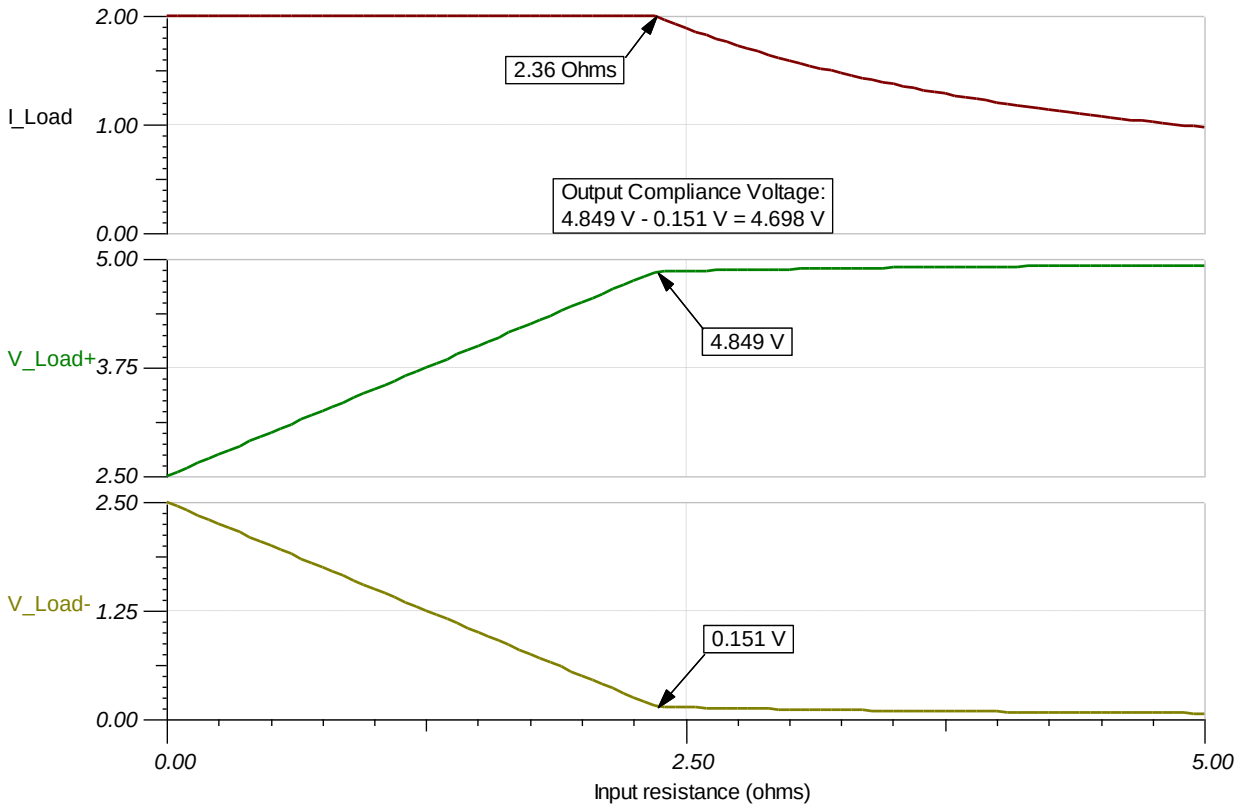

Figure 7: TINA-TI™ Maximum Load Resistance and Compliance Voltage

4.4 Simulated Result Summary

The simulation results are compared against the design goals in Table 4.

Table 4: Simulated Result Summary

	Goals	Simulated	Simulated Monte-Carlo
Offset (%FSR)	0.1	0.033	0.033
Positive Gain Error (%FSR)	N/A	2.55	2.6
Negative Gain Error (%FSR)	N/A	0.95	1.05
Total Gain Error (%FSR)	5	1.75	1.825
Load Compliance (V)	4.5	4.698	4.698

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1 and A.2.

5.1 PCB Layout

Trace thickness is a primary concern in this design due high current. Any traces in the design that carry a high current should have thickness that ensures a proper degree of current-carrying capacity. In this design, at least 100 mil traces were used for the high current paths.

The PCB layout for this design is shown in Figure 8.

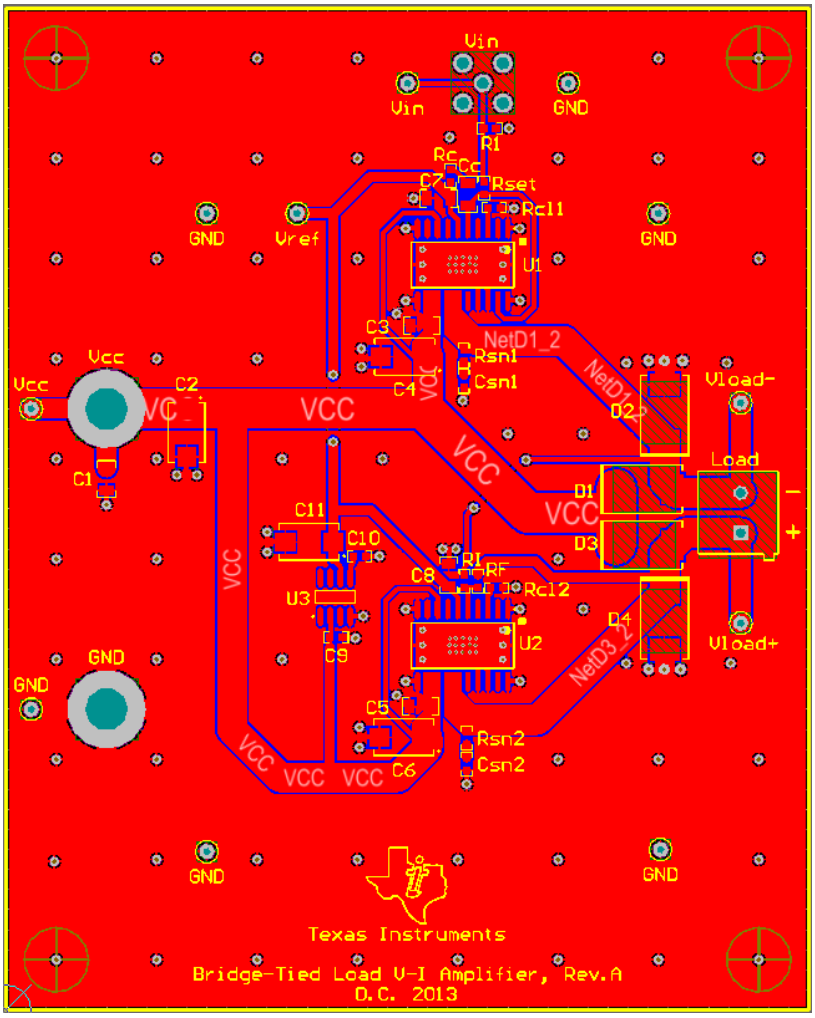

Figure 8: Altium PCB Layout

In addition to these rules, please reference and abide by general PCB layout guidelines.

6 Verification and Measured Performance

6.1 Transfer Function

Data was collected by sweeping V_{IN} from 0.5 V – 4.5 V dc while measuring the voltage across the load, V_{LOAD}, and load current, I_{LOAD}. Figure 9 displays a plot of I_{LOAD} Vs V_{IN}.

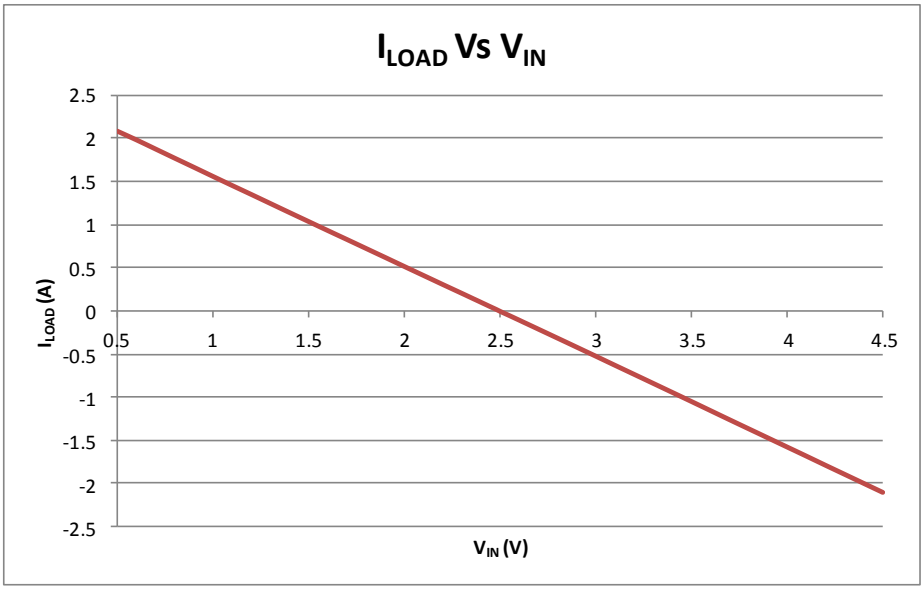

Figure 9: Measured I_{LOAD} vs. V_{IN}

Table 5: Measured Performance

	Results
Negative Full-Scale Current (A)	-2.096
Positive Full-Scale Current (A)	2.086
Zero-Scale Current (mA)	-0.5

To observe the errors in the circuit more easily, the error current of the load, I_{LOAD_ERROR}, was calculated by taking the difference between, I_{LOAD}(Ideal), and I_{LOAD}. The results are shown in Figure 10.

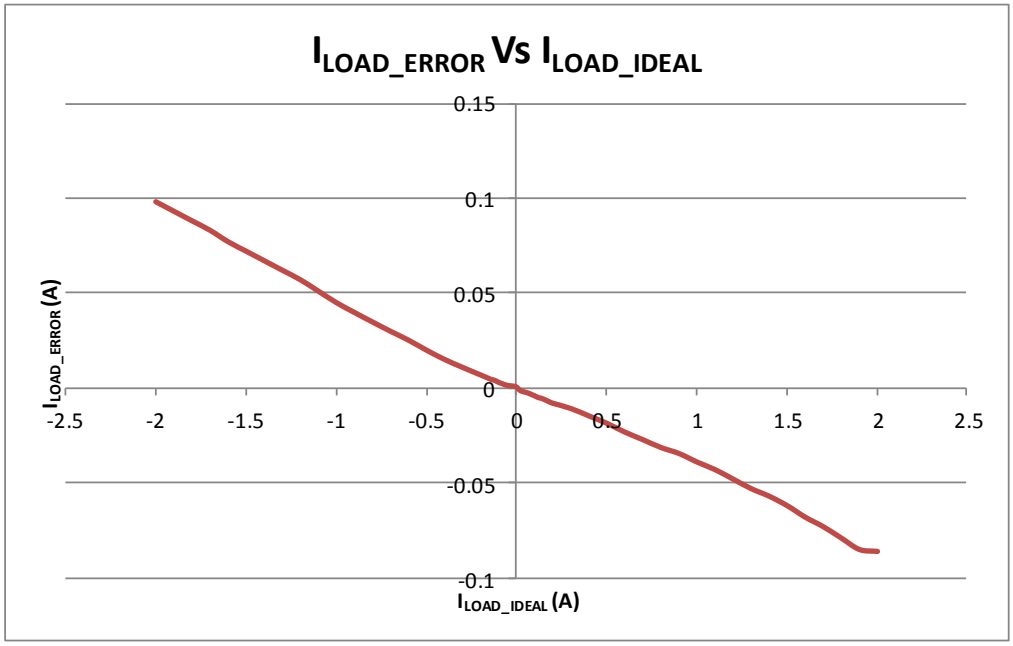

Figure 10: Measured I_{LOAD_ERROR} vs. I_{LOAD}(Ideal)

The positive, negative, and system gain errors were calculated using the equations in Section 0 and are displayed in Table 6.

Table 6: Measured Performance %FSR)

	Measured
Offset Error (%FSR)	0.0125
Positive Gain Error (%FSR)	4.8
Negative Gain Error (%FSR)	4.3
Total Gain Error (%FSR)	4.55

The measured output voltages of each amplifier versus V_{IN} while driving a 1 Ω load are shown in Figure 11.

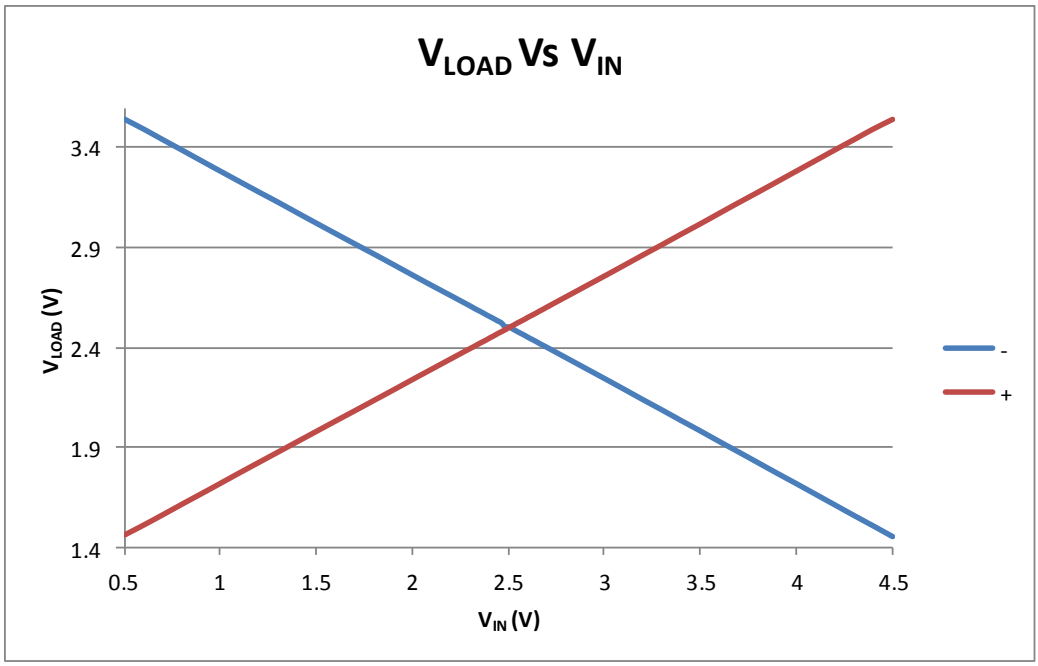

Figure 11: V_{LOAD} vs. V_{IN}

6.2 *Transient Response*

A full-scale 4 Vpp, 100 Hz triangle wave centered around 1 V dc is applied to V_{IN} to observe how the design reacts when a full-scale ramp is applied to the input. Figure 12 shows an oscilloscope screen capture of the input voltage, Channel 1, and the output current through the load resistor, Channel 2.

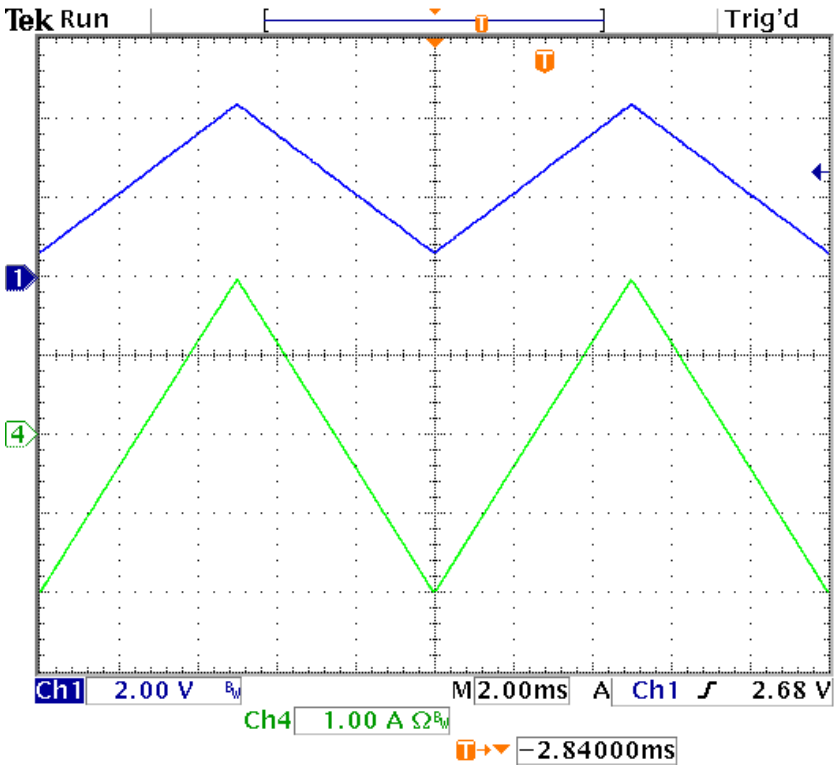

Figure 12: Full-Scale Triangle Wave Input

A full-scale 4 Vpp, 100 Hz full-scale step response centered at 1 V dc is applied to VIN to observe the full-scale settling response of the design. Figure 13 shows an oscilloscope screen capture of the input voltage, Channel 1, and the output current through the load resistor, Channel 2.

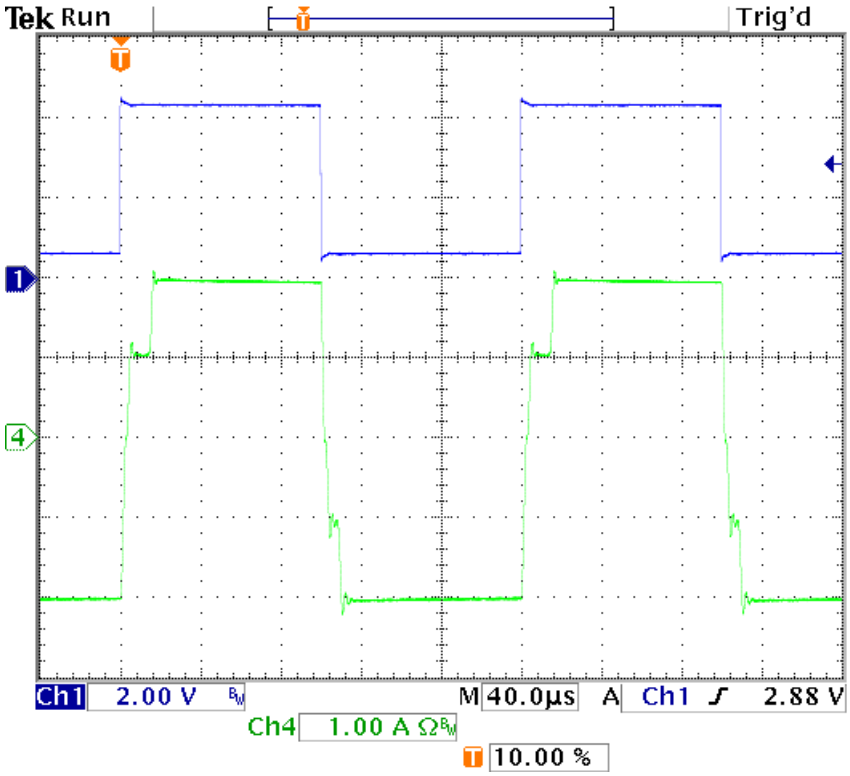

Figure 13: Full-Scale Settling Response

A 260 mVpp, 1 kHz small-signal input step centered around 1 V dc was applied to V_{IN} to test the small-signal stability of the design. Figure 14, Figure 15, and Figure 16 show the resulting oscilloscope screen captures of the input voltage, Channel 1, the output voltage at the negative terminal of the load , V_{LOAD-}, Channel 2, the output voltage at the positive terminal of the load, V_{LOAD+}, Channel 3, and the output current through the load resistor, Channel 4.

Figure 14 shows the resulting system response while sinking current when V_{IN} is set to 1.5 V. Figure 15 shows the resulting system response at mid-range when VIN is set to 2.5 V. Figure 16 shows the resulting system response while sourcing current when V_{IN} is set to 3.5 V. In all three circumstances, the design quickly settles to the final value with a properly damped response without overshoot or ringing. A slight glitch can be observed as the I_{LOAD} current passes through the transition region between when the I_{MON} circuit is sinking and sourcing current.

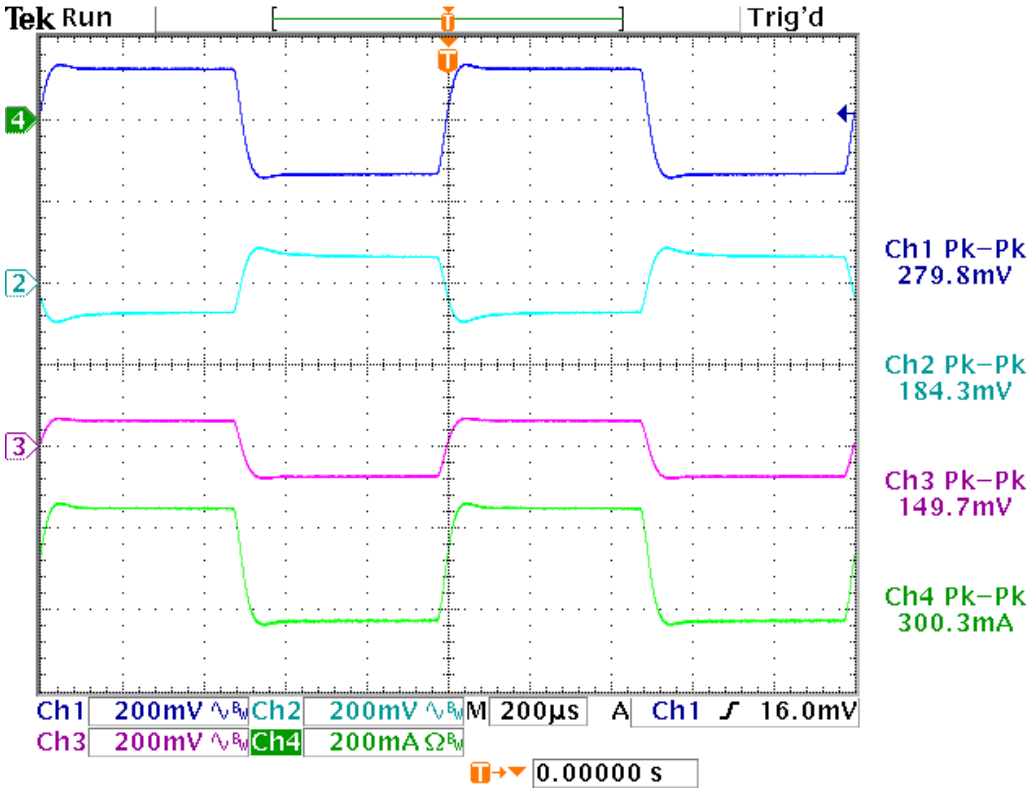

Figure 14: Small-Signal Stability as a Current Sink

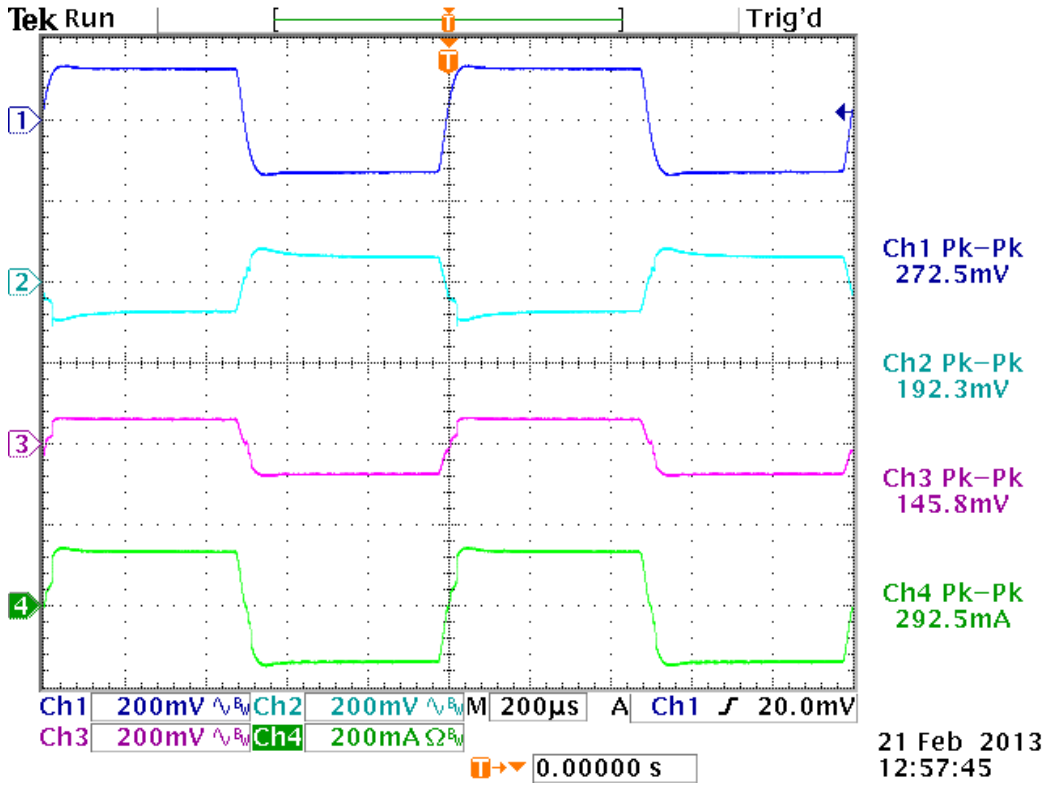

Figure 15: Small-Signal Stability at Mid-Range

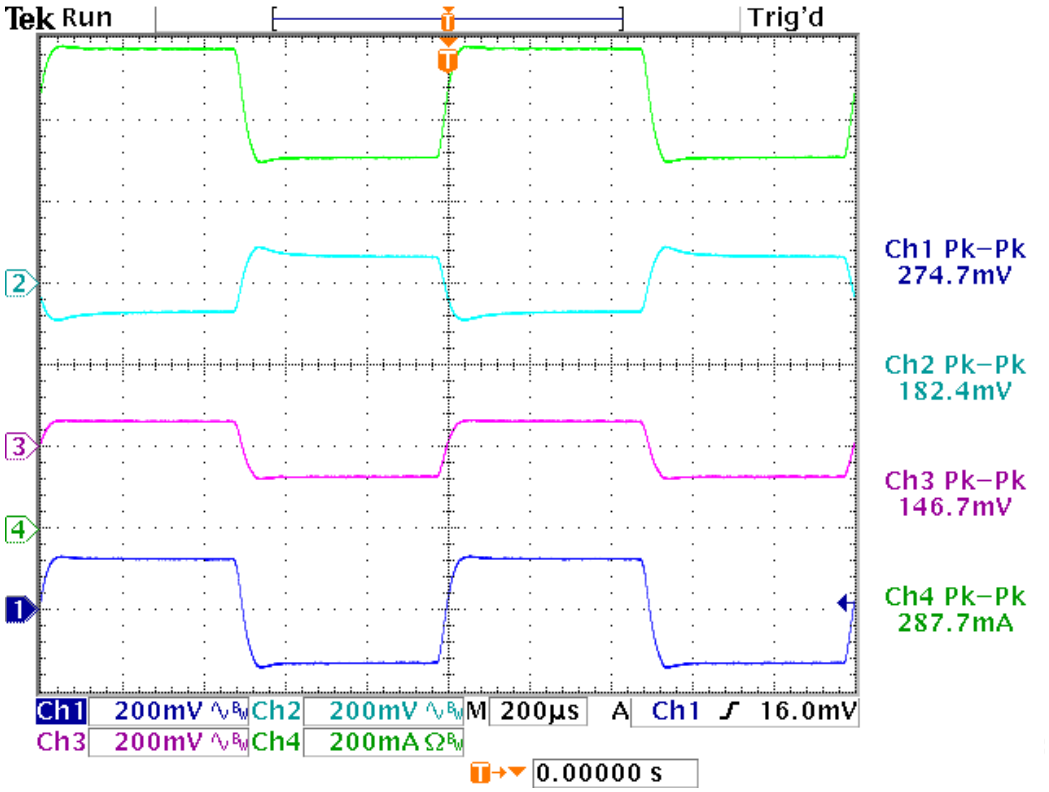

Figure 16: Small Signal Stability as a Current Source

6.3 Compliance Voltage

The compliance voltage of the circuit, V_{COMP}, is based on the supply voltage, V_{CC}, and the output swing-to-rail characteristics of the amplifier specified in the amplifier product datasheet. Figure 17 displays the output swing to both the positive and negative rails for the OPA569.

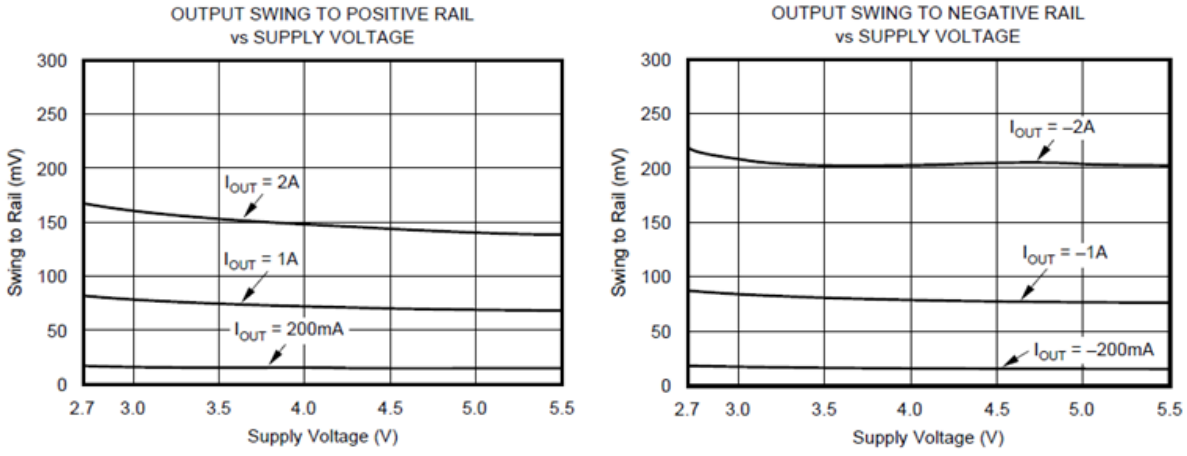

Figure 17: OPA569 Output Swing vs. Supply Voltage and Output Current

As shown in Figure 17, with ± 2 A output current, the positive swing is approximately 150 mV from the positive rail and the negative swing is 200 mV from the negative rail. A quick estimate of the load compliance voltage can be made by subtracting the 350 mV of output swing limitation from the 5 V power supply, leaving 4.65 V of output load compliance. The measured value was found to be 4.724 V.

Based on the measured maximum load compliance voltage the maximum load resistance, $R_{LOAD}(max)$, can be calculated as shown in the following equations.

$$R_{LOAD}(max) = \frac{V_{COMP}}{I_{LOAD}} \quad (12)$$

$$R_{LOAD}(max) = 2.362\,\Omega \quad (13)$$

6.4 Measured Result Summary

The measured results are compared against the design goals in Table 7.

Table 7: Comparison of Design Goals and Measured Performance

	Goals	Measured
Offset (%FSR)	1	0.0125
Positive Gain Error (+%FSR)	N/A	4.8
Negative Gain Error (-%FSR)	N/A	4.3
Total Gain Error (%FSR)	5	4.55
Load Compliance (V)	4.5	4.724

7 Modifications

The components selected for this design were based on the design goals outlined at the beginning of the design process. The circuit requires a power amplifier that has an internal current-monitoring circuit that can be used as feedback to create the V-I transfer function. The use of alternative amplifiers is not feasible in this exact configuration because of the lack of the I_{MON} circuit. However, almost all power amplifiers can be used in a BTL configuration with voltage feedback to the first amplifier. This would produce a standard voltage output system instead of a current output, but would still benefit from all of the performance benefits of a BTL design.

The R_{SET} and the R_{CL} resistors can be adjusted to lower the output current and output current limits depending on the design requirements. However, increasing the output current swing past the ± 2 A shown in this design is not possible without the risk of damage to the circuit.

To reduce cost in the reference circuit at the expense of accuracy, a low-cost shunt regulator can be used in place of the REF5025 to provide the +2.5 V reference.

8 Potential Application: TEC Driver

Additional data was collected by using a CP30338 Thermo-Electric Cooler, TEC, as the load of the circuit to observe the operating temperature characteristics of the TEC when used in conjunction with this circuit. A TEC creates a heat differential between its two plates based on the Peltier effect, which occurs when a current flows through the TEC. A stick-on resistive-temperature-detector (RTD) temperature probe was used to measure both sides of the TEC.

Data was collected by sweeping V_{IN} from 1.8 V – 2.5 V dc while measuring the temperature of the hot and cold sides of the TEC. Figure 18 displays a plot of the hot-side temperature of the TEC versus V_{IN}, while Figure 19 displays a plot of cold-side temperature versus V_{IN}.

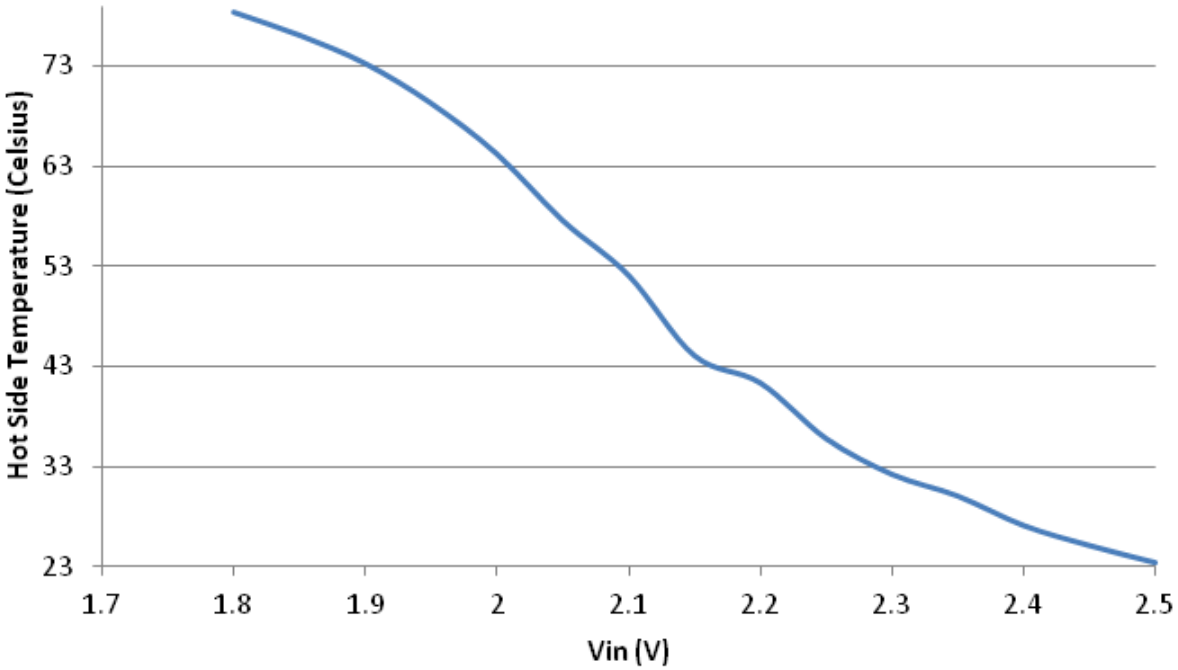

Figure 18: Hot-Side Temperature vs. V_{IN}

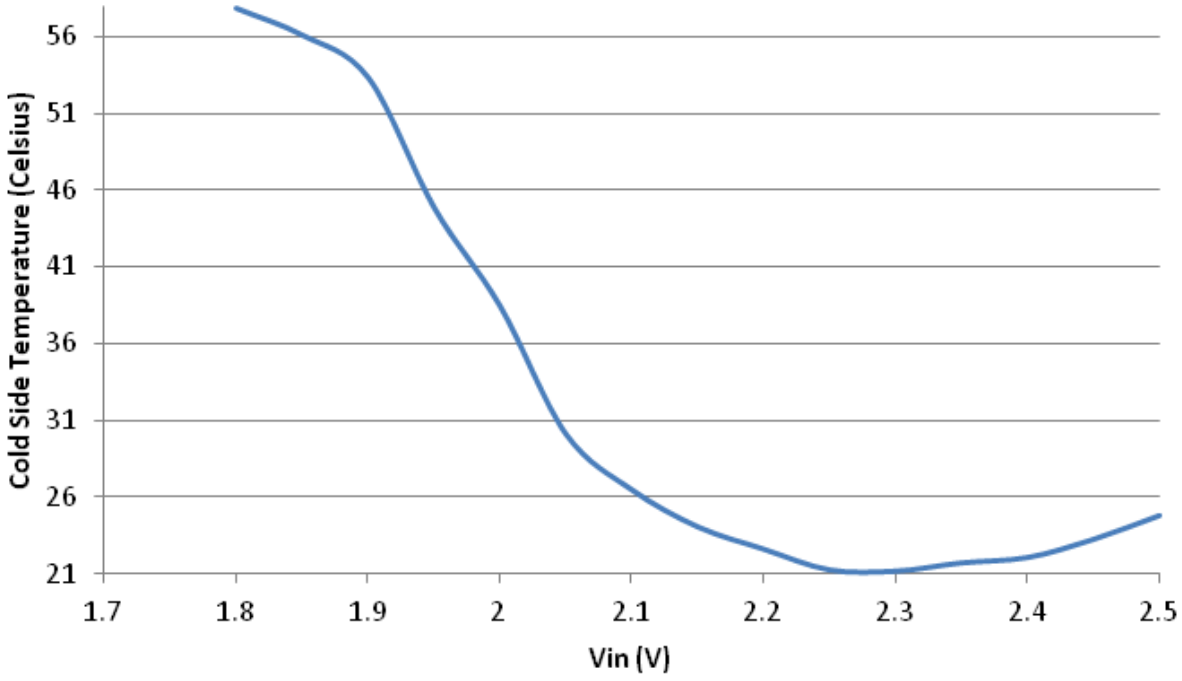

Figure 19: Cold-Side Temperature vs. V_{IN}

9 About the Authors

David F. Chan graduated from the Rochester Institute of Technology in May of 2012, where he earned a Bachelor of Science in Electrical Engineering Technology and a minor in both Management and Psychology. He joined Texas Instruments through the Applications Rotation Program in August 2012, where he worked with the Precision Analog - Linear and the Analog Centralized Applications teams.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

10 Acknowledgements & References

A special thanks to Neil Albaugh who originally created the base for this circuit as part of the TINA-TI™ example circuit library.

Appendix A.

A.1 Electrical Schematic

The electrical schematic is shown in Figure 20.

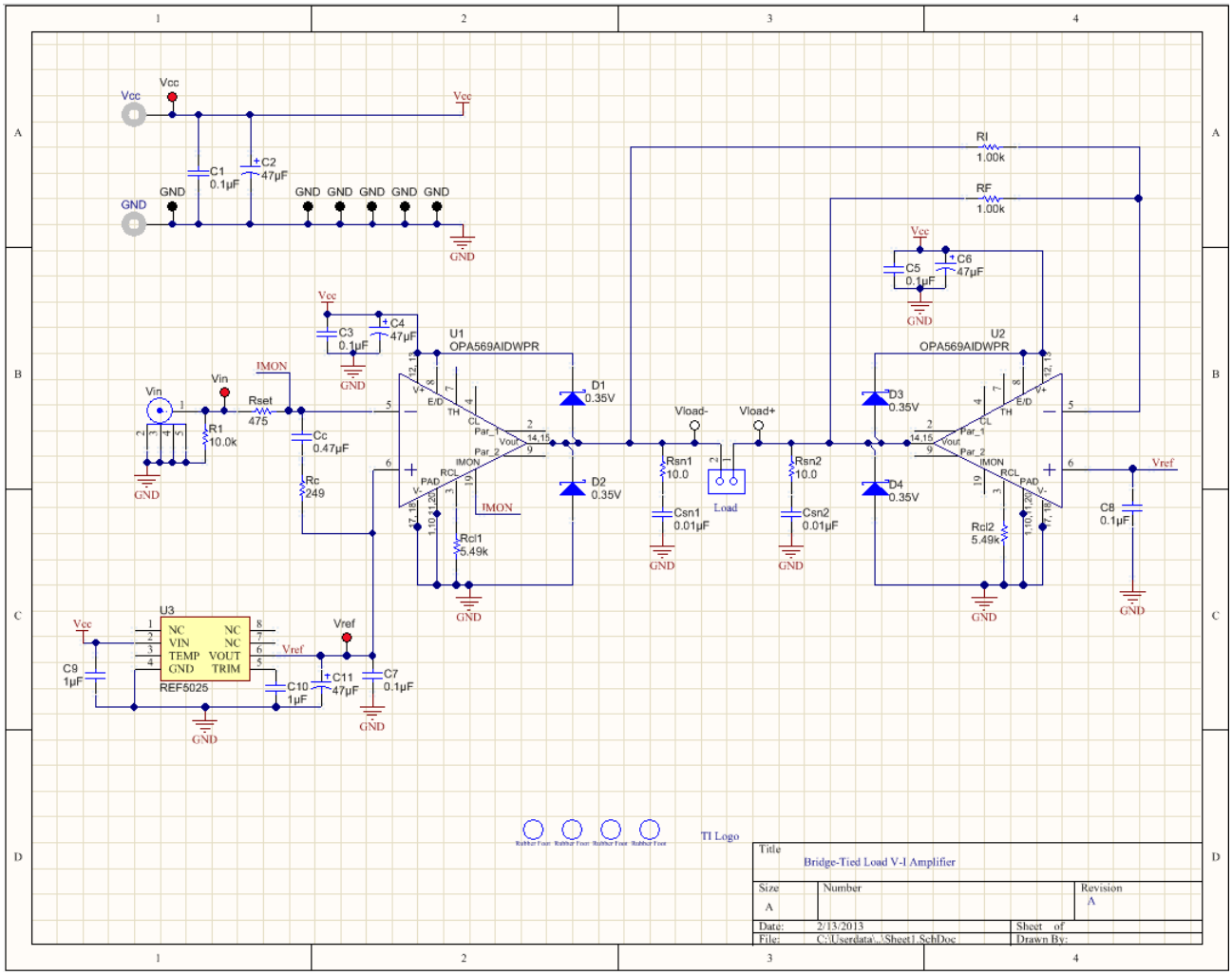

Figure 20: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 21.

Quantity	Value	Designator	Description	Manufacturer	Par Number	Supplier Part Number 1
5	0.1uF	C1, C3, C5, C7, C8	CAP, CERM, 0.1uF, 50V, +/-5%, X7R, 1206	AVX	12065C104JAT2A	478-3797-1-ND
4	47uF	C2, C4, C6, C11	CAP, TANT, 47uF, 16V, +/-20%, 0.7 ohm, 7343-31 SMD	Vishay-Sprague	293D476X0016D2TE3	718-1086-1-ND
2	1uF	C9, C10	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E105KA12D	490-5307-1-ND
1	0.47uF	Cc	CAP, CERM, 0.47uF, 100V, +/-10%, X7R, 1206	TDK	C3216X7R2A474K	445-2284-1-ND
2	0.01uF	Csn1, Csn2	CAP, CERM, 0.01uF, 50V, +/-5%, X7R, 0603	Kemet	C0603C103J5RACTU	399-1092-1-ND
4	0.35V	D1, D2, D3, D4	Diode, Schottky, 15V, 3A, SMC	International Rectifier	30BQ015TRPBF	VS-30BQ015PBFCT-ND
4		F1, F2, F3, F4	BUMPON CYLINDRICAL .312X.200 BLK	3M	SJ61A1	SJ5746-0-ND
2		GND, Vcc	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
1		Load	Conn Term Block, 2POS, 5.08mm PCB	Phoenix Contact	1715721	277-1263-ND
1	10.0k	R1	RES, 10.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-103-B-T5	RG16P10.0KBCT-ND
1	249	Rc	RES, 249 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07249RL	311-249HRCT-ND
2	5.49k	Rcl1, Rcl2	RES, 5.49k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-075K49L	311-5.49KHRCT-ND
2	1.00k	RF, RI	RES, 1.00k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-071KL	311-1.00KHRCT-ND
1	475	Rset	RES, 475 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07475RL	311-475HRCT-ND
2	10	Rsn1, Rsn2	RES, 10.0 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310R0FKEA	541-10.0HCT-ND
3	Red	TP1, TP9, TP13	Test Point, TH, Miniature, Red	Keystone	5000	5000K-ND
6	Black	TP2, TP3, TP4, TP5, TP6, TP7	Test Point, TH, Miniature, Black	Keystone	5001	5001K-ND
2	White	TP10, TP11	Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
2		U1, U2	IC OPAMP GP R-R 1.2MHZ 20SOIC	Texas Instruments	OPA569	296-26292-1-ND
1		U3	IC VREF SERIES PREC 2.5V 8-SOIC	Texas Instruments	REF5025	296-27641-1-ND
1		Vin	Connector, TH, SMA	Emerson Network Power	142-0701-201	J500-ND

Figure 21: Bill of Materials

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