Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics

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***Abstract*— We study the effects of the variation of ferroelectric material properties (thickness, polarization, and coercivity) on the performance of negative capacitance FETs (NCFETs). Based on this, we propose the concept of conservative design of NCFETs, where any unintentional yet reasonable and simultaneous variation (∼±3%) in ferroelectric parameters does not result in the emergence of hysteresis and causes only a reasonable variation in the ON-current (≤5%) and, within these constraints, the enhancement of ON-current due to the addition of the ferroelectric gate oxide, which is is maximized.**

***Index Terms*— Ferroelectric, negative capacitance FET (NCFET), sub-60 mV/decade.**

I. Introduction

NEGATIVE capacitance FETs (NCFETs) could operate at a sub-60-mV/decade subthreshold swing and a high ON-current [1], [2]. Recently, negative capacitance phenomena have been experimentally demonstrated in different systems: 1) isolated ferroelectric films [3]; 2) ferroelectric-dielectric bilayers [4], [5]; and 3) superlattices [6] and ferroelectric-gated transistors [7]–[9]. Simulation studies of NCFETs have also been reported in [2] and [10]–[13]. However, the effects of the variation of the ferroelectric material properties on the NCFET characteristics are yet to be understood. In this brief, we study the sensitivity of the ON-current in hysteresis-free NCFETs to the variation of ferroelectric material properties and propose a conservative design approach, where the ON-current is maximized under the constraint that ∼±3% variation of ferroelectric thickness, polarization, and coercive voltage does not result in more than 5% variation on the ON-current.

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II. Device Structure and Simulation Scheme

The structure of the NCFET is shown in Fig. 1(a). A bulk planar Si MOSFET with a gate length of 100 nm and an equivalent oxide thickness of 0.5 nm is the baseline MOSFET. The ferroelectric negative capacitance oxide sits on the top of the metal/high-k dielectric stack. The 2-D electrostatics, charge–voltage, and the transfer characteristics of the baseline MOSFET are simulated using TCAD Sentaurus. It should be noted that we intentionally considered a long-channel baseline transistor. This allows us to study of the effects of the variation of the ferroelectric parameter on the device without complications arising due to short-channel effects. The voltage across the ferroelectric is calculated using the equation: $V_{\rm FE} = (2\alpha Q + 4\beta Q^3) \times T_{\rm FE}$, where α and β are anisotropy constants, $T_{\rm FE}$ is the ferroelectric thickness, and Q is the surface charge density. α and β are calculated by fitting the ferroelectric Q–$V_{\rm FE}$ characteristics to yield the given values of remnant polarization $P_\circ$ and coercive field E_c. Hence, $V_{\rm FE}(Q = P_\circ) = 0$ and $dV_{\rm FE}/dQ(V_{\rm FE} = E_c T_{\rm FE}) = 0$. Based on this, $\alpha = -3\sqrt{3}/4 \times E_c/P_0$ and $\beta = 3\sqrt{3}/8 \times E_c/P_\circ^3$. The NCFET is simulated by self-consistently solving the charge–voltage characteristics of the ferroelectric obtained using these relations and of the baseline MOSFET obtained from TCAD [2].

III. Results and Discussion

Fig. 1(b) compares the I_D–V_G characteristics of the 8 baseline MOSFET and the NCFET with different $T_{\rm FE}$ and $P_\circ = 45\ \mu$C/cm^{-2} and $E_c = 500$ kV/cm at a drain voltage $V_D = 0.4$ V. These values of $P_\circ$ and E_c are in the same range as those of perovskite ferroelectrics such as $BaTiO_3$ [14], $Pb(Zr_{1-x}Ti_x)O_3$ [15], as well as Hf- and Zr-based binary oxide ferroelectrics [16]. We note in Fig. 1(b) that an increase in $T_{\rm FE}$ makes the I_D–V_G characteristics steeper and the ON-current $I_{\rm ON}$ (= I_D at $V_G = V_D$) higher. Above a critical $T_{\rm FE}$ (=104 nm), the I_D–V_G characteristics show hysteresis, which is similar to the observations in [2]. The improvement in $I_{\rm ON}$ and the emergence of hysteresis with an increasing $T_{\rm FE}$ could be explained by the capacitance matching condition in the NCFETs [2]. We note that, at small Q, higher order terms of Q in the expression of $V_{\rm FE}$ can be ignored and the ferroelectric capacitance $C_{\rm FE}$ could be approximated as

$$C_{\rm FE} = \frac{dQ}{dV_{\rm FE}} \approx \frac{1}{2\alpha T_{\rm FE}} = \frac{2}{3\sqrt{3}} \frac{P_\circ}{E_c T_{\rm FE}}. \quad (1)$$

In a given NCFET, the steepest subthreshold and the greatest improvement in $I_{\rm ON}$ without hysteresis ensue when

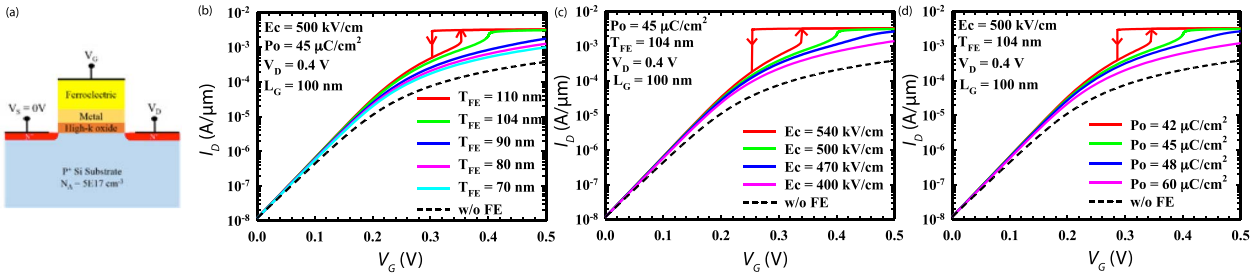

Fig. 1. (a) Schematic of the NCFET. The junction depth of source and drain is 10 nm, and the doping concentration of Si substrate and source/drain are 5×10^{17} cm^{-3} with boron and 10^{20} cm^{-3} with arsenic, respectively. The metallic layer between the high-k and FE oxide is used to create the uniform electric field in the Ferroelectric (FE) oxide, so that the monodomain approximation of the ferroelectric is valid [2]. Evolution of I_D–V_G characteristics of NCFET with the variation in (b) $T_{\rm FE}$, (c) E_c, and (d) $P_\circ$. $V_D = 0.4$ V. The minimum subthreshold swing S of the baseline MOSFET is 63 mV/decade, while the minimum S for the NCFET ranges between 57 and 59 mV/decade.

$|C_{\rm FE}| \approx C_{\rm MOS}$ and $|C_{\rm FE}| > C_{\rm MOS}$, where $C_{\rm MOS}$ is the MOSFET gate capacitance [2]. If $|C_{\rm FE}|$ becomes smaller than $C_{\rm MOS}$, hysteresis is expected [1], [2]. In the case shown in Fig. 1(a), with the increase in $T_{\rm FE}$, $|C_{\rm FE}|$ becomes smaller, and for $T_{\rm FE} \geq 104$ nm, $|C_{\rm FE}| > C_{\rm MOS}$. Fig. 1(c) shows the evolution of I_D–V_G characteristics of the NCFET as E_c is varied between 400 and 540 kV/cm while keeping $T_{\rm FE}$ and $P_\circ$ constant at 104 nm and 45 μC/cm^2, respectively. In (1), we note that $C_{\rm FE}$ has the same dependence on $T_{\rm FE}$ and E_c. Hence, above a critical $E_c = 500$ kV/cm with $T_{\rm FE}$ and $P_\circ$ fixed, the I_D–V_G characteristics becomes hysteric. Fig. 1(d) shows the evolution of the I_D–V_G characteristics of the NCFET as $P_\circ$ is varied between 42 and 60 μC/cm^2 keeping $T_{\rm FE}$ and E_c constant at 104 nm and 500 kV/cm, respectively. We note in Fig. 1(d) that the dependence on the NCFET I_D–V_G characteristics on $P_\circ$ has an opposite trend than that on $T_{\rm FE}$ and E_C. This is due to the fact that $C_{\rm FE}$ is proportional to $P_\circ$ [see (1)]. Hence, an increase in $P_\circ$ reduces the ON-current and the hysteresis.

For all practical purposes, a hysteresis-free operation on an NCFET with a maximized $I_{\rm ON}$ is desirable. The preceding analysis shows that the process-induced variations in ferroelectric parameters, $T_{\rm FE}$, $P_\circ$, and E_C, could result in hysteresis in an NCFET, although the NCFET may be designed to operate without hysteresis. In what follows next, we propose a conservative design approach, which follows the following three conditions.

1) The nominal NCFET design has no hysteresis.
2) An unintentional yet reasonable and simultaneous variation ($\sim\pm 3\%$) of all the ferroelectric parameters (thickness, polarization, and coercivity) does not result in the emergence of hysteresis and causes only a reasonable variation in the ON-current (<5%) at $V_D = 0.4$ V.
3) Within these constraints, the enhancement of ON-current due to the addition of the ferroelectric gate oxide is maximized.

$T_{\rm FE}$ is our key design parameter. $P_\circ$ and E_c are assumed to have nominal values of 45 μC/cm^2 and 500 kV/cm, respectively, and to change only due to unintentional process variations. In order to understand the design space, we plot the hysteresis window as a function of $T_{\rm FE}$ in Fig. 2 for nominal $P_\circ = 45$ μC/cm^2 and $E_c = 500$ kV/cm and, for the case, when $P_\circ$ and E_c are, respectively, 3% smaller and

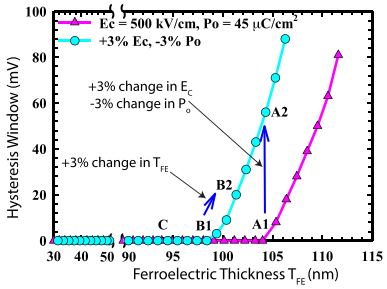

Fig. 2. Hysteresis window of the NCFET transfer characteristics as a function $T_{\rm FE}$ for the nominal values of $P_\circ$ and E_c and for the case when $P_\circ$ and E_c are, respectively, 3% smaller and 3% larger than the corresponding nominal values. (c) Maximum variation in ON-current due to $\pm 3\%$ variation in ferroelectric parameters and ON-current enhancement in the nominal NCFET as a function of $T_{\rm FE}$.

3% larger than the corresponding nominal values. The NCFET with $T_{\rm FE} = 104$ nm with nominal $P_\circ$ and E_c corresponds to point A1 in Fig. 2. A simultaneous 3% change in $P_\circ$ (decrease) and E_c (increase) would move the design point to A2, which has a hysteresis window of $\sim$56 mV. Next, we consider the device design corresponding to point B1 ($T_{\rm FE} = 98.4$ nm). The advantage of designing the device at point B1 is that a simultaneous 3% change of $P_\circ$ (decrease) and E_c (increase) would not result in hysteresis in this device. However, a 3% increase in the ferroelectric thickness would move the device characteristics to point B2, where there is a hysteresis of $\sim$20 mV. It is evident from this analysis that if $T_{\rm FE}$ is set to a value less than 95.5 nm [97% of the $T_{\rm FE}$ value in point B1 (refers to point C in Fig. 2)], a simultaneous 3% variation of all the ferroelectric parameters would not result in hysteresis.

We now analyze the variation of the ON-current at $V_D = 0.4$ V due to unintentional $\pm 3\%$ variation of the ferroelectric parameters in the hysteresis-free design space: $T_{\rm FE} < 95.5$ nm. Fig. 3(a) and (b) shows the transfer characteristics of the NCFET for $T_{\rm FE} = 95.5$ nm and $T_{\rm FE} = 40$ nm, respectively, with nominal $P_\circ$ and E_c. Also plotted in these figures are the transfer characteristics of the corresponding devices, where the unintentional increase in $I_{\rm ON}$ is maximum as a result of 3% increase in $T_{\rm FE}$ and E_c and 3% decrease in $P_\circ$ (denoted by $+3\%$ $T_{\rm FE}$, $+3\%$ E_c, -3% $P_\circ$), and the unintentional decrease in $I_{\rm ON}$

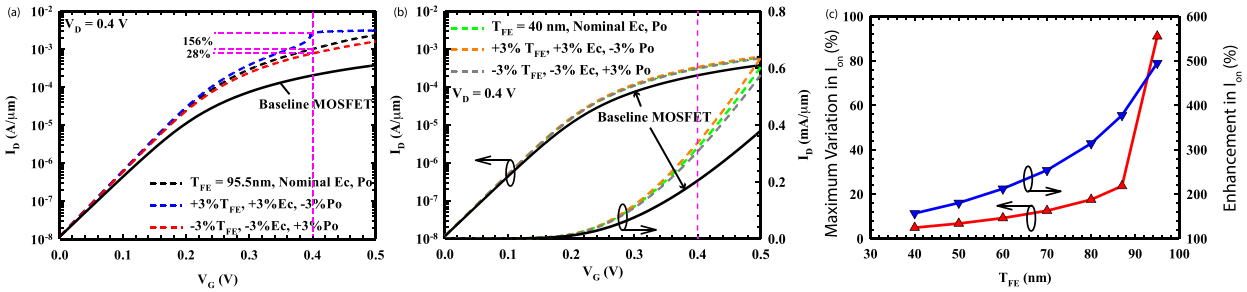

Fig. 3. I_D–V_G characteristics of the baseline MOSFET and NCFET with (a) $T_{FE} = 95.5$ nm and (b) $T_{FE} = 40$ nm. In each plot, there are three NCFET transfer characteristics, which correspond to nominal P_o and E_c, 3% increase in T_{FE} and E_c and 3% decrease in P_o (denoted by $+3\%$ T_{FE}, $+3\%$ E_c, -3% P_o) from the corresponding nominal values, and 3% decrease in T_{FE} and E_c and 3% increase in P_o from the corresponding nominal values (denoted by -3% T_{FE}, -3% E_c, $+3\%$ P_o). (c) Maximum variation in I_{ON} for 3% variation of ferroelectric parameters and enhancement of I_{ON} with respect to that of the nominal NCFET as a function of T_{FE}. %maximum variation $= (I_{ON}(+3\%T_{FE}, +3\%\ E_c, -3\%\ P_o) - I_{ON}(-3\%\ T_{FE}, -3\%\ E_c, +3\%\ P_o))/(2I_{ON}$ (nominal E_c, P_o)) $\times$ 100.

is maximum as a result of 3% decrease in T_{FE} and E_c and 3% increase in P_o (denoted by -3% T_{FE}, -3% E_c, $+3\%$ P_o). We note in Fig. 3(a) that, for $T_{FE} = 95.5$ nm, the unintentional $\pm 3\%$ variation could cause a change in I_{ON} as high as 156%. On the other hand, for $T_{FE} = 40$ nm, the $\pm 3\%$ variation in the ferroelectric parameter causes less than 5% change in I_{ON} with respect to that of the nominal NCFET. Even then, I_{ON} for $T_{FE} = 40$ nm is 50% higher than that of the baseline MOSFET. Fig. 3(c) shows the maximum variation in I_{ON} for 3% variation of the ferroelectric parameters and the enhancement of I_{ON} with respect to that of the baseline MOSFET as a function of T_{FE}. We note in Fig. 3(c) that the design space for the aforementioned conservative approach is $T_{FE} \leq 40$ nm.

IV. Conclusion

In summary, we studied the effect of variation in the ferroelectric material parameters (thickness, polarization, and coercive voltage) on the characteristics of NCFET. Based on this, we proposed a conservative design approach, where the sensitivity of the ON-current due to unintentional variation in the ferroelectric properties is significantly reduced in exchange for the enhancement in the ON-current. Such a variability aware design could still result in significant enhancements in the ON-current in the NCFETs.

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