UNIT-III

MEMORY SYSTEM

BASIC CONCEPTS:

Addressing mode determines the maximum size of memory that can be used in any computer.

Address	Memory Locations
16 Bit	$2^{16} = 64$ K
32 Bit	$2^{32} = 4$G (Giga)
40 Bit	$2^{40} = 1$T (Tera)

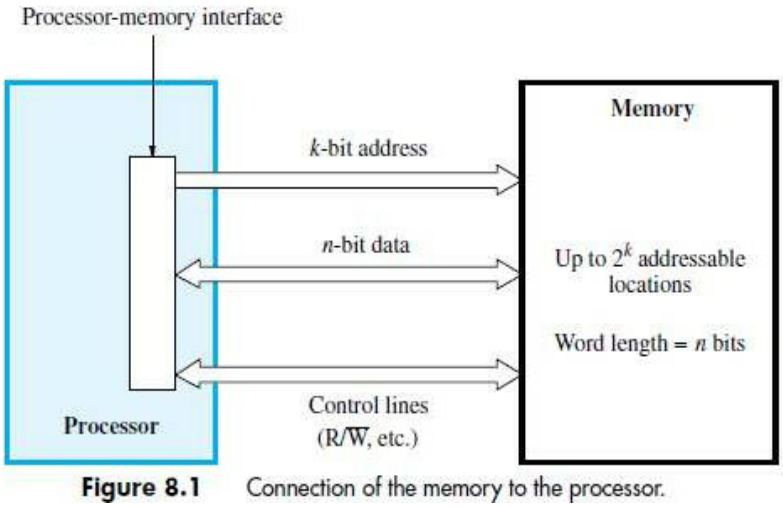

Figure 8.1 Connection of the memory to the processor.

- If MAR is k-bits long then
  → memory may contain upto 2^K addressable-locations.
- If MDR is n-bits long,then
  → n-bits of data are transferred between the memory and processor.
- Data transfer takes place over the processor-bus (Fig 8.1)
- Processor bus has:
  - o Address-Line
  - o Data-line
  - o Control-Line (R/W‟, MFC – Memory Function Completed).
- Control-Line is used to coordinate data transfers.
- The processor reads the data from the memory by
  → loading the address of the required memory-location into MAR and
  → setting the R/W‟ line to 1.
- Memory responds by
  → placing the data from the addressed-location onto the data-lines and
  → confirms this action by asserting MFC signal.
- Upon receipt of MFC signal, the processor loads the data from the data-lines into MDR.
- The processor writes the data into the memory-location by
  → loading the address of this location into MAR and
  → setting the R/W‟ line to 0.

- **Memory Access Time:** It is the time that elapses between
  → initiation of an operation and
  → completion of that operation.
- **Memory Cycle Time:** It is the minimum time delay required between the initiation of the two successivee memory-operations.

RAM (Random Access Memory):

In RAM, any location can be accessed for a Read/Write-operation in fixed amount of time,

Cache Memory:

It is a small, fast memory placed between
→ large slower main-memory and
→ processor.
It holds the currently active segments of a program and the data.

Virtual Memory:

- The address generated by the processor is referred to as a virtual/logical address.
- Virtual address-space is mapped onto the physical memory where data is actually stored.
- The mapping-function is implemented by MMU. (MMU = Memory Management Unit).
- Only the active portion of the address-space is mapped into locations in the physical memory.
- The remaining virtual-addresses are mapped onto the bulk storage devices such as magnetic disks.
- As the active portion of the virtual address-space changes during program execution, the MMU
- → changes the mapping-function and
- → transfers the data between disk and memory.
- During every memory-cycle, MMU determines whether the addressed-page is in the memory.
- If the page is in the memory.
  Requested word is accessed and execution proceeds.
  Otherwise, a page containing desired word is transferred from disk to memory.
- Memory can be classified as follows:
  1. RAM which can be further classified as follows:
     a. Static RAM
     b. Dynamic RAM (DRAM)
        ---> Synchronous DRAM
        ---> Asynchronous DRAM.
  2. ROM which can be further classified asfollows:as follows
     a. PROM
     b. EPROM
     c. EEPROM
  3. Flash Memory which can be further classified as:
     ---> Flash Cards
     ---> Flash Drives.

SEMI CONDUCTOR RAM MEMORIES

INTERNAL ORGANIZATION OF MEMORY-CHIP:

- Memory-cells are organized in the form of array (Fig 8.2).
- Each cell is capable of storing 1-bit of information.
- Each row of cells forms a memory-word.
- All cells of a row are connected to a common line called as **Word-Line**.
- Cells in each column are connected to **Sense/Write** circuit by 2-bit lines.

- Sense/Write circuits are connected to data-input or output lines of the chip.
- During a write-operation, the sense/write circuit
  → receive input information and
  → store input information in the cells of the selected word.

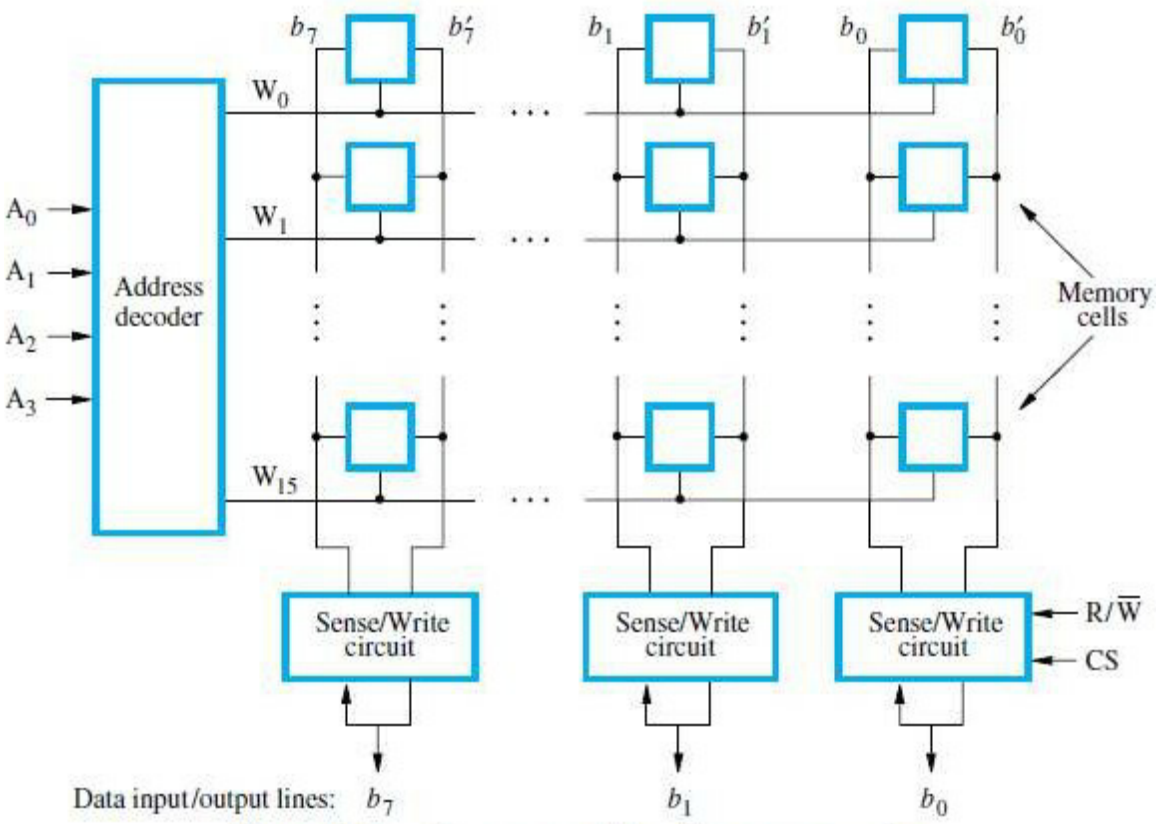

Figure 8.2 Organization of bit cells in a memory chip.

Bit Organization	Requirement of external connection for address, data and control lines
128 (16x8)	14
(1024) 128x8(1k)	19

- Data-input and data-output of each Sense/Write circuit are connected to a single bidirectional data-line.
- Data-line can be connected to a data-bus of the computer.
- Following two control lines are also used:
  - R/W → Specifies the required operation.
  - CS → Chip Select input selects the given chip in multichip memory system.

STATIC RAM (OR MEMORY):

Memories consist of circuits capable of retaining their state as long as power is applied are known.

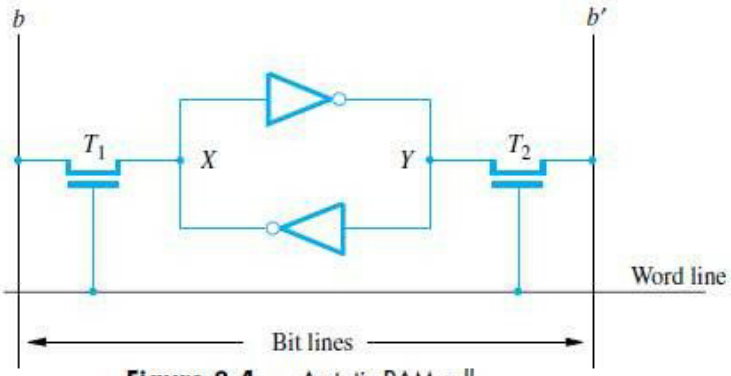

Figure 8.4 A static RAM cell.

- Two inverters are cross connected to form a latch (Fig 8.4).
- Latch is connected to 2-bit-lines by transistors T_1 and T_2.
- Transistors act as switches that can be opened/closed under the control of the word-line.
- When the word-line is at ground level, the transistors are turned off and the latch retain its state.

Read Operation:

- To read the state of the cell, the word-line is activated to close switches T_1 and T_2.
- If the cell is in state1,the signal on bit-line b is high and the signal on the bit-line b' is low.
- Thus, b and b' are complement of each other.
- Sense/Write circuit
  → monitors the state of b and b' and
  → sets the output accordingly.

Write Operation:

- The state of the cell is set by:
  → placing the appropriate value on bit-line b and its complement on b'
  → Then activates the word-line; This forces the cell into the corresponding state.
- Required signal on the bit-lines is generated by Sense/Write circuit.

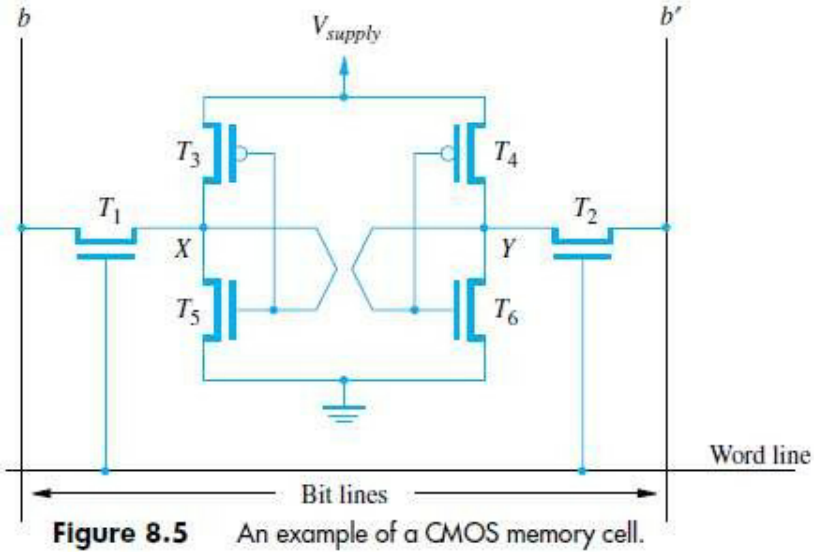

Figure 8.5 An example of a CMOS memory cell.

CMOS Cell:

- Transistor pairs (T_3, T_5) and (T_4, T_6) form the inverters in the latch (Fig 8.5).
- In state 1, the voltage at point X is high by having T_5, T_6 ON and T_4, T_5 as OFF.
- Thus,T_1 and T_2 return ON(Closed),bit-line b and b" will have high and low signals respectively.

Advantages:

- It has low power consumption„."the current flows in the cell only when the cell is active.
- Static RAM's can be accessed quickly. It access time is few nanoseconds.

Disadvantage: SRAMs are said to be volatile memories,,their contents are lost when power is interrupted.

ASYNCHRONOUS DRAM:

- Less expensive RAM can be implemented if simple cells are used.
- Such cells cannot retain their state indefinitely. Hence they are called **Dynamic RAM (DRAM).**
- Information is stored in a dynamic memory-cell in the form of a charge on a capacitor.
- This charge can be maintained only for tens of milliseconds.
- The contents must be periodically refreshed by restoring this capacitor charge to its full value.
- Inorder to store information in the cell,the transistor T isnturned ON (Fig 8.6)

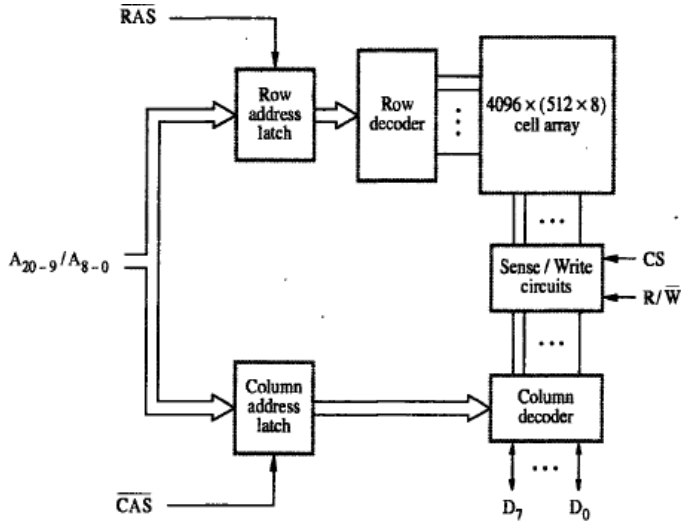

Figure 5.7 Internal organization of a 2M × 8 dynamic memory chip.

- Appropriate voltage is applied to the bit-line that charges the capacitor.
- After the transistor is turned off, the capacitor begins to discharge.
  Hence, information stored in a cell can be retrieved correctly before threshold value of capacitor drops down.

- During read operation,
  → Transistor is turned ON
  → Sense amplifier detects whether the charge on the capacitor is above the threshold value.
- If(charge on capacitor)>(threshold value)→Bit-line will have logic value '1'
- If(charge on capacitor)<(threshold value)→ Bit-line will set to logic value '0'

ASYNCHRONOUS DRAM DESCRIPTION:

- 4-bit cells in each row are divided into 512 groups of 8 (Fig 5.7)
- 21-bit address is needed to access a byte in the memory. 21-bit value is divided as follows:
  - 12 address bits- to select a row.
    i.e. A_{8-0} → specifies row-address of a byte.
  - 9 bits are needed to specify a group of 8 bits in the selected row.
    i.e. A_{20-9} → specifies column-address of a byte.

- During Read/Write-operation,
  → row-address is applied first.
  → row-address is loaded into row-latch in response to a signal pulse on **RAS** input of

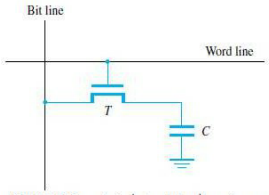

Figure 8.6 A single-transistor dynamic memory cell.

chip.

(RAS = Row-address Strobe ; CAS = Column-address Strobe)

- When a Read-operation is initiated, all cells on the selected row are read and refreshed.
- Shortly after the row-address is loaded, the column-address is
  → applied to the address pins
  → loaded into **CAS.**

- The information in the latch is decoded.
- And the appropriate group of 8 Sense/Write circuits is selected.
  - **R/W=1**(read-operation) → Output values of selected circuits are transferred to data-lines D_0-D_7.
  - **R/W=0**(write-operation) → Information on D_0-$D_7$are transferred to the selected circuits.
- RAS and CAS are active-low so that they cause latching of address when they change from high to low.
- To ensure that the contents of DRAM are maintained, each row of cells is accessed periodically.
- A special memory-circuit provides the necessary control signals RAS and CAS that govern the timing.
- Processor must take into account the delay in response of the memory.

Fast Page Mode:

- Transferring the bytes in sequential order is achieved by applying the consecutive sequence of
  column-address under the control of successive CAS signals.
- This scheme allows transferring a block of data at a faster rate.
- The capability of transferring a block is called as *fast page mode*.

SYNCHRONOUS DRAM:

- The operations are directly synchronized with clock signal (Figure8.8).
- The address and data connections are buffered by means ofregisters.
- The output of each sense amplifier is connected to alatch.
- A Read-operation causes the contents of all cells in the selected row to be loaded in theselatches.
- Data held in latches that correspond to selected columns are transferred into data-outputregister.
- Thus, data becoming available on the data-outputpins.

- First,therow-addressislatchedundercontrolofRAS'signal(Figure8.9).
- The memory typically takes 2 or 3 clock cycles to activate the selectedrow.
- Then,thecolumn-addressislatchedunderthecontrolofCAS'signal.
- After a delay of one clock cycle, the first set of data bits is placed on thedata-lines.
- SDRAM automatically increments column-address to access next 3 sets of bits in the selectedrow.

LATENCY AND BANDWIDTH:

A good indication of performance is given by two parameters:
1) Latency
2)Bandwidth.

Latency:

It refers to the amount of time it takes to transfer a word of data to or from the memory.

- For a single word transfer, the latency provides the complete indication of memory performance.
- For a block transfer, the latency denotes the time it takes to transfer the first word of data.

Bandwidth:

It refers to the number of bits or bytes that can be transferred in one second.

- Bandwidth mainly depends on
  ---> The speed of accessing the stored data
  ---> The number of bits that can be accessed in parallel.

DOUBLE DATA RATE SDRAM (DDR-SDRAM):

- Standard SDRAM performs all actions on the rising edge of the clock signal.
- DDR-SDRAM transfer data on both the edges (rising edge, trailing edge).
- Bandwidth of DDR-SDRAM is doubled for long burst transfer.
- To access the data at high rate, the cell array is organized into two banks.
  Each bank can be accessed separately.
- Consecutive words of a given block are stored in different banks.
- Such interleaving of words allows simultaneous access to two words.
- The two words are transferred on successive edge of the clock.

STRUCTURE OF LARGER MEMORIES

Dynamic Memory System:

- Physical implementation is done in the form of memory-modules.
- If a large memory is built by placing DRAM chips directly on the Motherboard, then it will occupy large amount of space on the board.
- These packaging consideration have led to the development of larger memory units known as SIMM
  and DIMM.
  SIMM → Single Inline Memory-Module
  DIMM → Dual Inline Memory-Module
- SIMM/DIMM consists of many memory-chips on small board that plugs into a socket on motherboard.

MEMORY-SYSTEM CONSIDERATION

MEMORY CONTROLLER:

- To reduce the number of pins, dynamic memory-chips use multiplexed-address inputs.
- Address is divided into two parts:
  1. High Order Address Bit
     - Select a row in cell array.
     - It is provided first and latched into memory-chip under the control of RAS signal.
  2. Low Order Address Bit
     - Selects a column.
     - They are provided on same address pins and latched using CAS signals.
- The Multiplexing of address bit is usually done by **Memory Controller Circuit** (Fig 5.11)
- Controller accepts a complete address and R/W signal from the processor.
- A Request signal indicates a memory access operation is needed.
  Then, the Controller
  → forwards the row and column portions of the address to the memory.
  → generates RAS & CAS signals
  → sends R/W CS signals to the memory.

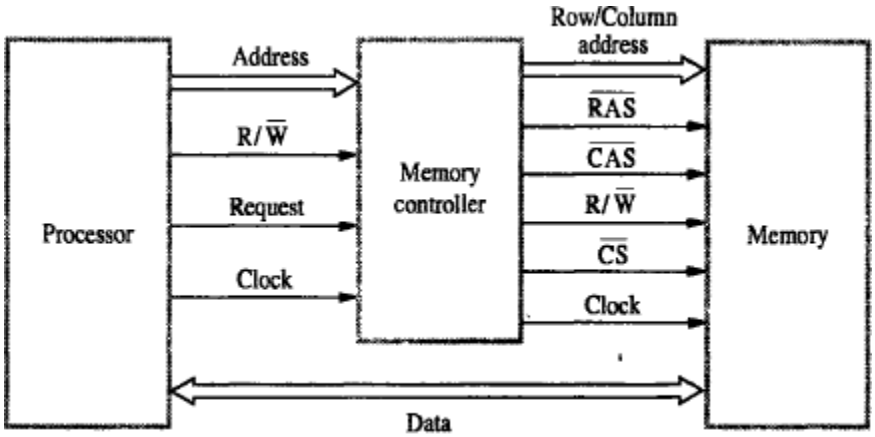

Figure 5.11 Use of a memory controller.

RAMBUS MEMORY:

- Rambus developed the implementation of narrow bus as wide bus is so expensive.
- Rambus technology is a fast signaling method used to transfer information between chips.
- The signals consist of much smaller voltage swings around a reference voltage V_{ref}.

which is about 2V.

- Two logical values are represented by 0.3V swings above and below V_{ref}.
- This type of signaling is generally known as **Differential Signaling**.
- Rambus provides a complete specification for the design of communication called as **Rambus Channel**.
- Rambus memory has a clock frequency of 400MHz.
- Data is transmitted on both the edges of clock so that effective data-transfer rate is 800MHZ.
- Chips that provide circuitry needed to interface Rambus channel are called **RDRAM.**
  --> RDRAM = Rambus DRAM
- Rambus channel has:
  - 9 Data-lines (1^{st}-8^{th}line ->Transfers the data, 9^{th}line->Paritychecking).
  - 1 Control-Line
  - 1 Power line.
- A two channel Rambus has 18 data-lines which has no separate Address-Lines.
- Communication between processor and RDRAM modules is carried out by means of packets transmitted
  on the data-lines.
- There are three types of packets:
  - Request
  - Acknowledge
  - Data.

READ ONLY MEMORY (ROM)

- Both SRAM and DRAM chips are volatile, i.e. they lose stored information if power is turned off.
- Many applications require non-volatile memory which retains the stored information if power is turned off.
- For example,
  - OS software has to be loaded from disk to memory i.e. it requires non-volatile memory.
- Non-volatile memory is used in embedded system.
- Since it involves only reading of stored data, it is called ROM.
  At Logic value '0' →Transistor(T) is connected to the ground point(P).
  Transistor switch is closed and voltage on bit-line nearly drops to zero (Fig 8.11).
- **At Logic value '1'** →Transistor switch is
  open.and the
  bit line remains at
  highvoltage.

- To read the state of the cell, the word-line is activated.
- Sense circuit at the end of the bit-line generates the proper output value.

TYPES OF ROM:

Different types of non-volatile memory are

1. PROM
2. EPROM
3. EEPROM&
4. Flash Memory (Flash Cards & FlashDrives)

PROM (PROGRAMMABLE ROM):

- PROM allows the data to be loaded by the user.
- Programmability is achieved by inserting a fuse at point P in a ROM cell.
- Before PROM is programmed, the memory contains all 0's.
- User can insert 1's at required location by burning-out fuse using high current-pulse.
- This process is irreversible.

Advantages:

1. It provides flexibility
2. It is faster
3. It is less expensive because they can be programmed directly by the user.

EPROM (ERASABLE REPROGRAMMABLE ROM):

- EPROM allows
  - → stored data to be erased and
  - → new data to be loaded.
- In a cell,a connection to ground is always made at P'and a special transistor is used.
- Transistor has the ability to function as
  - → a normal transistor
  - → a disabled transistor that is always turned off.
- Transistor can be programmed to behave as a permanently open switch, by injecting charge

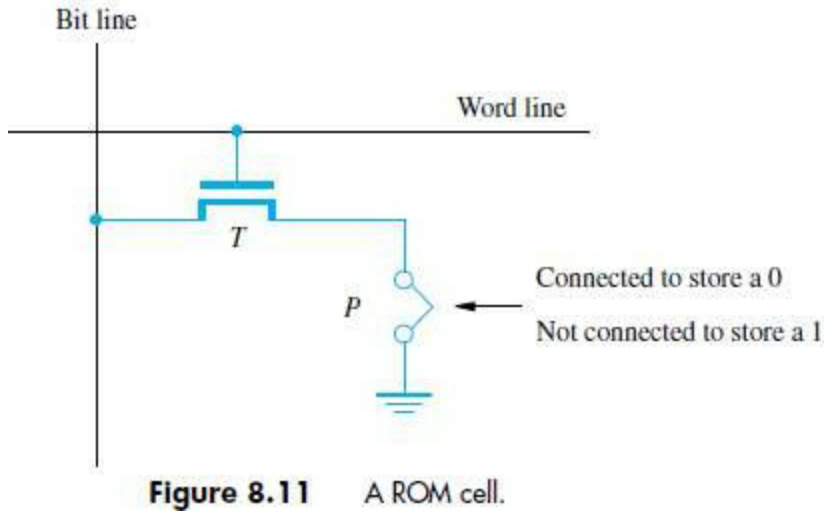

Figure 8.11 A ROM cell.

in to it.

- Erasure requires dissipating the charges trapped in the transistor of memory-cells. This can be done by exposing the chip to ultra-violet light.
- **Advantages:**
  1. Provides flexibility during the development-phase ofdigital-system.
  2. Capable of retaining stored information for a long time.
- **Disadvantages:**
  1. It must be physically removed from the circuit for reprogramming.
  2. Needs UV light to erase entire contents.

EEPROM (ELECTRICALLY ERASABLE ROM)

Advantages:

1. It can be both programmed and erased electrically.
2. It allows the erasing of all cell contents electively.

Disadvantage: It requires different voltage for erasing, writing and reading the stored data.

FLASH MEMORY:

- In EEPROM, it is possible to read and write the contents of a single cell.
- In Flash device, it is possible to read contents of a single cell and write entire contents of
- a block.
- Prior to writing, the previous contents of the block are erased.
  Eg: In MP3 player, the flash memory stores the data that represents sound.
- Single flash chips cannot provide sufficient storage capacity for embedded-system.
- **Advantages:**
  1.Flash drives have greater density which leads to higher capacity & low cost perbit.
  2. It requires single power supply voltage and consumes less power.
- There are two methods for implementing larger memory:
  1. Flash Cards
  2. Flash Drives

Flash Cards:

- One way of constructing larger module is to mount flash-chips on a small card.
- Such flash-card have standard interface.
- The card is simply plugged into a conveniently accessible slot.
- Memory-size of the card can be 8, 32 or 64MB.
- Eg: 1minute music can be stored in 1MB of memory. Hence 64MB flash cards can store an hour of music.

Flash Drives:

- Larger flash memory can be developed by replacing the hard disk-drive.
- Flash drives are designed to fully emulate the hard disk.
- Flash drives are solid state electronic devices that have no movable parts.

Advantages:

1. Shorter seek and access times which results in faster response.
2. Low power consumption attractive fo rbattery driven applications.
3. Insensitive to vibration.

Disadvantages:

1. Capacity of flash drive (<1GB) is less than hard disk(>1GB).

2. Higher cost per bit.
3. Flash memory will weaken after it has been written a number of times (typically atleast 1 million times).

SPEED, SIZE , COST

- Main-memory can be built with DRAM (Fig 8.14)
- Thus,SRAM's are used in smaller units where speed is of essence.
- Cache-memory is of two types:
  1. **Primary/Processor Cache** (Level1 or L1 cache)
     It is always located on the processor-chip.
  2. **Secondary Cache** (Level2 or L2 cache)
     It is placed between primary-cache and the rest of the memory.
- Memory is implemented using the dynamic components (SIMM, RIMM,DIMM).
- The access time of main-memory is about 10 times longer than the access time for L1 cache.

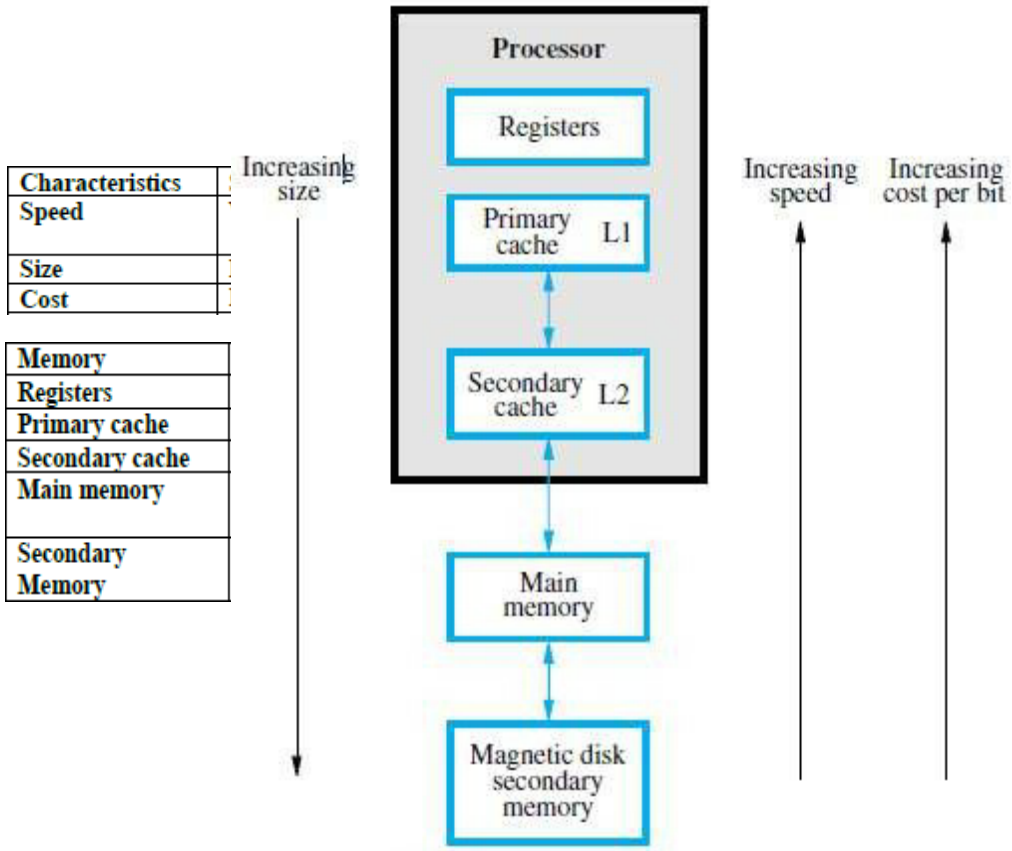

Figure 8.14 Memory hierarchy.

CACHE MEMORY

- The effectiveness of cache mechanism is based on the property called '**Locality of Reference'.**
  Locality of Reference:
  It refers to a phenomenon in which a computer program tends to access same set of memory locations for a particular time period.
  --> This property is mainly shown by loops and subroutine calls in a program.

- There are two ways with which data or instructions are fetched from memory and gets stored in cache:
  1. **Temporal locality:**
     It refers to the current memory locations which may be accessed soon by the program. This data is stored in cache memory, avoiding search for the same data in main memory when needed.
  2. **Spatial locality:**
     It refers to the data nearer to the currently accessed memory location that may be needed soon.
- Cache memory acts as a buffer between processor and RAM, speeding up the operations of the processor.
- If active segment of a program is placed in cache-memory, then total execution time can be reduced.
- **Block** refers to the set of contiguous address locations of particular size.
- Cache-line is used to refer to the cache-block.

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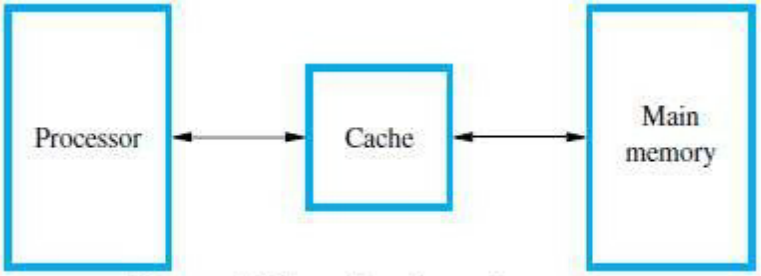

Figure 8.15 Use of a cache memory.

- Cache memory stores a reasonable number of blocks at a given time.
  These blocks are small in number compared to the total number of blocks in main memory.
- Correspondence between blocks of main memory and cache memory is specified by a mapping function.
- Cache control hardware decides the block to be removed to create space for the new block.
- The collection of rules for making replacement decision is called the **Replacement Algorithm.**
- Cache control-circuit determines whether the requested word currently exists in the cache.
- Whenever Processor needs to write data, it checks if it is already in cache. If so, it is termed as Write-hit.
- Copy of data from main memory is stored in cache. A write to cache may result in inconsistent problem since
  Cache and main memory will have different data.
- To solve this, Write-operation is done in two ways:
  1. Write-through protocol
  2. Write-back protocol.

  Write-Through Protocol:
  This protocol
  --> Updates cache and main memory simultaneously.
  --> Is Used when there are no frequent writes to cache.
  Disadvantage: High latency (delay) due to two writes.

  Write-Back Protocol:
  This protocol
  → updates only the cache
  → Memory is updated only when data in cache is to be replaced.

Replacement is done using replacement algorithms called LET, FIFO, LIFO etc.

Dirty/Modified Bit:

Each block of cache is marked with a bit to indicate if it was modified(dirty).

If so, it may require a write to memory when replacement is to be done in cache.

- **During Read-operation,**

  If the requested-word currently not exists in the cache, then **read-miss** will occur.
- To overcome the read miss, *Load–through/Early restart protocol* is used.

  Load–Through Protocol
  - Block of words that contains the requested-word is copied from the memory into cache.
  - After entire block is loaded into cache, the requested-word is forwarded to processor.
- **During Write-operation ,**

  If the requested word doesn't exist in the cache, then **write-miss** will occur.
  - If **Write-Through Protocol** is used, data is written directly into main memory.
  - If **Write-Back Protocol** is used,
    - → block containing the addressed word is first brought into the cache
    - → then the desired word in the cache is over-written with the new data.

MAPPING-FUNCTION

- There are three different mapping-functions:
  1. Direct Mapping
  2. Associative Mapping
  3. Set-Associative Mapping

DIRECT MAPPING

- The block-j of the main-memory maps onto block-j modulo-128 of the cache (Figure8.16).
- When the memory-blocks 0, 128, & 256 are loaded into cache, the block is stored in cache-block 0. Similarly, memory-blocks 1, 129, 257 are stored in cache-block1.
- Contention may arise when

  a) cache is has no enough space.

  b) More than one memory block is mapped onto a given cache block position.
- The contention is resolved by
  - allowing the new blocks to overwrite the currently resident block.
- Memory address determines the placement of block in the cache.

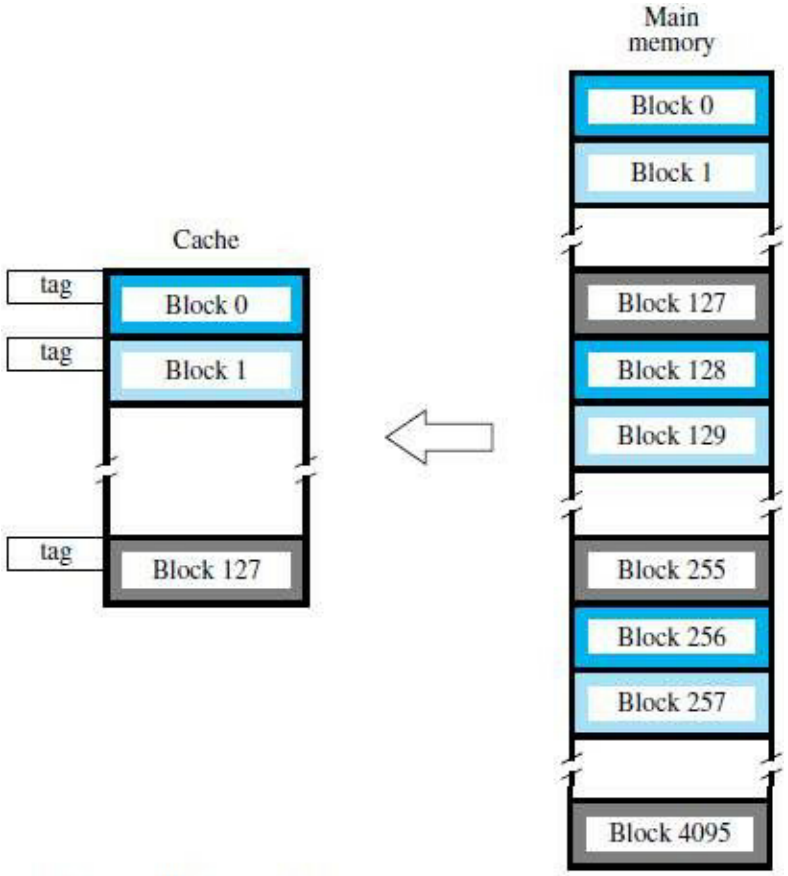

Figure 8.16 Direct-mapped cache.

- The memory-address is divided into three fields:
  Low Order 4 bit field:
  - Selects one of 16 words in a block.

  7 bit cache block field
  - 7-bits determine the cache position in which new block must be stored.

  5 bit Tag field
  - 5-bits memory-address of block is stored in 5 tag-bits associated with cache location.
- As execution proceeds,
  --> 5-bit tag field of memory address is compared with tag-bits associated with cache location.
  --> If they match, then the desired word is in that block of the cache.
  Otherwise, the block containing required word must be first read from the memory and then the word must be loaded into the cache.

ASSOCIATIVE MAPPING:

- In this mapping technique,the memory-block can be placed in any cache-block position. (Fig 8.17).
- 12 tag-bits will identify a memory-block when it is resolved in the cache.
- Tag-bits of an address received from processor are compared to the tag-bits of each block of cache.
- This comparison is done to see if the desired block is present in the cache.

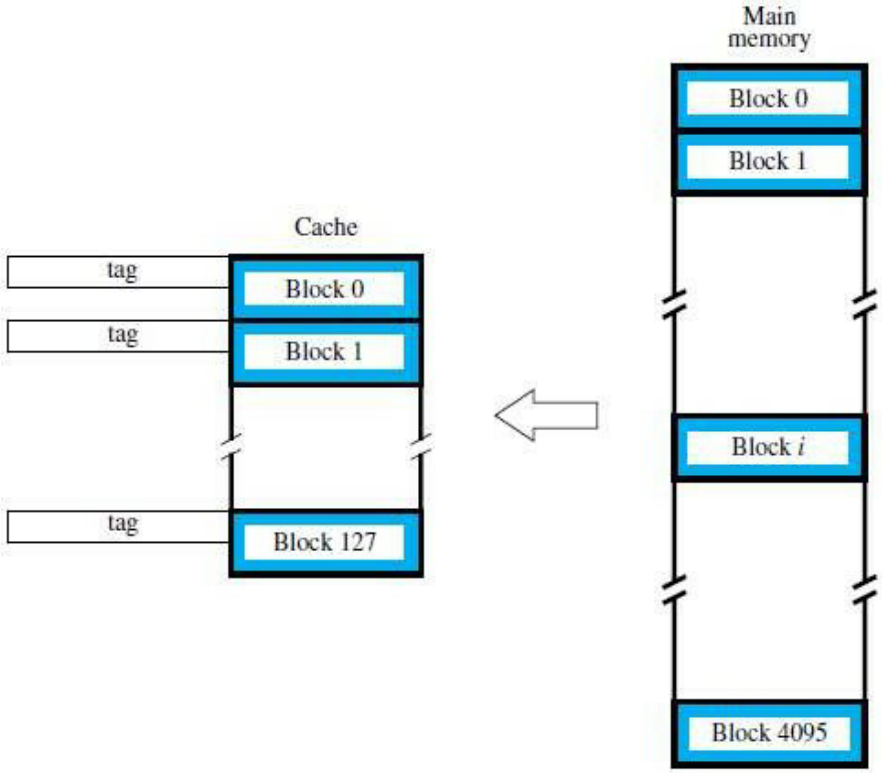

Figure 8.17 Associative-mapped cache.

- It gives complete freedom in choosing the cache location.
- A new block that has to be brought into the cache has to replace an existing block if the cache has no enough space
- Memory has to determine whether a given block is in the cache or not.

Advantage: More flexible than direct mapping technique.
Disadvantage: High cost

SET-ASSOCIATIVE MAPPING:

- It is the combination of direct and associative mapping. (Fig 8.18)
- Here, blocks of the cache are grouped into sets.
- Mapping allows a block of the main-memory to reside in any block of the specified set.
- Cache has two blocks per set, so the memory blocks 0, 64,128…… 4032 maps into cache set '0'.
- Cache can occupy either of the two block positions within the set.
- **6 bit set field**
  - Determines which set of cache contains the desiredblock.

  6 bit tag field
  - The tag field of the address is compared to the tags of the two blocks of the set.
  - This comparison is done to check if the desired block is present.

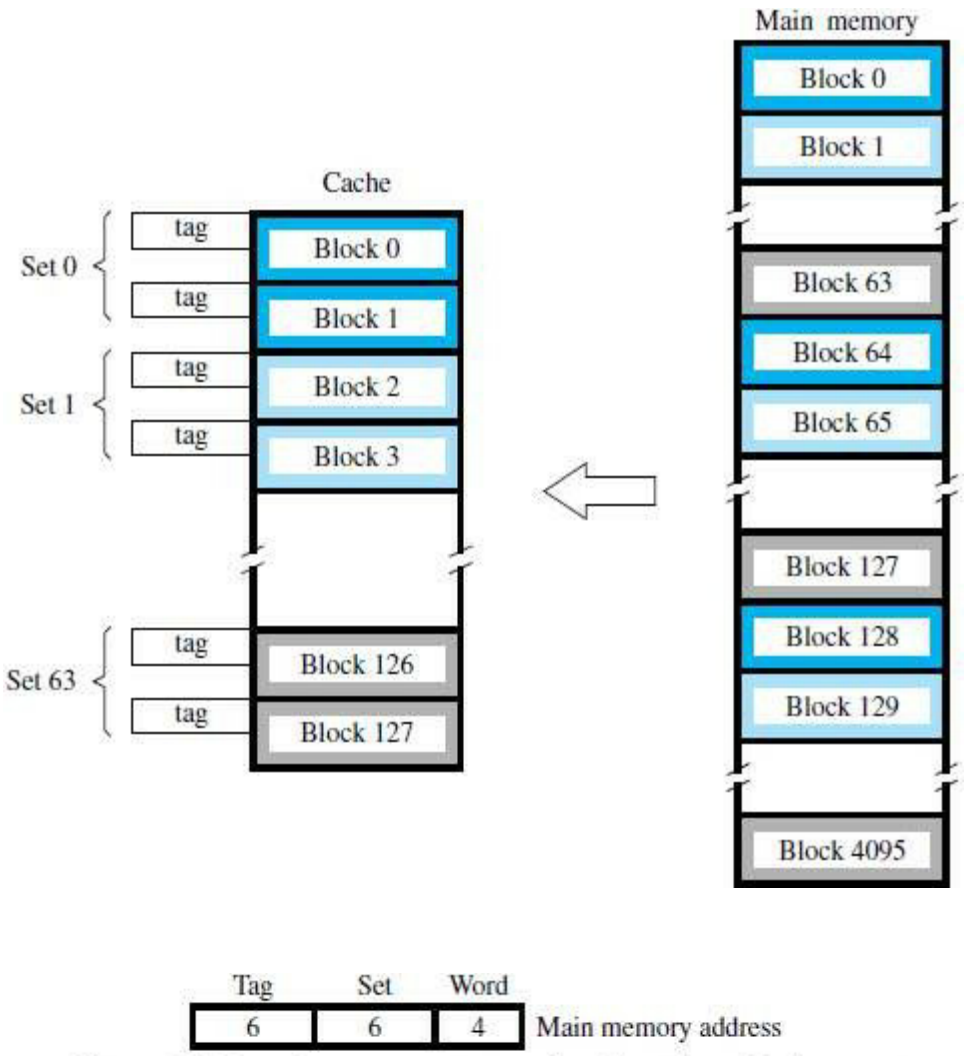

Figure 8.18 Set-associative-mapped cache with two blocks per set.

- Cache which contains one block per set is called **direct mapping.**
- Cache that has 'k' blocks per set is called as "**k-way set associative cache**".
- Each block contains a control bit called a **valid-bit**.
- Valid-bit indicates whether the block contains valid-data.
- Dirty bit indicates whether the block has been modified when it resides in cache.
  - **Valid-bit=0** → When power is initially applied to the system.
  - **Valid-bit=1** → When the block is loaded from main memory at first time.
- If the main memory block is updated by a source and if that block exists in the cache, then the valid-bit
  will be cleared to '0'.
- If the Processor and DMA uses the same copies of data then it is called as **Cache Coherence Problem**.
- **Advantages:**
  - Contention problem of direct mapping is solved by having few choices for block placement.
  - Hardware cost is decreased by reducing the size of associative search.

REPLACEMENT ALGORITHM

- In direct mapping method,
  - the position of each block is pre-determined and there is no need of replacement strategy.

- In associative and set associative method,
  - Block position is not pre-determined.
  - If the cache is full and if new blocks are brought into the cache,
    - then the cache-controller must decide which of the old blocks has to be replaced.
- When a block is to be overwritten, the block with longest time being referenced is overwritten.
- This block is called **Least recently Used (LRU) block** and the technique is called **LRU algorithm**.
- The cache-controller tracks the references to all blocks with the help of block counter.
- **Advantage:** Performance of LRU is improved by randomly deciding which block to be overwritten.
- Example:
  Consider 4 blocks/set in set associative cache.
  - 2 bit counter can be used for each block.
  - When a **'hit'** occurs, then block counter=0; The counter with values originally lower than the referenced one are incremented by 1 and all others remain unchanged.
  - When a **'miss'** occurs and if the set is full, the blocks with the counter value 3 is removed, the new block is put in its place and its counter is set to "0" and other block counters are incremented by 1.

PERFORMANCE CONSIDERATION

- Two key factors in the commercial success are :
  1. Performance
  2. Cost
- In other words, the best possible performance is at low cost.
- A common measure of success is called the **Price/Performance ratio.**
- Performance depends on
  → how fast the machine instructions are brought to the processor
  → how fast the machine instructions are executed.
- To achieve parallelism, *inerleaving* is used.
- Parallelism means both the slow and fast units are accessed in the same manner.

INTERLEAVING:

- Main memory of a computer is structured as a collection of physically separate modules.
- Each module has its own
  - ABR (Address Buffer Register)
  - DBR (Data Buffer Register).
- So, memory access operations may proceed in more than one module at the same time (Fig 5.25).
- Thus, the aggregate-rate of transmission of words to/from the main memory can be increased.

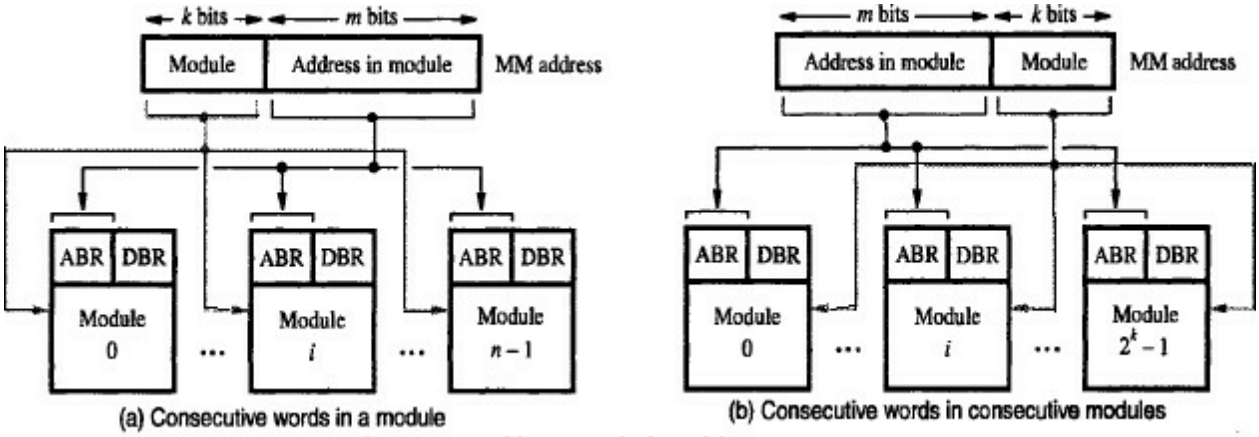

Figure 5.25 Addressing multiple-module memory systems.

- The low-order k-bits of the memory-address select a module.
    - While the high-order m-bits name a location within the module.

  In this way, consecutive addresses are located in successive modules.
- Thus, any component of the system can keep several modules busy at any one time T.
- This results in both
  → faster access to a block of data and
  → higher average utilization of the memory system as a whole.
- To implement the interleaved structure, there must be 2k modules;
  Otherwise, there will be gaps of non-existent locations in the address-space.

Hit Rate and Miss Penalty:

- The number of hits stated as a fraction of all attempted accesses to the cache is called the **Hit Rate**.
- The extra time needed to bring the desired information into the cache is called the **Miss Penalty**.
- High hit rates, well over 0.9 are essential for high-performance computers.
- Performance is adversely affected by the actions that need to be taken when a miss occurs.
- A performance penalty is incurred because of the extra time needed to bring a block of data from a slower
  unit to a faster unit.
- During that period, the processor is stalled waiting for instructions or data.
- We refer to the total access time seen by the processor when a miss occurs as the miss penalty.
- Let h be the hit rate, M the miss penalty, and C the time to access information in the cache. Thus, the average access time experienced by the processor is

$$t_{avg} = hC + (1 - h)M$$

VIRTUAL MEMORY

- It refers to the technique that automatically moves program/data blocks into the main memory when they are required for execution (Fig 8.24).
- The address generated by the processor is referred to as a **virtual/logical address**.
- The virtual-address is translated into physical-address by **MMU** (Memory Management Unit).
- During every memory-cycle, MMU determines whether the addressed-word is in the memory. If the word is in memory.
  --> Then, the word is accessed and execution proceeds.
  --> Otherwise, a page containing desired word is transferred from disk to memory.
- Using DMA scheme, transfer of data between disk and memory is performed effectively.

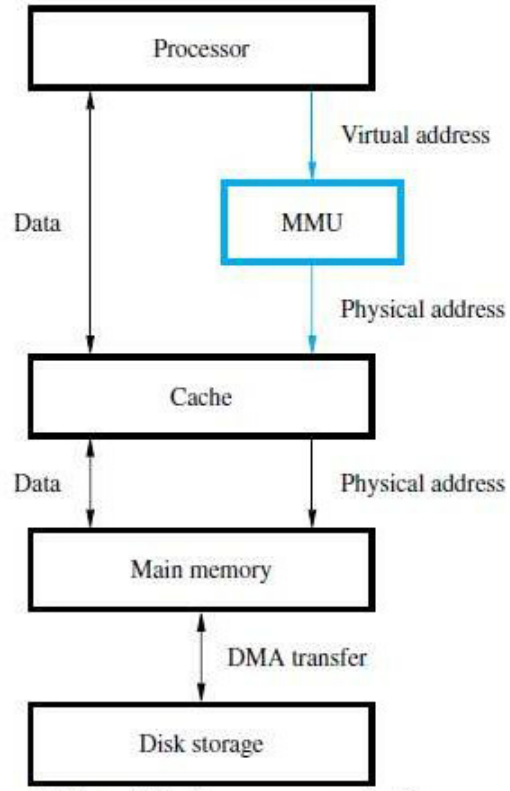

Figure 8.24 Virtual memory organization.

VIRTUAL MEMORY ADDRESS TRANSLATION:

- All programs and data are composed of fixed length units called **Pages** (Fig 8.25).
  - The Page consists of a block-of-words. The words occupy contiguous locations in the memory.
  - The pages are commonly range from 2K to 16K bytes in length.
- **Cache Bridge** speed-up the gap between main memory and secondary storage.
- Each virtual-address contains
  - Virtual Page number (Low order bit)and
  - Offset (High orderbit)
  - Virtual Page number + Offset → specifies the location of a particular word within a page.
- **Page-table:** It contains the information about
  → memory-address where the page is stored
  → current status of the page.
- **Page-frame:** An area in the main memory that holds one page.
- **Page-table Base Register:** It contains the starting address of the page table.
- *Virtual Page Number + Page-table Base register* → Gives the starting address of the page if that page currently resides in memory.
- **Control-bits in Page-table:** The Control-bits is used to
  - Specify the status of the page while it is in memory.
  - Indicate the validity of the page.

o Indicate whether the page has been modified during its stay in the memory.

-

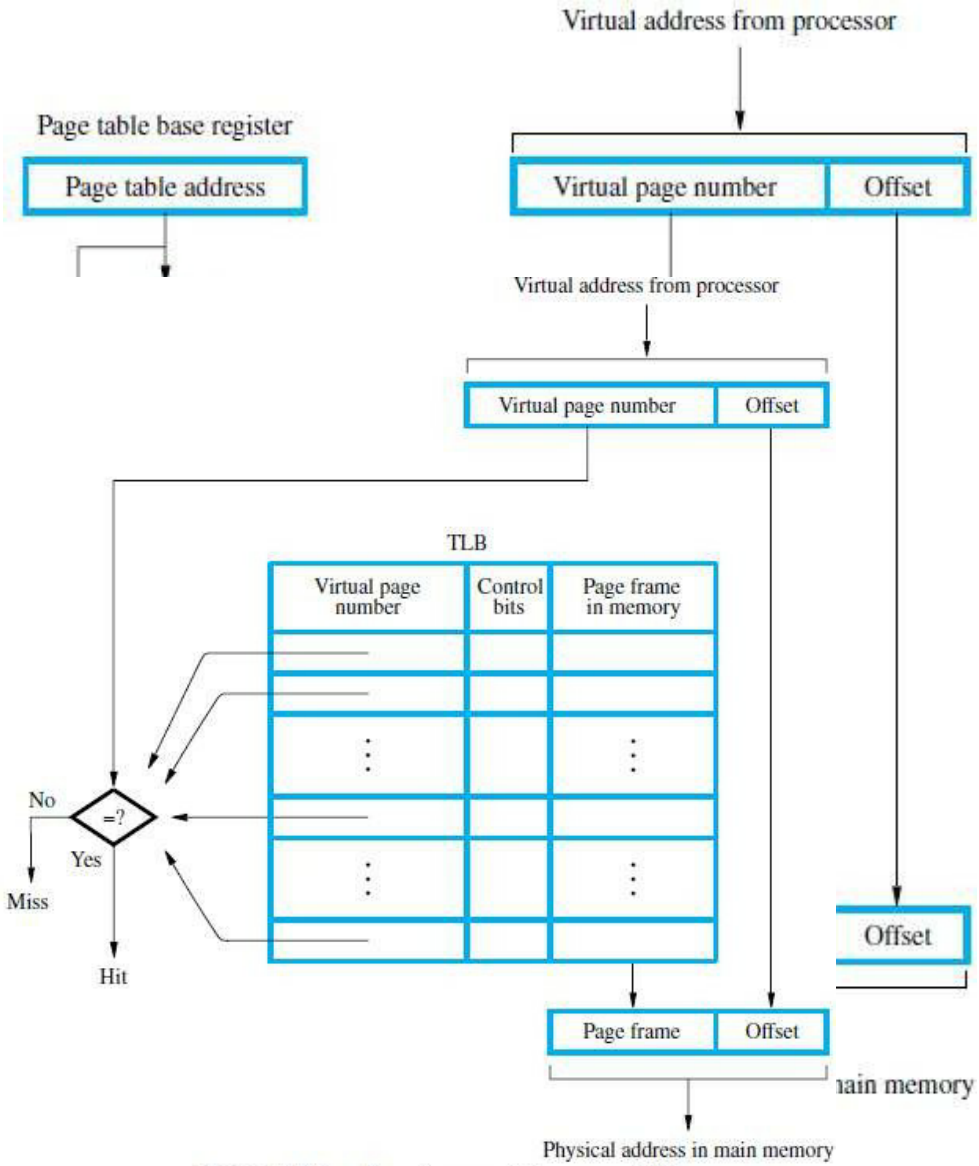

Figure 8.26 Use of an associative-mapped TLB.

TRANSLATION LOOKASIDE BUFFER (TLB):

- Page-table information is used by MMU for every read/write access (Fig 8.26).
- Page-table is placed in the memory but a copy of small portion of the page-table is located within MMU. This small portion is called **TLB** (Translation LookAside Buffer).
  - o TLB consists of the page-table entries that corresponds to the most recently accessed pages.
  - o TLB also contains the virtual-address of the entry.
- When OS changes contents of page-table, the control-bit will invalidate corresponding entry inTLB.
- Given a virtual-address, the MMU looks in TLB for thereferenced-page.
  - o If page-table entry for this page is found in TLB, the physical-address is obtained immediately. Otherwise, the required entry is obtained from the page-table & TLB is updated.

Page Faults:

- Page-fault occurs when a program generates an access request to a page that is not in memory.
- When MMU detects a page-fault, the MMU asks the OS to generate an interrupt.
- OS then
  → suspends the execution of the task that caused the page-fault and
  → begins execution of another task whose pages are in memory.
- When the task resumes, the interrupted instruction must continue from the point of interruption.
- If a new page is brought from disk when memory is full, disk must replace one of the resident pages. In this case, **LRU algorithm** is used to remove the least referenced page from memory.
- A modified page has to be written back to the disk before it is removed from the memory. In this case, **Write–Through protocol** is used.

MEMORY MANAGEMENT REQUIREMENTS

- Management routines are part of the Operating-system.
- Assembling the OS routine into virtual-address space is called **System Space**.
- Virtual space in which the user application programs reside is called the **User Space**.
- Each user space has a separate page-table.
- MMU uses the page-table to determine the address of the table to be used in the translation process.
- The process has two stages:
  - **User State:** In this state, the processor executes the user program.
  - **Supervisor State:** In this state, the processor executes the OS routines.

Privileged Instruction:

- In user state, the machine instructions cannot be executed.
- Hence a user-program is prevented from accessing the page-table of the system space.
- The control-bits in each entry can be set to control the access privileges granted to each program.
  - i.e. One program may be allowed to read/write a given page.
  - While the other programs may be given only read access.

SECONDARY-STORAGE

- Semi-conductor memories do not provide all the storage capability.
- Secondary-storage devices provide larger storage requirements.
- Some of the secondary-storage devices are:
  1. MagneticDisk
  2. Optical Disk
  3. Magnetic Tapes

MAGNETIC DISK:

- Magnetic Disk consists of one or more disk mounted on a common spindle.
- A **thin magnetic film** is deposited on each disk (Fig 8.27)
- Disk is placed in a **rotary-drive** so that magnetized surfaces move in close proximity to R/W heads.

- Each **R/W head** consists of:
  1) Magnetic Yoke
  2) Magnetizing-Coil.
- Digital information is stored on magnetic film by applying current pulses to the magnetizing-coil.
- Only changes in the magnetic field under the head can be sensed during the Read-operation.
- Therefore, if the binary states 0 & 1 are represented by two opposite states, then a voltage is induced in the head only at 0-1 and at 1-0 transition in the bit stream.
- A consecutive 0's and 1's are determined by using the clock.
- **Manchester Encoding** technique is used to combine the clocking information with data.

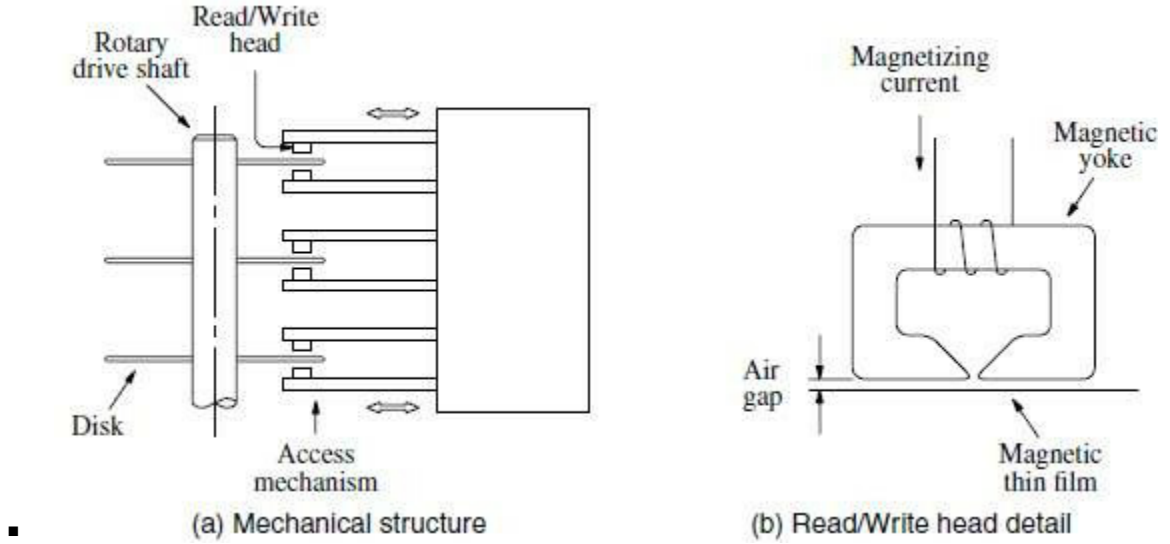

Figure 8.27 Magnetic disk principles.

- R/W heads are maintained at small distance from disk-surfaces in order to achieve high bitdensities.
- When disk moves at steady state, the air pressure develops between disk surfaces and the head. This air pressure forces the head away from the surface.
- The flexible spring connection between head and its arm mounting permits the head to fly at the desired distance away from the surface.

Winchester Technology:

- Read/Write heads are placed in a sealed, air filtered enclosure called the WinchesterTechnology.
- Read/write heads can operate closure to magnetic track surfaces because the dust particles which are a problem in unsealed assemblies are absent.

Advantages:

- Has larger capacity for a given physical size.
- Data intensity is high because the storage medium is not exposed to contaminating elements.

- Read/write heads of a disk system are movable.

- The disk system has three parts:
  1) Disk Platter (Usually called Disk)
  2) Disk-drive (spins the disk and moves Read/write heads)
  3) Disk Controller (controls the operation of the system)

ORGANIZATION AND ACCESSING OF DATA ON A DISK

- Each surface is divided into concentric **Tracks** (Fig 8.28)
- Each track is divided into **Sectors.**
- The set of corresponding tracks on all surfaces of a stack of disk form a **Logical Cylinder**.
- Data is accessed by specifying *the surface number, track number and the sector number.*
- Read/Write-operation start at sector boundaries.
- Data bits are stored serially on each track.

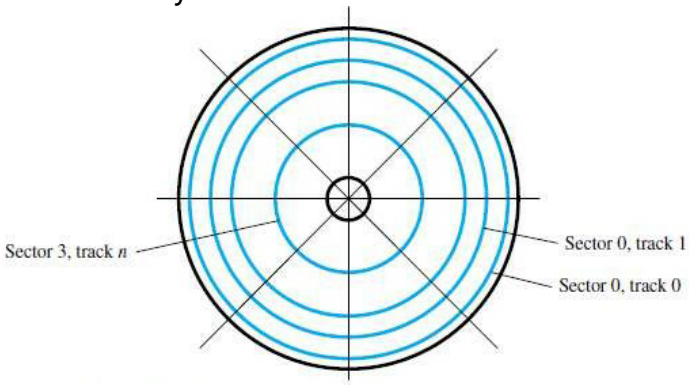

Figure 8.28 Organization of one surface of a disk.

- Each sector usually contains 512 bytes.
- **Sector Header** --> contains identification information.
  - It helps to find the desired sector on the selected track.
- **ECC** (Error checking code)- is used to detect and correct errors.
- An unformatted disk has no information on its tracks.
- The formatting process divides the disk physically into tracks and sectors.
- The formatting process may discover some defective sectors on all tracks.
- **Disk Controller** keeps a record of various defects.
- The disk is divided into logical partitions:
  --> Primary partition
  --> Secondary partition
- Each track has same number of sectors. So, all tracks have same storage capacity.
- Thus, the stored information is packed more densely on inner track than on outertrack.

Access Time:

- There are two components involved in the time-delay:
  Seek time: Time required to move the read/write head to the proper track.
  Latency/Rotational Delay: The amount of time that elapses after head is positioned over the correct track until
  the starting position of the addressed sector passes under the R/W head.

Seek time + Latency = Disk access time

DATA BUFFER OR CACHE:

- A disk-drive that incorporates the required SCSI circuit is referred as **SCSI Drive**.
- The SCSI can transfer data at higher rate than the disk tracks.
- A data buffer can be used to deal with the possible difference in transfer rate between disk and SCSI bus
- The buffer is a semiconductor memory.
- Buffer can also provide cache mechanism for the disk i.e. when a read request arrives at the disk, then
  controller first checks if the data is available in the cache/buffer.
  If data is available in cache.
  --> data can be accessed and placed on SCSI bus.
  --> Otherwise, the data will be retrieved from the disk.

DISK CONTROLLER:

- The disk controller acts as interface between disk-drive and system-bus (Fig 8.13)
- The disk controller uses DMA scheme to transfer data between disk and memory.
- When the OS initiates the transfer by issuing R/W request, the controller's register will load the following information:
  - **Memory Address:** Address of first memory-location of the block of words involved in the transfer.
  - **Disk Address:** Location of the sector containing the beginning of the desired block of words.
  - **Word Count:** Number of words in the block to be transferred.
  -

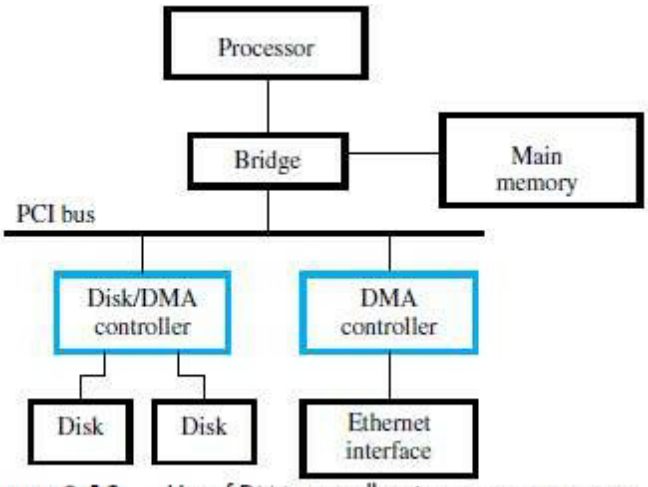

Figure 8.13 Use of DMA controllers in a computer system.

- The disk-address issued by the OS is a logical address.
- The corresponding physical-address on the disk may be different.
- Controller's major functions are:
  - **Seek** - Causes disk-drive to move the R/W head from its current position to desired track.
  - **Read** - Initiates a Read-operation, starting at address specified in the disk-address register.
    Data read serially from the disk are assembled into words and placed into the data buffer
    for transfer to the main memory.

- **Write** - Transfers data to the disk.
- **Error Checking** - Computes the error correcting code (ECC) value for the data read from a given sector and compares it with the corresponding ECC value read from the disk.
  --> In case of a mismatch, it corrects the error if possible;
  --> Otherwise, it raises an interrupt to inform OS that an error has occurred.
