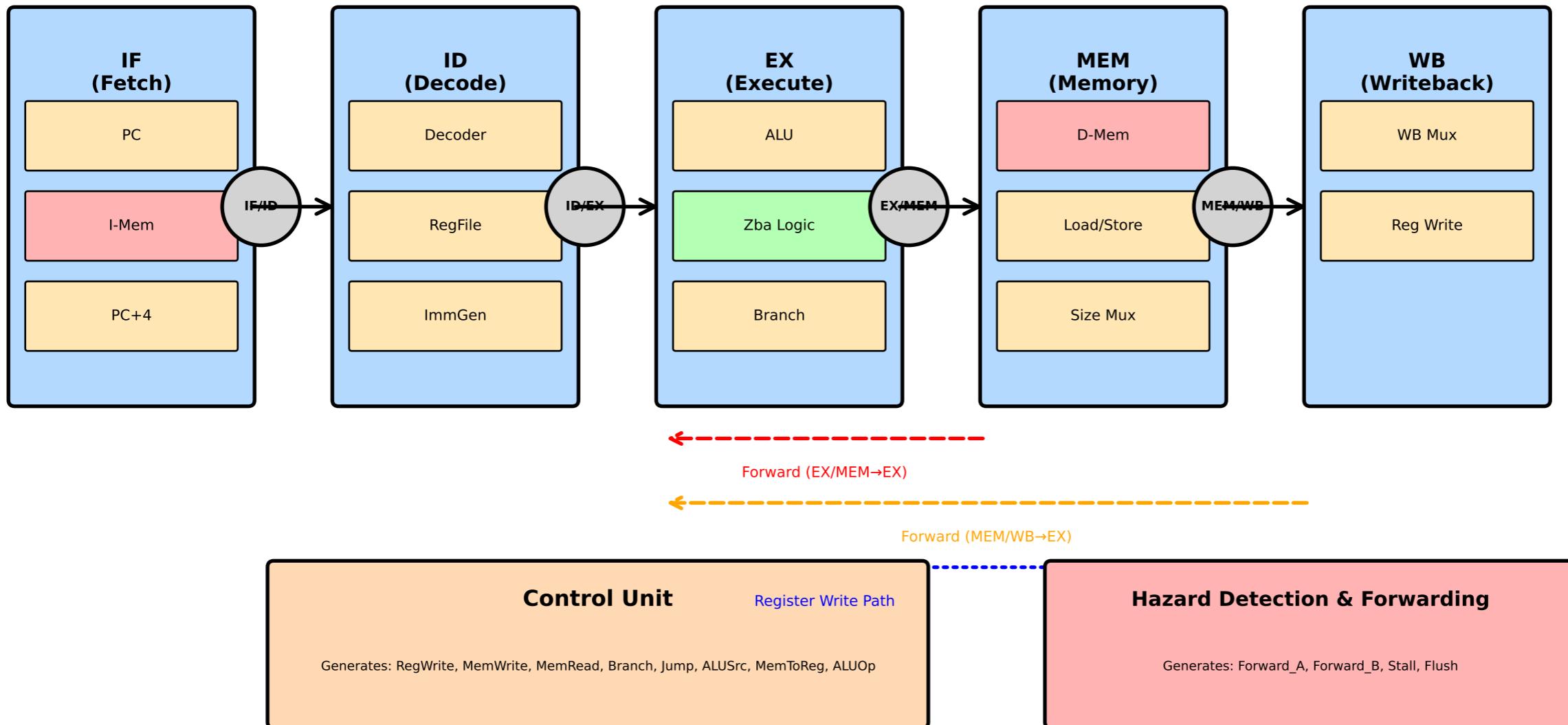


RISC-V 64I-Zba Processor Architecture

5-Stage Pipelined Implementation



Memory Interfaces:

Instruction Memory

Address: 64-bit
Data: 32-bit (read-only)

Data Memory

Address: 64-bit, Data: 64-bit
Size: B/H/W/D (read/write)

Zba Extension Instructions

```

SH1ADD: rd = (rs1 << 1) + rs2
SH2ADD: rd = (rs1 << 2) + rs2
SH3ADD: rd = (rs1 << 3) + rs2
ADD.UW: rd = zext(rs1[31:0]) + rs2

```

Features: Data Forwarding, Load-Use Stall, Branch Flush

Performance: ~1.2-1.5 CPI | 32 x 64-bit Registers | 4KB I-Mem + 4KB D-Mem

ISA: RISC-V RV64I Base + Zba (Address Generation) Extension