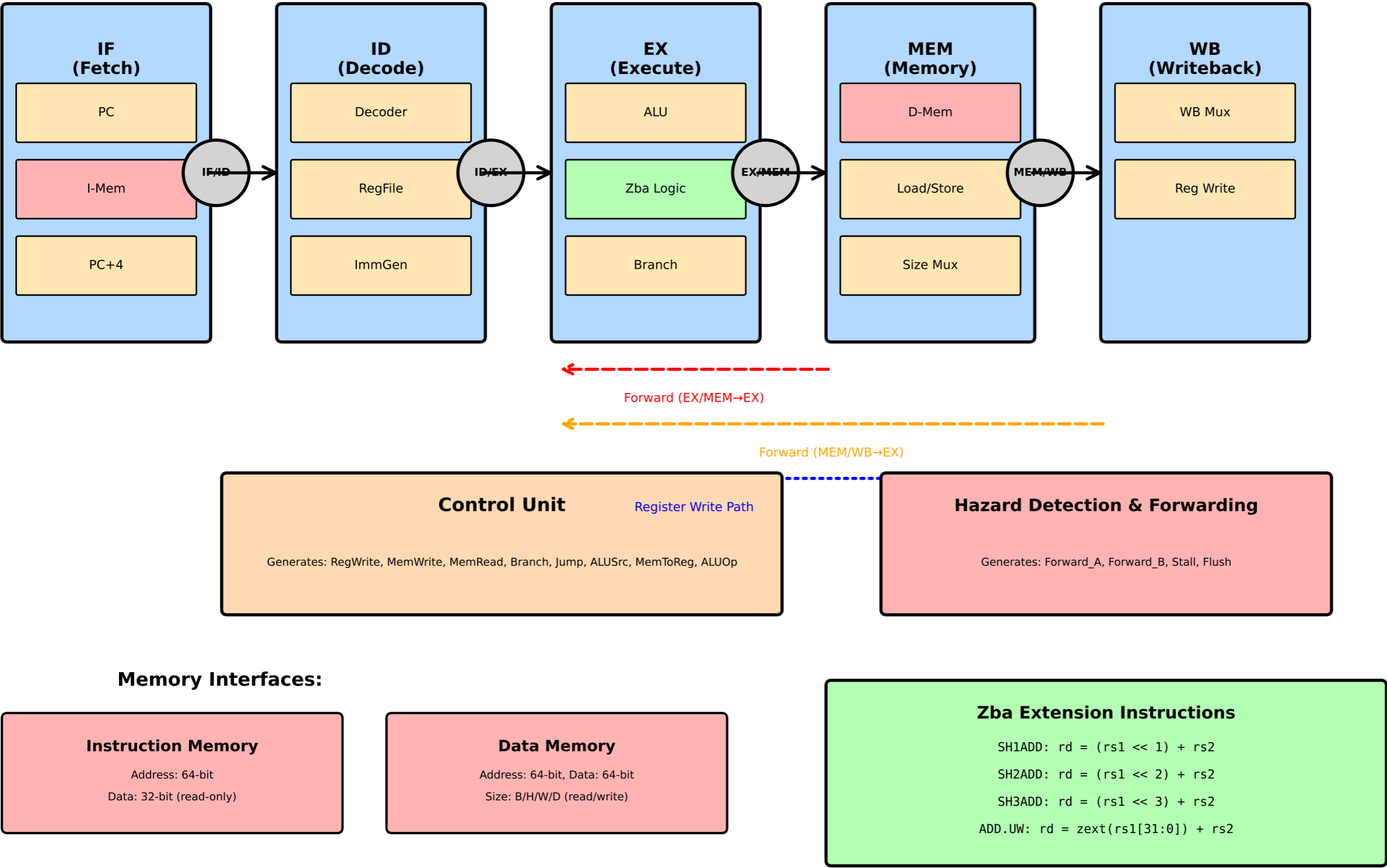


RISC-V 64I-Zba Processor Architecture

5-Stage Pipelined Implementation



Features: Data Forwarding, Load-Use Stall, Branch Flush

Performance: ~1.2-1.5 CPI | 32 x 64-bit Registers | 4KB I-Mem + 4KB D-Mem

ISA: RISC-V RV64I Base + Zba (Address Generation) Extension