EN4430 Analog IC Design

Assignment 01

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Due Date: 07 March 2025

This report is submitted as the fulfillment of Assignment 01 of Module EN4430

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1 Introduction

The operational transconductance amplifier (OTA) is a fundamental building block in analog integrated circuit design. This report presents the design, analysis, and simulation of both single-stage and two-stage OTAs. The single-stage OTA is based on a differential amplifier configuration, utilizing a current mirror biasing scheme and an active load. The two-stage OTA incorporates three current mirrors to enhance gain and output swing, building on the single-stage design. The design methodology, comprehensive calculations, device sizing, and simulation results are detailed to evaluate the performance of both configurations against specified requirements.

2 OTA Design Methodology

2.1 Circuit Architecture

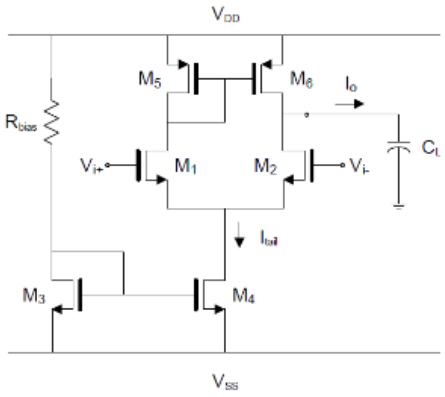

Figure 1: Single-Stage OTA Circuit

The single-stage OTA, as shown in Figure 1, is a differential amplifier featuring a differential pair (M_1, M_2) biased by an NMOS current mirror (M_3, M_4). A PMOS current mirror (M_5, M_6) serves as the active load, enhancing gain through high output impedance. This configuration amplifies the differential input (V_{i+}, V_{i-}) to produce an output current (I_o), with the tail current (I_{bias}) ensuring stable operation.

2.2 Performance Specifications

2.3 Design Assumptions

- ICMR$^-$: 0.5 V (minimum V_{CM} to keep NMOS and tail in saturation).
- ICMR$^+$: 0.9 V (maximum V_{CM} before PMOS or output limits are exceeded).

Table 1: Desired Project Performance Specifications

Parameter	**Project Specification**
Technology [Min. length of transistors (L_{min})]	45 nm CMOS
Supply voltage V_{DD}	1 V
GND	0 V
Output load capacitance C_L	2 pF
Nominal input common-mode voltage $V_{DD}/2$	0.5 V
Reference current I_{REF}	2 μA (adjust as needed)
Overall DC power consumption P_{total}	$\leq$ 1000 μW
Open-loop low-frequency (DC) gain A_{DC}	$\geq$ 100 (40 dB) (maximize)
Unity gain frequency f_U	$\geq$ 20 MHz (maximize)
Phase Margin PM	$>$ 45°
Slew rate (open-loop and closed-loop) SR	$>$ 10 V/μs

2.4 Transistor Parameter Extraction

Transistor parameters were extracted from Cadence simulation with a channel length $L = 1\,\mu$m (to minimize channel length modulation) and width $W = 10\,\mu$m for both NMOS and PMOS transistors. The supply voltage is $V_{DD} = 1\,$V, and the bias current is $I_o = 10\,\mu$A.

2.4.1 NMOS Parameters

- Effective Beta ($\beta_{eff,NMOS}$): $3.40095\,$mA/V^2 (approximated as $3\,$mA/V^2)
- Threshold Voltage ($V_{th,NMOS}$): $397.501\,$mV (approximated as $0.4\,$V)

2.4.2 PMOS Parameters

- Effective Beta ($\beta_{eff,PMOS}$): $2.86778\,$mA/V^2 (approximated as $3\,$mA/V^2)
- Threshold Voltage ($V_{th,PMOS}$): $-334.416\,$mV (approximated as $-0.3\,$V)

2.5 Process Transconductance Parameter Calculation

The effective beta (β_{eff}) is related to the process transconductance parameter μC_{ox} by:

$$\beta_{eff} = \mu C_{ox} \frac{W}{L}$$

where $W = 10\,\mu$m, $L = 1\,\mu$m, and $\frac{W}{L} = 10$.

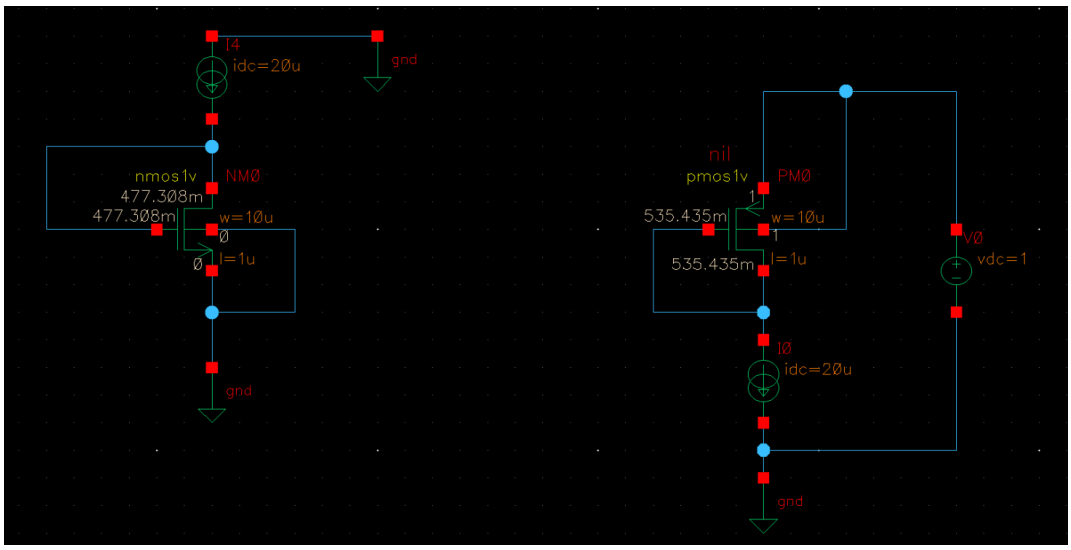

Figure 2: NMOS and PMOS Parameter Analysis Using Cadence

2.5.1 NMOS $\mu_n C_{ox}$ Calculation

$$\begin{aligned}
\beta_{eff,NMOS} &\approx 3\,\text{mA/V}^2 \\
\mu_n C_{ox} &= \frac{\beta_{eff,NMOS}}{\frac{W}{L}} \\
\mu_n C_{ox} &= \frac{3\,\text{mA/V}^2}{10} \\
\mu_n C_{ox} &= 0.3\,\text{mA/V}^2
\end{aligned}$$

2.5.2 PMOS $\mu_p C_{ox}$ Calculation

$$\begin{aligned}
\beta_{eff,PMOS} &\approx 3\,\text{mA/V}^2 \\
\mu_p C_{ox} &= \frac{\beta_{eff,PMOS}}{\frac{W}{L}} \\
\mu_p C_{ox} &= \frac{3\,\text{mA/V}^2}{10} \\
\mu_p C_{ox} &= 0.3\,\text{mA/V}^2
\end{aligned}$$

2.6 Device Sizing Calculations

All MOSFETs are assumed to operate in the saturation region. The following calculations determine the device sizes based on performance specifications.

2.6.1 Output Current (I_o) for Slew Rate

The slew rate (SR) is defined as the maximum rate of change of output voltage:

$$SR = \frac{I_o}{C_L}$$

where $SR > 10\,\text{V}/\mu\text{s}$ and $C_L = 2\,\text{pF}$. Solving for I_o:

$$I_o = SR \cdot C_L$$

Substituting $SR = 10 \times 10^6\,\text{V/s}$ (since $1\,\mu\text{s} = 10^{-6}\,\text{s}$) and $C_L = 2 \times 10^{-12}\,\text{F}$:

$$I_o = 10 \times 10^6 \cdot 2 \times 10^{-12} = 20 \times 10^{-6}\,\text{A} = 20\,\mu\text{A}$$

2.6.2 W/L Ratio for M_5 and M_6 (ICMR$^+$ Constraint)

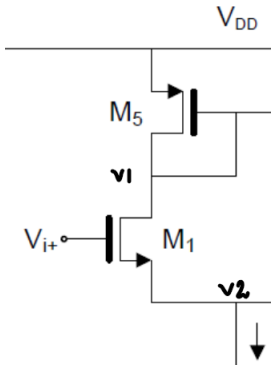

Figure 3: (ICMR$^+$ Constraint) Analysis

The drain-source voltage must satisfy the saturation condition(M1):

$$V_{DS} \geq V_{GS} - V_{th}$$

For ICMR$^+$ = 0.9 V, the voltage at node V_1 must be:

$$V_1 \geq V_{in} - V_{th}$$

Substituting $V_{in} = 0.9\,\text{V}$ and $V_{th} \approx 0.4\,\text{V}$:

$$V_1 \geq 0.9 - 0.4 = 0.5\,\text{V}$$

Thus, $V_1 = 0.5\,\text{V}$. The drain-source voltage is:

$$V_{DS} = V_{DD} - V_1 = 1 - 0.5 = 0.5\,\text{V}$$

Assuming $I_o = 10\,\mu\text{A}$ (half of the tail current for symmetry), the drain current is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

Rearranging for $\frac{W}{L}$:

$$\frac{W}{L} = \frac{2I_D}{\mu_n C_{ox}(V_{GS} - V_{th})^2}$$

Substituting $I_D = 10 \times 10^{-6}\,\text{A}$, $\mu_n C_{ox} = 0.3 \times 10^{-3}\,\text{A/V}^2$, and $V_{GS} - V_{th} = 0.5 - 0.3 = 0.2\,\text{V}$ (adjusting for $V_{GS} \approx V_1$):

$$\frac{W}{L} = \frac{2 \cdot 10 \times 10^{-6}}{0.3 \times 10^{-3} \cdot (0.2)^2} = \frac{20 \times 10^{-6}}{0.3 \times 10^{-3} \cdot 0.04} = \frac{20 \times 10^{-6}}{12 \times 10^{-6}} \approx 1.67 \approx 2$$

Choosing $L = 0.1\,\mu\text{m}$, $W = 0.2\,\mu\text{m}$.

2.6.3 Transconductance ($g_{m1,2}$) Calculation

- **Open-Loop Gain Derivation** for OTA The open-loop gain A_0 of the OTA is defined as the ratio of the output voltage to the input voltage:

$$A_0 = \frac{V_{out}}{V_{in}}$$

This can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{(r_{op} \| r_{on}) \cdot g_{m,n} \Delta V_{in}}{\Delta V_{in}}$$

Since ΔV_{in} cancels out, the gain simplifies to:

$$A_0 = (r_{op} \| r_{on}) \cdot g_{m,n}$$

where:

  - r_{op}: Output resistance of the M6 (PMOS transistor),
  - r_{on}: Output resistance of the M2 (NMOS transistor),

- **Gain-Bandwidth Product (GB)** Derivation The Gain-Bandwidth Product (GB) is defined as the product of the DC gain A_0 and the unity-gain bandwidth f_{GB}:

$$GB = A_0 \cdot f_{GB}$$

The unity-gain bandwidth f_{GB} for the OTA can be approximated as:

$$f_{GB} = \frac{1}{(r_{op} \| r_{on}) \cdot 2\pi C_L}$$

where:

- $g_{m1,2}$: Transconductance of the input NMOS transistor (M1, M2),
- C_L: Load capacitance at the output node.

The GB product becomes:

$$GB = [(r_{op} \| r_{on}) \cdot g_{m1,2}] \cdot \frac{1}{(r_{op} \| r_{on}) \cdot 2\pi C_L}$$

Simplifying, the GB can be expressed as:

$$GB = \frac{g_{m1,2}}{2\pi C_L}$$

Substituting $GB = 20 \times 10^6$ Hz and $C_L = 2 \times 10^{-12}$ F:

$$g_{m1,2} = 20 \times 10^6 \cdot 2\pi \cdot 2 \times 10^{-12} = 80\pi \times 10^{-6} \approx 251.33 \times 10^{-6}\,\text{S} = 251.33\,\mu\text{S}$$

2.6.4 W/L Ratio for M_1 and M_2

The drain current I_D for a MOSFET in saturation is given by:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

The transconductance g_m is the derivative of I_D with respect to V_{GS}:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox}\frac{W}{L}(V_{GS} - V_t)$$

Squaring both sides and relating to I_D:

$$g_m^2 = 2\mu C_{ox}\frac{W}{L}I_D$$

Rearranging for $\frac{W}{L}$:

$$\frac{W}{L} = \frac{g_m^2}{2\mu C_{ox} I_D}$$

Substituting $g_{m1,2} = 251.33 \times 10^{-6}\,\text{S}$, $\mu C_{ox} = 0.3 \times 10^{-3}\,\text{A/V}^2$, and $I_D = 10 \times 10^{-6}\,\text{A}$:

$$\frac{W}{L} = \frac{(251.33 \times 10^{-6})^2}{2 \cdot 0.3 \times 10^{-3} \cdot 10 \times 10^{-6}} = \frac{63.147 \times 10^{-12}}{6 \times 10^{-9}} \approx 10.52$$

To satisfy $ICMR^- \geq 0.5\,\text{V}$, a W/L ratio of 20 is chosen. Choosing $L = 0.1\,\mu\text{m}$, $W = 2\,\mu\text{m}$.

2.6.5 V_{GS} for M_1

The drain current is:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Rearranging for $V_{GS} - V_{TH}$:

$$(V_{GS} - V_{TH})^2 = \frac{2I_D}{\mu C_{ox}\frac{W}{L}}$$

Substituting $I_D = 10 \times 10^{-6}\,\text{A}$, $\mu C_{ox} = 0.3 \times 10^{-3}\,\text{A/V}^2$, and $\frac{W}{L} = 20$:

$$(V_{GS} - V_{TH})^2 = \frac{2 \cdot 10 \times 10^{-6}}{0.3 \times 10^{-3} \cdot 20} = \frac{20 \times 10^{-6}}{6 \times 10^{-3}} \approx 3.333 \times 10^{-3}\,\text{V}^2$$

$$V_{GS} - V_{TH} = \sqrt{3.333 \times 10^{-3}} \approx 0.0577\,\text{V}$$

$$V_{GS} = 0.4 + 0.0577 \approx 0.4577\,\text{V} \approx 0.46\,\text{V}$$

2.6.6 W/L Ratio for M_3 and M_4

The condition $V_{IN} > V_{GS}+V_{DSAT}$ must be satisfied, where $V_{IN} = ICMR^- = 0.5\,\text{V}$, $V_{GS} \approx 0.46\,\text{V}$, and $V_{DSAT} \leq 0.04\,\text{V}$.

$$\frac{W}{L} = \frac{2I_D}{\mu C_{ox} V_{DSAT}^2}$$

Substituting $I_D = 20 \times 10^{-6}\,\text{A}$, $\mu C_{ox} = 0.3 \times 10^{-3}\,\text{A/V}^2$, and $V_{DSAT} = 0.04\,\text{V}$:

$$\frac{W}{L} = \frac{2 \cdot 20 \times 10^{-6}}{0.3 \times 10^{-3} \cdot (0.04)^2} = \frac{40 \times 10^{-6}}{0.3 \times 10^{-3} \cdot 0.0016} = \frac{40 \times 10^{-6}}{4.8 \times 10^{-7}} \approx 83.33 \approx 84$$

Choosing $L = 0.1\,\mu\text{m}$, $W = 8.4\,\mu\text{m}$.

2.6.7 Summary of Calculated Values

Table 2: Summary of Calculated Values

Parameter	**Symbol**	**Approximated W/L**	**Chosen W/L**	**Unit**
Chosen Channel Length	L	-	0.1	μm
W/L Ratio for M_1, M_2	$\frac{W}{L}_{M1,M2}$	10.52	20	-
W/L Ratio for M_3, M_4	$\frac{W}{L}_{M3,M4}$	83.33	84	-
W/L Ratio for M_5, M_6	$\frac{W}{L}_{M5,M6}$	1.67	2	-
Output Current	I_o	-	20	μA
Transconductance	$g_{m1,2}$	-	251.33	μS
Gate-Source Voltage for M_1	V_{GS}	-	0.46	V
NMOS μC_{ox}	$\mu_n C_{ox}$	-	0.3	mA/V^2
PMOS μC_{ox}	$\mu_p C_{ox}$	-	0.3	mA/V^2
NMOS Threshold Voltage	$V_{th,NMOS}$	-	0.4	V
PMOS Threshold Voltage	$V_{th,PMOS}$	-	-0.3	V

3 Simulation Results

3.1 Open Loop OTA (Without Feedback)

3.1.1 Transient Analysis Setup

Table 3: Transient Analysis Parameters

Variable	Symbol	Value
Vin+ Delay Time	$vinp\_delay$	1 μs
Vin+ Zero Value	$vinp\_zero$	1 V
Vin+ One Value	$vinp\_one$	0 V
Vin+ Period of Waveform	$vinp\_period$	10 μs
Vin+ Rise Time	$vinp\_rise$	50 ns
Vin+ Fall Time	$vinp\_fall$	50 ns
Vin- Delay Time	$vinn\_delay$	1 μs
Vin- Zero Value	$vinn\_zero$	0 V
Vin- One Value	$vinn\_one$	1 V
Vin- Period of Waveform	$vinn\_period$	10 μs
Vin- Rise Time	$vinn\_rise$	50 ns
Vin- Fall Time	$vinn\_fall$	50 ns

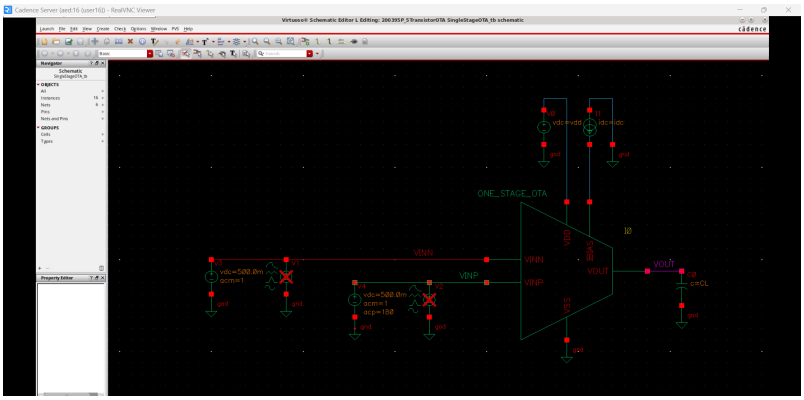

Figure 4: Single Stage - Open Loop OTA (without feedback) Testbench

3.1.2 Slew Rate Analysis

The slew rate (SR) is calculated based on the rising edge, representing the maximum rate of change of the output voltage (V_{OUT}):

$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

From the transient response, V_{OUT} transitions from 100 mV to 900 mV over 11.0399 μs to 11.161 μs:

$$SR = \frac{900 \times 10^{-3} - 100 \times 10^{-3}}{11.161 \times 10^{-6} - 11.0399 \times 10^{-6}} = \frac{800 \times 10^{-3}}{0.1211 \times 10^{-6}}$$

$$SR \approx 6.6061\,\text{V}/\mu\text{s}$$

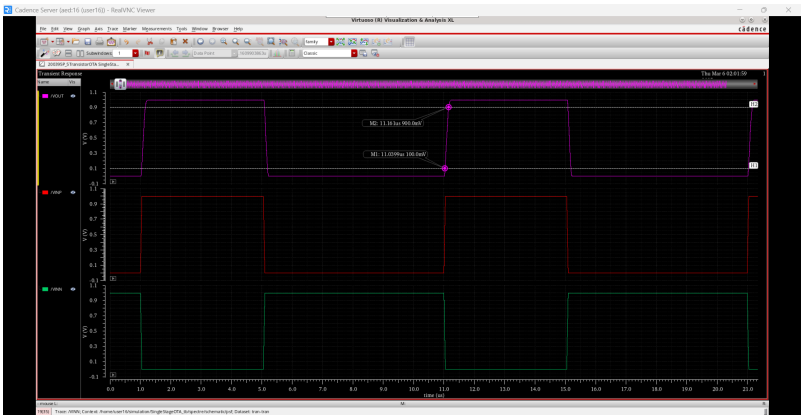

Figure 5: Single Stage - Slew Rate Visualization(Transient Response) for Open Loop Case

3.1.3 AC Analysis Setup

For the AC analysis, a 500 mV DC voltage with a 1 V AC signal, incorporating two signals with 0° and 180° phase shifts, was applied.

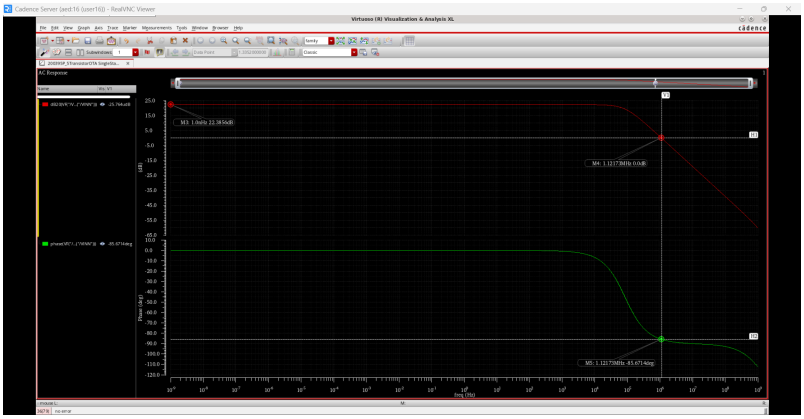

Figure 6: Single Stage - AC Response for Open Loop Case

3.1.4 AC Analysis Results

The AC analysis results are derived from the frequency response plot:

- **DC Gain**: Approximately 22.3856 dB at 1 nHz, below the specification of $\geq 40\,\text{dB}$.
- **Unity Gain Bandwidth (UGBW)**: Approximately 1.12173 MHz, below the specification of $\geq 20\,\text{MHz}$.
- **Phase Margin (PM)**: At 1.12173 MHz, the phase is -85.6714°, giving:

$$\text{PM} = 180^\circ - 85.6714^\circ \approx 94.3286^\circ$$

  This exceeds the specification of $> 45^\circ$.

Table 4: Comparison of Open Loop Results with Design Specifications

Parameter	Design Specification	Obtained Value	Unit
Open-loop DC Gain	$\geq 100\,(40\,\text{dB})$	22.3856 dB	dB
Unity Gain Frequency	$\geq 20\,\text{MHz}$	1.12173 MHz	MHz
Phase Margin	$> 45^\circ$	94.3286°	°
Slew Rate	$> 10\,\text{V}/\mu\text{s}$	6.6061 V/μs	V/μs

3.2 Closed Loop OTA (With Unity Gain Feedback)

3.2.1 Transient Analysis Setup

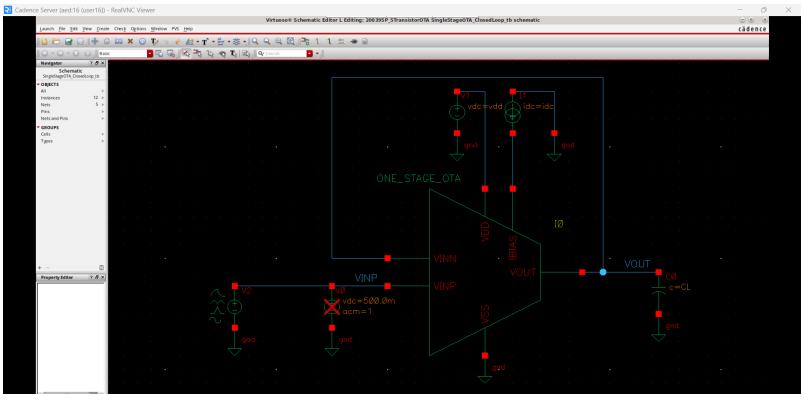

Figure 7: Single Stage - Closed Loop OTA (with unity gain feedback) Testbench

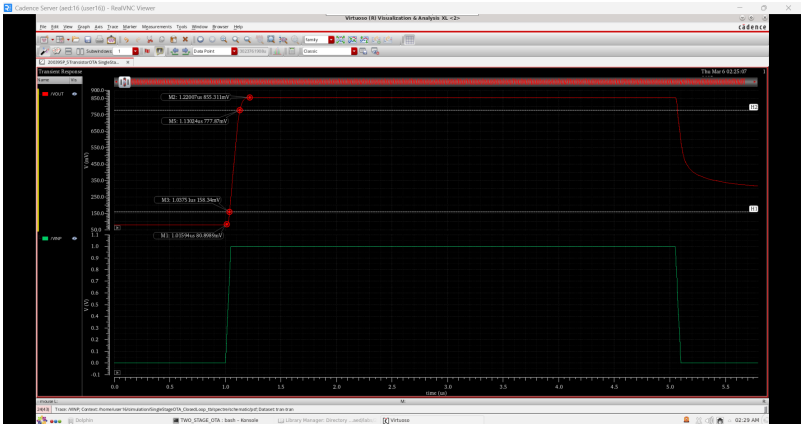

Figure 8: Single Stage - Transient Response(Slew Rate Analysis) for Closed Loop Case

Table 5: Transient Analysis Parameters

Variable	**Symbol**	**Value**
Vin+ Delay Time	$vinp\_delay$	1 μs
Vin+ Zero Value	$vinp\_zero$	1 V
Vin+ One Value	$vinp\_one$	0 V
Vin+ Period of Waveform	$vinp\_period$	10 μs
Vin+ Rise Time	$vinp\_rise$	50 ns
Vin+ Fall Time	$vinp\_fall$	50 ns

3.2.2 Pulse Input Configuration

The transient response is driven by a pulse input with the following parameters:

$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

From the transient response, V_{OUT} transitions from 158.34011 mV to 777.86979 mV over 1.0375 μs to 1.1302 μs:

$$SR = \frac{777.86979 \times 10^{-3} - 158.34011 \times 10^{-3}}{1.13024 \times 10^{-6} - 1.0375 \times 10^{-6}} = \frac{619.52968 \times 10^{-3}}{0.09274 \times 10^{-6}}$$

$$SR \approx 6.6803\,\text{V}/\mu\text{s}$$

3.2.3 AC Analysis Setup

For the AC analysis, a 500 mV DC voltage with a 1 V AC signal was applied to the $VINP$ terminal.

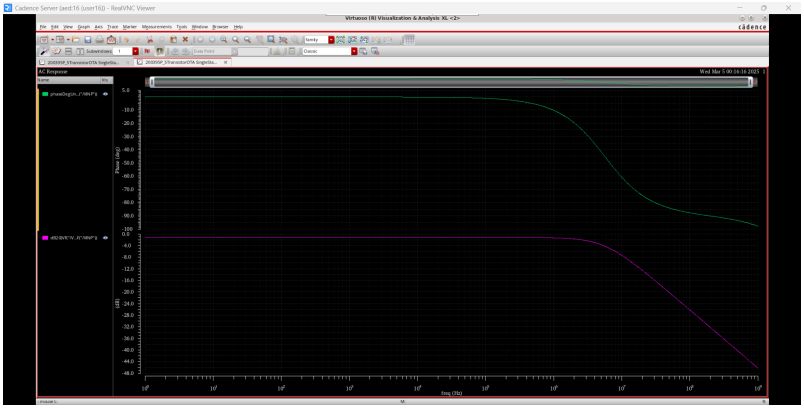

Figure 9: Single Stage - AC Response for Closed Loop Case

4 Two Stage OTA

4.1 Introduction to Two-Stage OTA Design

An enhancement to the differential amplifier involves the incorporation of self-biased loads. This configuration is referred to as a two-stage single-ended symmetric OTA, commonly known as a three current-mirror OTA. The input stage comprises a differential pair, while the sub-circuits consisting of M_1, M_3 and M_2, M_4 function as self-biased inverters. The transistors M_3, M_5, M_4, M_6, M_7, M_8, and M_9, M_{10} are configured as simple current mirrors. In the design of this symmetric OTA, the transistors are symmetrically matched such that $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$, and $M_7 = M_8$. This symmetry reduces the number of adjustable parameters to four transistor sizes and the tail current, simplifying the design process while maintaining balanced performance.

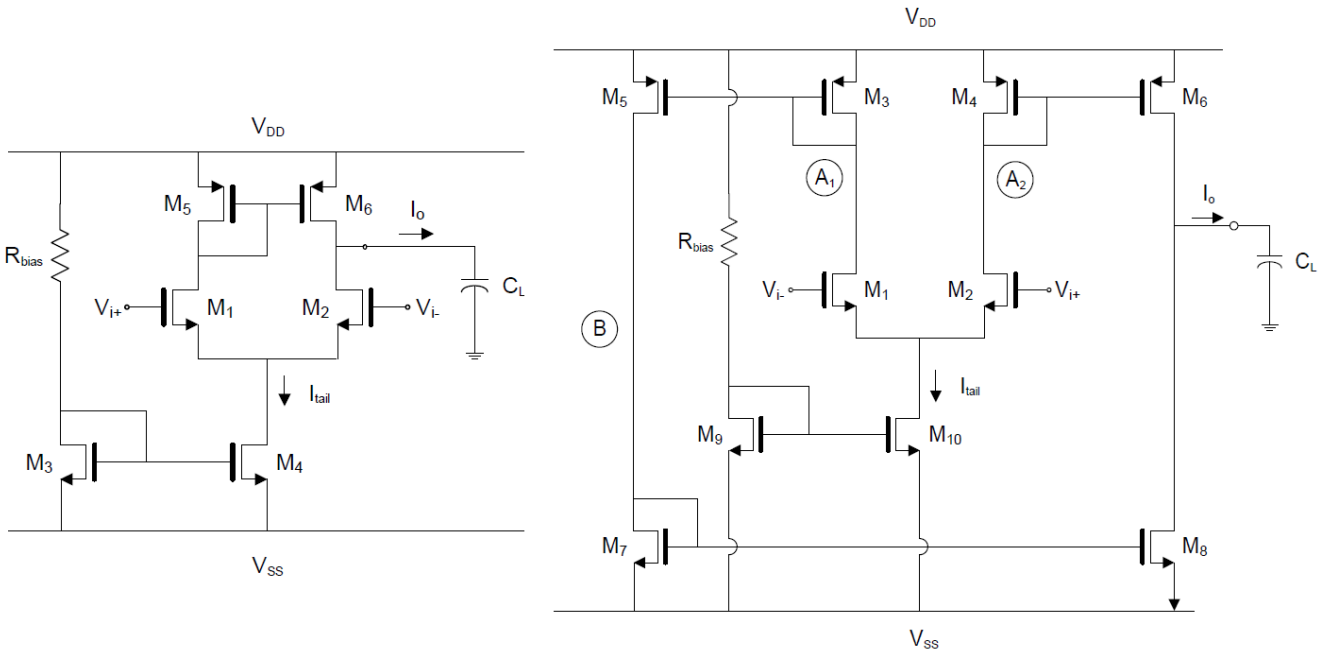

Figure 10: Single Stage And Two Stage OTAs

4.2 Device Sizing Calculations

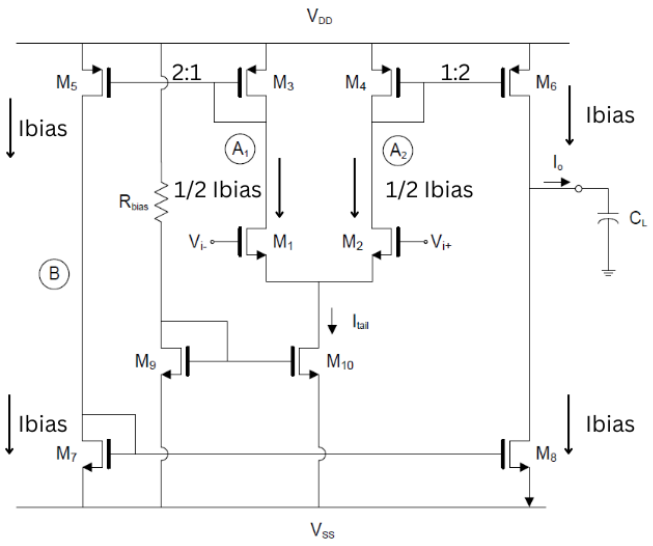

Figure 11: Two-stage single-ended symmetric OTA (Three current-mirror OTA)

4.3 Transition from Single-Stage to Two-Stage OTA Design

Having completed the calculations for the single-stage OTA, the next step involves determining the W/L ratios for the two-stage single-ended symmetric OTA. To facilitate this transition, mappings from the single-stage to the two-stage design can be established based on the previously calculated ratios. Specifically, the W/L ratio of 20, determined for M_1 and M_2 in the single-stage OTA, can be directly applied to M_1 and M_2 in the two-stage configuration, maintaining the input differential pair symmetry. Similarly, the W/L ratio of 2, originally calculated for M_5 and M_6 (related to M_3 and M_4 in the single-stage design), can be adopted for M_3 and M_4 in the two-stage OTA. For M_9 and M_{10}, which correspond to M_3 and M_4 in the single-stage case, the W/L ratio of 84 can be applied.

Further, considering the current distribution across each branch, the W/L ratios for the remaining MOSFETs can be derived. For instance, the W/L ratio for M_5 and M_6 can be set to twice that of M_3 and M_4, yielding $2 \times 2 = 4$. Likewise, the W/L ratio of 84, can be retained for M_7 and M_8 in the two-stage configuration, ensuring consistency in the current mirror design.

4.3.1 Summary of Calculated W/L Values

Notes: The W/L ratios are derived by mapping from the single-stage OTA design, with widths calculated using $L = 0.12\,\mu$m. The W/L ratio for M_5, M_6 is set to twice that of M_3, M_4 (i.e., $2 \times 2 = 4$), while M_7, M_8 and M_9, M_{10} retain the $W/L = 84$ from the single-stage M_3, M_4.

Table 6: Summary of W/L Ratios for Two-Stage OTA

Transistor Pair	W/L **Ratio**	**Width** (W)	**Unit**
M_1, M_2 (Differential Pair)	20	2.4	μm
M_3, M_4 (Self-Biased Inverters)	2	0.24	μm
M_5, M_6 (Current Mirror)	4	0.48	μm
M_7, M_8 (Current Mirror)	84	10	μm
M_9, M_{10} (Current Mirror)	84	10	μm

Parameter	**Value**
Channel Length (L)	120 nm (0.12 μm)
Bias Current (I_o)	20 μA
Load Capacitance (C_L)	2 pF

4.4 Simulation Results

4.4.1 Open Loop Case (Without Feedback)

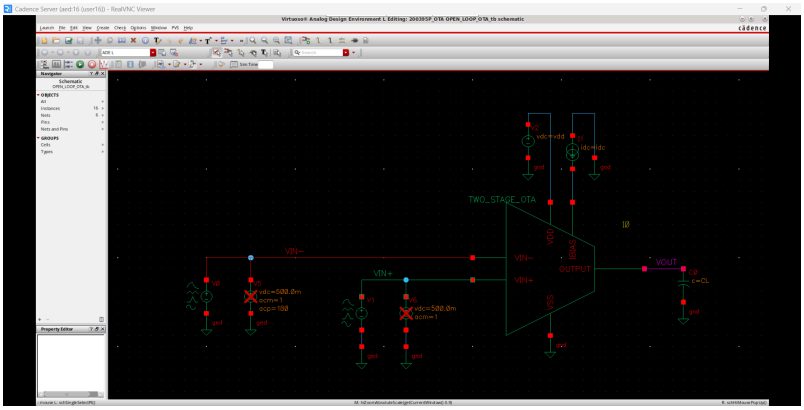

Figure 12: Two Stage Stage - Open Loop OTA (without feedback) Testbench

- **Transient analysis**

Table 7: Transient Analysis Parameters

Variable	Symbol	Value
Vin+ Delay Time	$vinp\_delay$	1 μs
Vin+ Zero Value	$vinp\_zero$	1 V
Vin+ One Value	$vinp\_one$	0 V
Vin+ Period of Waveform	$vinp\_period$	10 μs
Vin+ Rise Time	$vinp\_rise$	50 ns
Vin+ Fall Time	$vinp\_fall$	50 ns
Vin- Delay Time	$vinn\_delay$	1 μs
Vin- Zero Value	$vinn\_zero$	0 V
Vin- One Value	$vinn\_one$	1 V
Vin- Period of Waveform	$vinn\_period$	10 μs
Vin- Rise Time	$vinn\_rise$	50 ns
Vin- Fall Time	$vinn\_fall$	50 ns

- **Slew Rate Analysis**

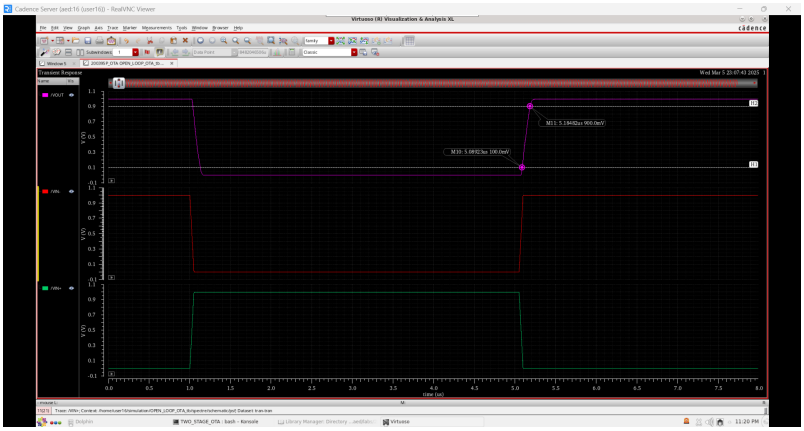

Figure 13: Two Stage Stage - Slew Rate Visualization For Open Loop Case

$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

From the transient response, V_{OUT} transitions from 100 mV to 900 mV over 5.08923 μs to 5.18482 μs:

$$SR = \frac{900 \times 10^{-3} - 100 \times 10^{-3}}{5.18482 \times 10^{-6} - 5.08923 \times 10^{-6}} = \frac{800 \times 10^{-3}}{0.09559 \times 10^{-6}}$$

$$SR \approx 8.3691\,\text{V}/\mu\text{s}$$

- **AC Analysis**

  For AC analysis, I provided the parameters as 1 V AC magnitude, 0.5 V DC common-mode voltage, and 0° and 180° phase shift two signals for Vin+ and Vin-.

Figure 14: Two Stage Stage - AC Response For Open Loop Case

  - **DC Gain**: Approximately 21.1052 dB at 1 nHz, below the specification of ≥ 40 dB.
  - **Unity Gain Bandwidth (UGBW)**: Approximately 10.2355 MHz, below the specification of ≥ 20 MHz.
  - **Phase Margin (PM)**: At 10.2355 MHz, the phase is $94.6495°$, giving:

$$\text{PM} = 180° - 94.6495° \approx 85.3505°$$

Table 8: Comparison of Open Loop Results with Design Specifications

Parameter	Design Specification	Obtained Value	Unit
Open-loop DC Gain	$\geq 100\,(40\,\text{dB})$	21.1052 dB	dB
Unity Gain Frequency	≥ 20 MHz	10.2355 MHz	kHz
Phase Margin	$> 45°$	85.3505°	°
Slew Rate	$> 10\,\text{V}/\mu\text{s}$	8.3691 V/μs	V/μs

4.4.2 Closed Loop Case (With Unity Feedback)

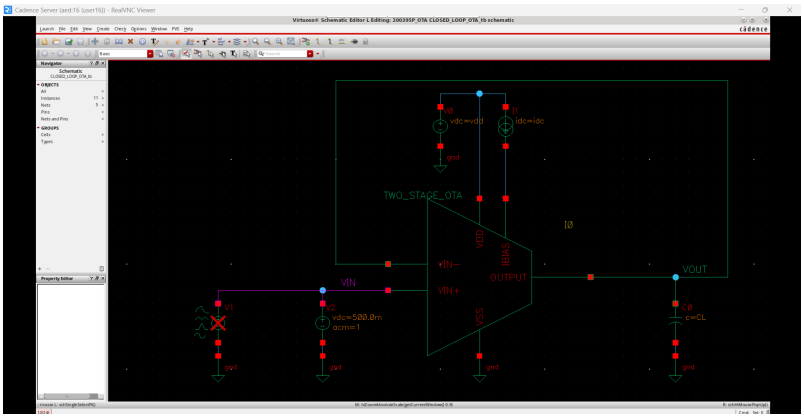

Figure 15: Two Stage Stage - Closed Loop OTA (with unity gain feedback) Testbench

- **Slew Rate Analysis (For Transient Response)**

Table 9: Transient Analysis Parameters

Variable	Symbol	Value
Vin+ Delay Time	$vinp\_delay$	1 μs
Vin+ Zero Value	$vinp\_zero$	1 V
Vin+ One Value	$vinp\_one$	0 V
Vin+ Period of Waveform	$vinp\_period$	10 μs
Vin+ Rise Time	$vinp\_rise$	50 ns
Vin+ Fall Time	$vinp\_fall$	50 ns

$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

From the transient response, V_{OUT} transitions from 275.849 mV to 809.658 mV over 14.5777 μs to 14.6207 μs:

$$SR = \frac{809.658 \times 10^{-3} - 275.849 \times 10^{-3}}{14.6207 \times 10^{-6} - 14.5777 \times 10^{-6}} = \frac{533.809 \times 10^{-3}}{0.043 \times 10^{-6}}$$

$$SR \approx 12.4142\,\text{V}/\mu\text{s}$$

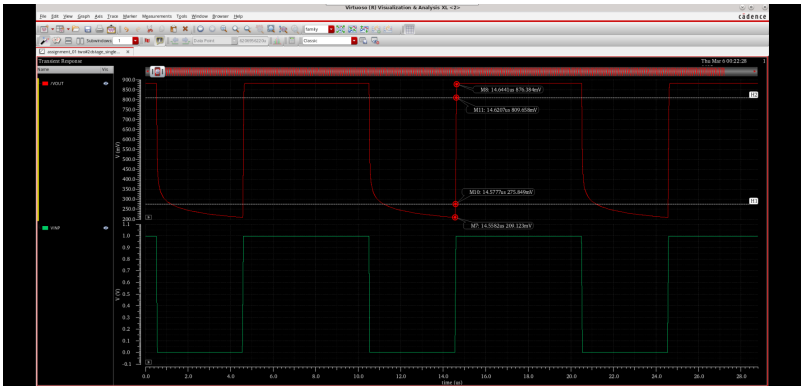

Figure 16: Two Stage Stage - Slew Rate Visualization For Closed Loop Case

- **AC Analysis**
  For AC analysis in a closed-loop configuration, the Vin+ terminal signal is defined with a 1 V AC magnitude and 0.5 V DC common-mode voltage. The Vin- terminal is connected to the output.

Figure 17: Two Stage Stage - AC Response For Closed Loop Case

A Single-Stage OTA Circuit Netlist

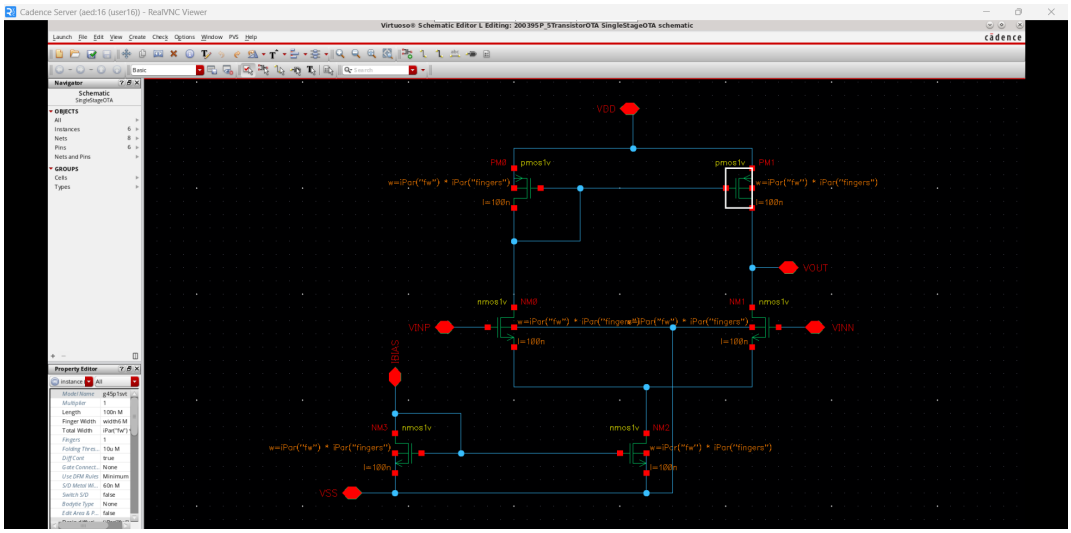

Figure 18: Single-Stage OTA Circuit Netlist

B Two-Stage OTA Circuit Netlist

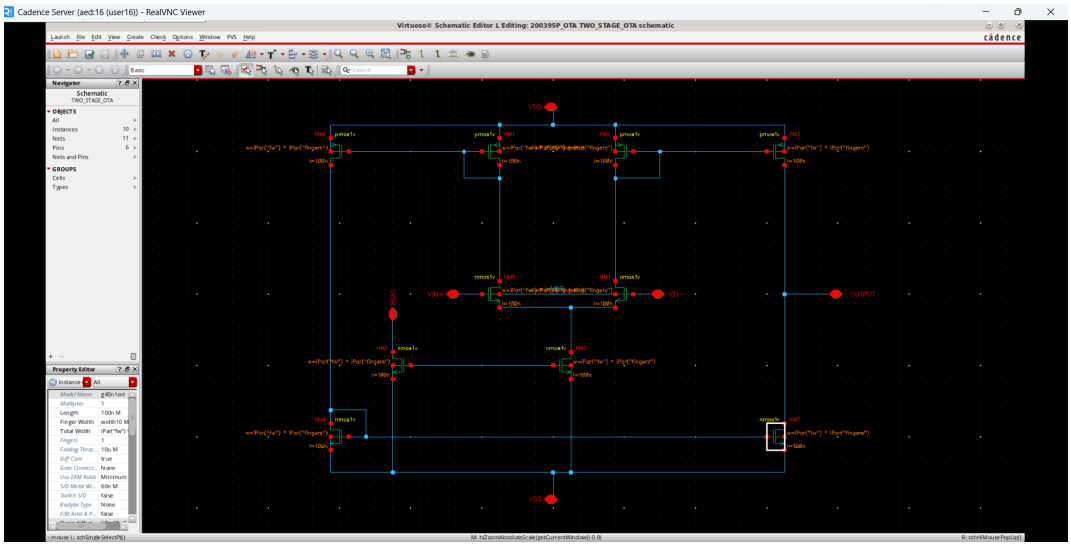

Figure 19: Two-Stage OTA Circuit Netlist