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ORIGINAL CONTRIBUTION

Design & Implementation of High Speed and Low Power PLL Using GPDK 45 nm Technology

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Abstract With progress in the design of phase locked loop (PLL) circuit, critical parameters like, power dissipation, phase noise, and area, has had to be considered within the analysis. The key aspect of effective PLL design is the lock-in time, which presents a major challenge in the PLL usage in high-speed communication systems. As the PLLs are gradually being used for synchronization, clock synthesis, and reducing the jitter in wireless communications, due to increment in the circuit operation rate, there is an immediate need to design PLL circuits with fast locking capacity. In this article, an efficient PLL, employing current starved voltage controlled oscillator is designed to maintain linearity of its gain, using the Cadence Virtuoso tool, which is then simulated using the Spectre tool. Since the PLLs are extensively implemented over high frequency ranges due to incurring less time to lock frequency, the designed PLL's lock time is set to 300 ns. Further, the designed PLL features a 3.09–3.2 GHz tuning range, a 5.2 GHz central frequency, small phase noise of − 71.51 dBc/Hz at 1000 kHz, along with 264 ps jitter. In addition, the proposed PLL dissipates a power of 50.8 µW, for 1 V supply. Extensive simulation results demonstrate that the proposed sub module architecture of the proposed PLL system performs better compared to the existing designs with respect to power consumption, operating frequency, phase noise, and jitter.

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Introduction

For the current and future communication systems, the key factors include power, cost, wide frequency range [1]. The PLL applications outline the basic modules of any communication on system chip. As shown in Fig. 1, PLL is a feedback system, utilizes the phase frequency detector (PFD) and related components to synchronize frequency, phase of an PLL output with input. PLL is used to generate a clock signal, which is generally a multiple of a reference clock, and is synchronized with the reference clock in phase. Both, the PFD and the PLL are essential components of electronic systems implemented for different applications including, communication systems, clock synchronization, frequency synthesis, and data recovery. However, the existing design of PLLs is not popular due to high power dissipation, complex circuit, and large chip area. Authors in [2] designed a high speed and low power PLL that can operate in the 3.5 GHz frequency range with a lock time of 508 ns using the 180 nm technology with a supply of 1.8 V.

The PFD, a sub block of PLL (see Fig. 1), presents a vital part in outlining the handling power of PLL. The PFD's power dissipation must be shrunk to reduce the total power consumption of the PLL. Existing designs include multiple transistors, which lead to the device being larger with higher power consumption [3]. In addition, the PLL's high frequency operation result in increased power consumption due to the circuit is higher switching rate. It shows the existing PFD attains a minimum power i,e 0.138 µW with lower frequency of operation [4]. Further, in [5], the authors discussed about PLL design with all

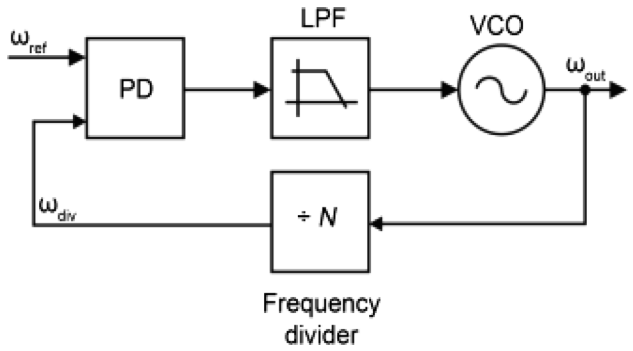

Fig. 1 PLL block diagram

the blocks, using Synopsys Tool with GPDK 90 nm. The proposed work demonstrates that the performance of each block in the PLL obtains power dissipation from 2 µW to 1 mW. Further, the UWB frequency ranges between 3.1 and 10.6 GHz, which has immense possible to be, implemented in the communication systems. Around 1.1 mW of power is consumed by high speed PFD (HSPFD); whereas, for the traditional charge pump with passive filter of 2nd order and VCO are 1235 nW and 0.687 W, respectively. Simultaneously, frequencies of 3.3 GHz and 3.2 GHz is achieved for the proposed design of HSPFD and CP with second order passive filter respectively; whereas, the voltage CRO is operated in the range of 6.5–7.138 GHz.

Authors [6] described the design of an efficient and low power digital PLL (DPLL) using the 45 nm CMOS technology on Cadence Virtuoso tool, consuming 485 mV of power. The proposed DPLL design is used for high speed, less jitter and large bandwidth with extremely fast acquisition time in wired or wireless communication for modulation or demodulation techniques. The PLL is used for recovering and synchronizing the clock, and the DPLL is used to generate the clock signals. The DPLL comprises of a block that detects phase of signals, a filter allowing low frequency signals, along with VCO, which generates oscillations at a frequency of 8500 MHz. The DPLL's average power dissipation is found to be 485 mW with a supply of 2 V. The results imply that the designed DPLL can be implemented for low power and high-speed applications. Authors in [7] presented the design of a PLL-based clock synthesizer used in reconfigurable converters (analog to digital converter) which is designed using Taiwan Semiconductor Manufacturing Company's 65 nm process technology, and the results are obtained from layout view with parasitic i.e., resistance, inductance, capacitance (RLC). The synthesizer produces clock frequencies ranging from 40 to 0.230 GHz with a $freq_{ref}$ of 0.01 GHz with 1.2 V input voltage. A 634 µA of current is consumed with a settling time of approximately 6 µs, with extreme jitter of 1300 ps in an area of 37 nm^2.

In [8], the authors focused on PLL system design in the Cadence Virtuoso tool using 180 nm process technology. A single-ended VCO is chosen due to enhanced performance such as, miniature chip size, low power dissipation, and high range frequency. Simulations are conducted using the Spectre simulator tool, and the proposed PLL design demonstrated an output frequency of 7200 MHz, with dissipating 3090 µW of power. Though the output frequency produced is high, the proposed design dissipates large amount of power. Hence, the proposed design is not preferable for high speed PLL. The authors in [9] implemented the infeasibility driven evolutionary algorithm (IDEA) to determine the passive components of low pass filter and device aspect ratios, which affect lock in time, phase noise in conjunction with power dissipation considering reasonable constraints. Considering channel length and MOSFET's width as key design parameters, the model is legitimate by PLL simulation. The results show that the PLL demonstrates random fluctuations in phase of − 126.3 dBc/Hz at KHz frequency offset, average dissipation of µW of power, and lock time of 50 ns. In addition, it is seen that the PLL locks early with higher power dissipation.

From the above recent studies, it can be inferred that high power dissipation occurs if the aim is to operate at higher output frequency. In addition, existing designs encounter high phase noise, which reduces the signal quality and occupies larger area. As a solution, we propose a PLL design using the 45 nm generic process development kit (GPDK) with minimum number of transistors consuming lesser area and ensuring low power dissipation by eliminating the reset path. Specifically, we propose a low-power PFD with high-speed using the modified gate diffusion input (MGDI) and pass transistor logic (PTL) designing logic. The PFD compares phase relationship between a reference signal and a feedback signal, and then generates the output signals, which indicate phase difference. These output signals are then used to adjust the frequency or phase of the feedback signal to achieve synchronization with the reference signal. Proposed PLL is divided into sub-blocks before combining them to form a high-speed PLL. The PLL sub-blocks are designed in the schematic editor, and the characteristics verification for the specifications is then adjusted. The proposed PLL is of second-order operating at 200 kHz loop bandwidth, and 1 V of supply to enable the operation of the CS-VCO. The novelty of the proposed PLL is that it obtains an output frequency of approximately 3.2 GHz with minimal power consumption. Key contributions of this study are as follows:

1. Power dissipation of the proposed PFD is reduced as compared to the existing studies by removing the reset path.

2. Speed of the proposed PFD is also improved by reducing the clock skew using true single phase clock (TSPC) and widening the acquisition range.
3. VCOs oscillation frequency is improved by increasing the number of stages compromising the circuit's complexity.
4. PLL's overall phase noise and jitter is improved considerably by using TSPC logic.

It must be noted that, in the current work, the dead-zone-free dual-edge triggered D flip-flop is assumed for the PFD architecture. It is also assumed that the design of CP consumes a power of 79.069 mW [4]. In addition, the CS-VCO is designed at an operating frequency of 10 MHz with control voltage of 1 V, which provides an output oscillation frequency of 1.119 GHz and a total power of 18.91 µW lastly, it must be noted that the power consumption will be higher as the output frequency increases.

The structure of remaining article is as mentioned below: Section "Proposed PLL Design" details with related sub-blocks. Section "Simulation Results" presents and discusses the simulation results of each sub-block, and compares the proposed design with recent existing studies. Finally, Section "Conclusion" concludes the study.

Proposed PLL Design

The PFD of a PLL system performs the comparator function and increases the PLL's speed by widening the acquisition range. The most common PFD design, despite using more power, comprises of two D flip flops and a logic gate [10]. Over the years, changes have occurred to eliminate the reset path in order to reduce the power dissipation. With the consideration that high power consumption and a low operating frequency are the major issues, in the current study, a novel PFD is proposed (shown in Fig. 2) which comprises of 10 NMOS transistors and 7 PMOS transistors. In the proposed design, reduced number of transistors is required as compared to the previous designs; hence, the power dissipation is minimized.

The starting state of the proposed PFD is based on low voltage level of both the PFD inputs i.e., feedback_clk and reference_clk. The output node *A* turns HIGH when the P1 and P2 transistors are turned ON. The pass transistor logic used by node *A* to link to the nodes N3 and N5 causes both, nodes *A* and *B* to enter a LOW logic state. An upward signal (UP) rises as a result of the N3 switching node *A* to a HIGH logic level when the refClk input has a rising edge. The downward signal (DOWN) rises when the feedback_Clk input has a rising edge since N5 causes node *B* to change to a HIGH logic level. If both, nodes *A* and *B* go HIGH, N4 and N6 transistors pull them back down quickly. As a result,

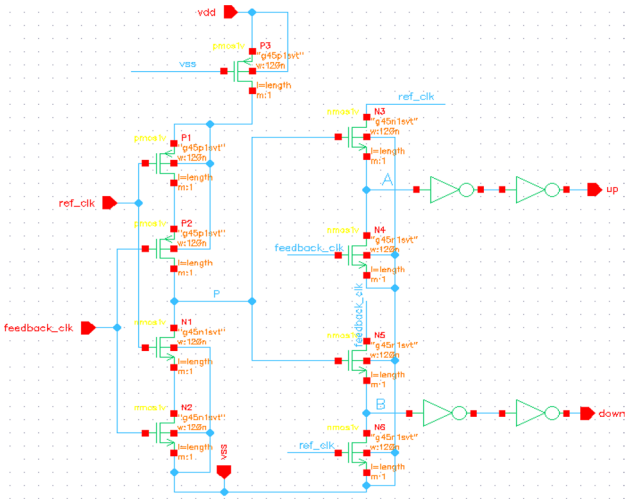

Fig. 2 Proposed PFD schematic

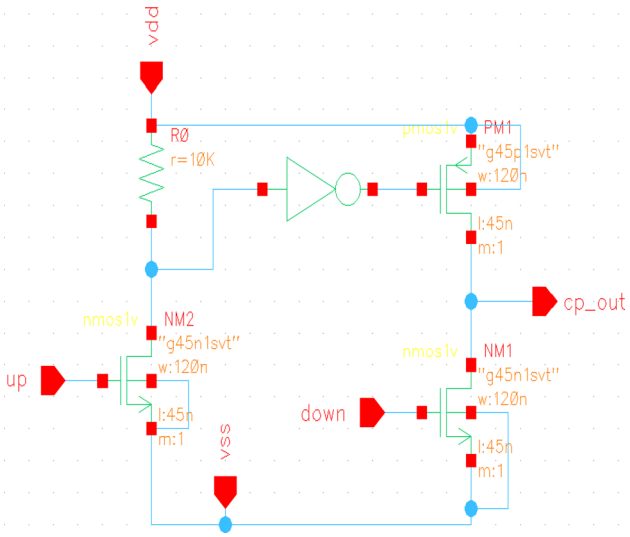

Fig. 3 Charge pump schematic

the reset circuit is removed using the pass transistors. To ensure complete swing output and eliminate the glitches, the inverter stages are cascaded soon before the UP and DOWN output signals. This circuit requires 17 transistors resulting in smaller area.

Charge Pump

The schematic for a CP with a loop filter is depicted in Fig. 3. The CP changes the difference in phase (error signal) to the current signal, when it serves as a bipolar switched current source in the PLL [11]. Hence, CP generates source, sink current pulses in proportion to difference in frequency, and phase difference amid the feedback and reference signal. The

loop filter is driven by the current pulses, which produces varied control voltage and, consequently, varies the PLL output frequency [12]. The CP acts as current sourcing or sinking device in harmony to the voltage applied. Tristate CPs, often considered as single-ended CPs, is mostly used owing to their small power necessities, flexibility, and reduced chip size, with pads, and peripheral components [13]. A CP circuit transforms the logic state of PFD to analog signal, which is then used by the VCO to modify the frequency. It is positioned between the VCO and the PFD block and connected to the loop filter.

In Fig. 3, two PFD outputs i.e., UP and DOWN, are applied to the CP, which then produces one output to be sent to the loop filter. Charging occurs when the CP's current flows across it, and enters the loop filter, which follows when the DOWN signal would be LOW and HIGH for UP signal [14]. On the other hand, discharge occurs when CP current leaves the loop filter, if the DOWN signal reaches high and the UP signal becomes LOW. In general, output of the CP is independent of the strength of the UP and DOWN input signals.

Schematic of CS-VCO

The VCO is an essential block as its performance controls multiple performance parameters of the PLL system. An input voltage produces the oscillating frequency. In VCO, the number of stages implemented can alter its output frequency. Further, VCO's oscillation frequency can be improved by increasing number of stages, in turn improve the phase noise as it is filtered at every stage. In fact, with greater number of stages '*N*', circuit complexity increases which increases the power dissipation. The VCO's input signal can alter the oscillation frequency of VCO, which is given as

$$\mathrm{Freq}_{\mathrm{osc}} = \frac{1}{NxC_{\mathrm{Total}}xV_{\mathrm{DD}}} \tag{1}$$

From Eq. (1), N denotes No. of stages, C_{Total} as total capacitance, and V_{DD} as supply voltage.

Figure 4 shows the schematic diagram of a CS based VCO, which performs the role of a ring oscillator, and is frequently used due to its wide frequency range and low power [15]. The top and bottom current sources (i.e., PM20 and NM11) reduce the amount of current available to the inverter, causing it to be current starved. The transistors in the center (i.e., PM8 and NM16) create an inverter. Further, PM25 and NM18 drain currents are identical, which are controlled through the control voltage V_{ctrl}. Mirrored currents delivered to all inverter step respectively. Specifically, the current is reflected to PM25 via the current mirror method as the V_{ctrl} varies in the primary current starving structure.

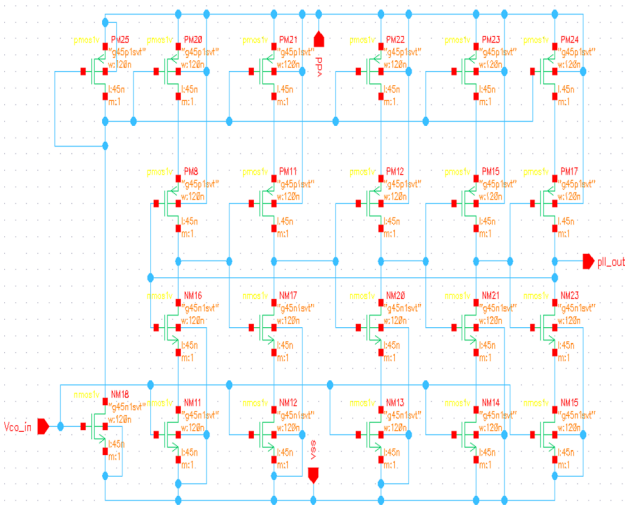

Fig. 4 Schematic of CS-VCO

The current is reflected from the PM25 transistor to all pull-up PMOS transistors. Drawback of the CS-VCO is that it consumes large amount of power, which necessitates the deployment of alternate circuit viz., the stacked sleep circuit that significantly reduces the power.

Schematic of Frequency Divider

The output of VCO is provided as input to the frequency divider, where the frequency is divided by two, in turn, its output will act as input to PFD. Then the reference signal is compared with this feedback signal, when both signals have same phase and same frequency, PLL arrives to lock mode and the output frequency will be double of the input frequency [16].

The signal generated by a VCO circuit, its frequency changes with the input voltage. An error signal is produced by the PFD when it compares phases of the two signals. By producing a signal with half frequency as that of the number of pulses counted, a counter circuit generates and counts the number of pulses in a signal. Two D flip-flops are used to create a counter circuit, as shown in Fig. 5. When clock signal changes, a D flip-flop circuit switches its output while keeping one bit of data.

Schematic of PLL

For evaluating the proposed PFD's effect on PLL performance, a PLL loop is used, as shown in Fig. 6, which implements a second order CP PLL. The four component of the PLL are the loop filter, VCO, PFD, and CP. The PFD generates and transmits the UP and DN signals to the charge pump, which then converts pulse width modulated signal into voltage or current. The loop filter combines this voltage

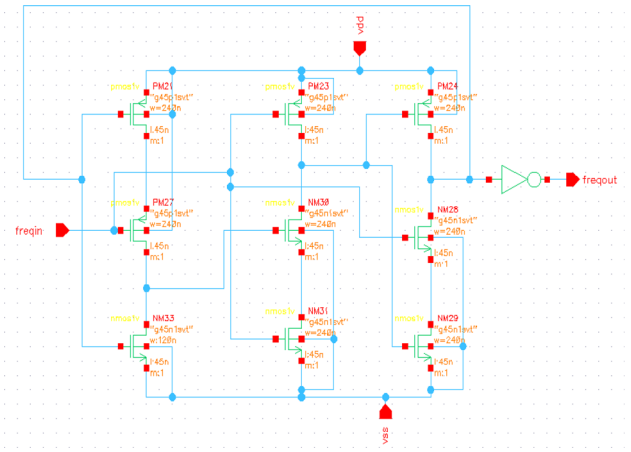

Fig. 5 Schematic of freq. divider

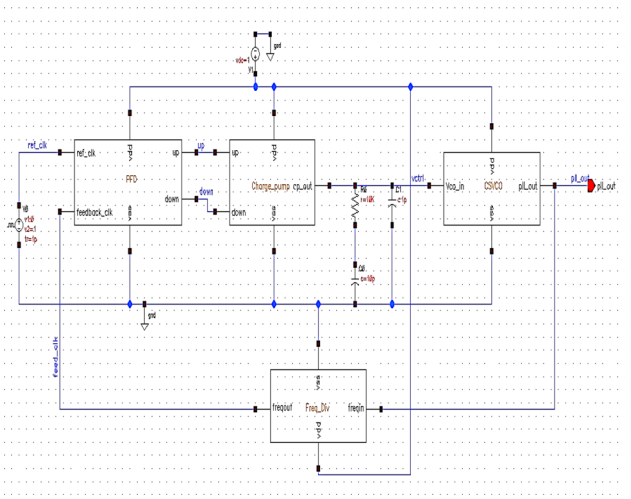

Fig. 6 Schematic of phase locked loop

and current to produce the control voltage. A VCO will produce a signal with high frequency, which is locked with reference to refclk in terms of phase, frequency, once it receives the control voltage.

Simulation Results

To conduct the simulations for evaluating performance of the proposed PLL design, schematic of all the blocks are created using 45 nm GPDK in Cadence Virtuoso software. The Spectre tool is used for simulation. Further, the analog design environment (ADE) tool is used to set the configuration for transient and direct current analysis. The static and dynamic power analysis is conducted using the same tool, which also provisions the evaluation and analysis of the output waveform. The discussion on the results obtained through each sub module of the proposed PLL is explained in the following sub sections.

Trans Analysis of PFD

Transient analyzes will analyze the circuits over a period of time, which changes from one steady state condition to another. This investigation reveals the manner in which voltage and current change throughout the transient period. Specifically, transient analysis is performed to understand the behavior of PFD during the transient duration, and to ensure that the circuit sustains these variations in current and voltage [10]. Since the PFD requires two input signals, i,e reference and feedback signal, PFD's function is to analyze both the phase and frequency of feedback signal and reference signals over the transient time. Due to the variation of both signals in terms of frequency and phase, reference signal may lead feedback signal or vice-versa, and will reach a stage where the phase will match. Following are the multiple cases analyze the PFD output.

Case 1: when refclk and feedclk are in same phase: in this case, there is no output signal spike since reference clock) and feedback clock are in phase. Subsequently, both the signals, UP and DOWN shoots up for a very short span of time on each rising edge, as shown in Fig. 7.

Case 2: when refclk leads feedclk: in this case, rising edge of refclk leads feedclk. During this period, the UP signal becomes high, as depicted in Fig. 8, and CP deliveries a positive polarity current; therefore, the output of VCO will become HIGH.

Case 3: when feedclk leads refclk: in this case, if the input (refclk signal) delays the feedback (feedclk signal), the DOWN signal will become HIGH, as shown in the Fig. 9, it provides negative polarity current; consequently, the output of VCO becomes low.

Next, the corner analysis is carried for designed PFD and is compared with the existing design. Corner analysis is carried out to understand the way in which the circuit

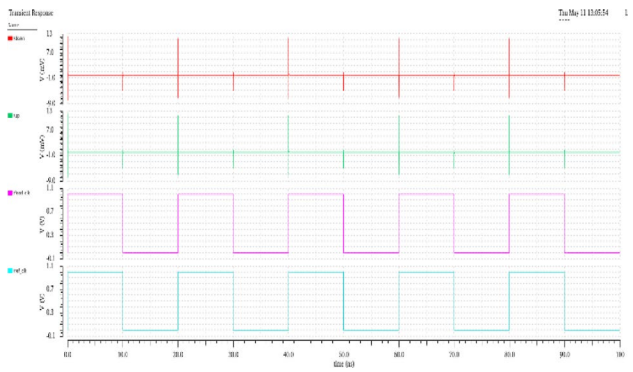

Fig. 7 PFD output representing refclk and feedclk are in same phase

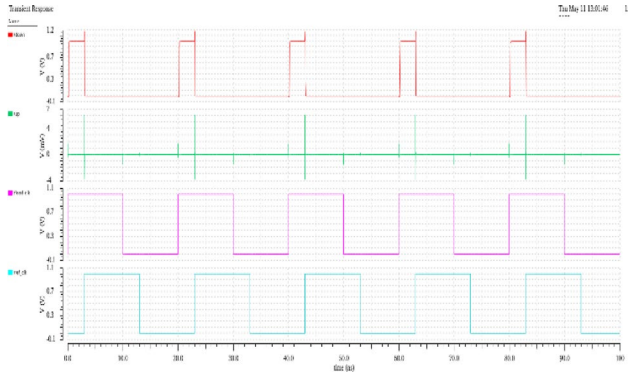

Fig. 8 PFD output representing refclk leading feedback clk

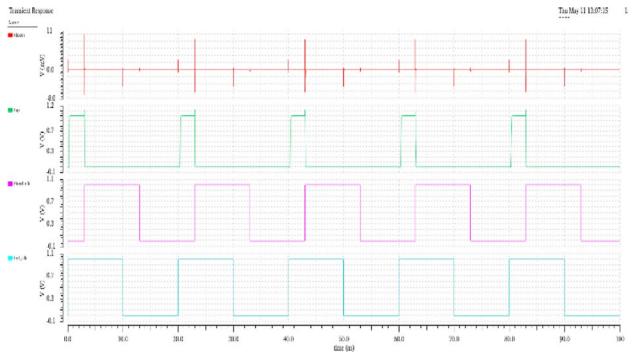

Fig. 9 PFD output representing feedclk leading refclk

acts with the variations in process corners [13]. The analysis for the proposed PFD is executed to simulate all the corner regions such as, fast fast (FF), then slow fast (SF), then slow slow (SS), then fast slow (FS) and, typical typical (TT). The comparison results are shown in Table 1 from which it can be noted that the average power of existing design is 132.96 nW, and the average power of the proposed design is 70.96 nW. This implies that the PFD designed consumes 46.6% lesser power with respect to existing designs. Hence, proposed PFD can be used for low power PLL applications, which are power critical.

As technology advances, it leads to miniaturization of device dimensions'. Therefore, process variation analysis of the circuits is essential. Hence, to confirm the designs

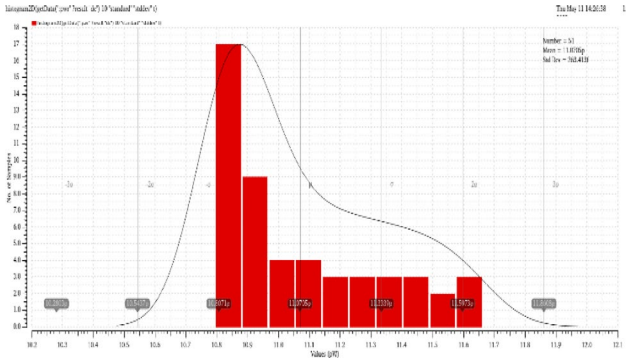

Fig. 10 Result of power distribution of static power dissipation using Monte Carlo simulation

proposed have ability to withstand adverse conditions Monte Carlo simulations are performed. The Monte Carlo analysis, which is a statistical analysis allowing a designer to reflect on the feasible effects of a random variation of certain circuit's parameter over its performance, is performed considering the static and dynamic power of PFD [17]. Specifically, this analysis aids in verification of consistency of the circuit, and simulates the entire corner regions. This analysis is performed by randomly selecting 50 samples, which represents the power distribution of static and dynamic power dissipation of PFD as shown in the Figs. 10 and 11.

The ratio of μ/σ represents the circuit sensitivity to process variation where μ and σ are the mean and standard deviation, respectively. In Figs. 10 and 11, various static power dissipated values have been distributed as shown, which represents minimum values, maximum values and average values, from which the mean and standard deviation is calculated and tabulated in Table 2 From the histogram presented in Figs. 10 and 11, it can be concluded that the static power and dynamic power will not vary in large margin for any process variations for the successive simulations. The mean average of UP–DOWN signal will be constant with the simulated value. Consequently, the performance of PFD will not depend on process variations.

Lastly, the mean and standard deviation is tabulated in Table 2 Again, the simulation is conducted for 50 samples, which represents larger number of runs, and higher

Table 1 Corner analysis comparison between the existing work and proposed work

Power	Process corners									
	Ref [4]					Proposed work				
	TT	FF	FS	SF	SS	TT	FF	FS	SF	SS
P_d (nW)	132	131.1	108.2	184.1	109.9	124	146	127	121.4	102.9
P_s (pW)	28.42	164.5	44.32	30.11	25.7	20.52	10.9	31.2	9.6	3.1
P_t (nW)	132	131.26	108.2	184.13	109.92	124.02	146	127.03	121.40	102.90
Avg (nW)	133.10					124.27				

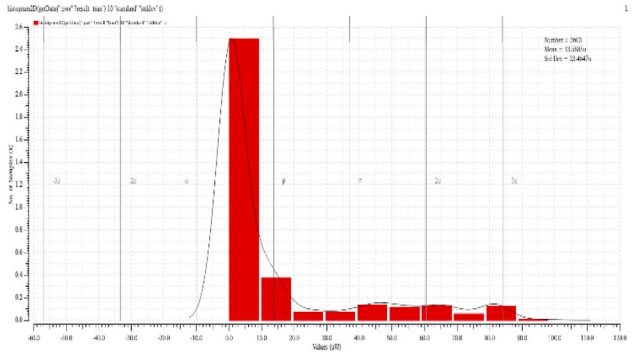

Fig. 11 Result of power distribution of dynamic power dissipation using Monte Carlo simulation

Table 2 Summary of Monte Carlo simulation for PFD

Parameters	Existing		Proposed	
	Mean	SD	Mean	SD
Static power	33.16 pW	9.58 pW	11.07 pW	263.41 fW
Dynamic power	138.2 nW	24.99 nW	13.58 µW	23.46 µW

chances that every component value within its tolerance range will be used for simulation. It can be clearly seen from the table that the mean of power dissipation obtained for the proposed method is lesser than the existing methods.

Trans Analysis of Charge Pump (CP)

Since the PFD's output consists of two signals i.e., UP and DOWN signals, for a period, these are fed as input to CP, and CP produces a single output. In order to find the stability of CP, maintaining constant voltage due to no difference in phase or frequency for a given period, transient analysis is performed [11]. In [18], a CP design is simulated using 180 nm CMOS process, with a supply voltage of 1.8 V and consuming 0.6 mW and 1.2 mW for CP1 and CP2 respectively. A power efficient CP is designed in [11] using the Miller Op-Amp to maintain a gain of 50 dB using the 90 nm GPDK technology and Cadence Virtuoso tool with a 1.2 V supply. This design dissipates a power of 134.6 µW. Further, in [19] a high-speed CP is designed using 65 nm CMOS process technology with 1.2 V supply, dissipating a power of 176 µW.

The output of CP with loop filter analysis is shown in Fig. 12. The CP charges when the UP signal is high and the DOWN signal is LOW, and discharges when the opposite occurs. The output remains constant when both signals are LOW or HIGH. Further, it can be seen that the CP consumes a dynamic power of 50 uW and a static power of 18.5 µW. Hence, the total power consumption is 68.5 µW,

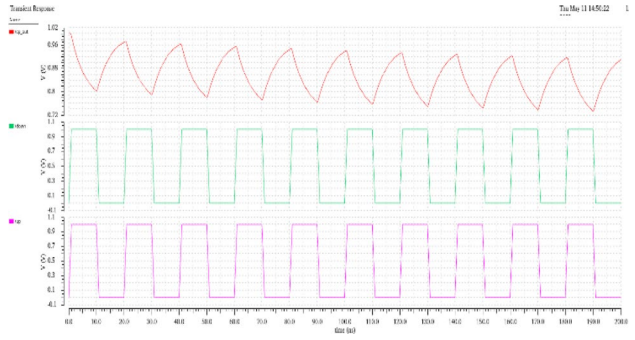

Fig. 12 Trans analysis of CP

which is 13% lesser than existing design, which consumes 79.069 µW. Overall, using the proposed CP design; power consumption is reduced by 13.3% in comparison to the study in [4]. In addition, as shown in Table 3, the proposed CP design requires lesser area, and demonstrates lower power dissipation with reduced supply voltage.

Trans Analysis of CSVCO

The output of CS-VCO is obtained at high frequency; hence, to determine the frequency and oscillation with sufficient accuracy, the transient analysis is performed. A two-stage VCO designed in [20] uses 40 nm CMOS technology with 1.1 V supply. 1.1 mW of power will be dissipated, with an output frequency of MHz is generated. The phase noise at 1 MHz offset is found to be − 98.05 dBc/Hz. However, the major issue of this study is that high power dissipation occurs, and the lock time is high i.e., 6.0 µs. The study in [21] uses 180 nm CMOS process operating at 1.8 V supply, with a reduced lock-time of 2.2 ns. However, the power dissipation is observed as 2.25 mW, which implies that the design may not be considered for low power PLL applications.

From the current study, the transient response of CS-VCO is shown in Fig. 13. The CS-VCO produces an output frequency of 5.2 GHz, and consumes a dynamic and static power of 31.32 µW and of 6.30 µW, respectively, for a supply of 1 V. It must be noted that since the output frequency of the implemented CS-VCO design is almost five times more than the existing studies, power consumption is higher than existing designs. However, in order to obtain high oscillation frequency, at times, power consumption maybe compromised [22]. Further, as the no. of transistors are less in comparison to the existing design, the area occupied is smaller and reduces by 22%. Further, in the periodic steady-state analysis (PSS), the output frequency is 5.2 GHz. In addition, the PSS analysis shows that phase noise and jitter of CS-VCO are 71.5 dBc/Hz and 264 ps, respectively (see Figs. 14 and 15). Lastly, Table 4 shows a comparison of implemented design with existing studies from which it

Table 3 Performance analysis of proposed charge-pump with existing works

Parameters	References				
	[18]	[11]	[19]	[4]	Current study
Technology (nm)	180	90	65	45	45
Voltage (V)	1.8	1.2	1.2	1	1
Total power (μW)	0.2 mW	134.6	176	79.069	68.5
No. of transistors	15	20	39	5	5
Circuit complexity	Complex	Complex	Complex	Simple	Simple

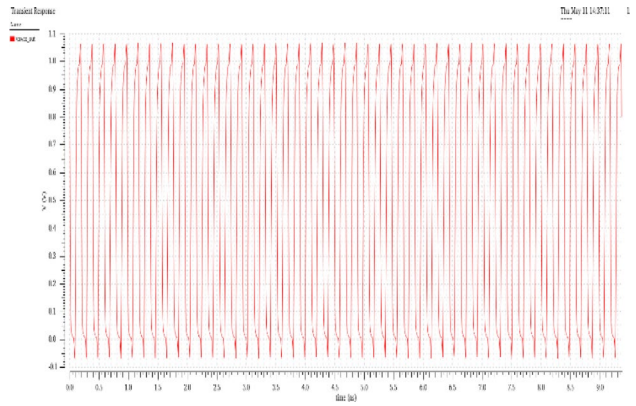

Fig. 13 Trans response of CSVCO

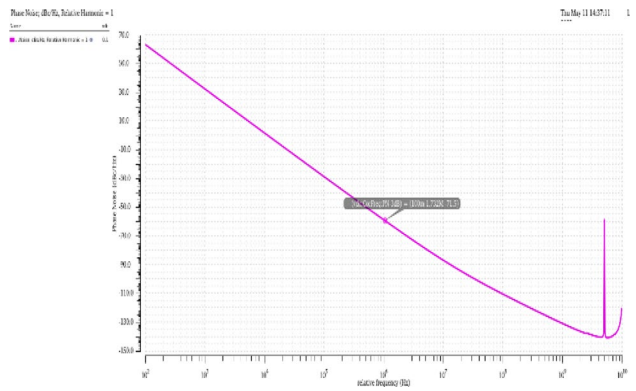

Fig. 14 Phase noise of CSVCO at 1 MHz

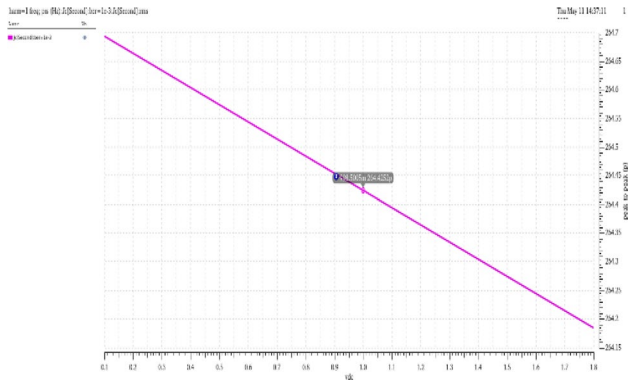

Fig. 15 Waveform of jitter of CSVCO

can be observed that proposed VCO design improves output frequency while reducing phase noise and power dissipation.

Practically, oscillators have variations in the amplitude and frequency. Short-term frequency variability of an oscillator is mainly due to noise, interference sources. Practical noise like thermal, shot and flicker will affect amplitude and frequency, while substrate and supply noise will be due to interferences sources. These sources lead to frequency variations, which are characterized as phase noise [23]. In [4], phase noise is improved in comparison to current study; however, the output frequency is lesser, and the number of transistors used are more and the phase noise is – 71 dBc/Hz, as shown in the Fig. 14. This value can still be improved by reducing random fluctuations in phase (frequency) which is caused due to jitter, as depicted in Fig. 15. Lastly, the oscillation frequency is found to be 5.2 GHz and which uses lesser number of transistors; leading to reduction in the area.

Trans Analysis of Frequency Divider

A frequency divider divides the VCO output signal by N times, and divides the input signal by a factor of two. Accordingly, it can be used as a divide by two counters [24]. The frequency divider [25] of a PLL integrates a phase detector, which samples both, the rising and falling edges of the reference clock. It is designed using 28 nm CMOS technology, which consumes 12 mW of power. In [26], the frequency divider circuit is designed using 180 nm technology in Cadence Virtuoso. The adaptive voltage level source circuit is implemented to reduce the power dissipation of pre-scalar circuits and D flip-flops. The average power dissipation of the design is 0.272 mW whereas, in dual modulus pre-scaler, it dissipates a power of 423.75 μW. The power consumption in [25] and [26] can be reduced further by implementing two D flip-flops in the circuit. In [27], the frequency divider is designed using 90 nm technology, used for implantable medical devices (IMD), which consumes a power of 0.223 mW. Figure 16 represents the transient analysis of frequency divider. Specifically, the power analysis of frequency divider shows

Table 4 Performance comparison between different VCOs

Parameters	[4]	[20]	[21]	Current study
Technology	90	90	180 nm	45 nm
Voltage (V)	1	1	1.8	1
Oscillation frequency (GHz)	1.12	6.7	7	5.2
Total Power (µW)	18.91	89.33	2.25 mW	37.62
Number of transistors	22	–	–	17
Structure	Ring	Ring	–	Ring
Phase noise dBc/Hz	− 126.3	− 114.46	103.2	− 71
Lock time	50 ns	–	2.2 ns	300 ns

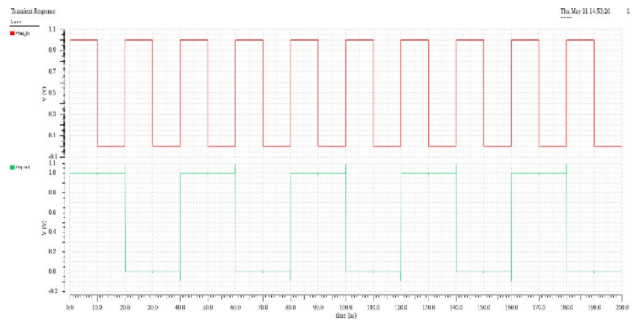

Fig. 16 Trans analysis of frequency divider

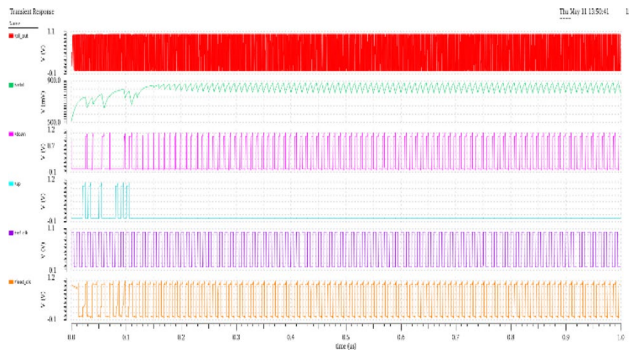

Fig. 17 Trans response of PLL

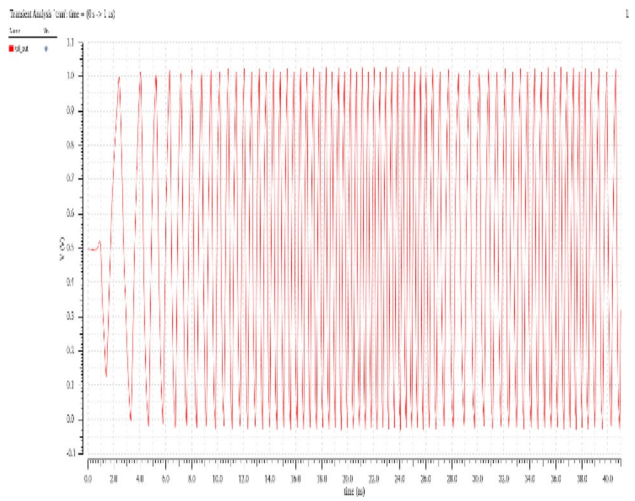

Fig. 18 Output waveform of PLL at input freq. 100 MHz

that the dynamic power and static power consumption is 79.69 µW and 62.4 nW, respectively.

Trans Analysis of PLL

To thoroughly understand the PLL transient behavior, the transient analysis is conducted [28]. A PLL, which is negative feedback system, is difficult to analyze qualitatively, due to the reality that the control variable is altered as it traverses through the loop [29]. The input and the feedback variable is a phase (or a frequency); however, in between these two stages, the variable is voltage amplitude. Hence, in order to track the phase and the frequency, an internal frequency oscillator is used and a transient analysis is conducted [30].

The transient response of PLL is depicted in Fig. 17. The refclk signal is fed as input and output of respective block is UP, DOWN, V_{ctrl} signals, and feedclk respectively, and feedclk signal is fed as input. The PLL output frequency ranges between 3.09 and 3.2 GHz, with an input frequency of 100 MHz, as shown in Fig. 18. Further, dynamic and static power dissipation is found as 46.06 µW and 4.74 µW, respectively. The proposed PLL design is compared with existing designs in terms of multiple key performance parameters. The obtained results are presented in Table 5, which represents proposed design consumes lesser power, and generates high output frequency.

Conclusion

In this article, a PLL system is proposed with sub modules, which are designed, using the Cadence Virtuoso tool and Spectre simulator in 45 nm GPDK technologies. The proposed design performance is analyzed with existing designs considering multiple key parameters. The power dissipation

Table 5 Performance comparison between different PLLs

Parameters	[4]	[5]	[6]	[7]	[8]	[9]	This work
Technology (nm)	45	90	45	65	180	120	45
Supply voltage (V)	1	1	2	1.2	1.8	1.2	1
Fosc (GHz)	1.119	3.1–10.6	8.5	230 MHz	7.2	1.26	5.2
Total power (W)	18.91 µ	2 µ-1 m	485 m	634 µ	3.09 m	1.523 m	50.8 µ

achieved for the proposed PFD is found to be 70.96 nW, and power consumption for the traditional CP of 2nd order passive filter and CS-VCO are observed as 68.5 µW and 37.62 mW, respectively. Further, all the sub blocks are integrated to form a high speed and low power PLL, which results in high frequency generation. The work in this paper improves the performance of each blocks of PLL, and demonstrates a power dissipation of approximately 50.80 mW in the frequency range of 3.09–3.20 GHz. The results make it evident that the proposed design significantly improves the power dissipation, phase noise and output frequency.

As a future scope for research, it is required to improve the phase noise and reduce the PLL's lock-in-time, area and power dissipation.

Author Contributions All authors have contributed equally.

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Data Availability Not applicable.

Code Availability Not applicable.

Declarations

Conflict of interest There are no conflicts of interest.

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