EN4430: Analog IC Design

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Three Current-Mirror OTA simulation to achieve desired specifications

A simple differential amplifier is depicted in Fig. 1 (a). This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror. The NMOS active load version of this circuit can be found in [1], where the systematic design and optimization procedure of this circuit using g_m/I_D design methodology is explained in detail.

An improvement of the differential amplifier in Fig. 1 (a) is to use self-biased loads. This modified circuit in Fig. 1 (b) is called a two-stage single-ended symmetric OTA (also known as three current-mirror OTA). The input stage is a differential pair, the sub-circuits composed of $M_{1,3}$ and $M_{2,4}$ are self-biased inverters, and the transistors $M_{3,5}$, $M_{4,6}$, $M_{7,8}$ and $M_{9,10}$ are simple current mirrors. When designing the symmetrical OTA, transistors $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$ and $M_7 = M_8$. This reduces the number of adjustable parameters to four transistor sizes and the tail current. You can refer to the uploaded lab assignments in the A1 drive folder and to Chapter 6 of [2] and Chapter 9 of [3] for further reading.

The following required design specifications summarized in the Table 1, are provided for this project, with the goal of maximizing the product of the open-loop low-frequency (DC) gain (A_{DC}) and the small-signal unity gain bandwidth (f_U) (i.e, maximize the Gain Bandwidth Product (GBW)).

Table 1: Required Project Performance Specifications

Parameter	**Project Specification**
Technology [Min. length of transistors (L_{min})]	45 nm CMOS
Supply voltage V_{DD}	1 V
GND	0 V
Output load capacitance C_L	20 pF
Nominal input common-mode voltage $V_{DD}/2$	0.5 V
Reference current I_{REF}	2 μA (change accordingly)
Overall DC power consumption P_{total}	$\leq$ 1000 μW
Open-loop low-frequency (DC) gain A_{DC}	$\geq$ 100 (40 dB) (maximize)
Unity gain frequency f_U	$\geq$ 20 MHz (maximize)
Phase Margin PM	$> 45^\circ$
Slew rate (both open-loop and closed-loop) SR	$>$ 10 V/μs

Instructions

Please submit your report (at least 5 pages without appendix) including the following information;

- Design methodology and details of the calculation and device sizes
- Simulation results (AC/Transient Simulations showing DC gain, UGBW, PM, and Slew rate)
- A (table of) comparison between design/simulation results and a brief explanation
- Attach the Circuit netlist in Appendix

For more details, please refer to ECEN 474/704 Lab 7: Operational Transconductance Amplifiers.

Due Date: 7 March 2024 by 11.59 PM

References

[1] M. N. Sabry, H. Omran, and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/id design methodology," *Microelectronics Journal*, vol. 75, pp. 87–96, 2018.

[2] T. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*. Wiley, 2011, vol. 2.

[3] B. Razavi, *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2018, vol. 2.

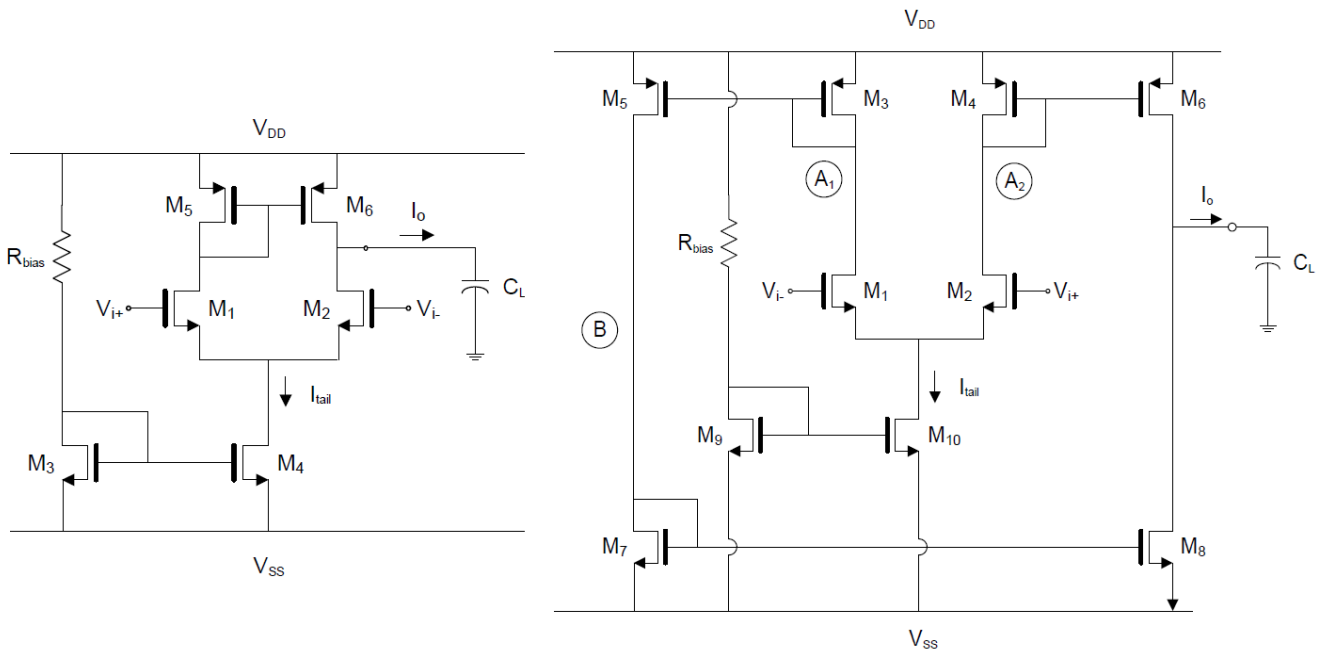

Figure 1: (a) Simple Differential Amplifier used as a single-stage basic OTA (also known as the 5-transistor OTA (b) A two-stage single-ended symmetric OTA (also known as three current-mirror OTA)