EN4430: Analog IC Design

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Index No: XXXXX

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A Type-II PLL-based Clock Multiplier Layout in IHP SG13G2 Process

Group Project

The US CHIPS Act has allocated US$53 billion to this industry, most of which has been earmarked for chip fabrication [1]. The question is, who will design the chips that must fill the capacity of these fabrication lines? There is a shortage of chip design talent in the USA and around the globe who have practical experience in the entire chip design flow [2]. Gaining this experience takes years of training in a chip design lab or industry setting. According to Peter Kinget (Professor of Electrical Engineering, Columbia University, USA), "providing practical experience is crucial in order to teach IC design successfully" [3].

Figure 1 illustrates the development stages that the industry follows for chips of moderate complexity. Beginning with product definition and performance specifications, engineers embark upon the design of the chip and, in about six to nine months, complete the first "draft". The result is in the form of tens or hundreds of "schematics". Next, the chip goes to "layout"; i.e., designers create geometries (mostly squares and rectangles) that must be built on the actual chip. Since layout introduces its own "parasitics," the result may not meet the performance targets, requiring iteration with the design. Anticipating that the package in which the chip will be housed will contribute additional parasitics, we account for them in this iteration phase as well. This cycle takes three to six months. After the chip layout is completed and is verified to match the schematics, it is sent for fabrication, e.g., to Taiwan Semiconductor Manufacturing Co. (TSMC). Fabrication requires three to four months. Upon return, the chip is mounted in a suitable package and undergoes test and characterization; this phase takes another three to four months [1].

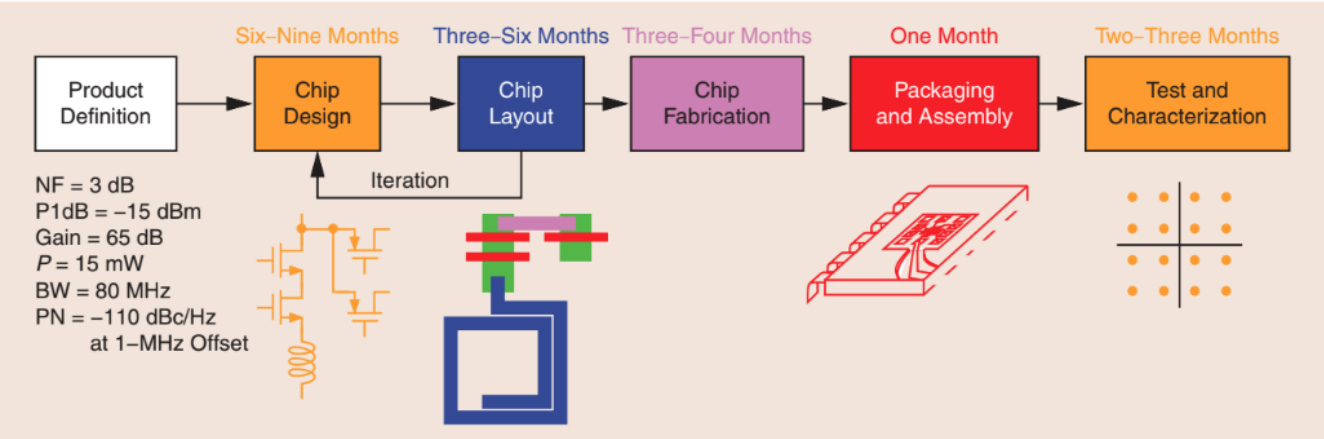

Figure 1: A typical chip development time frame [1].

Open Source Analog/RF/Mixed Signal IC Design Flow

There are numerous ways in which you can install the open-source chip design tools for this course. The simplest, "default" method is to use the pre-packaged Docker container provided by: IIC-OSIC tools. A research team led by Prof. Harald Pretl from Johannes Kepler University (JKU) developed this Docker container. Using this container, we can easily setup open-source tools and access it through Virtual Network Computing (VNC). You can find clear installation instructions on how to set this up on Dr. Kwantae Kim's Blog. Regardless of how you install the tools, you will occasionally need to look at their documentation. Here is a list of useful links.

- Xschem: http://repo.hu/projects/xschem/xschem_man/xschem_man.html
- Ngspice: https://ngspice.sourceforge.io/docs.html
- KLayout: https://www.klayout.de/
- Magic: http://opencircuitdesign.com/magic/

We use an open-source analog design flow as illustrated in Figure 2 which is also mentioned at Analog/Mixed/RF flow, with the following tools (Note - commercial analog design tools like Virtuoso and Calibre are not openly supported for this open-source PDK):

- PDK files from IHP Open Source PDK.
- Schematic entry with Xschem.
- Simulation with Ngspice.
- Layout, extraction and DRC with KLayout.
- LVS with netgen/KLayout.
- Parasitic extraction with Magic.
- Manual routing of design using KLayout into the analog user project.

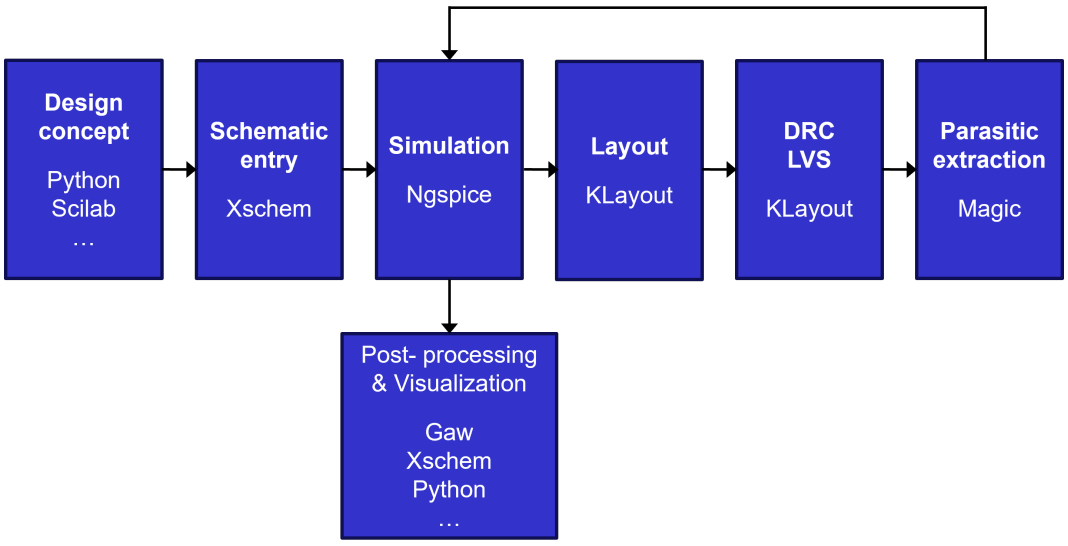

Figure 2: The open-source analog design flow from EE628.

IHP SG13G2 PDK

SG13G2 is a high performance BiCMOS technology with a 130nm CMOS process: IHP 130nm BiCMOS Open Source PDK documentation. It contains bipolar devices based on SiGe:C npn-HBT's with up to 300 GHz transit frequency (fT) and 500 GHz maximum oscillation frequency: BJT Devices. The SG13G2 process provides 2 gate oxides: A thin gate oxide (sg13_lv) for the 1.2 V digital logic and a thick oxide (sg13_hv) for a 3.3 V supply voltage: MOSFET Devices. For both modules NMOS, PMOS and isolated NMOS (iNMOS) transistors are offered. Further passive components like poly silicon resistors: Resistor Devices, inductors: Inductor Devices and MIM capacitors: Capacitor Devices are available. These devices also have corresponding python-based parametric cells (p-cells) that you can access in KLayout: P-Cells.

The backend option offers 5 thin Al metal layers, two thick Al metal layers (2 and 3 μm thick) and a MIM layer. The metals are organized as Metal1-Via1-Metal2-Via2-Metal3-Via3-Metal4-Via4-Metal5-MIM formation-TopVia1-TopMetal1-TopVia2-TopMetal2-Passivation.

IHP-Open-DesignLib is repository, which contains open source IC designs using IHP SG13G2 BiCMOS processs: IHP-Open-DesignLib documentation. It is also a central point for design fabrication under the concept of IHP Free MPW runs funded by a public German project FMD-QNC (16ME083). Project funds can be used exclusively to produce chip designs for non-commercial activities, such as university education, research projects, and others. In the project, a continuation for the provision of free area for the open source community is to be worked out. Criteria for selection of designs submitted by the open source community is specified here. More information about Process Specifications and Layout Rules have been uploaded in the A4 drive folder.

In order to set IHP-SG13G2 as the default PDK in xschem, run the command iic-pdk ihp-sg13g2.

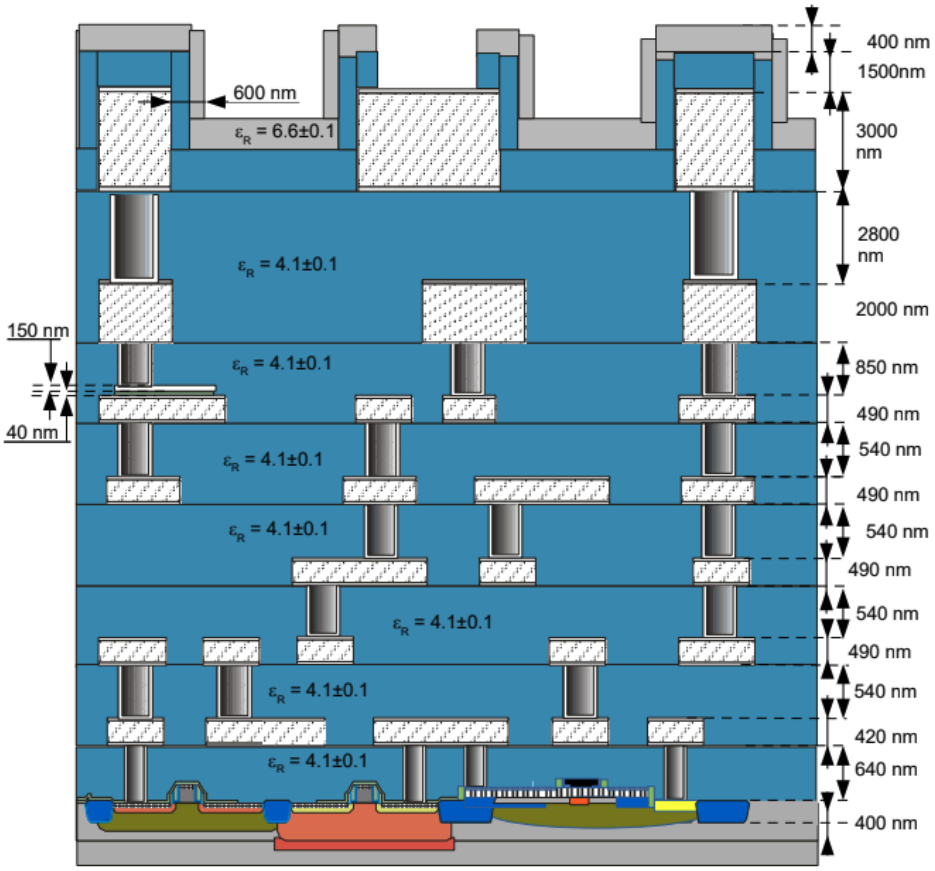

Figure 3: Cross-Section Schematic of SG13G2 Process

Project Description

The project is to design a charge-pump (CP) based (Type-II) PLL which uses a standard fractional-N architecture, where an output frequency divider (FD) is used to set the frequency multiplication with respect to the reference clock input. The output frequency f_{out} is N * f_{ref}, where N is the division ratio of $XDIV_{OUT}$ and f_{ref} is the input clock frequency. N can be between 1 and 15, and is designed for a 10 MHz reference input, which implies an output frequency between 10 MHz and 150 MHz.

The tiny_pll project contains all the schematics and symbols of the top-level design shown in Figure 4, albeit designed using the SKY130 PDK open-source and taped-out on Tiny-tapeout 08 [4]. You may use the same schematic designs for reference, but port the technology from SKY130 PDK to IHP SG13G2. You are free to make any modifications you prefer to the design, such as implement a DSM instead of the FD or an integer-N instead of fractional-N or you can increase the range of N beyond 15.

The teams are expected to perform the layout designs of the sub-cells of the PLL IP listed below.

- Phase-frequency detector (PFD)
- Charge pump (CP)
- Loop filter
- Voltage-controlled oscillator (VCO)
- Frequency divider (FD)

Once the projects have passed physical verification (DRC/LVS) and post-layout simulations after parasitic extraction (PEX), then the filler generation process is done using KLayout. The maximum area granted to a community member is 2 mm^2, which includes the sealring. An example of the area provided for the design is given in the test_layout.gds file, which is a 300 μm × 300 μm space. After the final GDSII file has been generated and submitted, the selected designs will be processed at the IHP pilot line facility (clean room). This process takes around 4 to 6 months depending on the technology. After this process, the designers can obtain the chip die and package the die into QFN32 chips as shown in Figure 5.

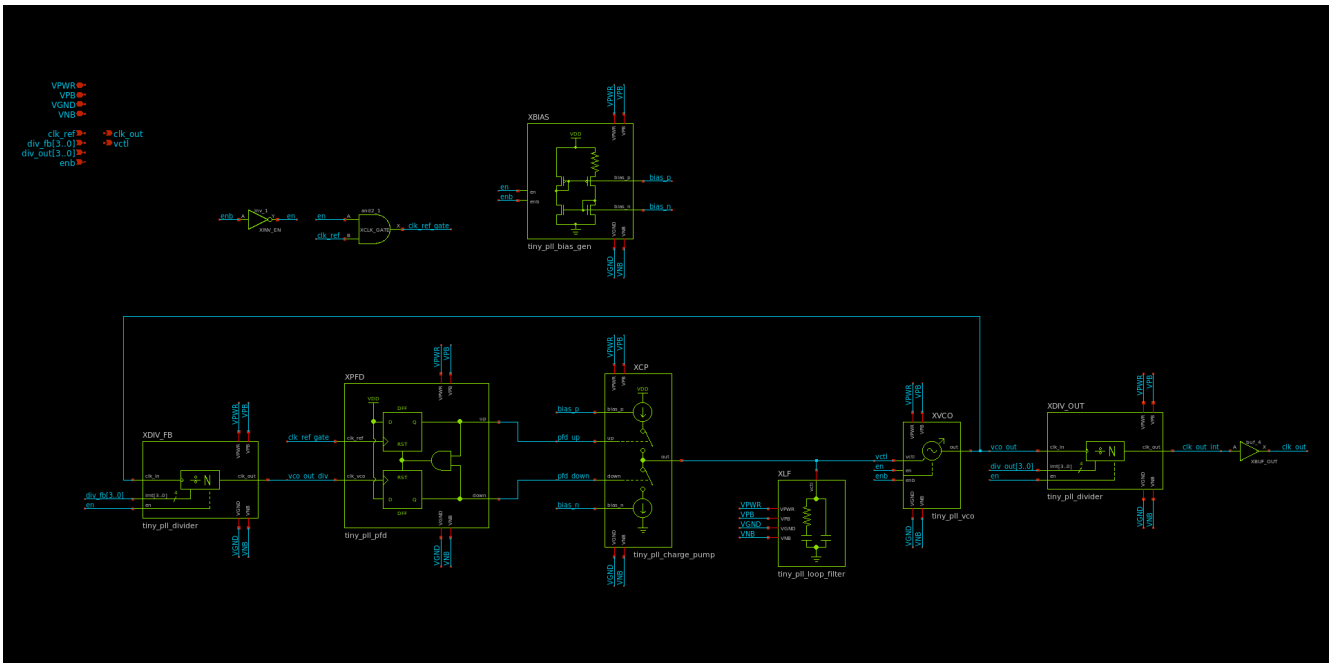

Figure 4: The top-level schematic design of tiny_pll

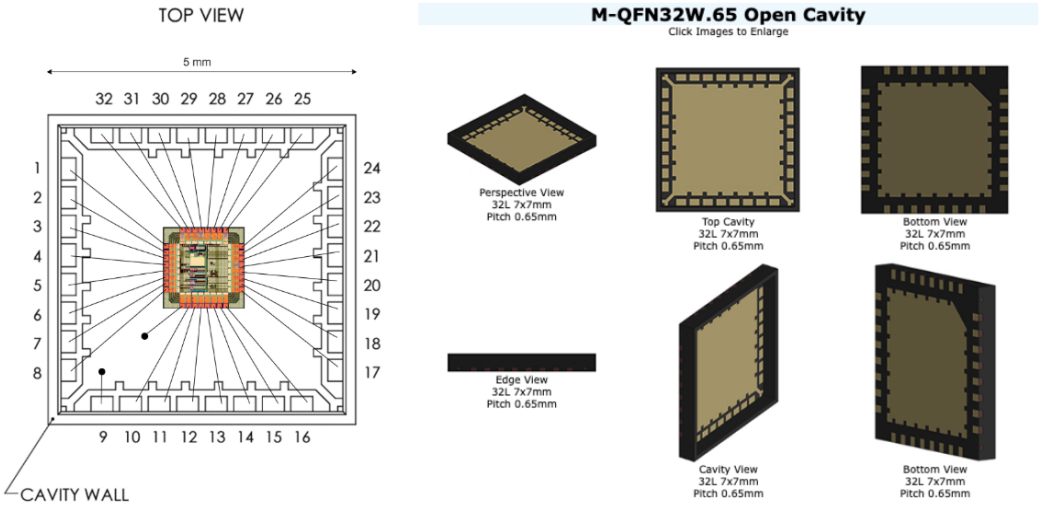

Figure 5: M-QFN32W.65 Open cavity (air cavity) packages for wirebonding the chips from EE628.

Instructions

The design goals of this project are as follows:

- The design should be as simple as possible to reduce the chance of failure.
- The design should be as small as possible so it can be incorporated into future IHP tapeout designs with minimal area overhead (less than 0.03 mm^2).

Please complete the projects in the github repo cmos-pll-ihp-sg13g2 along with the README documentation for your projects.

Hard Deadline: 24 April 2025 by 11.59 PM
Design Review: 25 April 2025 by 11.59 PM
Resubmission: 2 May 2025 or 11 Jul 2025
Tapeout: 9 May 2025 or 18 Jul 2025

Note - These are hard deadlines and teams are expected to have the designs completed for review by the above deadlines, if they are planning on going for the tapeout.

References

[1] B. Razavi, "Education of chip designers at a large scale: A proposal [society news]," *IEEE Solid-State Circuits Magazine*, vol. 16, no. 2, pp. 76–83, 2024.

[2] The Economist, "America is building chip factories. now to find the workers," *The Economist*. [Online]. Available: https://www.economist.com/united-states/2023/08/05/america-is-building-chip-factories-now-to-find-the-workers

[3] P. Kinget, "Teaching ic design: From concepts to testing a fabricated custom chip [society news]," *IEEE Solid-State Circuits Magazine*, vol. 15, no. 3, pp. 87–93, 2023.

[4] M. Venn, "Tiny tapeout: A shared silicon tape out platform accessible to everyone," *IEEE Solid-State Circuits Magazine*, vol. 16, no. 2, pp. 20–29, 2024.

Appendix

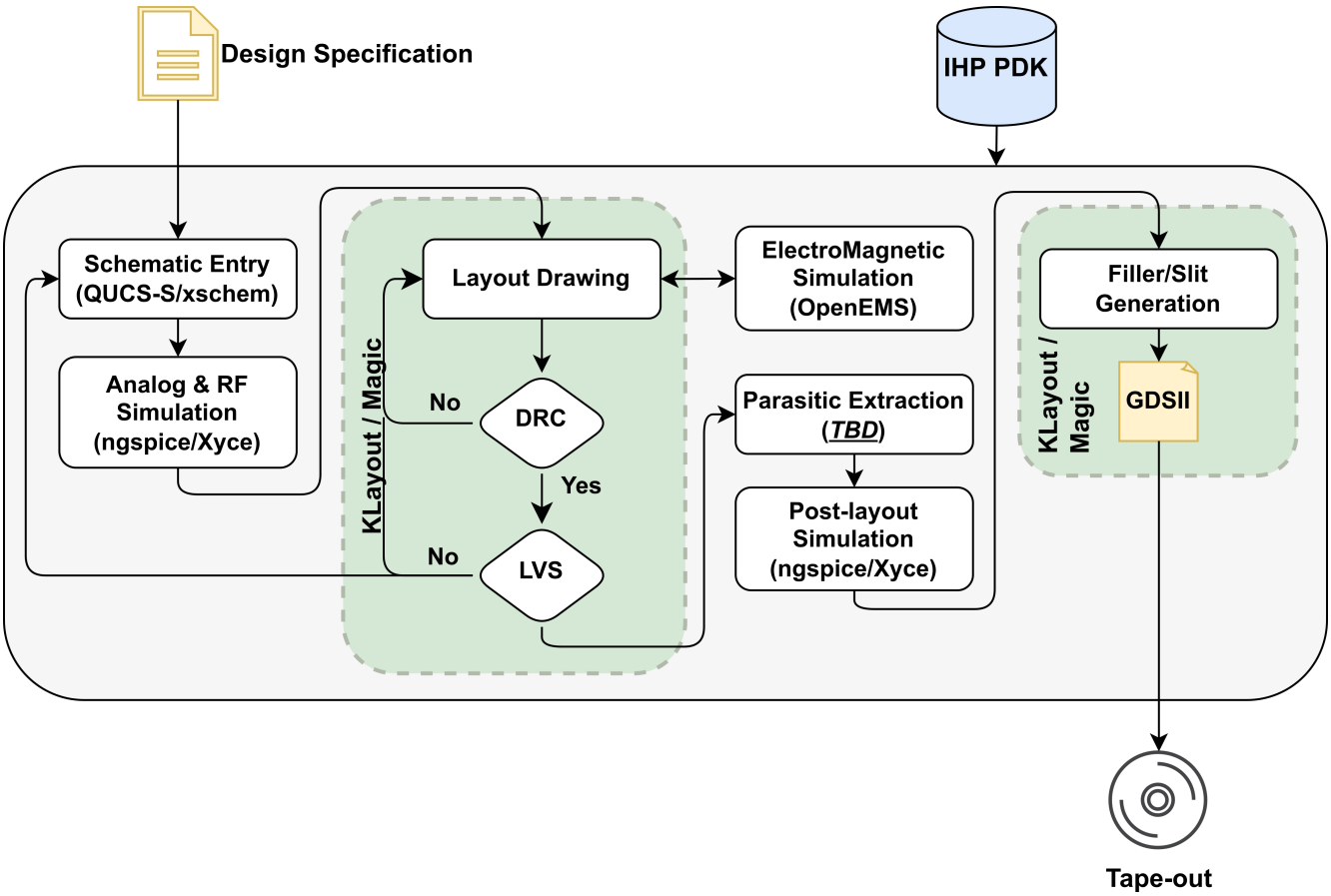

Figure 6: The open Source Analog/RF/Mixed Signal IC Design Flow