Comparison of LC and Ring VCOs for PLLs in a 90 nm Digital CMOS Process

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Abstract – *This paper gives a performance, power and area comparison of LC vs. Ring VCOs for application to PLL designs in a standard 90 nm digital CMOS process. We develop an analytical framework for determining the best match for a high-speed clock synthesizer design based on the constraints of the application. A type-II PLL is utilized in this study because of its capability for allowing independent adjustments to the damping factor, the loop-bandwidth and loop gain.. Cadence SpectreRF is used to verify our analysis.*

Keywords: LC VCO, Ring, VCO, PLL, digital CMOS process.

1 Introduction

Phase locked loops (PLLs) are commonly used in modern integrated circuit based high-speed digital systems to perform a variety of clock processing tasks such as clock frequency multiplication and clock de-skewing. Figure-1 shows a typical circuit diagram of a type-II 3rd order PLL design used for a clock frequency multiplication application. It takes the low frequency reference clock input, RCLK, and multiplies it by the divider ratio, N, to generate a high frequency clock, CLK. The PLL consists of a phase-frequency detector (PFD), charge-pump (CP), loop filter (LF), voltage controlled oscillator (VCO) and divider.

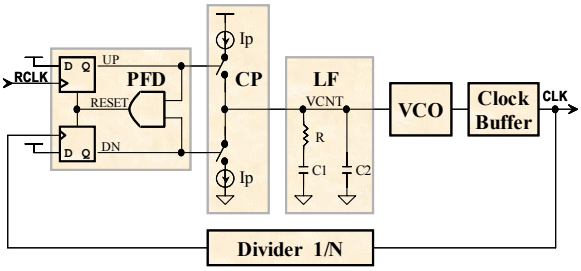

Figure-1. Circuit diagram of type-II 3rd order PLL

A VCO is one of the key components in a PLL, and it has a great impact on the PLL's overall performance. For CMOS based VCO design in current technology, LC and Ring based VCOs are two typical choices used in PLL design [1]. LC VCOs have a superior phase noise performance compared with Ring VCOs. However, an LC VCO has a small tuning range, large layout area and possibly higher power [2]. For reasons of design simplicity and cost effectiveness, a Ring VCO based PLL is often considered first to determine if it can meet the performance requirements.

This paper studies the performance, power, and layout area trade-offs between the LC and Ring VCO based PLL designs in a standard 90 nm digital CMOS process. Our ultimate goal is to provide a method to determine the best choice between LC and Ring based PLL designs to meet a given performance specification. Section 2 discusses the PLL architecture and presents the analysis for the LC and Ring VCO based PLL comparison. Simulated performance results based on Cadence SpectreRF are given in Section 3. The trade-off among the performance, power and layout is also discussed in Section 3.

2 PLL Architecture and Analysis

A type-II 3rd order PLL architecture is used in this paper and shown in Figure-1. The type-I PLL is not chosen due to its difficulty in adjusting loop bandwidth, and loop gain independently. In addition, it has limited acquisition range and is difficult to implement in high-performance digital integrated circuits [1]. Both LC and Ring VCO based PLL use a common topology consisting of PFD, CP, LF, and Divider. However, the CP current gain and LF frequency response are individually adjustable in order to optimize the PLL performance as needed.

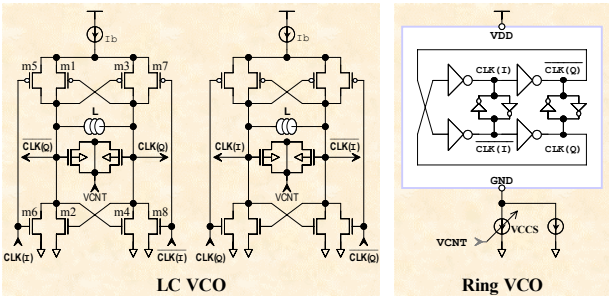

Figure-2. Circuit schematic of LC and Ring VCO

The circuits for the LC and Ring VCOs designed in this paper are shown in Figure-2. The frequency control for an LC VCO is through an NMOS based varactor, assuming that a diode varactor is unavailable in a standard digital CMOS process. A Ring VCO uses a voltage controlled current sink in parallel with a constant current sink which keeps the VCO running at a

minimum required clock frequency. Both LC and Ring VCOs generate differential in-phase, CLK(I), and quadrature-phase, CLK(Q), clocks [1].

2.1 Frequency, Power and Area Analysis

The oscillation frequency and power dissipation for a differential Ring oscillator are defined in Eq.1 and Eq.2, respectively [3]:

$$f_{Ring} = \frac{1}{2Nt_D} \approx \frac{1}{\eta N(t_R + t_F)} \approx \frac{1}{2\eta N t_R} \approx \frac{I_{TAIL}}{2\eta N q_{MAX}} \quad \text{Eq.1}$$

$$P_{Ring} = I_{TAIL} V_{DD} N = \frac{\eta N q_{MAX}}{T_D} V_{DD} = 2\eta N q_{MAX} V_{DD} f_{Ring} \quad \text{Eq.2}$$

In these equations, N, t_D, t_R and t_F are number of stages, each stage delay time, rise time and fall time, V_{DD} is the supply voltage, I_{TAIL} is the current going through each stage and q_{MAX} is the maximum charge at each stage. Each stage of the Ring VCO shown in Figure-2 includes two large paralleled inverters and two small reversed direction inverters to create latches.

The oscillation frequency and power dissipation for a differential LC oscillator are defined in Eq.3 and Eq.4, respectively [4][5]:

$$F_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad \text{Eq.3}$$

$$P_{LC} = 2R_S I_{PEAK}^2 = 2C\frac{R_S}{L}V_{PEAK}^2 = 2R_S C^2 \omega_O^2 V_{PEAK}^2 = \frac{2R_S}{L^2\omega_O^2}V_{PEAK}^2 \quad \text{Eq.4}$$

$$Q = \frac{\omega_O L}{R_S} \Rightarrow R_S = \frac{\omega_O L}{Q} \quad \text{Eq.5}$$

$$gm_{m1} + gm_{m2} \geq \frac{R_S}{(\omega_O L)^2} \quad \text{Eq.6}$$

Here, L is the inductance of a spiral inductor, C is the capacitance of the varactor plus all parasitic capacitance from MOS devices and the spiral inductor, I_{PEAK} and V_{PEAK} are the peak current through and voltage across the inductor, ω_O is 2π times the oscillation frequency, f_{LC}, and R_S is the serial AC resistance of the inductor, which is a function of the inductor's quality factor as shown in Eq.5. The sum of the transconductances (gm) m1 and m2 for the LC VCO must satisfy Eq.6 to meet the start-up requirement [6]. For an actual implementation, a minimum value of twice gm is required to guarantee LC VCO start-up. Once the required gm, device sizes and associated capacitance for cross-couple CMOS, varactor are found, and inductor can be easily derived [4][5]. Then, the power and area can be determined from the known device sizes.

The PFD, CP and LF normally dissipate negligible power compared to the power used by VCO due to their lower frequency operation. However, the LF layout area could take a large percentage of the overall PLL area, which strongly depends on the required capacitor size used in the LF in order to meet the PLL bandwidth requirement. Power dissipation of the Clock Buffer and Divider shown in Figure-1 can be easily estimated using the first order calculation of Eq.7.

$$P = \frac{1}{2}(\sum_i C_i)V_{DD}^2 f \quad \text{Eq.7}$$

Here, f and C_i are the clock frequency and individual parasitic capacitance at the nodes of interest.

2.2 Performance and Circuit Analysis

PLL design starts from a target output clock frequency with a required jitter performance as well as the available reference clock frequency and the power and area constraints discussed in Section 2.1. Depending on the application, other requirements must also be met such the as loop stability, settling-time, hold / pull-in / lock-in range, and so on. In our study, the jitter performance, power, and area are used to determine the trade-off between LC and Ring VCO based PLLs.

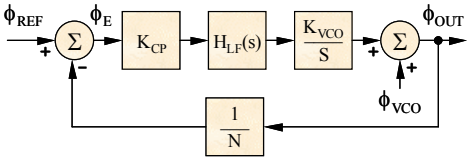

Figure-3. Linear model of a PLL

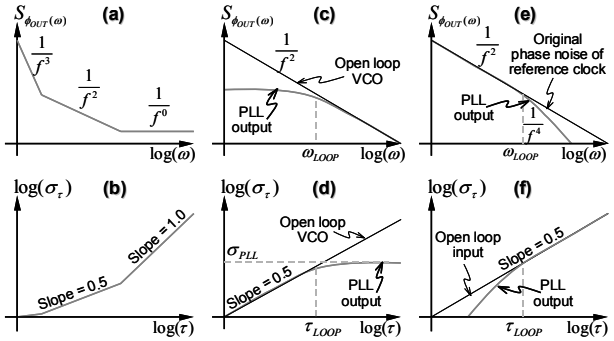

Figure-4. (a)~(b) phase noise and timing jitter of a free running VCO, (c)~(d) phase noise and timing jitter of a PLL with ideal reference clock and noisy VCO, (e)~(f) phase noise and timing jitter of a PLL with noisy reference clock and ideal VCO.

Figure-3 illustrates the linear model of a PLL based on Figure-1, which provides an intuitive way to derive the phase noise transfer function from the input reference clock and VCO to the PLL output as shown in Eq.8 and Eq.9, separately. Eq.8 and Eq.9 indicate that PLL is a low pass filter to input reference clock but a high-pass filter to the VCO. Eq.8 also indicates that the phase noise from the input reference clock linearly increases with divider ratio, N, when $s \rightarrow 0$. Example phase noise and timing jitter transfer function plots of a PLL are shown in Figure-4 [7] and the phase noise to timing jitter conversion is done through Eq.10 [1]. Based on Eq.8 and Eq.9, PLL bandwidth must be optimized in order to minimize the phase noise at the PLL

output. The optimized PLL loop bandwidth for minimum phase noise is given in Eq.11 [8].

$$\frac{\phi_{OUT}}{\phi_{REF}} = \frac{K_{CP}H_{LF}(s)K_{VCO}N}{sN + K_{CP}H_{LF}(s)K_{VCO}} \quad \text{Eq.8}$$

$$\frac{\phi_{OUT}}{\phi_{VCO}} = \frac{sN}{sN + K_{CP}H_{LF}(s)K_{VCO}} \quad \text{Eq.9}$$

$$Jitter_{[\sec]} = \frac{\sqrt{\int_{-\infty}^{+\infty} 10^{\frac{PhaseNoise_{[dBc/Hz]}}{10}}}}{2\cdot\pi\cdot f} \quad \text{Eq.10}$$

$$\omega_{LOOP(opt)} = f\cdot\left(\frac{\delta\tau_{VCO} + \frac{K_{VCO}}{2\pi\cdot f^2}\cdot\frac{\delta V_{LF}}{N}}{\delta\tau_{REF} + \frac{K_{VCO}}{2\pi\cdot f}\cdot\frac{\delta I_{CP}}{K_{CP}}}\right) \quad \text{Eq.11}$$

In the above equations, $\delta\tau_{VCO}$, $\delta\tau_{REF}$, δV_{LF} and δI_{CP} are the VCO RMS timing jitter, reference clock RMS timing jitter, LP RMS voltage and CP RMS current.

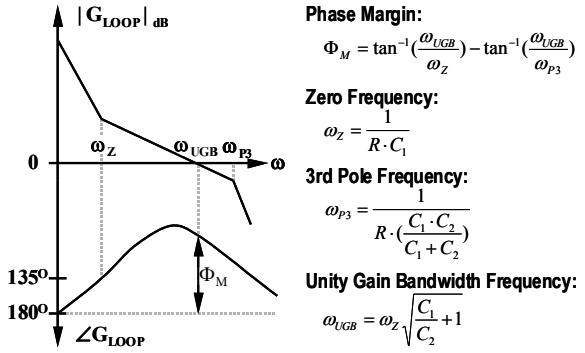

Figure-5. A type-II 3rd order conceptual PLL loop gain Bode plot

The next step is to derive the required device sizes for the LF based on the given optimized PLL loop bandwidth and the desired PLL loop phase margin. An example of a type-II 3rd order conceptual PLL loop gain Bode plot is shown in Figure-5, and the optimized LF capacitor and resistor sizes which are relatively immune to process variation are given by Eq.12 ~ Eq.17 [9].

$$\frac{C_1}{C_2} = 2\cdot(\tan^2\Phi_M + \tan\Phi_M\sqrt{\tan^2\Phi_M + 1}) = \alpha \quad \text{Eq.12}$$

$$\omega_{LOOP(opt)} \approx \omega_{UGB} = \omega_Z\sqrt{\frac{C_1}{C_2}+1} \Rightarrow \omega_Z = \frac{\omega_{UGB}}{\sqrt{\frac{C_1}{C_2}+1}} \quad \text{Eq.13}$$

$$\Phi_M = \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_Z}\right) - \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_{P3}}\right)$$
$$\Rightarrow \omega_{P3} = \frac{\omega_{UGB}}{\tan\left(\tan^{-1}\left(\frac{\omega_{UGB}}{\omega_Z}\right) - \Phi_M\right)} \quad \text{Eq.14}$$

$$C_2 = \frac{\omega_{P3}}{\omega_Z} - \alpha \quad \text{Eq.15}$$

$$C_1 = \alpha\cdot C_2 \quad \text{Eq.16}$$

$$R = \frac{1}{\omega_Z\cdot C_1} \quad \text{Eq.17}$$

The phase noise performances of differential Ring and LC VCOs are expressed in Eq.18~19 [3] and Eq.20 [9], respectively. Their timing jitters are also calculated from the phase noise response through Eq.10 [1].

$$L_{RING}\{\Delta\omega\} = \frac{8}{3\eta}N\frac{\kappa T}{P_{Ring}}\left(\frac{V_{DD}}{V_{CHAR}} + \frac{V_{DD}}{R_L I_{TAIL}}\right)\frac{\omega_O^2}{\Delta\omega^2} \quad \text{Eq.18}$$

$$V_{CHAR} = \frac{V_{GS} - V_{TH}}{\gamma} \Rightarrow Long\_Channel$$
$$V_{CHAR} = \frac{E_C L_{CHANNEL}}{\gamma} \Rightarrow Short\_Channel \quad \text{Eq.19}$$

$$L_{LC}\{\Delta\omega\} = \frac{F\kappa T R_S}{V_{PEAK}^2 Q}\frac{\omega_O^2}{\Delta\omega^2} \quad \text{Eq.20}$$

Here, R_L, κ, T, V_{GS}, V_{TH}, E_C, $L_{CHANNEL}$ and γ are the load resistance, Boltzmann constant, temperature, MOS gate-source voltage, MOS threshold voltage, critical electrical field, MOS channel length, and channel coefficient. E_C is defined as the value of the electrical field resulting in half the carrier velocity expected from low field mobility, and γ is about 2/3 for a long channel device in the saturation region and is typically 4/3 ~ 2 for short channel devices [3]. A simulation-based method to estimate the effective phase noise of a PLL and it individual blocks can be found in reference [10].

3 Simulation and Comparison

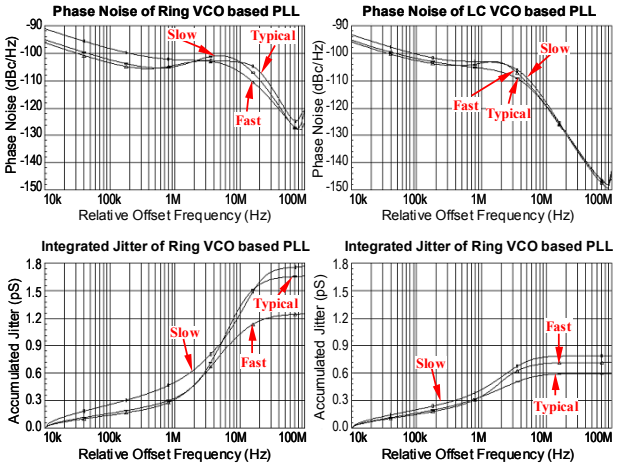

Figure-6. Simulated Phase noise and integrated RMS jitter for both Ring and LC VCO based PLLs at 106.25MHz input reference and 4.25GHz output clock.

The design verification process uses Cadence SpectreRF to perform a PLL phase noise simulation. The simulation results and its resulting integrated RMS jitter values for both Ring and LC VCO based PLLs using the standard 90 nm digital CMOS process and operating at a 106.25 MHz input reference clock and a 4.25 GHz output clock (Divider ratio N=40) are shown in Figure-6. The optimized PLL loop bandwidths at this frequency are about 10 MHz and 2 MHz for Ring and LC VCO based PLLs, respectively. The results

imply that a Ring VCO based PLL can be used in a 8.5 Gbps Fibre Channel design which requires PLL RMS jitter to be less than 1.8 pS. Figure-7 shows the VCO layout used for the performance comparison of Figure-6. The size of the LC VCO is about 4 times that of the Ring VCO. However, the total PLL layouts only show a 2X total area difference when the PFD, CP, LF Divider and clock buffer are also included.

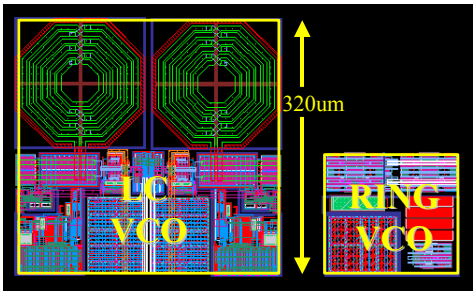

Figure-7. LC VCO and Ring VCO Layout

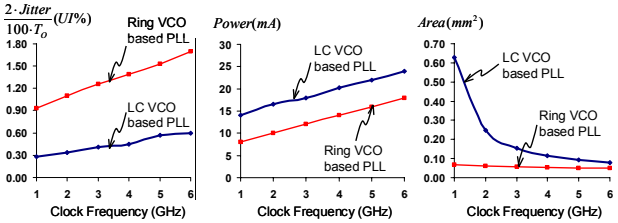

Figure-8. PLL Jitter, Power, and Area Comparison

The comparison of jitter, power and area between LC and Ring VCO based PLLs is shown in Figure-8. Both types of PLLs suffer from the short channel effect, which increases the jitter in percentage of bit period. For a PLL design which requires a wide frequency range, an LC VCO based PLL would need multiple VCOs to switch between frequency ranges, which would make the area comparison in Figure-8 incomplete.

	ADVANTAGES	DISADVANTAGES
Ring VCO based PLL	Common approach for digital chips Many ways to control frequency Multi-phase clock generation Wide frequency tuning range	High phase noise → widen loop BW to reduce High VCO gain → sensitive to disturbance Not suitable for SONET transmit clocks Poor stability at high frequency
LC VCO based PLL	Common approach for RF design Good stability Long-term and period jitter filtering Low long-term and period jitter Low phase noise	Large layout area → large area for inductor Narrow tuning frequency range Require a lot of characterization Poor integration and more complicated design

Table-1. LC and Ring VCO based PLL trade-off

Table-1 presents a summary of the trade-off between Ring and LC VCO based PLL designs. Each of them has its own particular advantages and disadvantages. Generally, a Ring VCO based PLL has wider loop bandwidth with higher phase noise response and is most suitable for clock and data recovery circuits, while an LC VCO based PLL has narrower loop bandwidth with superior phase noise response which is well matched for RF applications.

4 Conclusions

We have presented a comparison of LC and Ring VCO based PLL designs in a standard 90 nm digital CMOS process technology. The power, layout area, frequency operation and optimization of loop bandwidth to minimize phase noise are all considered in order to obtain a fair comparison. The results show that a Ring VCO based PLL design can meet the performance requirements of a certain high-speed clock synthesizer application if the PLL loop bandwidth is properly optimized. Furthermore, a Ring VCO based PLL has the advantages of larger tuning range and smaller layout area compared with an LC VCO based PLL. Of course, an LC VCO based PLL design exhibits a superior phase noise performance but this advantage is mitigated to some extent by short channel effects.

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