# EN4430: Analog IC Design

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Index No: XXXXX

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## Fully Differential CC VCO simulation to achieve desired specifications

Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. The rapid increase of the systems' clock frequency poses challenges in generating and distributing the clock with low uncertainty and low power. We require more innovative techniques at both system and circuit levels that minimize the clock timing uncertainty with minimum power and area overhead. Voltage-controlled oscillators (VCOs) play a very important role in achieving such techniques. The design of high frequency, low power and low phase noise VCOs in integrated circuit technologies has remained a challenge in the past few decades. This is because of the continued down-scaling of supply voltages and increased parasitics of process nodes, which result in low-Q circuit inductors and capacitors.

The design of the VCO depends to some extent on the phase-locked loop (PLL) in which it is embedded [1]. We begin with the simple LC oscillator shown in Figure 1, where $R_p$ models the loss of each tank. The tank quality factor, the output swing, and the PN of the foregoing oscillator strongly depend on the inductor's design. Hence, it is important to understand how to design the optimal inductor. We construct a basic oscillator by using two cross-coupled (CC) NMOS devices and selecting $(\frac{W}{L})_{1,2}$, such that $M_1$ and $M_2$ steer their tail current completely and rapidly while sensing sinusoids at $X$ and $Y$. Since the basic oscillator has been achieved, it must now be modified for continuous and discrete tuning. The former is created by varactors, and the latter is realized by switched capacitors. We add MOS varactors to the output nodes so as to provide continuous tuning. With these modifications, we build the Type I CC-VCO, which is shown in Figure 1. For more details on guidance on how to simulate and characterize the CC-VCO, please refer to ELEN 665 RF Communication Circuits – Laboratory 6: Analysis and Simulation of a CC-VCO.

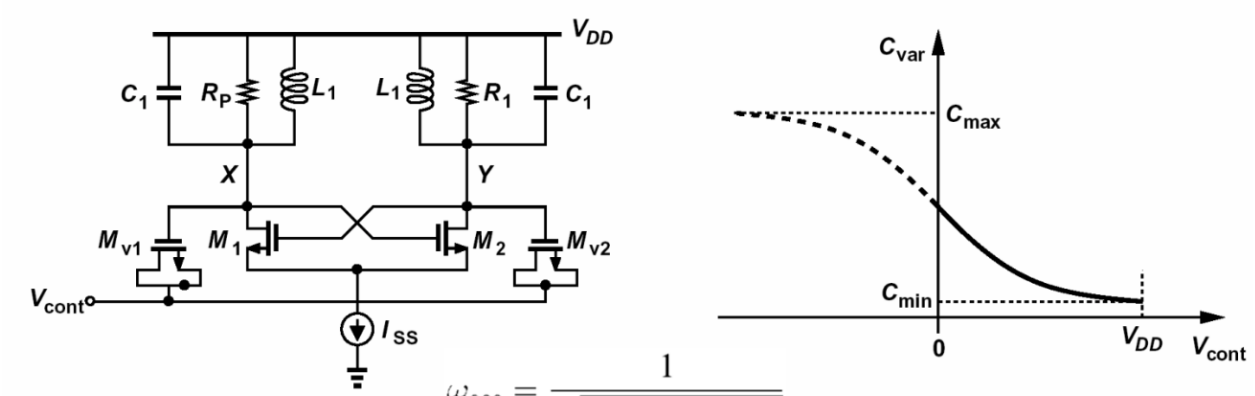


Figure 1: A type I CC voltage-controlled oscillator (VCO) with MOS varactors

An improvement of CC-VCO is shown in Figure 2, where we use an additional cross-coupled (CC) PMOS device stage which provides swing around the output common-mode (CM) level of $V_{DD}/2$, which can be set by selecting the appropriate device dimensions. This also ensures that the output swing is twice that of the previous topology, meaning it will be a fully differential implementation. You may use a suitable component to simulate the symmetric inductor. The following required design specifications summarized in the Table 1, are provided for this project,

Table 1: Desired Project Performance Specifications

| **Parameter** | **Project Specification** |
|---|---|
| Technology [Min. length of transistors ($L_{min}$)] | 45 nm CMOS |
| Supply voltage $V_{DD}$ | 1 V |
| Nominal input common-mode voltage $V_{DD}/2$ | 0.5 V |
| Bias current $I_{bais}$ | 1 mA (change accordingly) |
| Oscillation frequency $f_0$ | 3 GHz |
| Tuning range | $>$ 20% (i.e - 2.7 GHz to 3.3 GHz) |
| $K_{VCO}$ | ? GHz/V |

## Instructions

Please submit your report (at least 5 pages without appendix) including the following information;

- Design methodology and details of the calculation and device sizes
- Transient simulation results (up to 10 ns after steady state) and its frequency spectrum (FFT) showing the frequency of oscillation ($f_0$) and sidebands
- Parametric simulation results of frequency of oscillation ($f_0$) vs. control voltage ($V_{cont}$)
- [Optional] Periodic steady state (pss) simulation and phase noise (PS) simulation results
- Attach the circuit netlist in the appendix

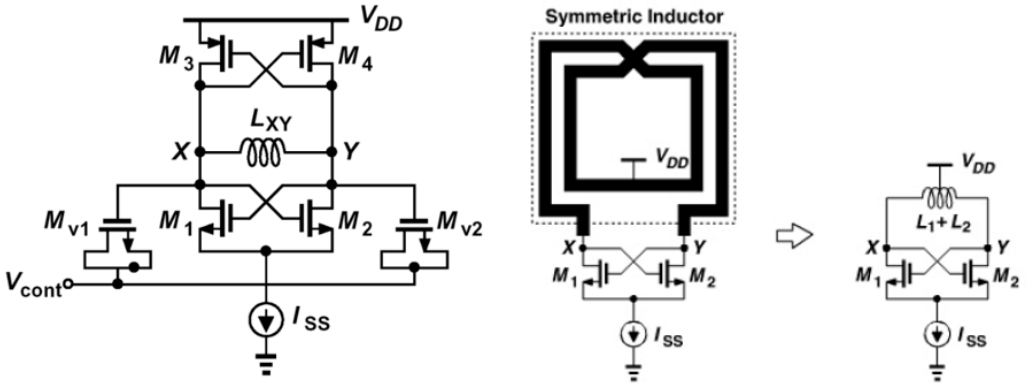


Figure 2: A type IV CC VCO with MOS varactors and a symmetric inductor

For more guidance, refer to two videos and the LC Tank Voltage Controlled Oscillator Tutorial uploaded in the A2 drive folder.

**Due Date: 14 March 2024 by 11.59 PM (email to kithminrw@gmail.com)**

Note - It is not essential for you to achieve the most optimal design with the best tuning range. If you can attempt to cover the most important simulations and relevant test benches for those simulations and present your work, it will be adequate to get the full assignment grades.

## Oscillator Phase Noise

Noise is injected into an oscillator by the devices that constitute the oscillator itself, including the active transistors and passive elements. This noise will disturb both the amplitude and frequency of oscillation. This is depicted in Figure 3, and more information is available in the LC Tank Voltage Controlled Oscillator Tutorial.

- Amplitude noise is usually unimportant because non-linearities that limit the amplitude of oscillation also stabilizes the amplitude noise.
- Phase noise, on the other hand, is essentially a random deviation in frequency which can also be viewed as a random variation in the zero crossing points of the time-dependent oscillator waveform.

An oscillator is a frequency selective (or narrow band, high-quality factor (Q)) circuit and will tend to reject out-of-band (i.e. frequencies offset from $f_o$ by $\Delta f$) signals to some degree. This rejection increases at larger offsets from $f_o$. As a result, the effect of the noise sources is to produce "skirts" on either side of the ideal impulse function of the oscillator in the frequency domain. To measure or quantify phase noise, one considers a unit bandwidth at an offset $\Delta f$ with respect to $f_o$ (i.e. - relative offset frequency), and calculate the noise power in this bandwidth and divide the result by the average carrier power.

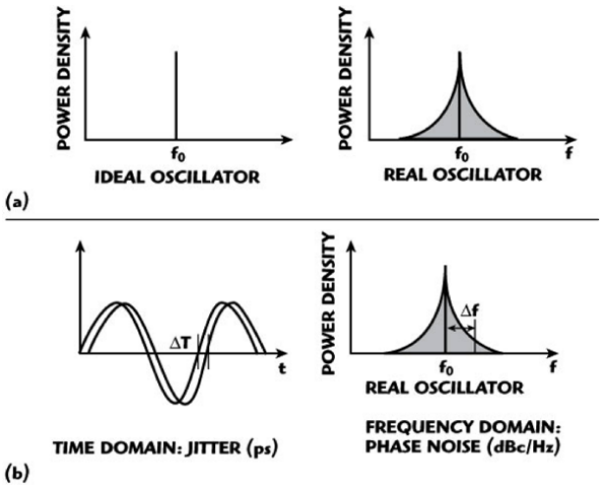


Figure 3: a) Frequency Spectrum of Ideal and Real Oscillators. b) Jitter in the Time Domain and Phase Noise in the Frequency Domain in a Real Oscillator

## References


[1] B. Razavi, "The design of a millimeter-wave vco [the analog mind]," *IEEE Solid-State Circuits Magazine*, vol. 14, no. 3, pp. 6–12, 2022.