EN4430: Analog IC Design

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A PFD-CP Type-II $\Delta\Sigma$ Fractional-N Phase Locked Loop Simulation

CMOS phase-locked loops (PLL) are widely used in most of the system-on-chips (SoC) as the clock generator for digital circuits and wireline transceivers, or the frequency synthesizer for the wireless transceivers. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Within these systems, well-timed clocks are generated with PLLs and then distributed on-chip with clock buffers. The rapid increase of the systems' clock frequency poses challenges in generating and distributing the clock with low uncertainty and low power. Analog and mixed-signal PLL (AMS-PLL) are most widely used architecture for clock generators and frequency synthesizers.

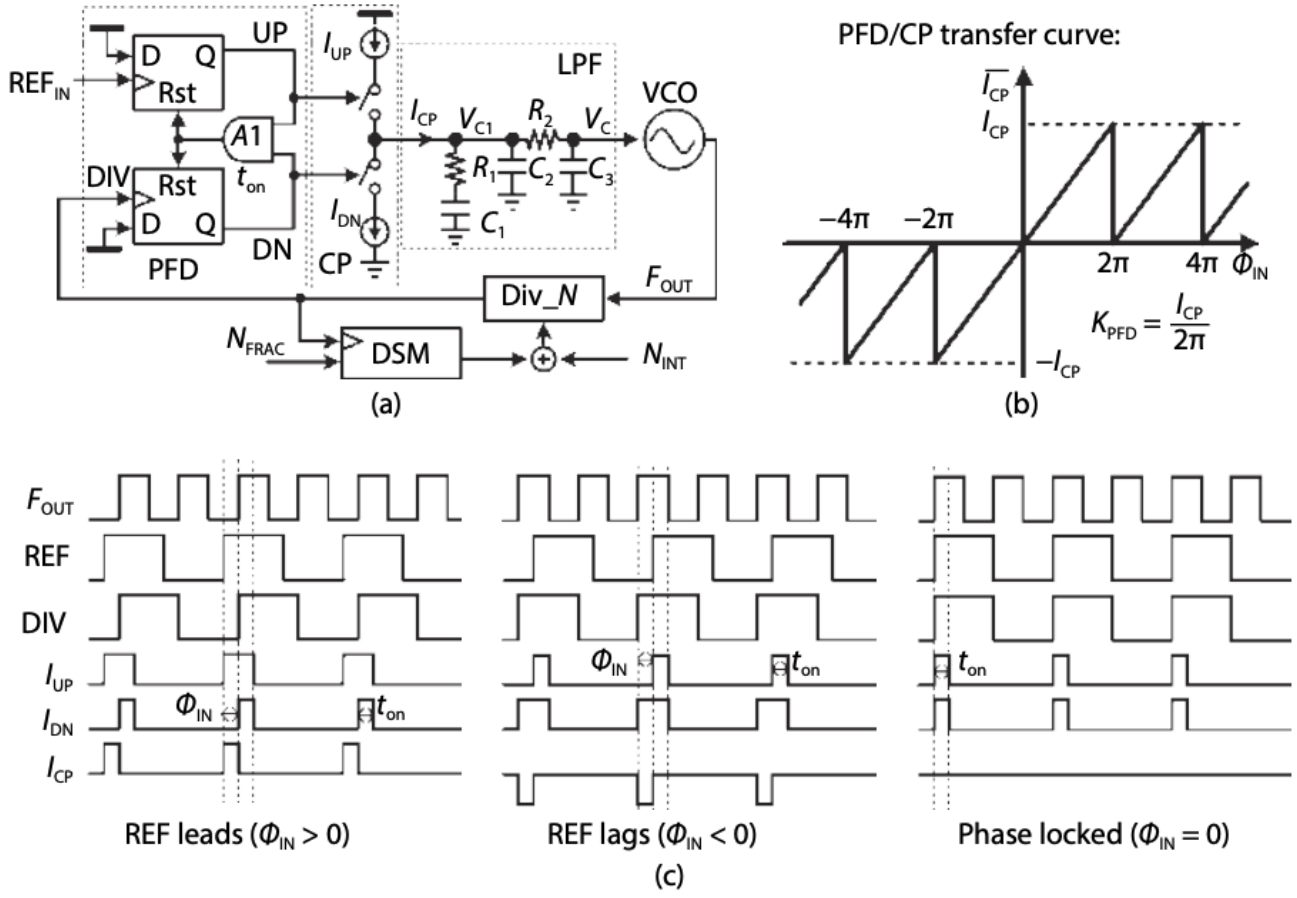

Figure 1: (a) A basic PFD-CP (Type-II) PLL (b) Transfer curve of PFD and CP. (c) Timing diagram.

Figure 1(a) shows the block diagram of the basic PFD-CP (Type-II) PLL, which is an implementation of an AMS-PLL architecture. It consists of a tri-state phase/frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage-controlled oscillator (VCO) and a divide-by-N frequency divider (Div_N). The ratio between the VCO output frequency (f_{VCO}) and the reference frequency (f_{REF}) is N; i.e. $N = \frac{f_{VCO}}{f_{REF}}$. The delta–sigma ($\Delta\Sigma$) modulator (DSM) is used to modulate the division ratio of the divider so as to obtain a fractional division ratio to achieve the function of the fractional-N PLL [1]. For the integer-N PLL, of which N is an integer number, the DSM is not required. Delta-sigma ($\Delta\Sigma$) modulation is a method for encoding analog signals into digital signals as found in an analog-to-digital converter (ADC). It is also used to convert high bit-count, low-frequency digital signals into lower bit-count, higher-frequency digital signals as part of a digital-to-analog converter (DAC).

The operation principle of the PFD-CPPLL is presented by the timing diagram shown in Figure 1(c). As an example, the division ratio N shown in Figure 1(c) is 2. Φ_{IN} shown in Figure 1(c) is the input phase error between the reference clock (REF_{IN}) and the divider feedback clock (DIV).

- When the PLL is unlocked and Φ_{IN} is positive, Φ_{IN} is detected by the PFD and CP generates a positive current pulse I_{CP} to charge the LPF so as to increase f_{VCO} to reduce Φ_{IN}.
- When the PLL is unlocked and Φ_{IN} is negative, CP generates a negative current pulse I_{CP} to discharge the LPF so as to decrease f_{VCO} to reduce $|\Phi_{IN}|$.
- At the locking state, Φ_{IN} keeps zero so that the VCO tuning voltage V_C keeps stable. As a result, $f_{VCO} = N \cdot f_{REF}$ (N shown in Figure 1(c) is 2).

As indicated in Figure 1(c), the pulse width of I_{CP} equals to $|\Phi_{IN}|$. Hence, the average CP output current is proportional to the Φ_{IN}, as the PFD/CP transfer curve shown in Figure 1(b). As we can see, the gain of PFD/CP, K_{PFD}, is $I_{CP}/(2\pi)$. Unlike the PLLs with other types of the phase detector (PD) such the XOR gate and mixer, which suffer from the issue of limited frequency lock range due to the limited monotonic Φ_{IN} range of these PDs, the lock range of the PFD-based PLL is unlimited because the linear Φ_{IN} range of the tri-state PFD is from -2π to 2π (see Figure 1(b)), and the PFD output polarity keeps positive or negative when $\Phi_{IN} > 2\pi$ ($f_{REF} > \frac{f_{VCO}}{N}$) or $\Phi_{IN} < -2\pi$ ($f_{REF} < \frac{f_{VCO}}{N}$), respectively. This makes the PFD be able to distinguish the polarity of the frequency difference between f_{REF} and ($\frac{f_{VCO}}{N}$) so that an additional frequency locked loop with a separated frequency detector for initial frequency acquisition is not required. Hence, the PFD-CPPLL architecture is simple and robust, and thus, the PFD-CPPLL becomes the most widely used AMS-PLL architecture [2]. Table 1 covers an overview of the different types of AMS-PLL architectures and their pros and cons.

Table 1: Summary of the features of the AMS-PLL architectures [2].

Table 1. Summary of the features of the AMS-PLL architectures

Architecture	Pros	Cons	Suitable application scenarios
CPPLL	Simple and robust	1. CP-induced in-band phase noise is multiplied by N^2 (N is division ratio) 2. Divider noise contributes in-band phase noise	1. Jitter and PLL power requirements are not stringent 2. Generates low-jitter clock without ultra-low jitter reference clock
ILPLL	Both in-band and outband phase noise are suppressed simultaneously	Large spur induced at large division ratio N	Generates ultra-low-jitter clock with small N and ultra-low-jitter reference clock
SSPLL	1. Ultra-low in-band phase noise 2. No divider-induced phase noise	Narrow PD monotonic input range	Generates high frequency (e. g. > 20 GHz) ultra-low-jitter clock with large N and ultra-low-jitter reference clock
SPLL	1. Ultra-low in-band phase noise 2. Wider PD monotonic input range than that of SSPLL	Divider-induced phase noise still exists	Generates low frequency (e. g. < 10 GHz) ultra-low-jitter clock with large N and ultra-low-jitter reference clock

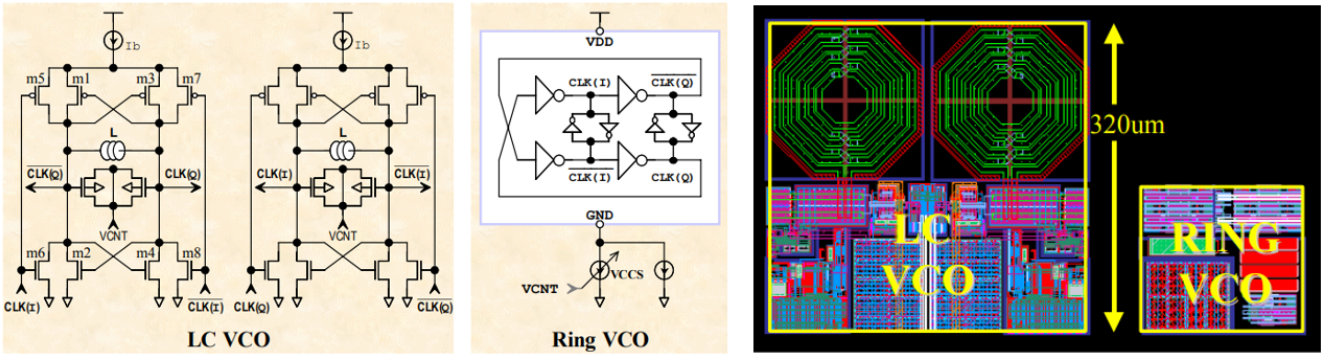

Figure 2: (a) LC QVCO and Ring QVCO circuit schematic (b) LC QVCO and Ring QVCO layout [4].

In order to implement this design, you can refer to the uploaded video DESIGN OF CMOS 45NM BASED FRACTIONAL - N PLL in the A3 drive folder, which covers the architecture of the PLL shown in Figure 1(a). A modification to this architecture is to use the Ring-VCO instead of an LC-VCO. Ring VCOs typically have a wider tuning range than LC VCOs [3]. This is because the frequency of a ring VCO can be adjusted over a broader range by varying the control or supply voltage V_C. Ring VCOs generally occupy less silicon area compared to LC VCOs, which require large inductors and are simpler to design and integrate into CMOS processes, whereas LC VCOs require careful design of the inductor and capacitor components as shown in Figure 2 [4]. However, LC VCOs usually have superior phase noise performance compared to ring VCOs, making them more suitable for low phase noise applications.

In the fractional-N PLL, since the range of the input phase error is usually more than one VCO period at locking state because the division ratio of the divider is modulated by the DSM [1], the nonlinearity of the PFD/CP I/O characteristics, which are induced by the CP current mismatch and the PFD non-ideality, degrade the in-band phase noise due to the DSM quantization noise folding. Furthermore, such nonlinearity also degrades the fractional spur level, which is at the offset frequency of $N_{Frac} \cdot f_{REF}$ (N_{Frac} is the fractional part of the division ratio) and its harmonics [2]. Hence, for simplicity of the frequency divider, instead of the DSM we use a 4-bit binary counter ($= 2^4 =$ modulo-16 or MOD-16), as shown in Figure 3. Counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter where "n" is the number of counter stages used and which is called the Modulus. The modulus of a counter is the number of output states the counter goes through before returning itself back to zero, i.e, one complete cycle. For more details about Millimeter-Wave Frequency Dividers, see Razavi et al. [5].

Instructions

Please submit your report (at least 5 pages without appendix) including the following information;

- Design methodology and details of the calculation and device sizes
- Transient simulation results at maximum output frequency (up to after lock time) and its frequency spectrum (FFT) showing the frequency of oscillation (f_0) and sidebands
- [Optional] Parametric simulation results of output frequency of oscillation f_{OUT} vs. fractional division ratio (N). You may need to use Matlab to obtain the exact plot.
- Discuss an improvement that can help achieve an Integer-N PLL using the architecture in Figure 1(a). (Assume that the DSM is not used).
- Attach the circuit netlist in the appendix

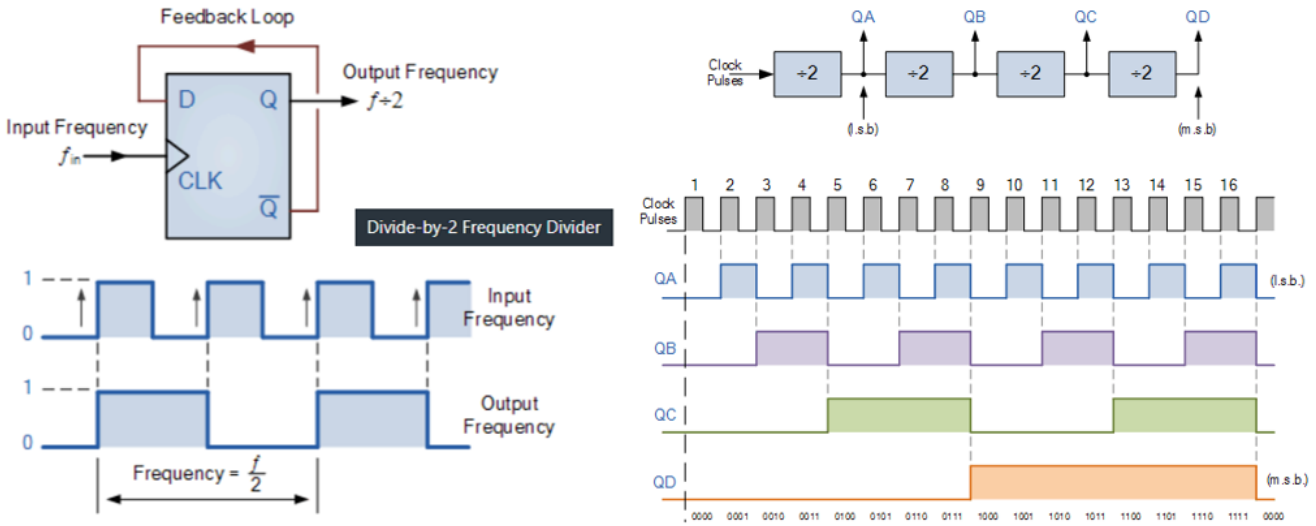

Figure 3: (a) Frequency Division using Divide-by-2 Counter (b) 4-bit Binary (Modulo-16) Counter.

For more details, please refer to Badiger, N.A., Iyer, S. Design & Implementation of High Speed and Low Power PLL Using GPDK 45 nm Technology. J. Inst. Eng. India Ser. B 105, 239–249 (2024) [6] and also read The Design of a Millimeter-Wave Frequency Synthesizer (2023), Razavi et al. [7].

Due Date: 4 April 2025 by 11.59 PM (email to kithminrw@gmail.com)

The following required design specifications, summarized in the Table 2, are provided for this project,

Table 2: Desired Project Performance Specifications

Parameter	**Project Specification**
Technology [Min. length of transistors (L_{min})]	45 nm CMOS
Supply voltage V_{DD}	1 V
Nominal input common-mode voltage $V_{DD}/2$	0.5 V
Reference frequency f_{REF}	200 MHz
Fractional division ratio N	$2 \leq N \leq 16$
Output frequency range f_{OUT}	$f_{OUT,min}$ GHz - $f_{OUT,max}$ GHz
PLL lock time t_{lock}	$t_{lock,min}$ ps - $t_{lock,max}$ ps
Overall average DC power consumption $P_{total,avg}$	? μW

References

[1] B. Razavi, "The delta-sigma modulator [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 10–15, 2016.

[2] Z. Zhang, "Cmos analog and mixed-signal phase-locked loops: An overview," *Journal of Semiconductors*, vol. 41, no. 11, p. 111402, nov 2020. [Online]. Available: https://dx.doi.org/10.1088/1674-4926/41/11/111402

[3] B. Razavi, "The ring oscillator [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 11, no. 4, pp. 10–81, 2019.

[4] M.-T. Hsieh and G. Sobelman, "Comparison of lc and ring vcos for plls in a 90 nm digital cmos process," 01 2006.

[5] B. Razavi, "The design of a millimeter-wave frequency divider [the analog mind]," *IEEE Solid-State Circuits Magazine*, vol. 14, no. 4, pp. 6–16, 2022.

[6] N. Badiger and S. Iyer, "Design implementation of high speed and low power pll using gpdk 45 nm technology," *Journal of The Institution of Engineers (India) Series B*, 01 2024.

[7] B. Razavi, "The design of a millimeter-wave frequency synthesizer [the analog mind]," *IEEE Solid-State Circuits Magazine*, vol. 15, no. 2, pp. 6–13, 2023.