# Department of Electronics and Telecommunication Engineering
# University of Moratuwa

B.Sc. (Eng) Semester 5
EN3013 – Analog Circuit Design
Assignment 02

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Objectives: To learn the design aspects of a voltage-controlled oscillator (VCO).

Software Required:

LT Spice XVII – Open source tool

Design of a VCO

The VCO is an important IP in many communication applications. Industry demands for the VCO circuits which are low-cost, low-power, and high stability. In a communication system, VCO is required especially in PLL circuits, clock recovery circuits and frequency synthesizer circuits.

**STEP-1**

1. Launch LT-Spice simulator.
2. Open your LAB-1 ring oscillator design. Check whether the following transistor directives are used in your design.
   NMOS Transistor: L = 10u W=100u
   .MODEL CMOSN NMOS KP=96u VTO=0.786 LAMBDA=0.01 TOX=21n
   GAMMA=0.586 GAMMA=0.586 CGDO=402p CGSO=402p CGBO=362p
   PMOS Transistor: L=10u W=200u
   .MODEL CMOSP PMOS KP=96u VTO=-0.906 LAMBDA=0.01 TOX=21n
   GAMMA=0.486 GAMMA=0.486 CGDO=54p CGSO=54p CGBO=336p
   Please note the minus sign and units carefully.

3. Modify the inverters with a header switch and a footer switch as shown below.

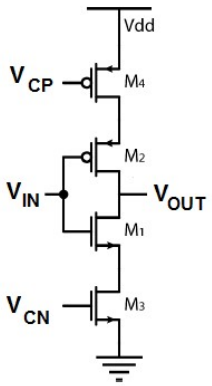


**Figure 1**

4. Supply the appropriate control voltages to $V_{CP}$ and $V_{CN}$ and observe the output frequency.

5. Change the control voltages $V_{CP}$ and $V_{CN}$ and plot the output frequency versus the control voltages.
6. Modify the circuit to have a common control voltage ($V_C$). You may investigate all three methods given below and select one method which suits your circuit better.
   a) Remove footer switch so that you can control using the header switch with $V_{CP}$.
   b) Remove header switch so that you can control using the footer switch with $V_{CN}$.
   c) Insert a circuit so that a common single input voltage controls both $V_{CP}$ and $V_{CN}$.

**STEP-2**

1. Identify the clock parameters which need improvements.
2. Modify your circuit and/or transistor parameters to improve the output waveform.
3. What is your observation about $V_{out}$ (peak-to-peak) in your output?
4. How do you rectify this shortcoming?
5. Modify your circuit and simulate your final design until you get a reasonably good VCO.
6. Plot the output frequency versus the control voltage and indentify the linear region where you can confidently say $f_{out} = K. V_{in}$.

**STEP-3**

1. Get the timing diagram for STEP-1 and STEP-2 from the associated waveform viewer in LT-Spice.
2. Save & Print the timing diagram in .jpeg format.
3. Prepare a simple report with your answers and observations for STEP-1 and STEP-2. Attach the copy of your printed timing diagram. Submit the report to your assigned instructor within 14 days. Your report will be evaluated for 10 marks by your instructor.