Department of Electronic & Telecommunication Engineering
University of Moratuwa

EN3013 - ANALOG CIRCUIT DESIGN

ASSIGNMENT 2: VOLTAGE CONTROLLED OSCILLATOR

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This report is submitted as the fulfillment of Assignment - 02 of module EN3013

1 DESIGN OF VOLTAGE CONTROLLED OSCILLATOR

1.1 Objective

In this assignment, the objective is to gain hands-on experience in designing a voltage-controlled oscillator (VCO) for communication applications. The focus is on using LT Spice simulator and optimizing the VCO circuit for low-cost, low-power, and high stability, considering its importance in PLL circuits, clock recovery, and frequency synthesizers.

1.2 Procedure

STEP-1

1. Modify the inverters of the ring oscillator with a header switch and a footer switch.

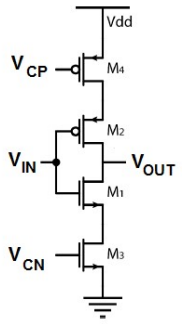

Figure 1 — Header and footer switches for CMOS inverter

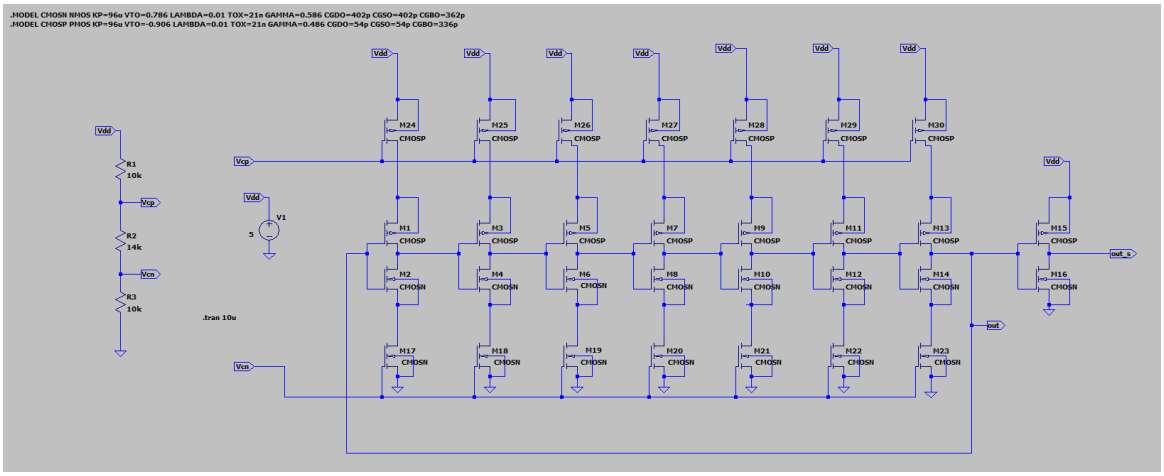

Figure 2 — VCO based on ring oscillator

2. Supply the appropriate control voltages to V_{CP} and V_{CN} and observe the output frequency. Control voltages were supplied using a voltage divider circuit to ensure that V_{GS} of the header and footer switches are the same.
   When R2 = 10k,

$$V_{CP} = 3.33\,\text{V}, \quad V_{CN} = 1.66\,\text{V}, \quad \text{Frequency} = 1.745\ \text{MHz}$$

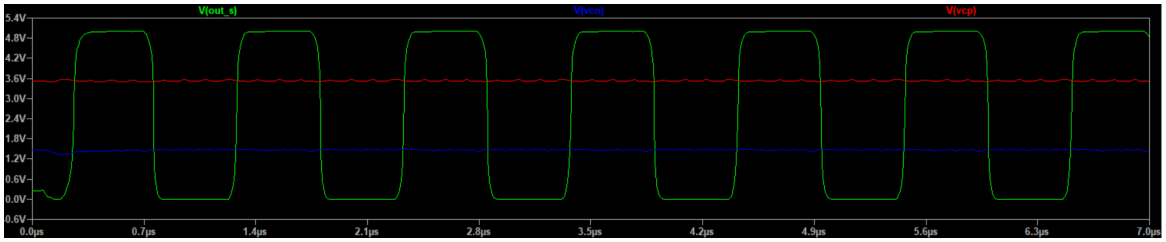

Figure 3 — Output waveform of VCO

3. Change the control voltages V_{CP} and V_{CN} and plot the output frequency versus the control voltages.

V_{CP} (V)	V_{CN} (V)	Period (ns)	Frequency (MHz)
3.52	1.48	1046	0.956
3.43	1.57	770.8	1.297
3.3	1.66	573.2	1.745
3.22	1.78	429	2.33
3.08	1.92	324	3.086
2.91	2.08	248	4.032
2.74	2.26	193.8	5.16
2.5	2.5	154.7	6.464

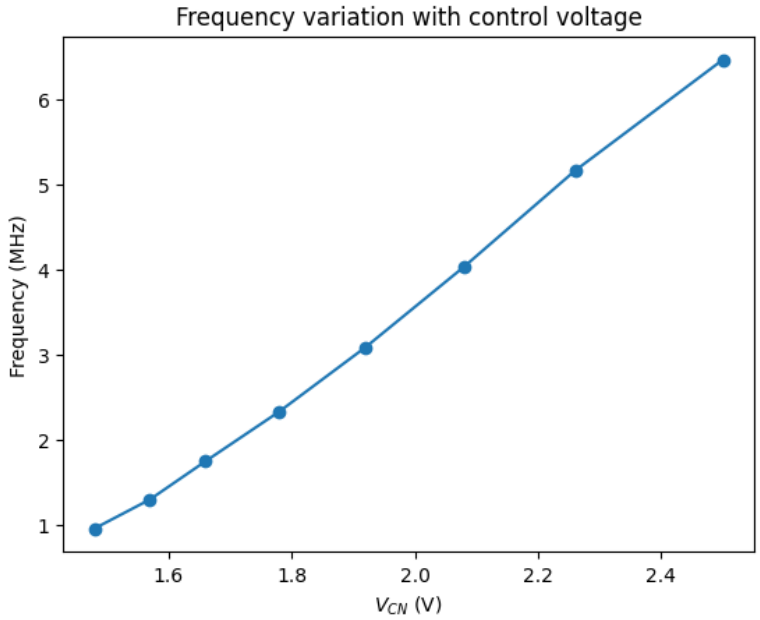

Figure 4 — Variation of output frequency with control voltages

4. Modify the circuit to have a common control voltage (V_C).
   This was achieved by using an additional pair of transistors to mirror the current of the NMOS transistors to the PMOS transistors.

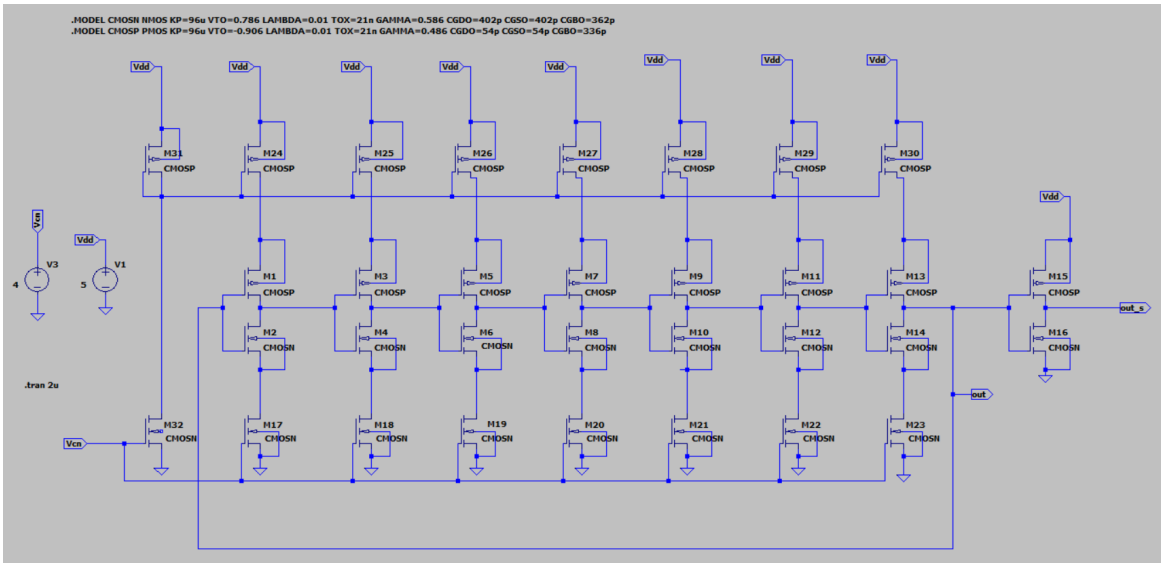

Figure 5 — Modified VCO circuit with a common control voltage

STEP-2

1. Identify the clock parameters that need improvements.
   - Rise time and fall time are noticeable
   - There is a small noise before rising and falling edges

2. Modify your circuit and/or transistor parameters to improve the output waveform.
   The waveform improved when TOX=300n was set for the output inverter in the oscillator.

(a) Before (b) After

Figure 6 — Modifications to improve the output waveform

3. What is your observation about V_{out} (peak-to-peak) in your output?
   $V_{pp} = 4.999$ V
   Due to the channel resistances, the peak-to-peak voltage of the waveform is slightly lower than the supply voltage. There is a small voltage drop across the transistors.

4. How do you rectify this shortcoming?
   In this circuit, the V_{pp} difference is not significant enough to require adjustment. However, it can be improved if needed by increasing W or decreasing L to decrease the channel resistance.

5. Plot the output frequency versus the control voltage and identify the linear region.

V_{CN} (V)	Period (ns)	Frequency (MHz)
1.00	9587.00	0.104
1.50	948.40	1.054
1.75	503.00	1.988
2.00	312.00	3.205
2.25	216.80	4.613
2.50	166.40	6.010
2.75	139.00	7.194
3.00	119.20	8.389
3.25	107.80	9.276
3.50	100.48	9.952
3.75	95.26	10.498
4.00	91.00	10.989

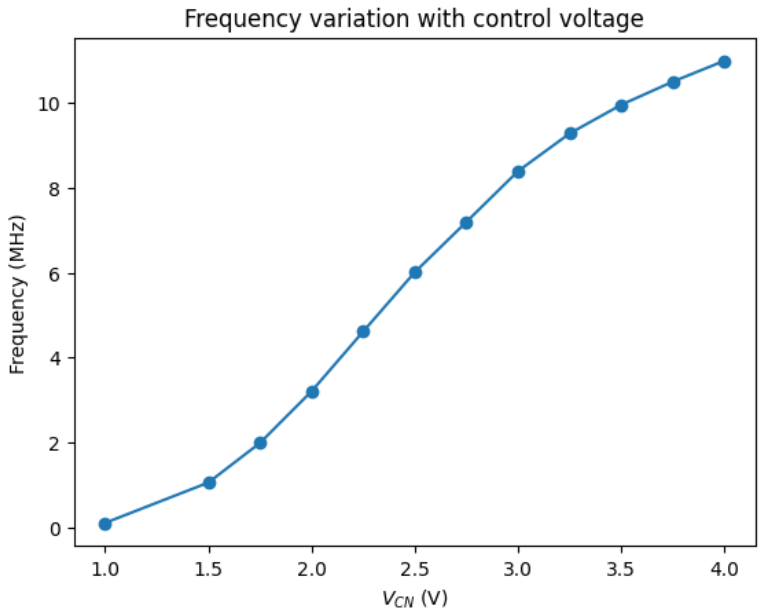

Figure 7 — Frequency variation with control voltage after modifications (using a single control voltage)

According to the graph, the VCO output is approximately linear in the 1.75 V - 2.75 V range for V_{CN}.