Department of Electronics and Telecommunication Engineering
University of Moratuwa

B.Sc. (Eng) Semester 5
EN3013 – Analog Circuit Design
Assignment 01

Objectives: To learn the design aspects of a ring oscillator.

Software Required:

LT Spice XVII – Open source tool

Design of Ring Oscillator

Ring oscillators are simple circuits and easy to implement using CMOS transistors. It plays an important role in several digital applications. In this lab, the techniques of designing ring oscillator circuits based on NOT gates are studied. The response of the designed ring oscillator is to be analyzed in the time domain.

The ring oscillator is a closed loop that comprises an odd number of identical NOT gates, forming an unstable negative feedback circuit. The period of oscillation (T) is twice the sum of the gate delays in the ring.

STEP-1

1. Launch LT-Spice simulator.
2. Design a CMOS inverter circuit using pmos4 and nmos4 transistors. Set the supply voltage to be 5V and apply 0-5V 100MHz pulses at the input of the inverter.

   Some transistors may have many parameters in common. Instead of defining transistor parameters for every instance, transistors are grouped by model name and have parameters in common. The transistors of the same model can have different sizes and the electrical behavior is scaled to the size of the instance.

   Syntax: .model <modname> <type>[(<parameter list>)]

   You may set the transistor parameters by selecting:
   EDIT -> SPICE DIRECTIVES

   NMOS Transistor: L = 10u W=100u
   .MODEL CMOSN NMOS KP=96u VTO=0.786 LAMBDA=0.01 TOX=21n GAMMA=0.586
   PMOS Transistor: L=10u W=200u
   .MODEL CMOSP PMOS KP=96u VTO=-0.906 LAMBDA=0.01 TOX=21n GAMMA=0.486

Please note the minus sign and units carefully. CMOSN and CMOSP are the model names for the Transistors and do not use NMOS or PMOS as model names.
KP – Transconductance Parameter (A/V^2)
VTO – Zero-bias threshold voltage (V)
LAMBDA – Channel-length modulation (1/V)
TOX – Oxide Thickness (m)
GAMMA – Bulk threshold parameter ($V^{1/2}$)

3. Measure the gate delay of the NOT gate.
4. How do you justify your reading?
5. Why the PMOS transistor W is selected almost twice than that of NMOS transistor?
6. Observe the effect by setting the same W (100u) for both PMOS and NMOS transistors.

STEP-2

1. Add the parasitic capacitances for PMOS and NMOS transistors. You may add these values in your model directives.
   NMOS Transistor: CGDO=402p CGSO=402p CGBO=362p
   PMOS Transistor: CGDO=54p CGSO=54p CGBO=336p

   CGDO – Gate-drain overlap capacitance per meter channel width (F/m)
   CGSO – Gate-source overlap capacitance per meter channel width (F/m)
   CGBO – Gate-bulk overlap capacitance per meter channel width (F/m)

2. Measure the gate delay.
3. Justify your reading with engineering background.
4. Observe the effect in frequency, rise time and fall time of the designed NOT gate by changing L and W parameters of the PMOS and NMOS transistors.

STEP-3

1. Choose one odd number between 3 and 11. Say your choice is N {3,5,7,9, or 11}
2. Copy the NOT gate designed in STEP-2 and place N times one after other in a raw. Connect the inputs and outputs of the NOT gates to form a Ring Oscillator. Connect the VDD and GND as well.
3. Observe the waveform. Adjust the transistor parameters to get a reasonably good wave form which has reasonably good clock properties such as raise time, fall time, and duty cycle.
4. Add an additional inverter at the output of the Ring Oscillator to smooth the output waveform.

STEP-4

1. Get the timing diagram for STEP-2 and STEP-3 from the associated waveform viewer in LT-Spice.
2. Save & print the timing diagram in .jpeg format.
3. Prepare a simple report (not more than two pages) and attach the copy of your printed timing diagram. Submit the report to your assigned instructor within 14 days. Your report will be evaluated for 10 marks by your instructor.