Department of Electronic & Telecommunication Engineering
University of Moratuwa

EN3013 - ANALOG CIRCUIT DESIGN

ASSIGNMENT 1: RING OSCILLATOR

Supervisors:
Dr. Thayaparan Subramaniam
Instructors:
Mr. Pahan Mendis

Group No : 04

MALANBAN K.	*200373X*
MANIMOHAN T.	*200377M*
PASQUAL A.C.	*200445V*

This report is submitted as the fulfillment of Assignment - 01 of module EN3013

1 DESIGN OF RING OSCILLATOR

1.1 Objective

The objective of this assignment is to gain a comprehensive understanding of the design principles associated with ring oscillators using CMOS technology. The primary focus is on utilizing LT Spice XVII, an open-source simulation tool, to design a ring oscillator circuit based on NOT gates.

1.2 Procedure

STEP-1

1. Design a CMOS inverter circuit using pmos4 and nmos4 transistors.

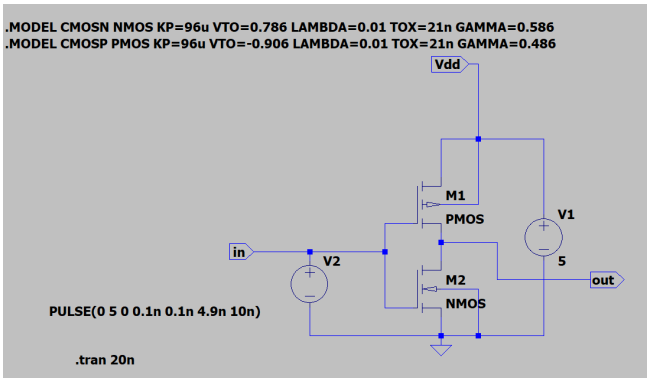

Figure 1 — NOT gate

2. Measure the gate delay of the NOT gate.

$$\text{Rise/fall time} = 0.1\,\text{ns}$$

$$t_{pLH} = 280\,\text{ps}$$

$$t_{pHL} = 430\,\text{ps}$$

$$\text{Gate delay} = \frac{t_{pLH} + t_{pHL}}{2} = 355\,\text{ps}$$

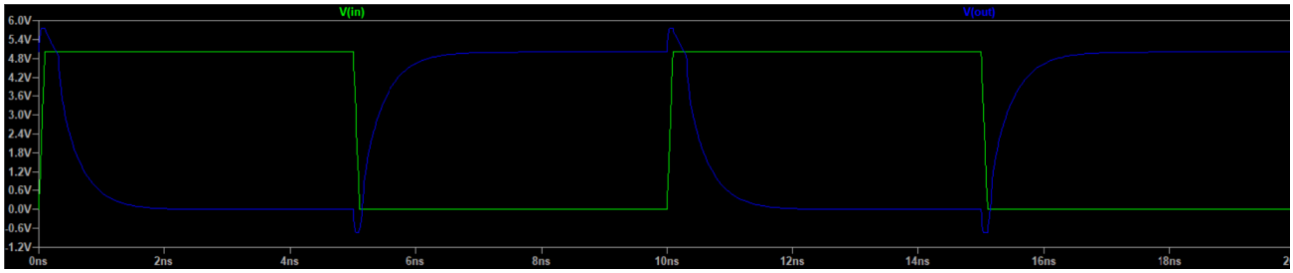

Figure 2 — Inverter output

3. How do you justify your reading?
   The gate of PMOS and NMOS transistors has a capacitance that depends on the size of gate and the characteristics of the oxide layer. Therefore, there is a delay before a change in the voltage applied to the gates propagate to the output of the inverter.

4. Why is the PMOS transistor width selected almost twice that of NMOS transistor?
   The mobility of electrons is nearly twice the mobility of holes in semiconductors. Therefore, the channel resistance of a PMOS transistor is twice that of a NMOS transistor with the same dimensions. For the inverter to have the same rise and fall times, the channel resistances of both transistors need to be the same. The resistance is inversely proportional to the W/L ratio. To get the same resistance, the PMOS transistor needs to have twice the width.

5. Observe the effect by setting the same width (100u) for both PMOS and NMOS transistors.

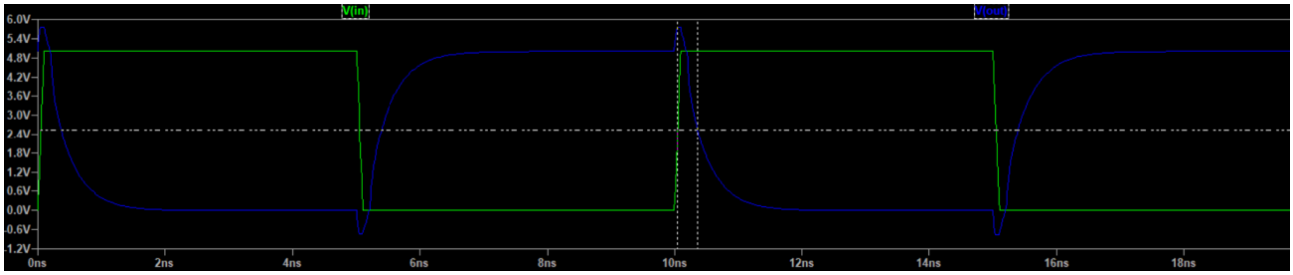

Figure 3 — The effect by setting the same width (100u) for both PMOS and NMOS transistors

With the initial parameter settings:

$$t_{rise} = 747\,\text{ps}, t_{fall} = 750\,\text{ps}$$

With the same width:

$$t_{rise} = 766\,\text{ps}, t_{fall} = 700\,\text{ps}$$

There is a significant difference between rise and fall times of the inverter.

STEP-2

1. Add the parasitic capacitances for PMOS and NMOS transistors.
2. Measure the gate delay.

$$t_{pLH} = 287\,\text{ps}$$

$$t_{pHL} = 444\,\text{ps}$$

$$\text{Gate delay} = 365.5\,\text{ps}$$

3. Justify your reading with engineering background.
   CGDO, CGSO specify the gate-to-drain and gate-to-source overlap capacitance. These occur in the regions where the gate oxide overlaps with or is close to the source or drain areas. These additional capacitances will further increase the gate delay as observed.

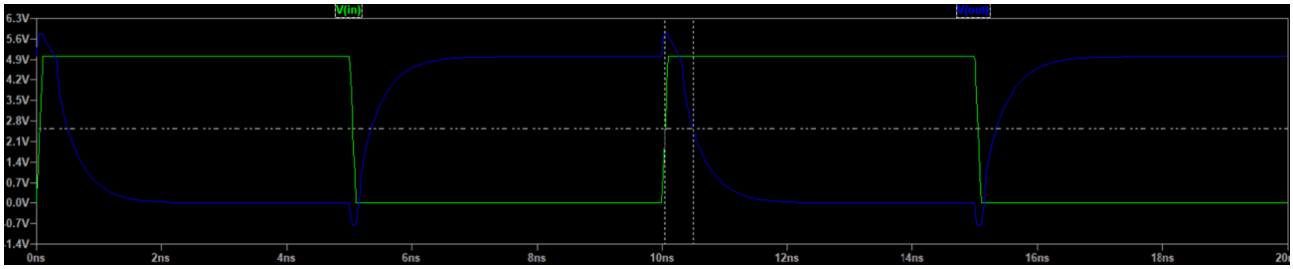

Figure 4 — Inverter output with parasitic capacitances

4. Observe the effect on frequency, rise time, and fall time of the designed NOT gate by changing L and W parameters of the PMOS and NMOS transistors.

NMOS L,W	PMOS L,W	t_{pLH}	t_{pHL}	Gate delay (ps)	Rise time (ps)	Fall time (ps)
10, 100	10, 200	287	444	365.5	747	750
10, 100	10, 100	356.4	356.4	356.4	766	700
10, 50	10, 100	294	454	374	762	762
10, 150	10, 300	263	441	352	741	726
5, 100	5, 200	111	156	133.5	210	217
15, 100	15, 200	560	945	752.5	1676	1645

According to the above observations, increasing the length of both transistors increases the propagation delay, rise time and fall time as the channel resistance increases. Increasing the width of the transistors decreases the rise and fall times due to the reduction of resistance and improved transconductance. Setting equal widths for both transistors gives unequal rise and fall times.

STEP-3

1. Ring oscillator formed using N = 7 NOT gates

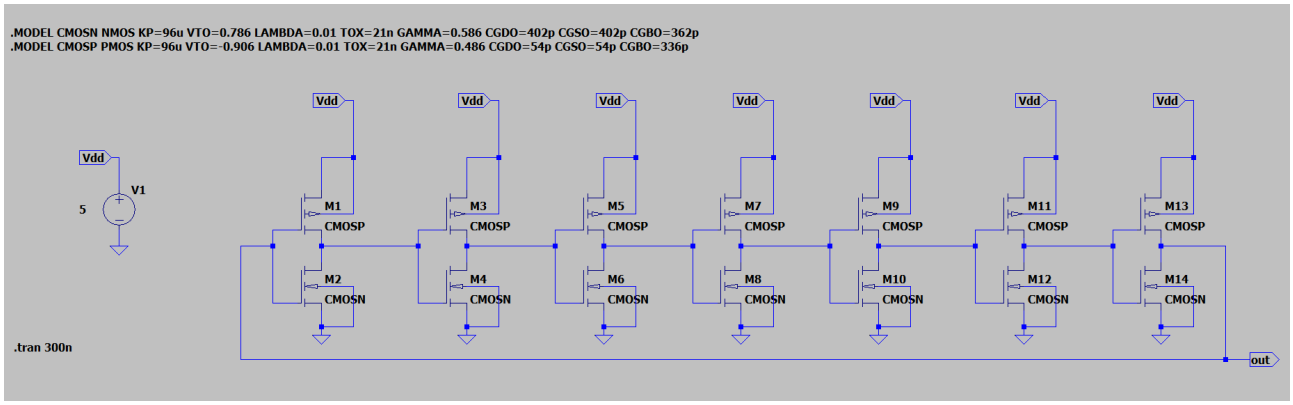

Figure 5 — Ring Oscillator

2. Observe the waveform.

3. Add an additional inverter at the output of the ring oscillator to smooth the output waveform.

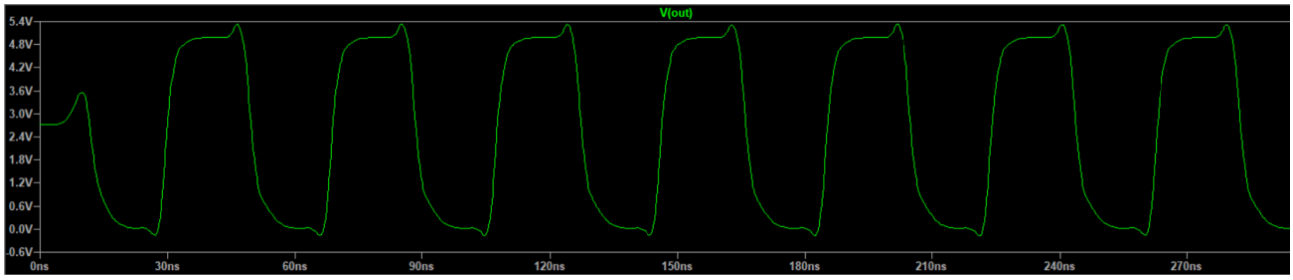

Figure 6 — Ring Oscillator (before output inverter)

The best waveform was achieved by changing the parameters of the output inverter.
NMOS: VTO=0.586 TOX=300n
PMOS: VTO=-1.106 TOX=300n

$$\text{Frequency} = 25.4\,\text{MHz}$$

$$\text{Duty cycle} = 50\ \%$$

$$t_{rise} = 0.897\,\text{ns},\quad t_{fall} = 0.633\,\text{ns},\quad \text{Period} = 39.3\ \text{ns}$$

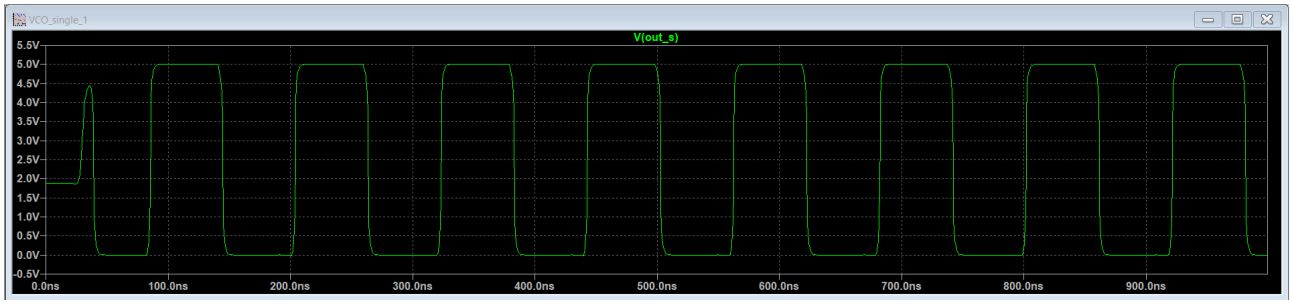

Figure 7 — After adding output inverter with modified parameters

***