Universal Controllers for PWM Converters: a Normalized Approach

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***Abstract*—Linear controllers based on small-signal models are widely used in Pulse-Width-Modulated (PWM) converters due to their simple implementation. Several compensator tuning methods for the three fundamentals DC-DC PWM converters have been developed to achieve desired closed-loop performance. However, most of the existing procedures develop compensator coefficients that depend on the actual parameters of the converter, requiring recalculation of the coefficients for different parameter combinations. This paper introduces a powerful and straightforward normalized control design tool for PWM converters. The proposed normalization technique leads to converter's models and compensator coefficients that are independent on the filter parameters, as well as the voltage and power ratings. The design of linear controllers in the normalized domain enables the direct application of the same controller to any combination of converter's parameters. A unified normalized model for the three fundamental PWM topologies is derived. A normalized controller design example for a voltage mode synchronous buck converter is shown. Simulation and experimental results for two different buck converters are presented to validate the normalization concept and highlight the strong contribution to the field made by this approach, which results in a significant asset for practicing engineers.**

***Index Terms*—Digital Control, Modeling, Normalization, PWM Converters, Linear Control,Universal Controller**

I. Introduction

PWM converters are widely used in industrial and commercial applications due to their low cost and simple implementation. Most PWM converters rely on closed-loop controllers to ensure proper regulation and reliable transient response. Traditionally, linear compensators are employed to achieve the desired dynamic characteristics. The design of these controllers is usually based on small-signal models and averaging methods [1, 2]. These techniques neglect the high frequency ripple components, and employ conventional linearization methods to understand the dynamic behavior of the power converters [3, 4].

Among the many characteristics of dynamic performance, output voltage overshoot/undershoot and recovery time are often considered the most important ones. Several tuning methods have been proposed in order to design and tune proper compensators for each one of the three fundamental DC-DC topologies: buck [5–7], boost [8–10] and buck-boost [11, 12] converters.

The implementation of digital controllers offers significant advantages such as re-programmability, reliability and simplicity. Numerous control strategies have been also proposed for the fundamental DC-DC topologies [13, 14]. However, most of the proposed methodologies obtain the corresponding compensator coefficients for a particular combination of converter's parameters, requiring the design and computation of new coefficients for diverse combinations of resonant tank elements, input-output voltages and power ratings.

This paper introduces the concept of normalized controller design procedure. The proposed methodology is illustrated in Fig. 1. The fundamental PWM converters can be translated to a normalized domain which is independent of the converter's parameters. By normalizing the sensed variables, a compensator designed in the normalized plane can be applied to any combination of PWM converter parameters, ensuring the same normalized response. It must be noted that this paper does not focus on a new control method or compensator tuning strategy, it rather focuses on a straightforward tool that can be extended to any controller design procedure. A general normalized model for the three fundamental PWM topologies is derived and, as an application example, a voltage-mode controller for the synchronous buck converter is designed and analyzed. The derived compensator coefficients are not dependent on the converter parameters other than the steady-state duty cycle and the normalized switching frequency. The method is validated with experimental results for two different buck converters employing the same normalized controller.

II. Normalization Procedure

In this section the proposed normalization procedure is introduced. The analysis is performed on the three fundamental DC-DC PWM topologies: buck, boost and buck-boost. However, this methodology can be extended for buck and noost derived topologies as inverters or PFC's.

By selecting the appropriate base parameters, the normalization procedure enables the elimination of the model dependence on inductor and capacitor values, output and input voltages, and power rating. Therefore, a valid model for any converter's parameter combination is obtained. These normalization base quantities are the filter characteristic impedance, resonant period, reference voltage (desired closed-loop output voltage) and current:

$$Z_0 = \sqrt{\frac{L}{C}}; \quad T_0 = 2\pi\sqrt{LC}; \quad v_{ref}; \quad i_{ref} = \frac{|v_{ref}|}{Z_0}$$

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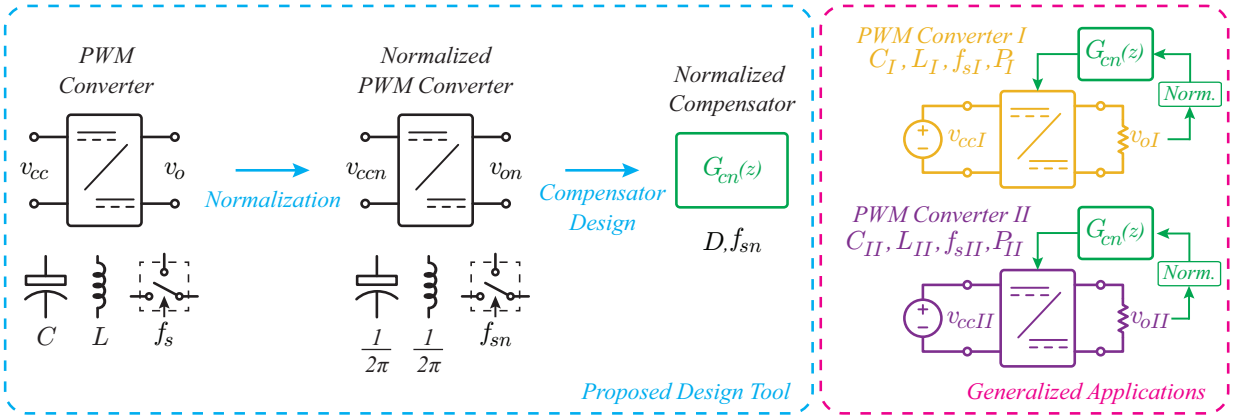

Fig. 1: Proposed normalization control design procedure. The normalized system is not dependent on the converter's parameters. The obtained compensator can be applied to different combinations.

By using the previous set of base parameters, the normalized variables can be derived as follows:

$$t_n = \frac{t}{T_0}; \quad Z_{xn} = \frac{Z_x}{Z_0}; \quad v_{xn} = \frac{v_x}{|v_{ref}|}; \quad i_{xn} = \frac{i_x}{i_{ref}}$$

The converters shown in Fig. 2 are obtained as a result of the normalization procedure. Once the normalization process is done, the capacitor and inductor values result in a normalized value of $\frac{1}{2\pi}$, while the output voltage is defined by v_{ref}. As shown, the normalized PWM topologies are independent on the converter parameters.

The behavior of each normalized power converter can be described by their corresponding differential equations:

Buck

ON

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = v_{ccn} - v_{on} \quad (1)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = i_{Ln} - i_{on} \quad (2)$$

OFF

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = -v_{on} \quad (3)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = i_{Ln} - i_{on} \quad (4)$$

Boost

ON

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = i_{ccn} \quad (5)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = -i_{on} \quad (6)$$

OFF

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = v_{ccn} - v_{on} \quad (7)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = i_{Ln} - i_{on} \quad (8)$$

Buck-Boost

ON

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = v_{ccn} \quad (9)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = i_{on} \quad (10)$$

OFF

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = v_{on} \quad (11)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = -i_{Ln} + i_{on} \quad (12)$$

By employing conventional techniques, the averaged differential equations that that represent the behavior of the normalized power converters can be obtained as follows:

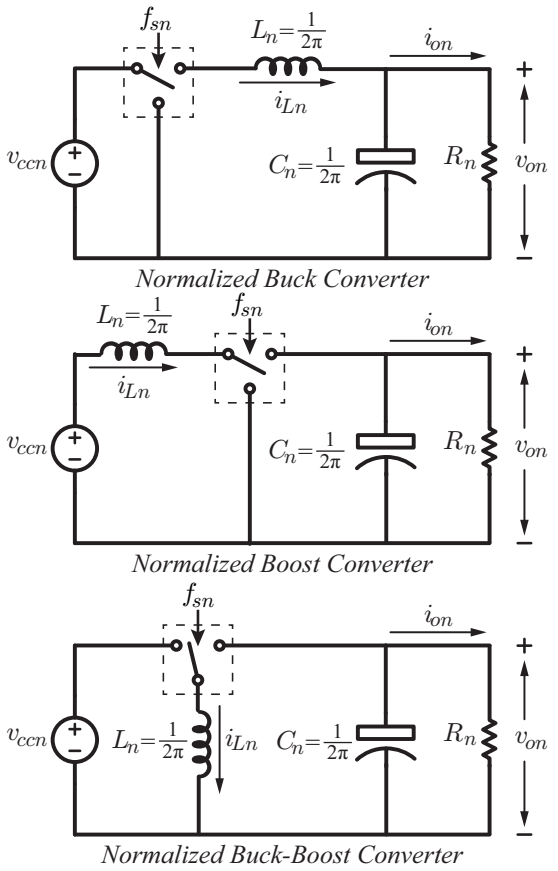

Fig. 2: The three fundamental PWM converters in the normalized domain.

Buck:

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = dV_{ccn} - v_{on} \quad (13)$$

$$\frac{1}{2\pi}\frac{dv_{on}}{d_{tn}} = i_{Ln} - I_{on} \quad (14)$$

Boost:

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = dV_{ccn} - d'v_{on} \quad (15)$$

TABLE I: Table: Normalized Coefficients

Topology	m_1	m_2	m_3	k_ω
Buck	d	1	d	1
Boost	1	1	1	d'
Buck-Boost	d	-1	d	$-d'$

$$\frac{1}{2\pi}\frac{dv_{on}}{d_{tn}} = d' i_{Ln} - I_{on} \tag{16}$$

Buck-Boost:

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = dV_{ccn} + d' v_{on} \tag{17}$$

$$\frac{1}{2\pi}\frac{dv_{on}}{d_{tn}} = -d' i_{Ln} + I_{on} \tag{18}$$

The described normalization concept can be extended to other PWM topologies as buck derived inverters and boost derived PFC's, providing a useful tool to analyze a generalized behavior of the power converters.

III. Unified Normalized Model of the Fundamental PWM Converters

As it can be observed in (13)-(17), the averaged differential equations of the three fundamental PWM converters show similar structure that can be unified to derive a normalized system of equations. By defining the auxiliar coefficients m_1, m_2, m_3 and k_ω specified in Table I, the unified model is obtained as

$$\frac{1}{2\pi}\frac{di_{Ln}}{dt_n} = m_1 V_{ccn} - k_w v_{on}, \tag{19}$$

$$\frac{1}{2\pi}\frac{dv_{on}}{dt_n} = k_w i_{Ln} - m_2\frac{v_{on}}{R_n}, \tag{20}$$

$$i_{in} = m_3 i_{Ln}, \tag{21}$$

A. Steady State Analysis

The steady-state operating points can be obtained by making the derivative terms of (19) and (20) equal to zero.

$$0 = m_1 V_{ccn} - k_w v_{on} \tag{22}$$

$$0 = k_w i_{Ln} - m_2\frac{v_{on}}{R_n} \tag{23}$$

Therefore, the steady-state operating points are given by:

$$V_{on} = \frac{M_1}{K_\omega} V_{ccn} \tag{24}$$

$$I_{Ln} = \frac{M_2}{K_\omega} I_{on} \tag{25}$$

Since the desired output voltage has been defined as the normalization base quantity, the normalized v_{on} is 1 for buck and boost converters, and -1 for the buck-boost topology. The coefficient $\frac{M_1}{K_\omega}$ determines the steady-state input voltage ratio (DC gain of the converter), and $\frac{M_2}{K_\omega}$ the steady-state ratio between output and inductor currents. By replacing the corresponding auxiliary variables, the operating conditions for the normalized fundamental PWM converters can be obtained as follows:

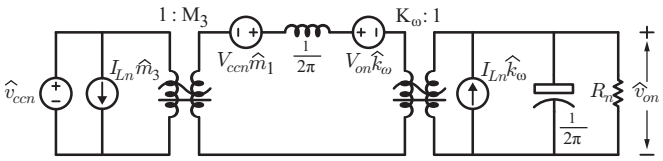

Fig. 3: Normalized small-signal equivalent circuit for the three fundamental PWM converters.

$$\text{Buck} : V_{ccn} = \frac{1}{D} \tag{26}$$

$$\text{Boost} : V_{ccn} = 1 - D \tag{27}$$

$$\text{Buck} - \text{Boost} : V_{ccn} = \frac{1}{D} - 1 \tag{28}$$

B. Small-Signal Analysis

The normalized average model can be linearized around a quiescent operating point to derive a unified small-signal model. By perturbing and linearizing (19)-(21), the normalized small-signal model is obtained as follows

$$\frac{1}{2\pi}\frac{d\hat{i}_{Ln}}{dt_n} = \left(M_1\hat{v}_{ccn} + V_{ccn}\hat{m}_1 - K_\omega\hat{v}_o - V_o\hat{k}_\omega\right) \tag{29}$$

$$\frac{1}{2\pi}\frac{d\hat{v}_{on}}{dt_n} = \left(I_L\hat{k}_\omega + K_\omega\hat{i}_{Ln} - \frac{V_{on}}{R_n}\hat{m}_2 - M_2\frac{\hat{v}_{on}}{R_n}\right) \tag{30}$$

$$\hat{i}_{inn} = \left(M_3\hat{i}_{Ln} + I_{Ln}\hat{m}_3\right) \tag{31}$$

where the averaged perturbed variables are illustrated as $x = X + \hat{x}$. The system of equations (29)-(31) can be expressed as the equivalent unified normalized circuit shown in Fig. 3. The normalized small-signal model can be solved using conventional linear circuit analysis to find useful relationships as the converter transfer functions, input impedance, and output impedance.

As shown by the developed model, the behavior of the normalized converters only depends on the operating point defined by the duty cycle D, rather than different circuit parameters. As shown in Fig. 3, the normalized small-signal model is independent of the filter parameters and input-output voltage values, providing a generalized method for analyzing PWM converters behavior. The small-signal models for the three basic PWM topologies can be obtained replacing by the corresponding coefficients.

IV. Normalized Controller

The advantages of designing compensators in the normalized space are explored in this section. The normalized domain enables the design of universal compensators which are independent of the converter's parameters, obtaining a generalized solution applicable to any combination of parameters. First, it is shown that discrete transfer functions are independent of the

sampling and the switching frequency when the normalized approach is employed. Finally, a normalized voltage-mode compensator for synchronous buck converters is shown as an example. The proposed methodology can be applied to any PWM topology and different control architectures (dual-loop control, current mode control, etc).

A. Frequency Independence of the Normalized Discrete Controller

Considering a generic transfer function of order n as:

$$G(s) = K\frac{(s+\omega_{z1})}{(s+\omega_{p1})}...\frac{(s+\omega_{zh})}{(s+\omega_{pm})} = K\frac{\prod_{i=1}^{h}(s+\omega_{zi})}{\prod_{j=1}^{m}(s+\omega_{pj})} \tag{32}$$

Where K, ω_{zi} and ω_{pj} are the gain, zeros and poles of the system respectively.

Assuming the transfer function to be part of a switching system with normalized switching frequency ω_{sn}, it is possible to represent the position of the poles and zeros as a proportion of ω_{sn}:

$$G(s) = K\frac{\prod_{i=1}^{h}(s+\alpha_i\omega_{sn})}{\prod_{j=1}^{m}(s+\beta_j\omega_{sn})} \tag{33}$$

where the coefficients α_i and β_j are the relationship between $\omega_{i,j}$ and ω_{sn}.

In order to implement the system in a digital microcontroller, the discrete-time transfer function needs to be obtained. Using bi-linear transformation $\left(s \approx \frac{2}{T_{sn}}\frac{1-z^{-1}}{1+z^{-1}}\right)$, with T_{sn} the normalized sampling time of the discrete system, the discretized system results:

$$G(z) = K\frac{\prod_{i=1}^{h}(\frac{2}{T_{sn}}\frac{1-z^{-1}}{1+z^{-1}}+\alpha_i\omega_{sn})}{\prod_{j=1}^{h}(\frac{2}{T_{sn}}\frac{1-z^{-1}}{1+z^{-1}}+\beta_j\omega_{sn})} \tag{34}$$

Conventionally, for PWM applications, the sampling frequency is set equal to the switching frequency $T_{sn} = \frac{2\pi}{\omega_{sn}}$, leading into a cancellation of terms with ω_{sn} and T_{sn} in (34):

$$G(z) = K\frac{\prod_{i=1}^{n}(2\frac{1-z^{-1}}{1+z^{-1}}+\alpha_i 2\pi)}{\prod_{j=1}^{n}(2\frac{1-z^{-1}}{1+z^{-1}}+\beta_j 2\pi)} \tag{35}$$

$$G(z) = K\frac{\prod_{i=1}^{n}\left[(1-z^{-1})+\alpha_i\pi(1+z^{-1})\right]}{\prod_{j=1}^{n}\left[(1-z^{-1})+\beta_j(\pi 1+z^{-1})\right]} \tag{36}$$

As it can be concluded from (36), for $T_{sn} = \frac{1}{f_{sn}}$, the coefficients of the system remain invariant. Therefore, assuming $G(z)$ a compensator designed in the normalized domain, the same compensator can be applied to an infinite number of PWM converters with any combination of parameters, achieving the same normalized response.

B. Application Example: Normalized Voltage-mode Buck Converter

By using the model of Fig. 3, and replacing the corresponding parameters of Table I, the normalized expression for the control to output transfer function in the normalized buck converter is derived as:

TABLE II: Table: Compensator Coefficients

$a_1 = 2N_1$	$a_2 = N_1(2+N_1)$	$a_3 = N_1^2$
$b_1 = 2N_2 - 1$	$b_2 = N_2(1-2N_2)$	$b_3 = -N_2^2$
	$K_c = \left(\frac{\Delta B+\pi\sqrt{P}}{\pi+\Delta B\sqrt{P}}\right)^2 \frac{Df_{sn}^2}{(\Delta B)^2}$	
$P = \frac{1-\sin(\phi_m)}{1+\sin(\phi_m)}$	$N1 = \frac{\pi\sqrt{P}-\Delta B}{\pi\sqrt{P}+\Delta B}$	$N2 = \frac{\pi-\Delta B\sqrt{P}}{\pi+\Delta B\sqrt{P}}$

$$G_{dvn}(s) = \frac{1}{D}\frac{1}{(\frac{s}{2\pi})^2+\frac{s}{2\pi R_n}+1} \tag{37}$$

As it can be observed from (37), the characteristic double pole of the buck convert is located at the normalized natural frequency $\omega_{0n} = 2\pi$, and it does not depend on any particular values of L and C. At the same time, the static gain G_{dvn0} does not depend on the input voltage of the converter, and it is just defined by the steady-state duty cycle D. In this way, the transfer function of the system is the same for any set of buck converters operating with the same duty cycle, independently on their filter parameters, or input and output voltages.

By analyzing the transfer function in (37), a lead compensator can be employed in order to achieve the desired phase margin (ϕ_m) at a given crossover frequency (f_c). A proportional integral (PI) compensator is also included, in order to provide zero steady-state error at the output voltage. As the compensator is implemented in a microcontroller, the effects of the digital implementation must be considered in order to achieve stable operation. The effects of the sampling and computational delay can be approximated as a first order system with a time constant equal to one and half of the normalized sampling period T_{sn}. The effect of the computational delay is a significant phase reduction for frequencies close to the Nyquist frequency, and it can be computed as $\phi_{delay} = -540\frac{f}{f_{sn}}$. Therefore an extra lead compensator is added in order to account the effects of the sampling. Finally, the proposed compensator in the continuous domain is a three-poles-three-zeros (3P3Z):

$$G_c(s) = K_c\left(1+\frac{\omega_L}{s}\right)\left(\frac{1+\frac{s}{w_{z1}}}{1+\frac{s}{w_{p1}}}\right)\left(\frac{1+\frac{s}{w_{z2}}}{1+\frac{s}{w_{p2}}}\right) \tag{38}$$

Conventional tuning methods are employed for designing the voltage compensator coefficients. For a desired ϕ_m at a given f_c, the pole and zero of the lead compensator can be obtained as follows:

$$f_z = f_c\sqrt{\frac{1-\sin\phi_m}{1+\sin\phi_m}}; \quad f_p = f_c\sqrt{\frac{1+\sin\phi_m}{1-\sin\phi_m}} \tag{39}$$

The position of the poles and zeros of (38) can be written in function of the normalized switching frequency by defining the desired $f_c = \frac{f_{sn}}{\Delta B}$, with ΔB as the relationship between the desired bandwidth and the normalized switching frequency $\left(\frac{f_{sn}}{f_c}\right)$, and $f_L = \frac{f_{0n}}{10} = 0.1$. Therefore, the gain of the

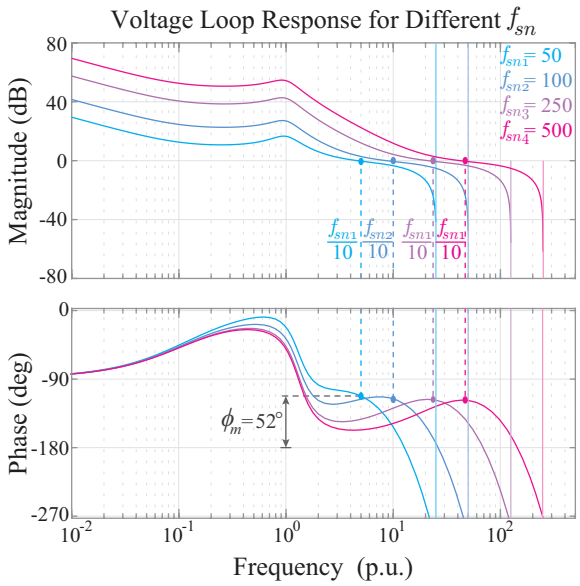

Fig. 4: Voltage loop response for the normalized buck converter with normalized compensator for different f_{sn}.

compensator to achieve the desired f_c can be derived as:

$$K_c = D\frac{f_{sn}}{\Delta B}^2 \sqrt{\frac{1-\sin\phi_m}{1+\sin\phi_m}} \tag{40}$$

The continuous compensator can be mapped into the discrete domain by using the bilinear transformation. Rearranging terms, it results:

$$G_c(z) = K_c \frac{1+a_1z^{-1}+a_2z^{-2}+a_3z^{-3}}{1+b_1z^{-1}+b_2z^{-2}+b_3z^{-3}} \tag{41}$$

The coefficients a_i, b_i and K_c can be defined as functions of the constants values detailed in Table II. As shown, the obtained expressions are independent of the converter's parameters. The factor K_c is the only term of the compensator that depends on the converter's operating point D and the normalized switching frequency f_{sn}.

For example, for design requirements $\phi_m = 52°$ and $\Delta B = 10$, the compensator is obtained as

$$G_c(z) = 0.027Df_{sn}^2 \frac{1-2.58z^{-1}+2.21z^{-2}-0.63z^{-3}}{1-1.14z^{-1}+0.15z^{-2}-0.0054z^{-3}} \tag{42}$$

By normalizing the sensed variables, this compensator can be applied to any buck converter with different combinations of L, C, v_{cc} and v_o.

The voltage loop response for the normalized buck converter for different f_{sn} employing the voltage compensator of (42) is shown in Fig. 4. As shown, different loop responses have the same ϕ_m and relative bandwidth ΔB.

V. Simulation and Experimental Results

In this section the simulation and experimental results for two different buck converters using the same normalized compensator are analyzed. The parameters of each converter are summarized in Table III.

TABLE III: Table: Experimental Parameters

Parameter	Buck I	Buck II
V_{cc}	24 V	36 V
V_{ref}	12 V	18 V
L	240 μH	508 μH
C	24 μF	33.3 μF
Z_0	3.16 Ω	3.90 Ω
T_0	476.86 μs	817 μs
f_s	104 kHz	61 kHz

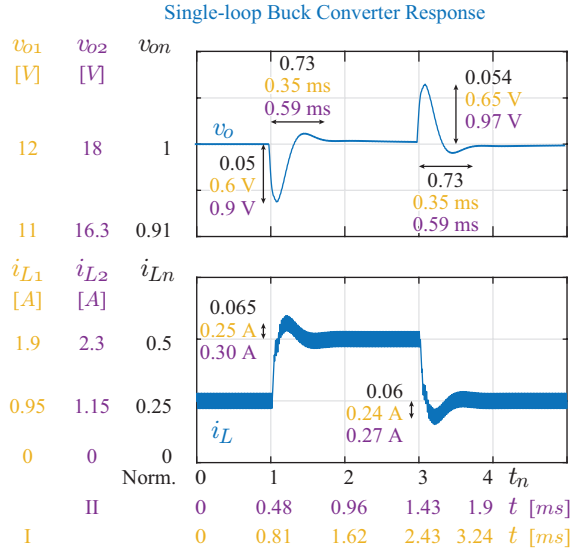

Fig. 5: Step response for two different buck converters. The responses of the two buck converter are identical to the normalized response.

The time domain response for the two different buck converters and the normalized one with $f_{sn} = 50$ under a current load step is shown in Fig 5. The illustrated response shows the same normalized dynamics for the three converters. As shown, for different Z_o and T_o, and the same normalized compensator, the system displays the same normalized closed-loop responses in terms of recovery time and overshoot values.

The experimental results for the two different buck converters of Table III are shown in Fig. 6 and 7. Both converters operate with the normalized compensator derived in the previous section for $f_{sn} = 50$.

The frequency response of the voltage loop is illustrated in Fig. 6. Both loops have the same normalized responses, with closed-loop bandwidth of about ten times smaller than their corresponding switching frequency, $10.6(9.41kHz)$ and $9.1(6.81kHz)$ times, and phase margin of $50.91°$ and $51.24°$ for buck I and II respectively.

The time domain response for a load step from 0.25 to 0.5 of the normalized current of each converter is illustrated in Fig. 7. As shown, the load step amplitudes, current and voltage

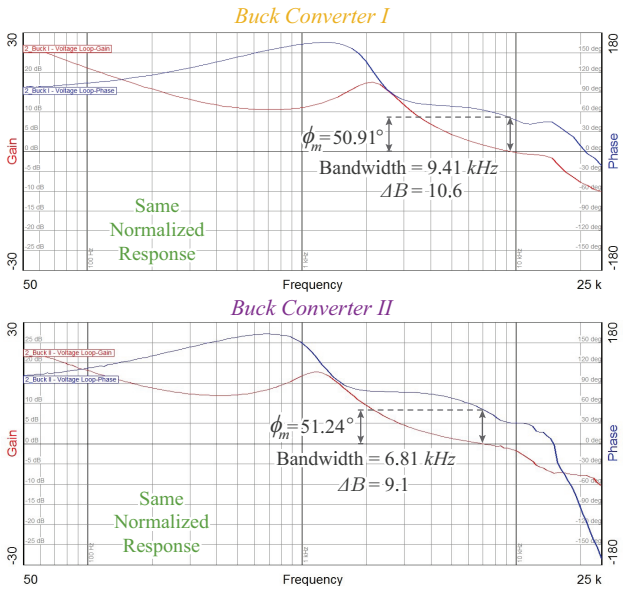

Fig. 6: Experimental voltage loop response for buck I and II using the same normalized compensator.

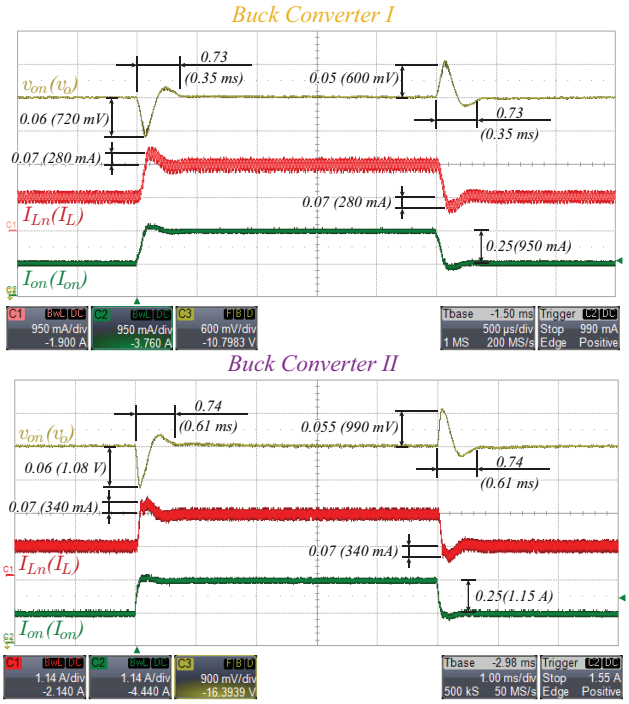

Fig. 7: Experimental voltage loop response for buck I and II using the same normalized compensator.

overshoot and recovery times are different for each converters. However, both systems show similar transient responses with the same normalized settling time and overshoot values. For buck I, the normalized settling time is 0.72 (0.5 ms), and it is 0.73 (0.35ms) for buck II, while the normalized voltage and current overshoots are around 0.06 and 0.07 respectively.

VI. Conclusions

In this paper, a straightforward normalized controller design procedure for PWM converters is introduced. The proposed normalization method leads to models that are independent from the filter component parameters, power ratings, and input and output voltages. A design example for a voltage mode compensator for buck converters was derived and analyzed. The obtained compensator is independent of most of the converter parameters, and it only depends on the normalized switching frequency and the steady-state duty cycle. Experimental results for two buck converters employing the normalized compensator were provided in order to validate the proposed methodology. This work introduces a normalized approach that enables obtaining a set of universal controllers for PWM converters, which can be successfully implemented in converters with any combination of parameters. This contribution represents a direct and important asset for practicing engineers.

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