Worksheet 2.4 or 7

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Branch: BE-CSE (LEET)
Section/Group: ON20BCS-809/A
Semester: 4th Sem
Date of Performance: 01/04/2022
Subject Name: MPI Lab
Subject Code: 22E-20CSP-253

1. Aim/Overview of the practical:

a) Shift Left 16-bit number by 1bity.
b) Shift Left 16-bit number by 2bit.

2. Task to be done:

Write an 8085 Microprocessor program to shift left of 16-bit number by 1bt and 2bit.

3. Apparatus/Simulator used (For applied/experimental sciences/materials-based labs):

I. 8085 Jubin simulator version 2 (Microprocessor Simulator)
II. Java (jdk/ jre1.8.0_321)

4. Algorithm/Flowchart (For programming-based labs):

Algorithm to find left shift of 16-bit number by 1bit:

I. Load the data to the HL pair from 2000, 2001 memory address.
II. Add the HL pair with the same to find the 1bit Left shift using DAD.
III. Store the 1bit left shifted value from HL pair to 2002,2003 memory location.
IV. End the execution using HLT.

Algorithm to find left shift of 8-bit number by 2bit:

I. Load the data to the HL pair from 2000, 2001 memory address.
II. Add the HL pair with the same to find the 1bit Left shift using DAD.
III. Add the HL pair with the same to find the 2bit Left shift using DAD
IV. Store the 1bit left shifted value from HL pair to 2002,2003 memory location.
V. End the execution using HLT.

5. Description/ Code:

Program to find the left shift of 16-bit number by 1bit:

```
# ORG 1000H
        LHLD 2000
        DAD H
```

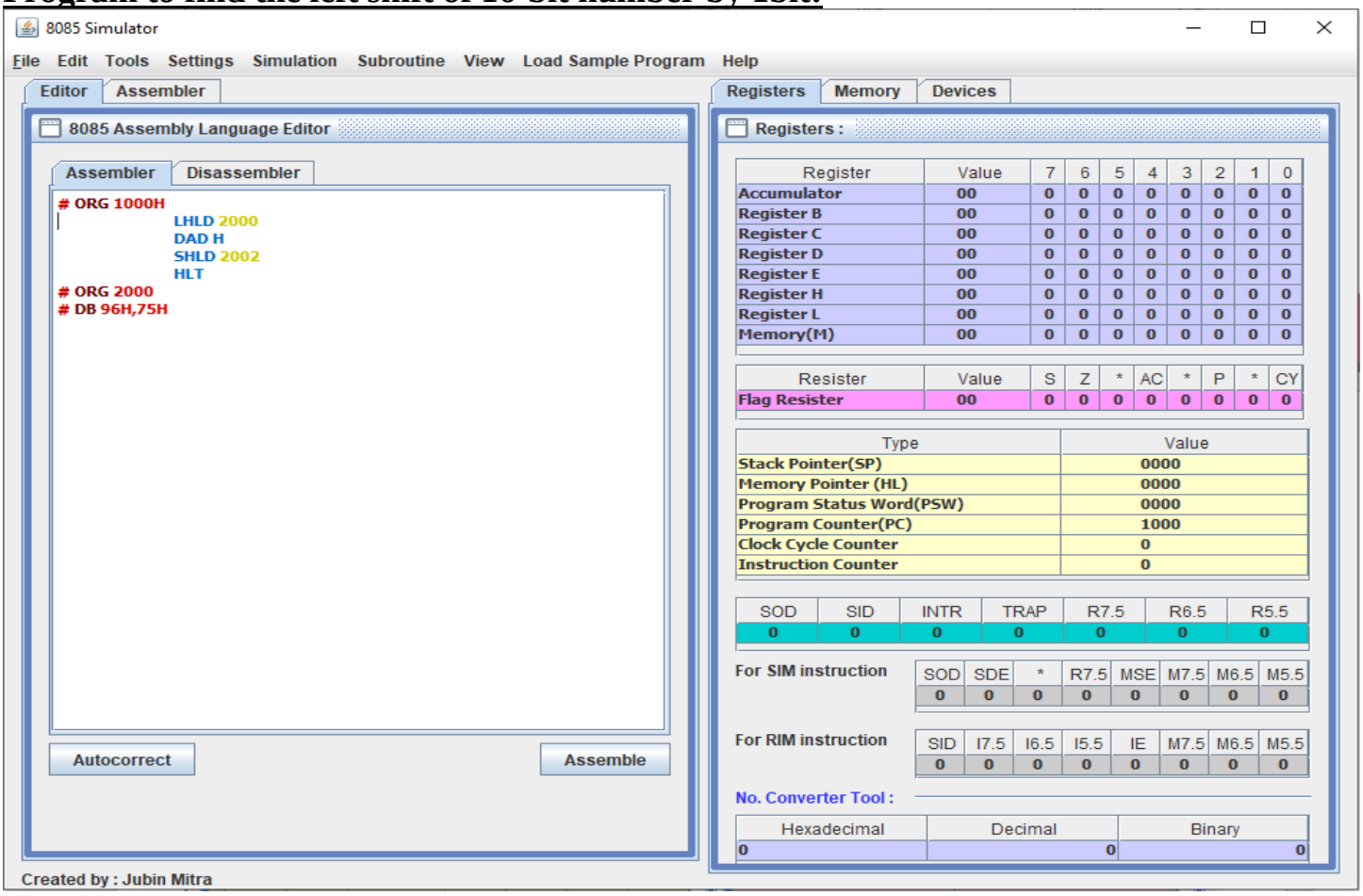
```
        SHLD 2002
        HLT
# ORG 2000H
# DB 96H,75H
```

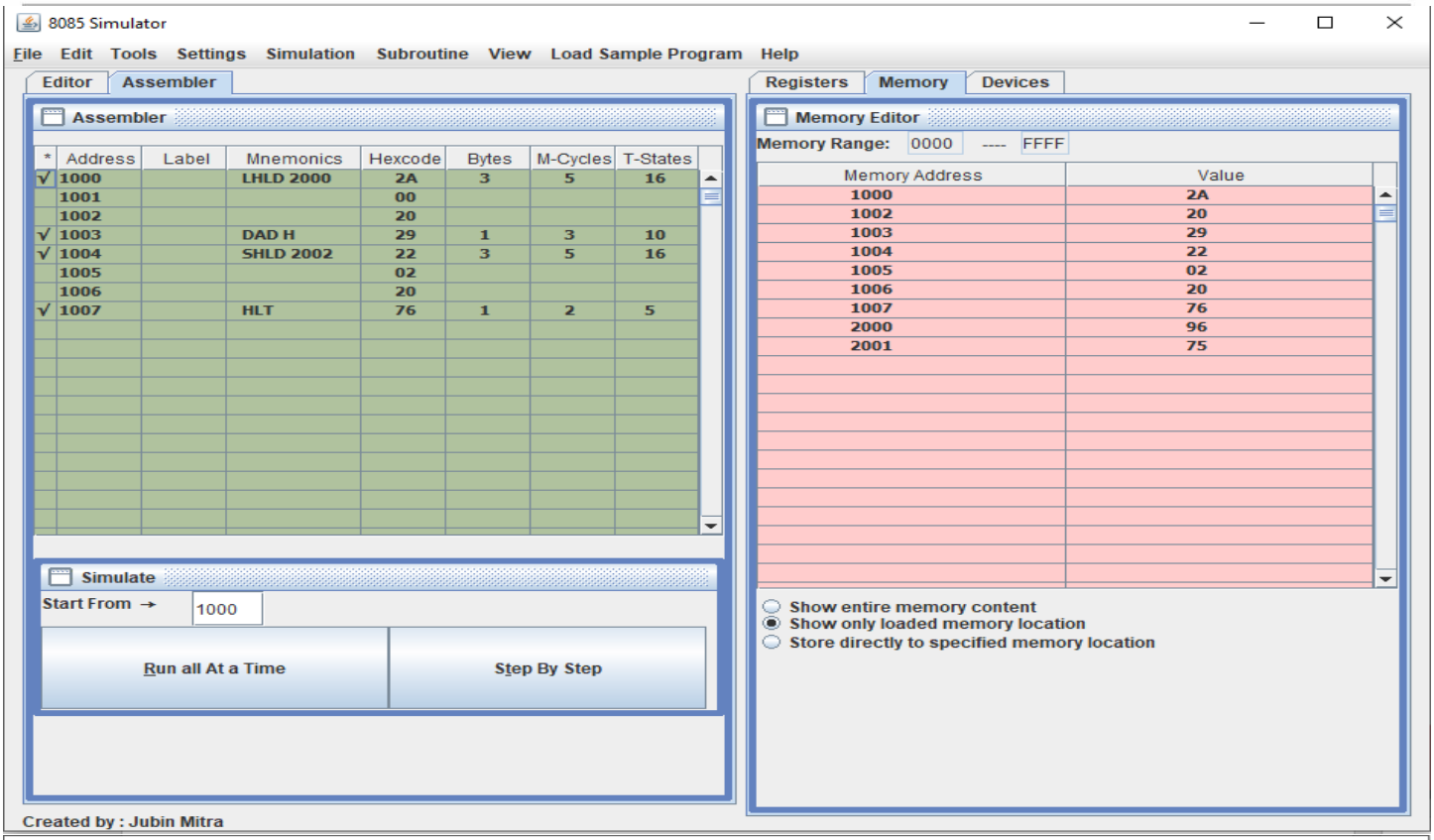
Program to find the left shift of 16-bit number by 2bit:

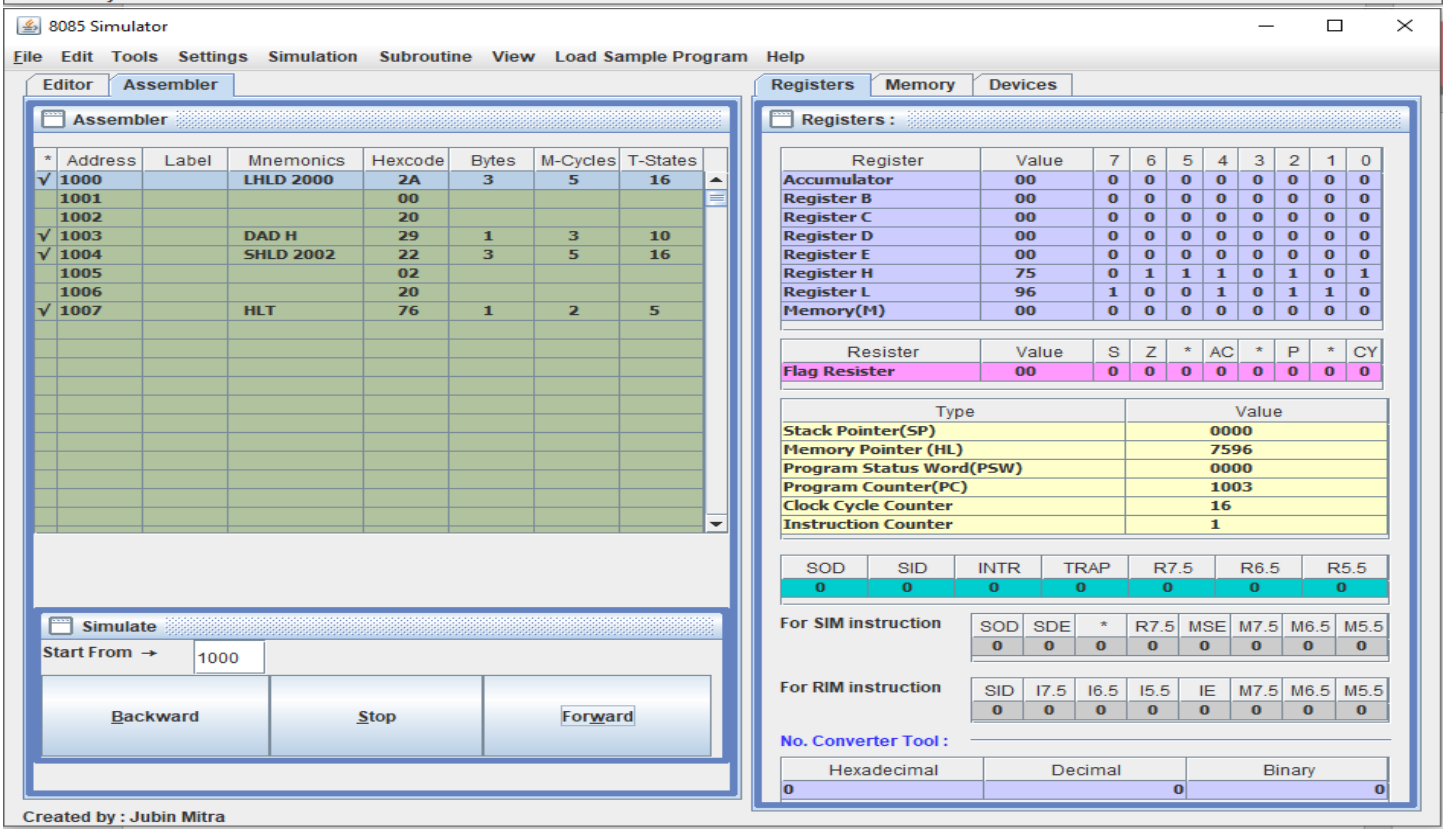
```
# ORG 1000H
        LHLD 2000
        DAD H
        DAD H
        SHLD 2002
        HLT
# ORG 2000H
#DB 96H,75H
```

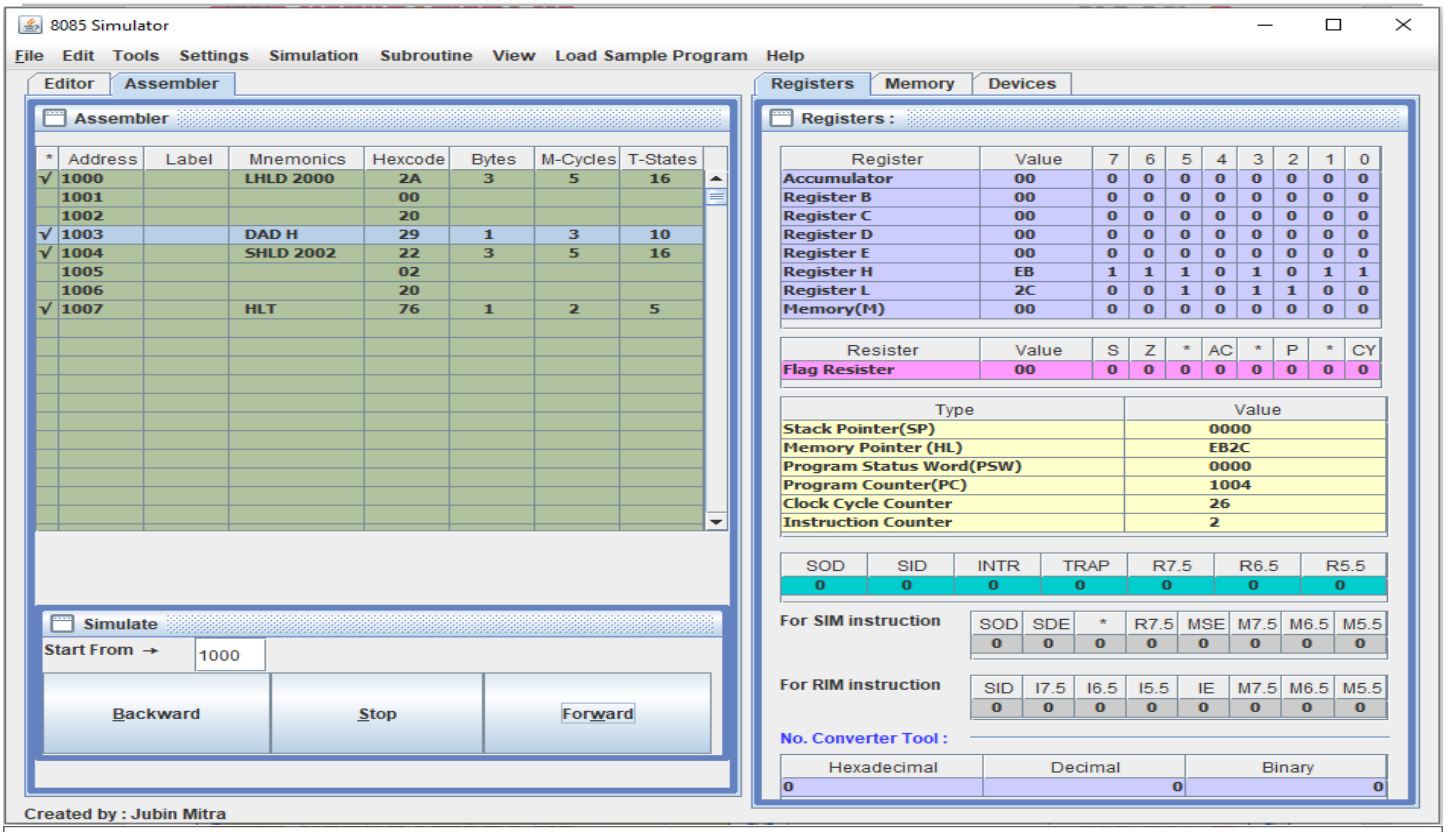
6. Result/Output/Writing Summary:

Program to find the left shift of 16-bit number by 1bit:




8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LHLD 2000 2A 3 5 16
1001 00
1002 20
√ 1003 DAD H 29 1 3 10
√ 1004 SHLD 2002 22 3 5 16
1005 02
1006 20
√ 1007 HLT 76 1 2 5
Simulate
Start From → 1000
Run all At a Time
Step By Step
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
1000 2A
1002 20
1003 29
1004 22
1005 02
1006 20
1007 76
2000 96
2001 75
Show entire memory content
Show only loaded memory location
Store directly to specified memory location
Created by : Jubin Mitra


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LHLD 2000 2A 3 5 16
1001 00
1002 20
√ 1003 DAD H 29 1 3 10
√ 1004 SHLD 2002 22 3 5 16
1005 02
1006 20
√ 1007 HLT 76 1 2 5
Simulate
Start From → 1000
Backward
Stop
Forward
Registers Memory Devices
Registers :
Register Value 7 6 5 4 3 2 1 0
Accumulator 00 0 0 0 0 0 0 0 0
Register B 00 0 0 0 0 0 0 0 0
Register C 00 0 0 0 0 0 0 0 0
Register D 00 0 0 0 0 0 0 0 0
Register E 00 0 0 0 0 0 0 0 0
Register H 75 0 1 1 1 0 1 0 1
Register L 96 1 0 0 1 0 1 1 0
Memory(M) 00 0 0 0 0 0 0 0 0
Resister Value S Z * AC * P * CY
Flag Resister 00 0 0 0 0 0 0 0 0
Type Value
Stack Pointer(SP) 0000
Memory Pointer (HL) 7596
Program Status Word(PSW) 0000
Program Counter(PC) 1003
Clock Cycle Counter 16
Instruction Counter 1
SOD SID INTR TRAP R7.5 R6.5 R5.5
0 0 0 0 0 0 0
For SIM instruction
SOD SDE * R7.5 MSE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
For RIM instruction
SID I7.5 I6.5 I5.5 IE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
No. Converter Tool :
Hexadecimal Decimal Binary
0 0 0
Created by : Jubin Mitra



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		SHLD 2002	22	3	5	16
	1005			02			
	1006			20			
√	1007		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	EB	1	1	1	0	1	0	1	1
Register L	2C	0	0	1	0	1	1	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

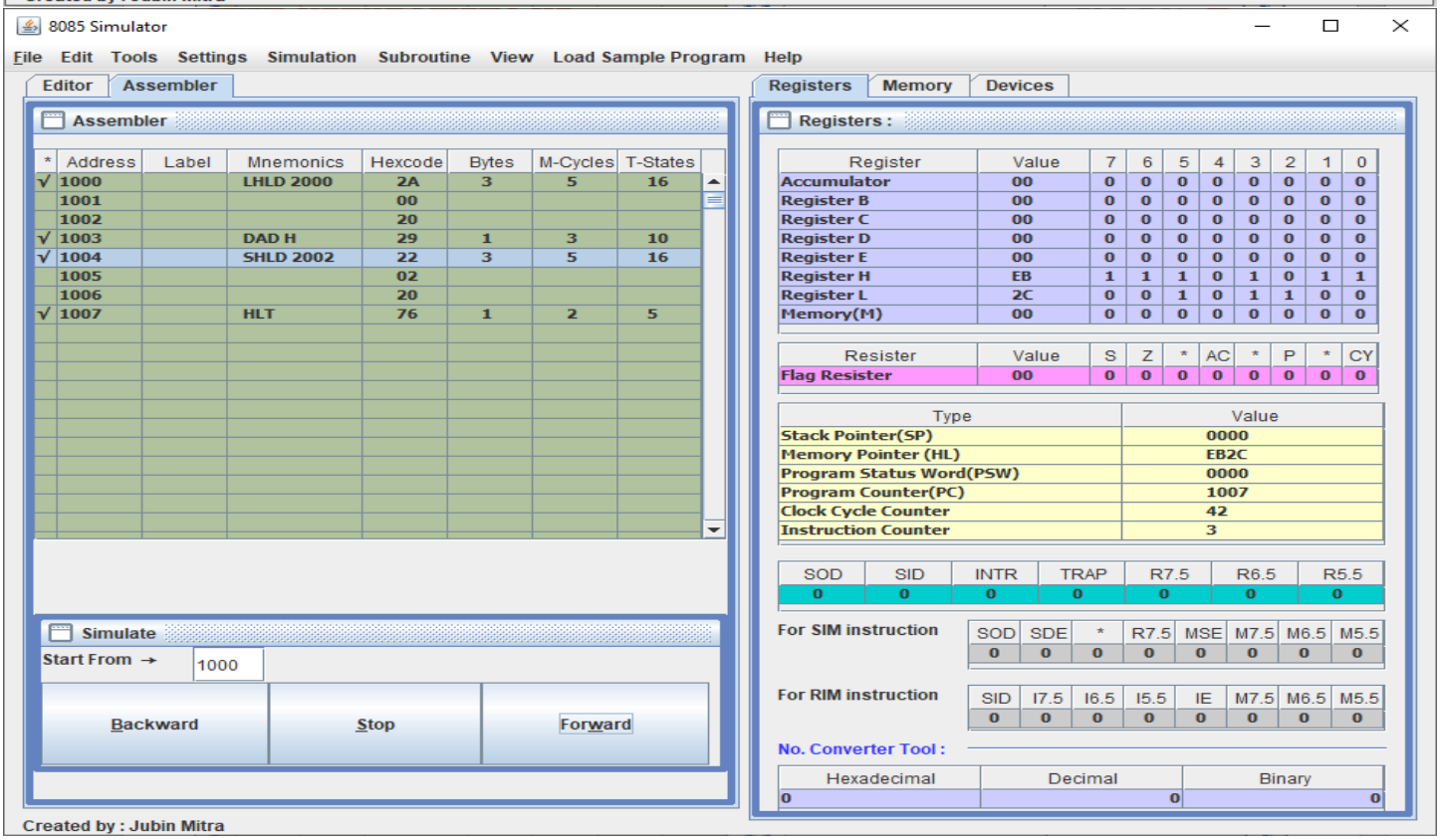
Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	EB2C
Program Status Word(PSW)	0000
Program Counter(PC)	1004
Clock Cycle Counter	26
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

Hexadecimal	Decimal	Binary
0	0	0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		SHLD 2002	22	3	5	16
	1005			02			
	1006			20			
√	1007		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	EB	1	1	1	0	1	0	1	1
Register L	2C	0	0	1	0	1	1	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

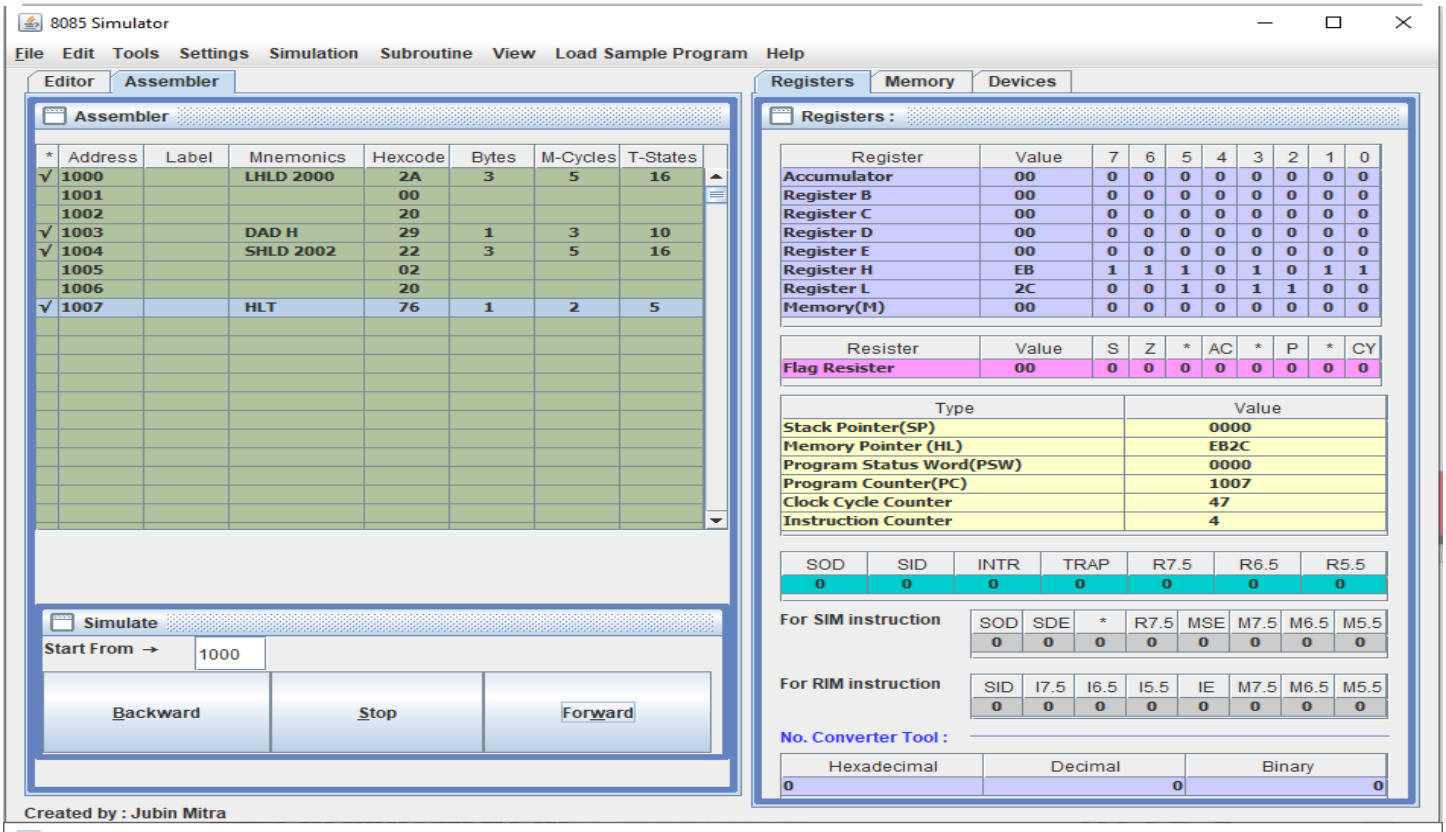
Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	EB2C
Program Status Word(PSW)	0000
Program Counter(PC)	1007
Clock Cycle Counter	42
Instruction Counter	3

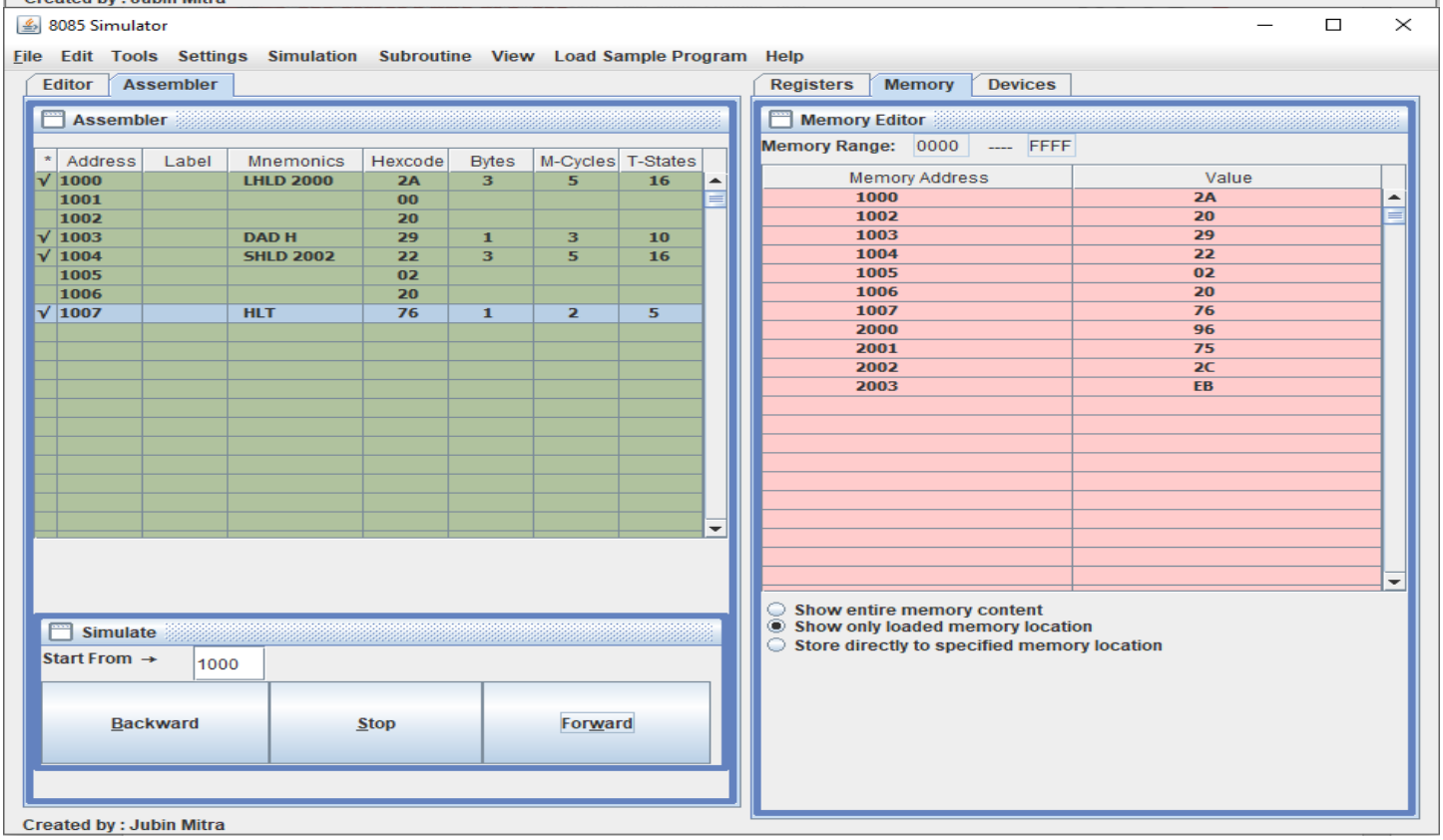
SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

Hexadecimal	Decimal	Binary
0	0	0


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LHLD 2000 2A 3 5 16
1001 00
1002 20
√ 1003 DAD H 29 1 3 10
√ 1004 SHLD 2002 22 3 5 16
1005 02
1006 20
√ 1007 HLT 76 1 2 5
Simulate
Start From → 1000
Backward Stop Forward
Created by : Jubin Mitra
Registers Memory Devices
Registers :
Register Value 7 6 5 4 3 2 1 0
Accumulator 00 0 0 0 0 0 0 0 0
Register B 00 0 0 0 0 0 0 0 0
Register C 00 0 0 0 0 0 0 0 0
Register D 00 0 0 0 0 0 0 0 0
Register E 00 0 0 0 0 0 0 0 0
Register H EB 1 1 1 0 1 0 1 1
Register L 2C 0 0 1 0 1 1 0 0
Memory(M) 00 0 0 0 0 0 0 0 0
Resister Value S Z * AC * P * CY
Flag Resister 00 0 0 0 0 0 0 0 0
Type Value
Stack Pointer(SP) 0000
Memory Pointer (HL) EB2C
Program Status Word(PSW) 0000
Program Counter(PC) 1007
Clock Cycle Counter 47
Instruction Counter 4
SOD SID INTR TRAP R7.5 R6.5 R5.5
0 0 0 0 0 0 0
For SIM instruction
SOD SDE * R7.5 MSE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
For RIM instruction
SID I7.5 I6.5 I5.5 IE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
No. Converter Tool :
Hexadecimal Decimal Binary
0 0 0


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LHLD 2000 2A 3 5 16
1001 00
1002 20
√ 1003 DAD H 29 1 3 10
√ 1004 SHLD 2002 22 3 5 16
1005 02
1006 20
√ 1007 HLT 76 1 2 5
Simulate
Start From → 1000
Backward Stop Forward
Created by : Jubin Mitra
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
1000 2A
1002 20
1003 29
1004 22
1005 02
1006 20
1007 76
2000 96
2001 75
2002 2C
2003 EB
Show entire memory content
Show only loaded memory location
Store directly to specified memory location

Program to find the left shift of 16-bit number by 2bit:

8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

8085 Assembly Language Editor

Assembler Disassembler

```
# ORG 1000H
        LHLD 2000
        DAD H
        DAD H
        SHLD 2002
        HLT
# ORG 2000
# DB 96H,75H
```

Autocorrect Assemble

Registers Memory Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	1000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra

8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		DAD H	29	1	3	10
√	1005		SHLD 2002	22	3	5	16
	1006			02			
	1007			20			
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Run all At a Time Step By Step

Registers Memory Devices

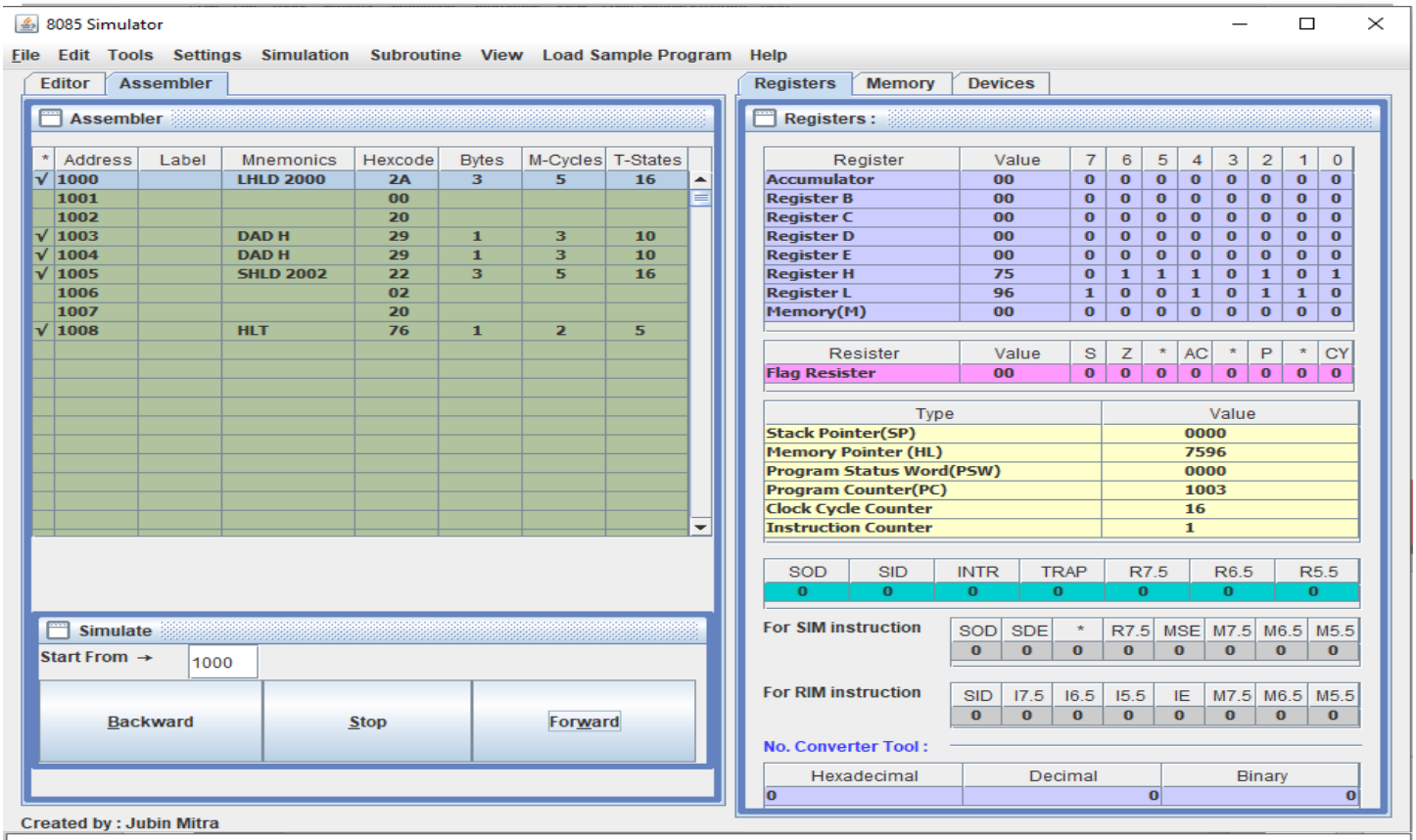
Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
1000	2A
1002	20
1003	29
1004	29
1005	22
1006	02
1007	20
1008	76
2000	96
2001	75

Show entire memory content
Show only loaded memory location
Store directly to specified memory location

Created by : Jubin Mitra



8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		DAD H	29	1	3	10
√	1005		SHLD 2002	22	3	5	16
	1006			02			
	1007			20			
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	75	0	1	1	1	0	1	0	1
Register L	96	1	0	0	1	0	1	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	7596
Program Status Word(PSW)	0000
Program Counter(PC)	1003
Clock Cycle Counter	16
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

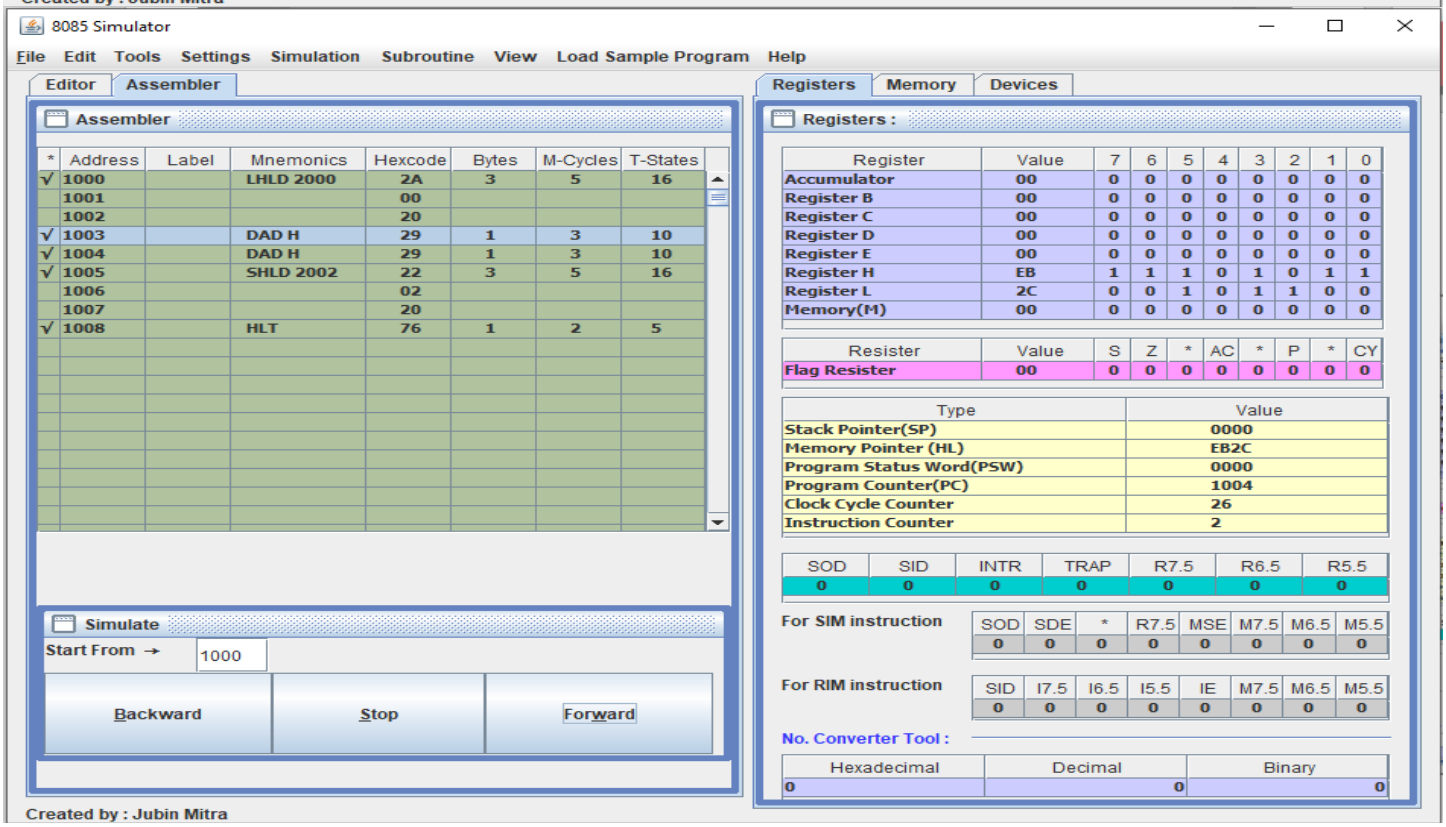
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		DAD H	29	1	3	10
√	1005		SHLD 2002	22	3	5	16
	1006			02			
	1007			20			
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	EB	1	1	1	0	1	0	1	1
Register L	2C	0	0	1	0	1	1	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	EB2C
Program Status Word(PSW)	0000
Program Counter(PC)	1004
Clock Cycle Counter	26
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

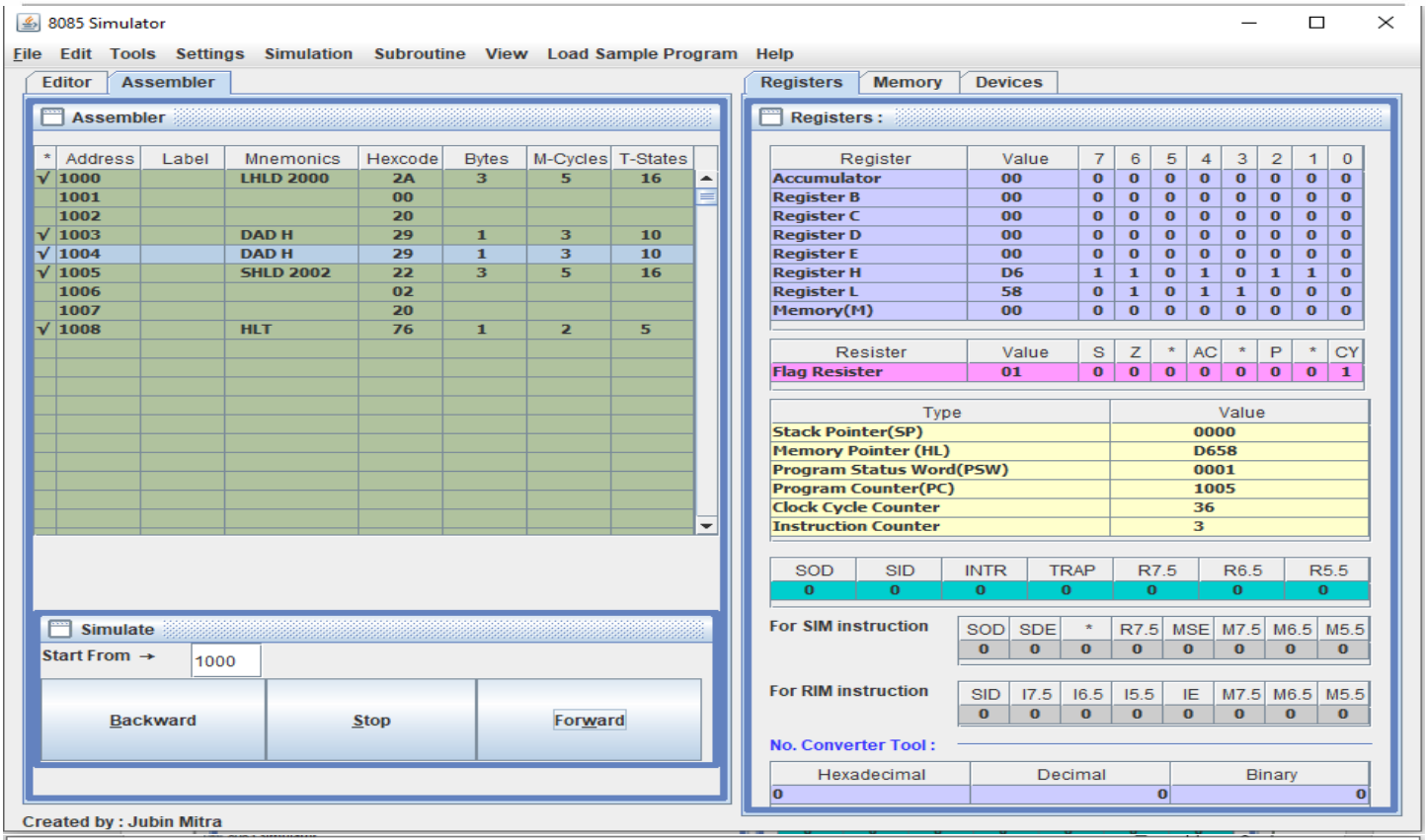
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		DAD H	29	1	3	10
√	1005		SHLD 2002	22	3	5	16
	1006			02			
	1007			20			
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	D6	1	1	0	1	0	1	1	0
Register L	58	0	1	0	1	1	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	01	0	0	0	0	0	0	0	1

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	D658
Program Status Word(PSW)	0001
Program Counter(PC)	1005
Clock Cycle Counter	36
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

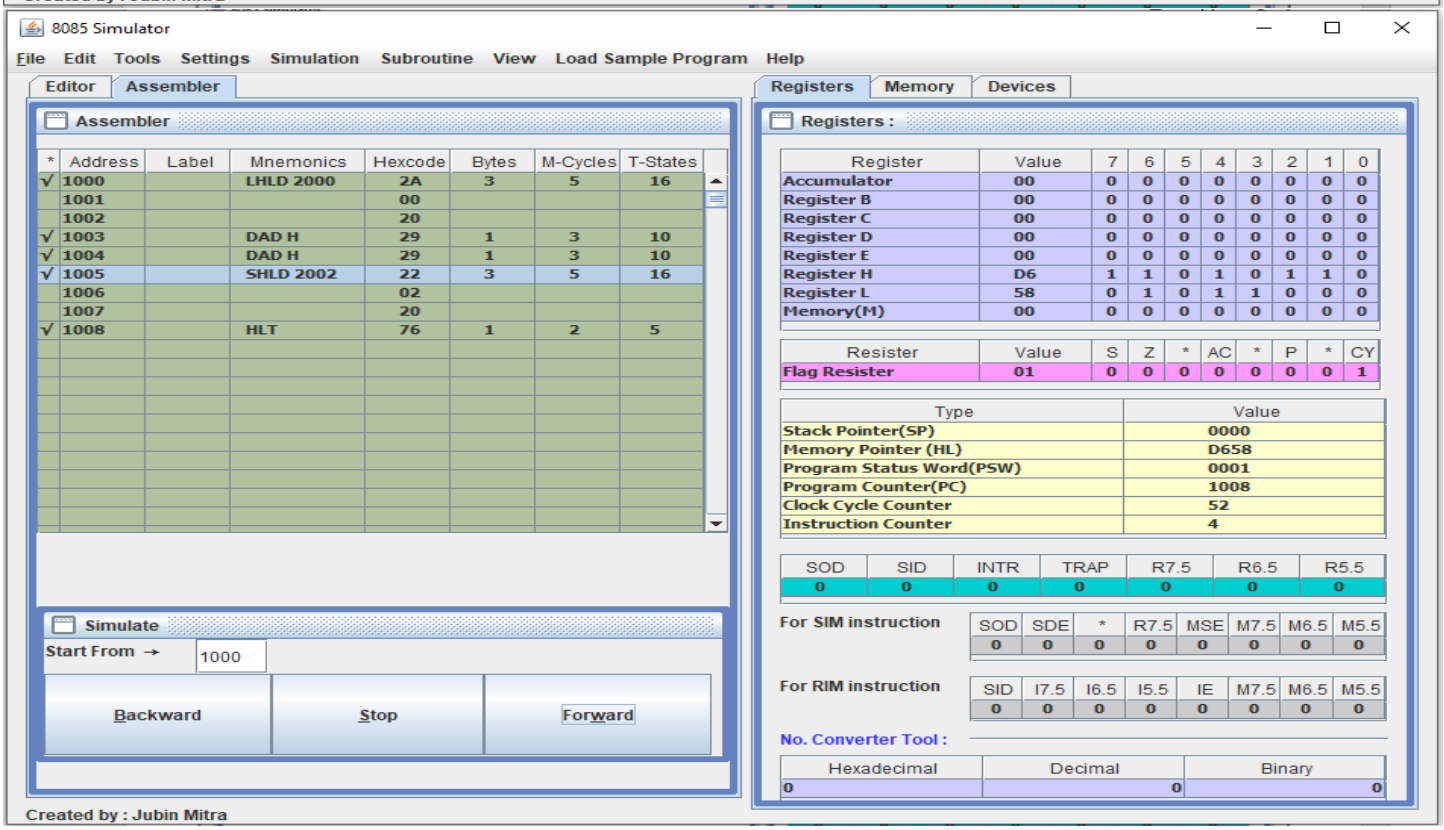
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LHLD 2000	2A	3	5	16
	1001			00			
	1002			20			
√	1003		DAD H	29	1	3	10
√	1004		DAD H	29	1	3	10
√	1005		SHLD 2002	22	3	5	16
	1006			02			
	1007			20			
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	D6	1	1	0	1	0	1	1	0
Register L	58	0	1	0	1	1	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	01	0	0	0	0	0	0	0	1

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	D658
Program Status Word(PSW)	0001
Program Counter(PC)	1008
Clock Cycle Counter	52
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

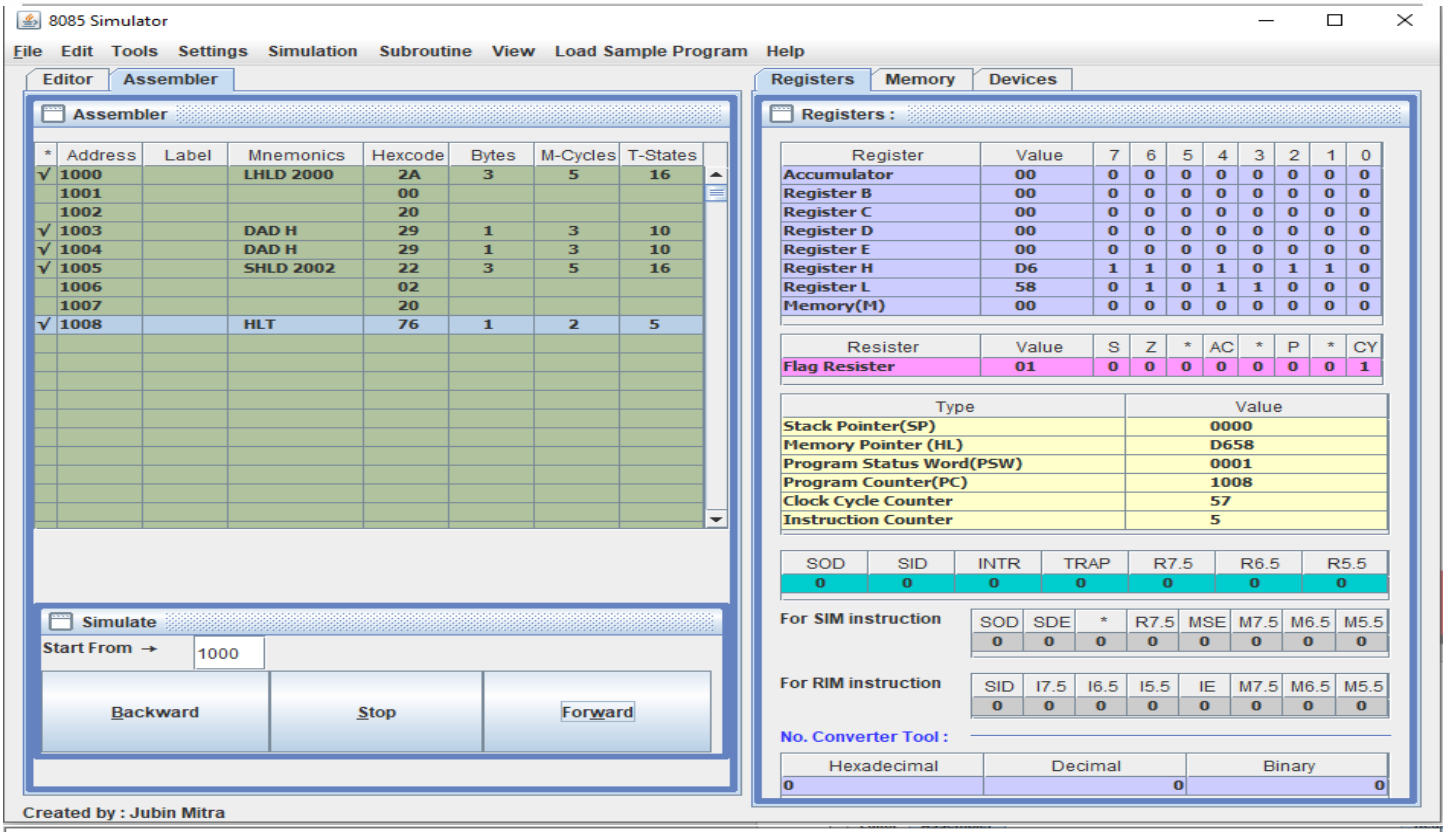
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

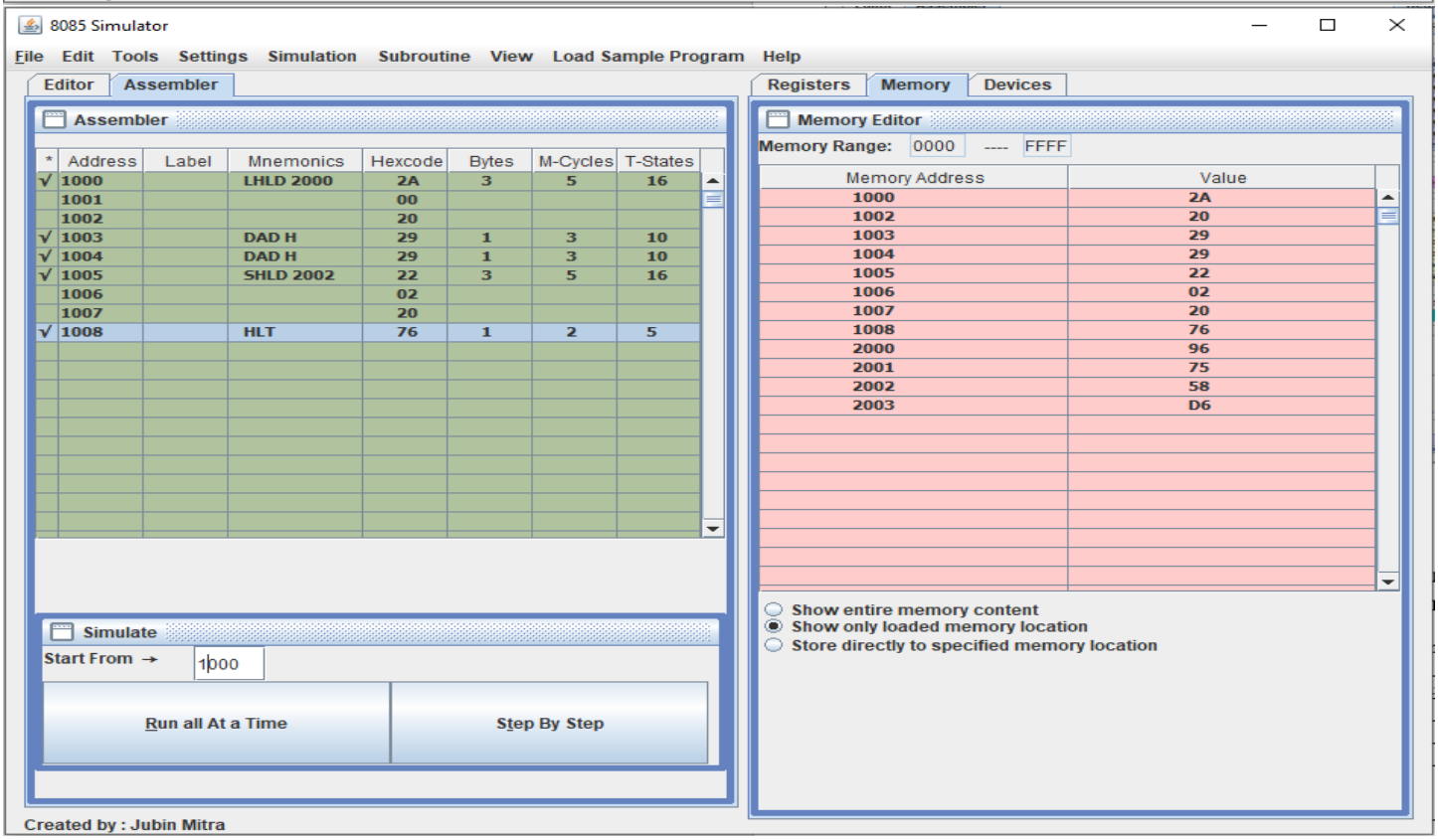
For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LHLD 2000 2A 3 5 16
1001 00
1002 20
√ 1003 DAD H 29 1 3 10
√ 1004 DAD H 29 1 3 10
√ 1005 SHLD 2002 22 3 5 16
1006 02
1007 20
√ 1008 HLT 76 1 2 5
Simulate
Start From → 1000
Backward Stop Forward
Created by : Jubin Mitra
Registers Memory Devices
Registers :
Register Value 7 6 5 4 3 2 1 0
Accumulator 00 0 0 0 0 0 0 0 0
Register B 00 0 0 0 0 0 0 0 0
Register C 00 0 0 0 0 0 0 0 0
Register D 00 0 0 0 0 0 0 0 0
Register E 00 0 0 0 0 0 0 0 0
Register H D6 1 1 0 1 0 1 1 0
Register L 58 0 1 0 1 1 0 0 0
Memory(M) 00 0 0 0 0 0 0 0 0
Resister Value S Z * AC * P * CY
Flag Resister 01 0 0 0 0 0 0 0 1
Type Value
Stack Pointer(SP) 0000
Memory Pointer (HL) D658
Program Status Word(PSW) 0001
Program Counter(PC) 1008
Clock Cycle Counter 57
Instruction Counter 5
SOD SID INTR TRAP R7.5 R6.5 R5.5
0 0 0 0 0 0 0
For SIM instruction SOD SDE * R7.5 MSE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
For RIM instruction SID I7.5 I6.5 I5.5 IE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
No. Converter Tool :
Hexadecimal Decimal Binary
0 0 0


8085 Simulator
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LHLD 2000 2A 3 5 16
1001 00
1002 20
√ 1003 DAD H 29 1 3 10
√ 1004 DAD H 29 1 3 10
√ 1005 SHLD 2002 22 3 5 16
1006 02
1007 20
√ 1008 HLT 76 1 2 5
Simulate
Start From → 1000
Run all At a Time Step By Step
Created by : Jubin Mitra
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
1000 2A
1002 20
1003 29
1004 29
1005 22
1006 02
1007 20
1008 76
2000 96
2001 75
2002 58
2003 D6
Show entire memory content
Show only loaded memory location
Store directly to specified memory location

Learning outcomes (What I have learnt):

1. Learnt to find the 1bit left shift of 16-bit number.
2. Learnt to find the 2bit left shift of 16-bit number.

Evaluation Grid (To be created as per the SOP and Assessment guidelines by the faculty):

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			