

Worksheet 2.2 or 5

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Branch: BE-CSE (LEET)

Section/Group: ON20BCS-809/A

Semester: 4th Sem

Date of Performance: 22/03/2022

Subject Name: MPI Lab

Subject Code: 22E-20CSP-253

1. Aim/Overview of the practical:

- 1's complement of 16-bit number.
- 2's complement of 16-bit number.

2. Task to be done:

Write an 8085 Microprocessor program to find the 1's and 2's Complement of 16-bit number.

3. Apparatus/Simulator used (For applied/experimental sciences/materials-based labs):

- 8085 Jubin simulator version 2 (Microprocessor Simulator)
- Java (jdk/ jre1.8.0_321)

4. Algorithm/Flowchart (For programming-based labs):

Algorithm to find the 1's and 2's complement of 16-bit number:

- Load HL pair with operand from 3000 and 3001 memory address.
- Move the lower order from register L to Accumulator.
- Calculate the 1's complement and store in accumulator.
- Move the Results from Accumulator to register L.
- Move Higher order from register H to accumulator.
- Calculate the 1's complement and store in accumulator.
- Move the Results from Accumulator to the register H.
- Store the 1's complemented Result in the 3002 and 3003 memory address.
- Increment the HL pair by 1 to find the 2's complement.
- Store the 2's complemented value into the 3004 and 3005 memory address.
- End the execution using HLT.

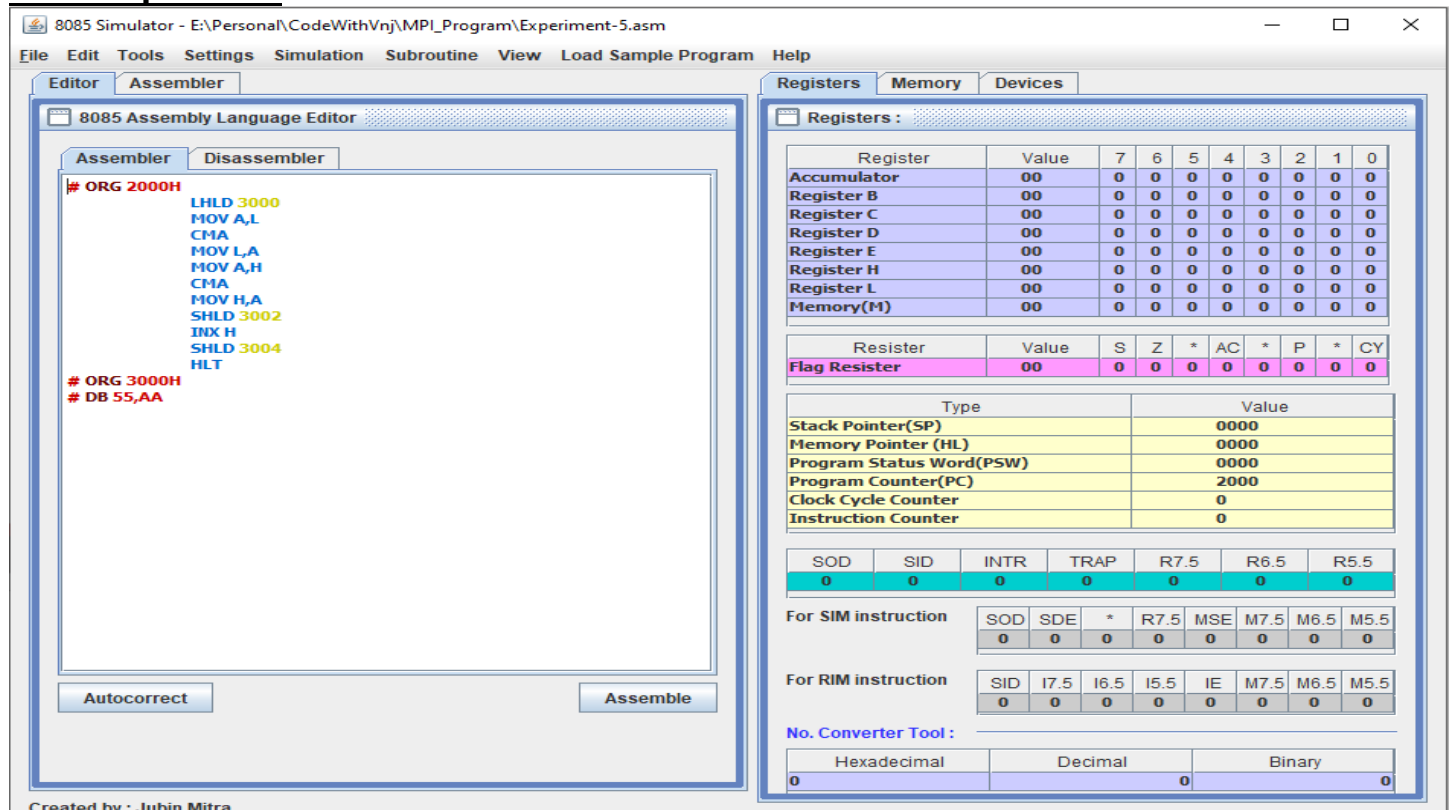
5. Description/ Code:

Program to find 1's and 2's complement of 16-bit number:

```
# ORG 2000H
    LHLD 3000
    MOV A, L
    CMA
    MOV L, A
    MOV A, H
    CMA
    MOV H, A
    SHLD 3002
    INX H
    SHLD 3004
    HLT
# ORG 3000H
# DB 55, AA
```

6. Result/Output/Writing Summary:

1's Complement:



The screenshot shows the 8085 Simulator interface. The main window displays the assembly code for finding the 1's and 2's complement of a 16-bit number. The code is as follows:

```
# ORG 2000H
    LHLD 3000
    MOV A, L
    CMA
    MOV L, A
    MOV A, H
    CMA
    MOV H, A
    SHLD 3002
    INX H
    SHLD 3004
    HLT
# ORG 3000H
# DB 55, AA
```

The right-hand pane shows the state of the registers and memory. The registers are listed with their values and flags. The memory locations 3000H and 3002H are also shown.

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Register	Value	S	Z	*	AC	*	P	*	CY
Flag Register	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	2000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction							
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction							
SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-5.asm

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Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
✓ 2004		CMA	2F	1	1	4
✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Run all At a Time Step By Step

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Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
2000	2A
2002	30
2003	7D
2004	2F
2005	6F
2006	7C
2007	2F
2008	67
2009	22
200A	02
200B	30
200C	23
200D	22
200E	04
200F	30
2010	76
3000	55
3001	AA

☐ Show entire memory content
☒ Show only loaded memory location
☐ Store directly to specified memory location

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-5.asm

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Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
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✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

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Registers

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	AA	1	0	1	0	1	0	1	0
Register L	55	0	1	0	1	0	1	0	1
Memory(M)	00	0	0	0	0	0	0	0	0

Register	Value	S	Z	*	AC	*	P	*	CY
Flag Register	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	AA55
Program Status Word(PSW)	0000
Program Counter(PC)	2003
Clock Cycle Counter	16
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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Assembler

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2002			30			
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✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
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200A			02			
200B			30			
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✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	AA	1	0	1	0	1	0	1	0
Register L	55	0	1	0	1	0	1	0	1
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	AA55
Program Status Word(PSW)	5500
Program Counter(PC)	2004
Clock Cycle Counter	20
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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Editor Assembler

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✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	AA	1	0	1	0	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	AA	1	0	1	0	1	0	1	0
Register L	55	0	1	0	1	0	1	0	1
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	AA55
Program Status Word(PSW)	AA00
Program Counter(PC)	2005
Clock Cycle Counter	24
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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Editor Assembler

Assembler

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✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	AA	1	0	1	0	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	AA	1	0	1	0	1	0	1	0
Register L	AA	1	0	1	0	1	0	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	AAAA
Program Status Word(PSW)	AA00
Program Counter(PC)	2006
Clock Cycle Counter	28
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
✓ 2004		CMA	2F	1	1	4
✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	AA	1	0	1	0	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	AA	1	0	1	0	1	0	1	0
Register L	AA	1	0	1	0	1	0	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	AAAA
Program Status Word(PSW)	AA00
Program Counter(PC)	2007
Clock Cycle Counter	32
Instruction Counter	5

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
✓ 2004		CMA	2F	1	1	4
✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	AA	1	0	1	0	1	0	1	0
Register L	AA	1	0	1	0	1	0	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	AAAA
Program Status Word(PSW)	5500
Program Counter(PC)	2008
Clock Cycle Counter	36
Instruction Counter	6

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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✓ 2006		MOV A,H	7C	1	1	4
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200A			02			
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200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	55	0	1	0	1	0	1	0	1
Register L	AA	1	0	1	0	1	0	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	55AA
Program Status Word(PSW)	5500
Program Counter(PC)	2009
Clock Cycle Counter	40
Instruction Counter	7

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
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200A			02			
200B			30			
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200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Created by : Jubin Mitra

Registers Memory Devices

Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
2000	2A
2002	30
2003	7D
2004	2F
2005	6F
2006	7C
2007	2F
2008	67
2009	22
200A	02
200B	30
200C	23
200D	22
200E	04
200F	30
2010	76
3000	55
3001	AA
3002	AA
3003	55

☐ Show entire memory content
☒ Show only loaded memory location
☐ Store directly to specified memory location

2's Complement:

8085 Simulator - E:\Personal\CodeWithVn\MPI_Program\Experiment-5.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
✓ 2004		CMA	2F	1	1	4
✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Created by : Jubin Mitra

Registers

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	55	0	1	0	1	0	1	0	1
Register L	AB	1	0	1	0	1	0	1	1
Memory(M)	00	0	0	0	0	0	0	0	0

Register	Value	S	Z	*	AC	*	P	*	CY
Flag Register	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	55AB
Program Status Word(PSW)	5500
Program Counter(PC)	200D
Clock Cycle Counter	62
Instruction Counter	9

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-5.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
✓ 2004		CMA	2F	1	1	4
✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	55	0	1	0	1	0	1	0	1
Register L	AB	1	0	1	0	1	0	1	1
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	55AB
Program Status Word(PSW)	5500
Program Counter(PC)	2010
Clock Cycle Counter	78
Instruction Counter	10

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

Created by : Jubin Mitra

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-5.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 2000		LHLD 3000	2A	3	5	16
2001			00			
2002			30			
✓ 2003		MOV A,L	7D	1	1	4
✓ 2004		CMA	2F	1	1	4
✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
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✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Backward Stop Forward

Registers **Memory** **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	55	0	1	0	1	0	1	0	1
Register L	AB	1	0	1	0	1	0	1	1
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	55AB
Program Status Word(PSW)	5500
Program Counter(PC)	2010
Clock Cycle Counter	83
Instruction Counter	11

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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8085 Simulator - E:\Personal\CodeWithVn\MPI_Program\Experiment-5.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
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✓ 2005		MOV L,A	6F	1	1	4
✓ 2006		MOV A,H	7C	1	1	4
✓ 2007		CMA	2F	1	1	4
✓ 2008		MOV H,A	67	1	1	4
✓ 2009		SHLD 3002	22	3	5	16
200A			02			
200B			30			
✓ 200C		INX H	23	1	1	6
✓ 200D		SHLD 3004	22	3	5	16
200E			04			
200F			30			
✓ 2010		HLT	76	1	2	5

Simulate

Start From → 2000

Run all At a Time Step By Step

Registers Memory Devices

Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
2003	7D
2004	2F
2005	6F
2006	7C
2007	2F
2008	67
2009	22
200A	02
200B	30
200C	23
200D	22
200E	04
200F	30
2010	76
3000	55
3001	AA
3002	AA
3003	55
3004	AB
3005	55

☐ Show entire memory content
☒ Show only loaded memory location
☐ Store directly to specified memory location

Created by : Jubin Mitra

Learning outcomes (What I have learnt):

1. Learnt to find the 1's complement of 16-bit number.
2. Learn to find the 2's complement of 16-bit number.

Evaluation Grid (To be created as per the SOP and Assessment guidelines by the faculty):

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			