Worksheet 2.1

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Branch: BE-CSE (LEET)
Section/Group: ON20BCS-809/A
Semester: 4th Sem
Date of Performance: 22/03/2022
Subject Name: MPI Lab
Subject Code: 22E-20CSP-253

1. Aim/Overview of the practical:

a) 1's complement of 8-bit number.
b) 2's complement of 8-bit number.

2. Task to be done:

Write a 8085 Microprocessor program to find the 1's and 2's Complement of 8-bit number.

3. Apparatus/Simulator used (For applied/experimental sciences/materials-based labs)**:**

I. 8085 Jubin simulator version 2 (Microprocessor Simulator)
II. Java (jdk/ jre1.8.0_321)

4. Algorithm/Flowchart (For programming-based labs)**:**

Algorithm to find the 1's and 2's complement of 8-bit number:

I. Load the number from memory location 2000 to accumulator.
II. Calculate the 1's complement using CMA. This will store the calculated 1's complement into the accumulator.
III. Store the 1's complement value in to the 2001 memory location.
IV. To find the 2's complement adds immediate 01 via ADI 01 into the 1's complemented value which is stored in accumulator.
V. Store the 2's complement value at the 2002 memory location.
VI. End the execution using HLT

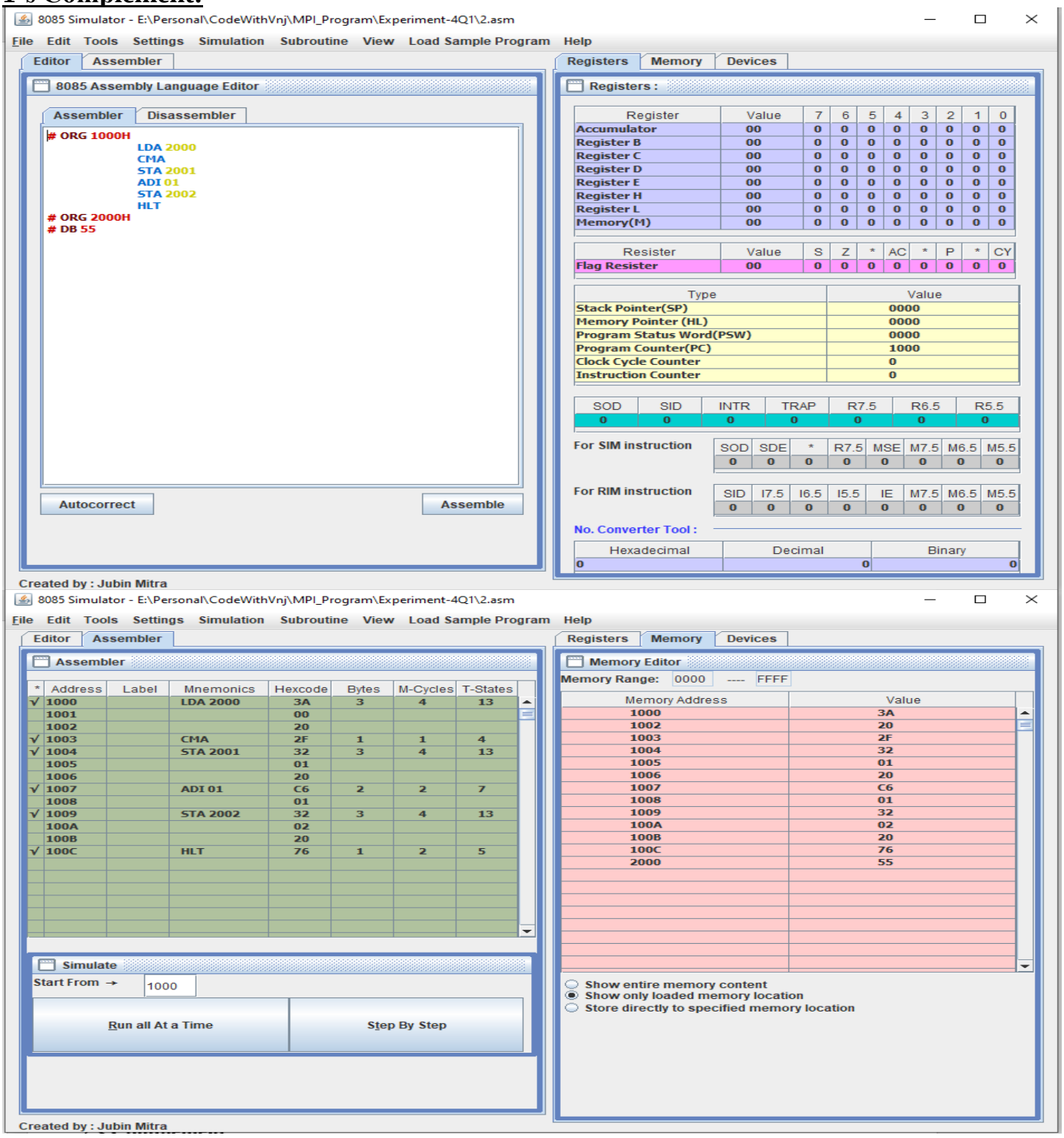
5. Description/ Code:

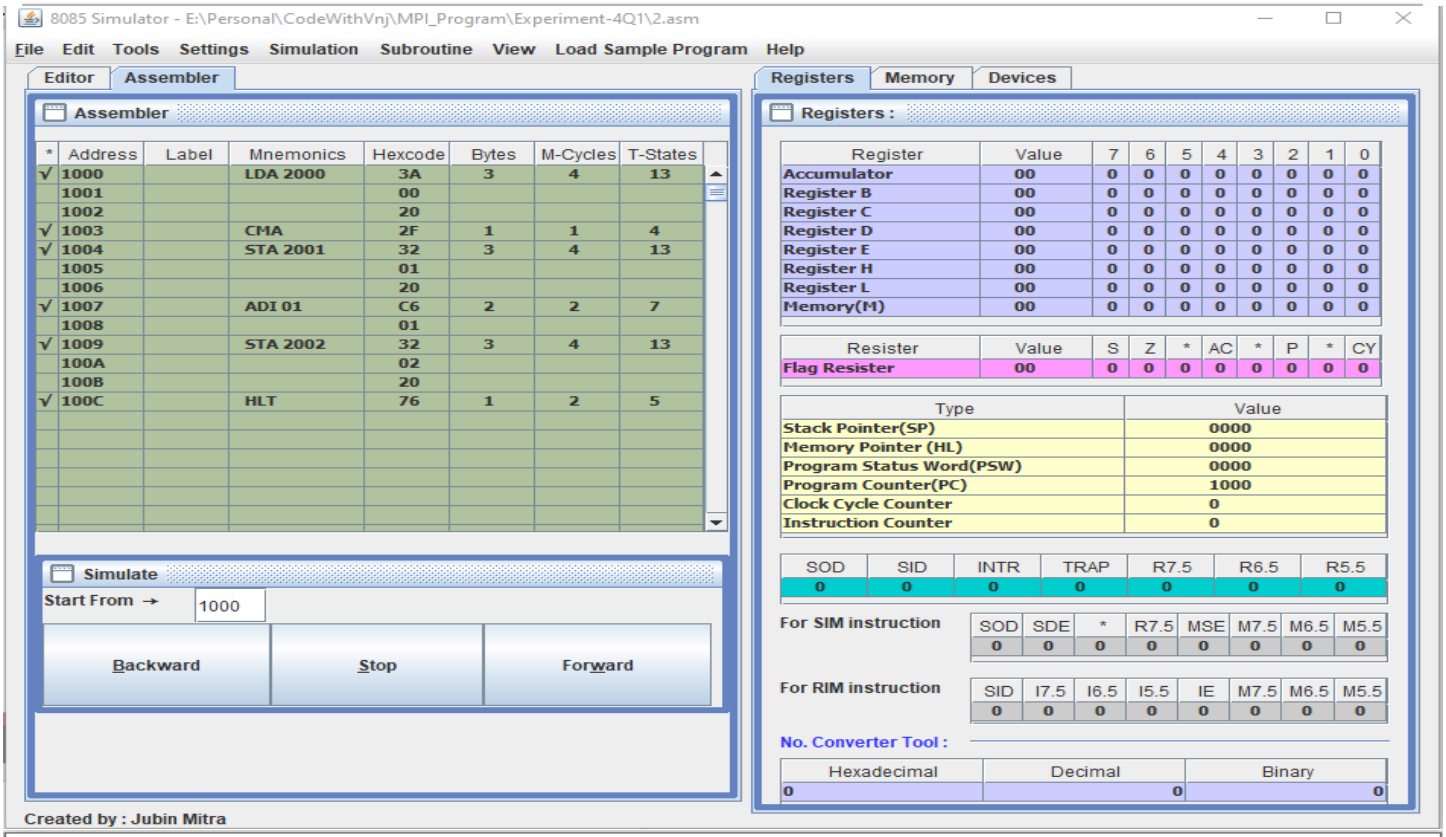
Program to find 1's and 2's complement of 8-bit number:

```
# ORG 1000H
        LDA 2000
        CMA
        STA 2001
        ADI 01
        STA 2002
        HLT
# ORG 2000H
# DB 55
```

6. Result/Output/Writing Summary:

1's Complement:





8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-4Q1\2.asm

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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LDA 2000	3A	3	4	13
	1001			00			
	1002			20			
√	1003		CMA	2F	1	1	4
√	1004		STA 2001	32	3	4	13
	1005			01			
	1006			20			
√	1007		ADI 01	C6	2	2	7
	1008			01			
√	1009		STA 2002	32	3	4	13
	100A			02			
	100B			20			
√	100C		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	1000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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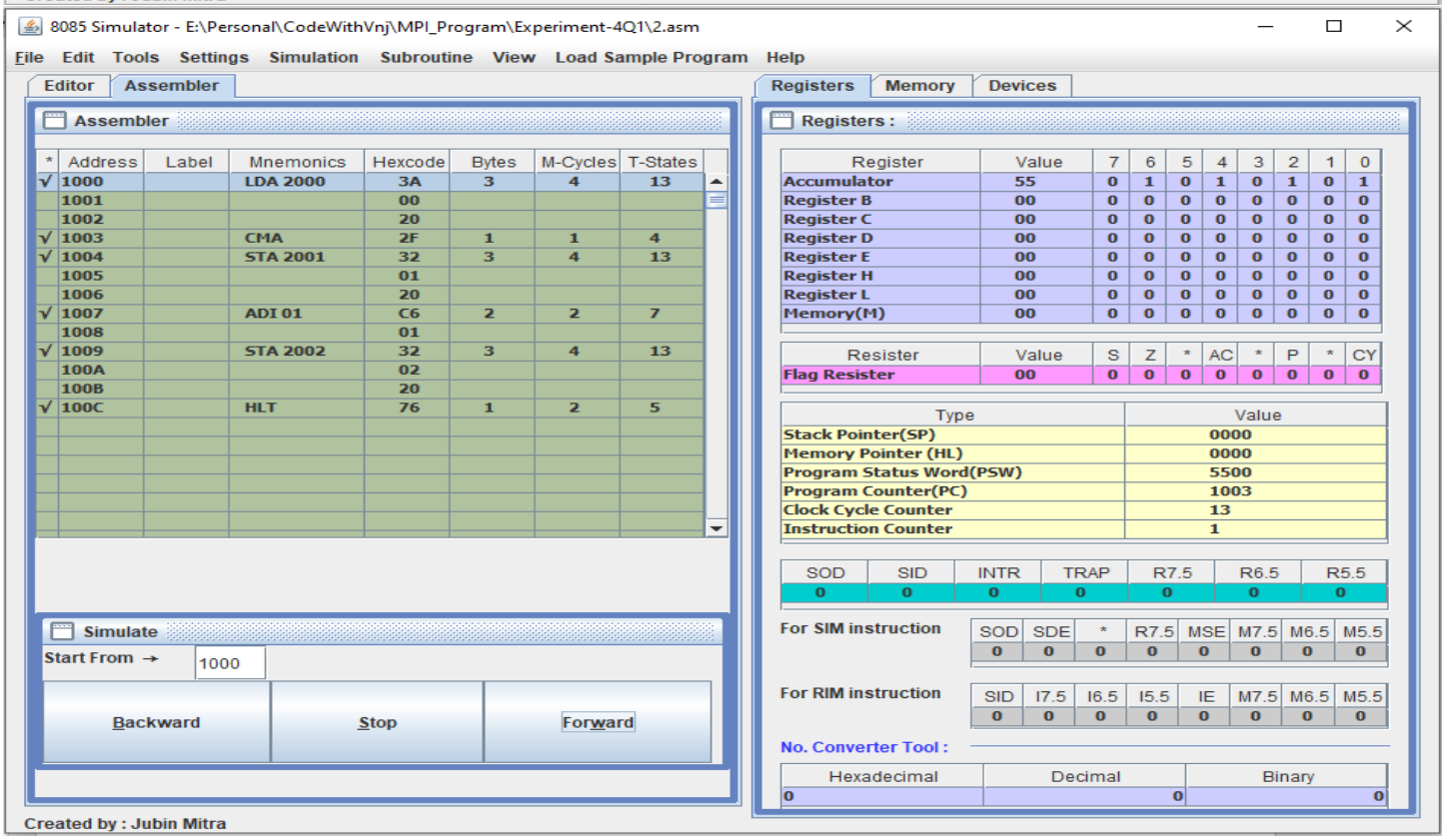

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LDA 2000	3A	3	4	13
	1001			00			
	1002			20			
√	1003		CMA	2F	1	1	4
√	1004		STA 2001	32	3	4	13
	1005			01			
	1006			20			
√	1007		ADI 01	C6	2	2	7
	1008			01			
√	1009		STA 2002	32	3	4	13
	100A			02			
	100B			20			
√	100C		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	55	0	1	0	1	0	1	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	5500
Program Counter(PC)	1003
Clock Cycle Counter	13
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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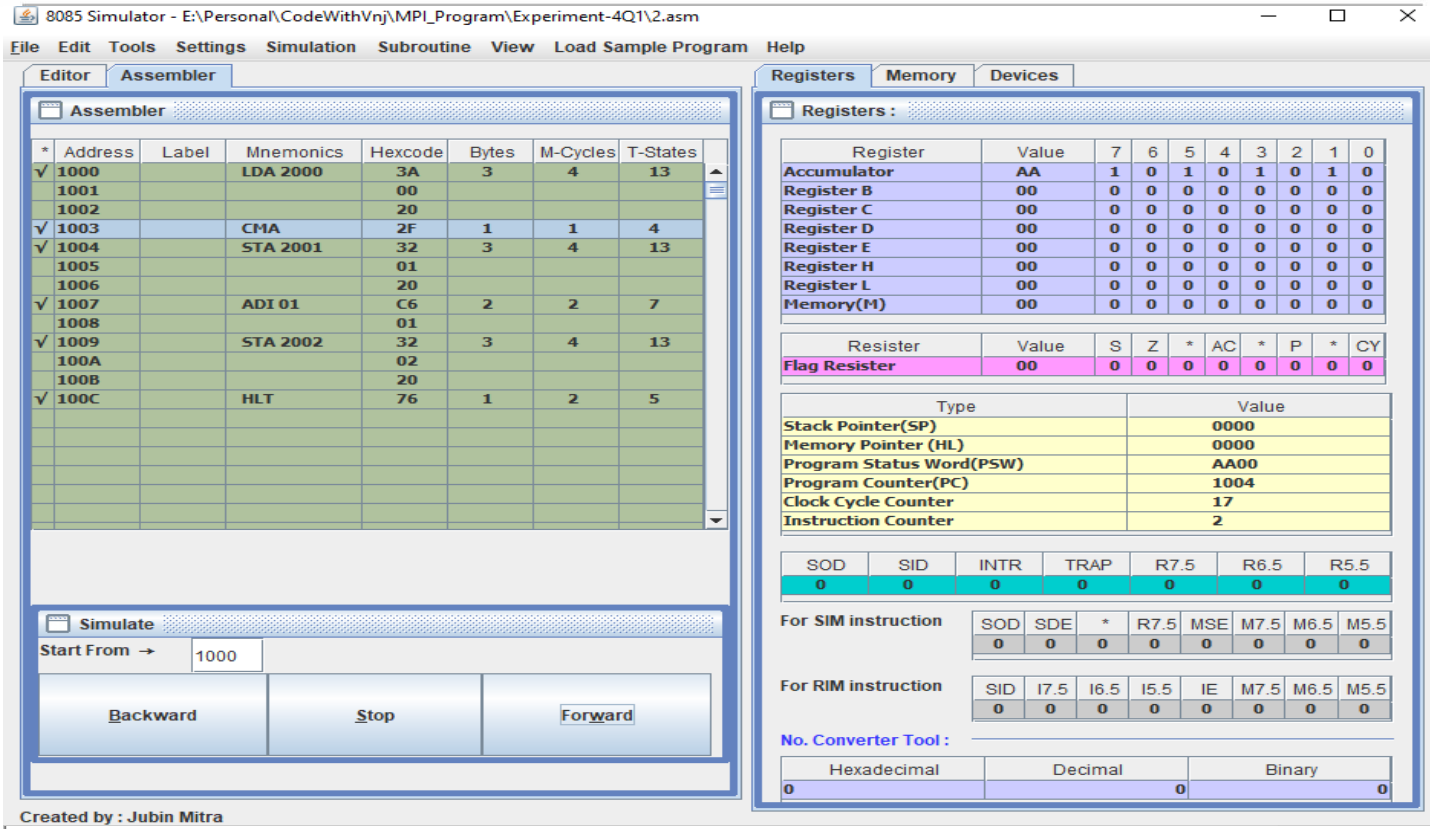


*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LDA 2000	3A	3	4	13
	1001			00			
	1002			20			
√	1003		CMA	2F	1	1	4
√	1004		STA 2001	32	3	4	13
	1005			01			
	1006			20			
√	1007		ADI 01	C6	2	2	7
	1008			01			
√	1009		STA 2002	32	3	4	13
	100A			02			
	100B			20			
√	100C		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	AA	1	0	1	0	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	AA00
Program Counter(PC)	1004
Clock Cycle Counter	17
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

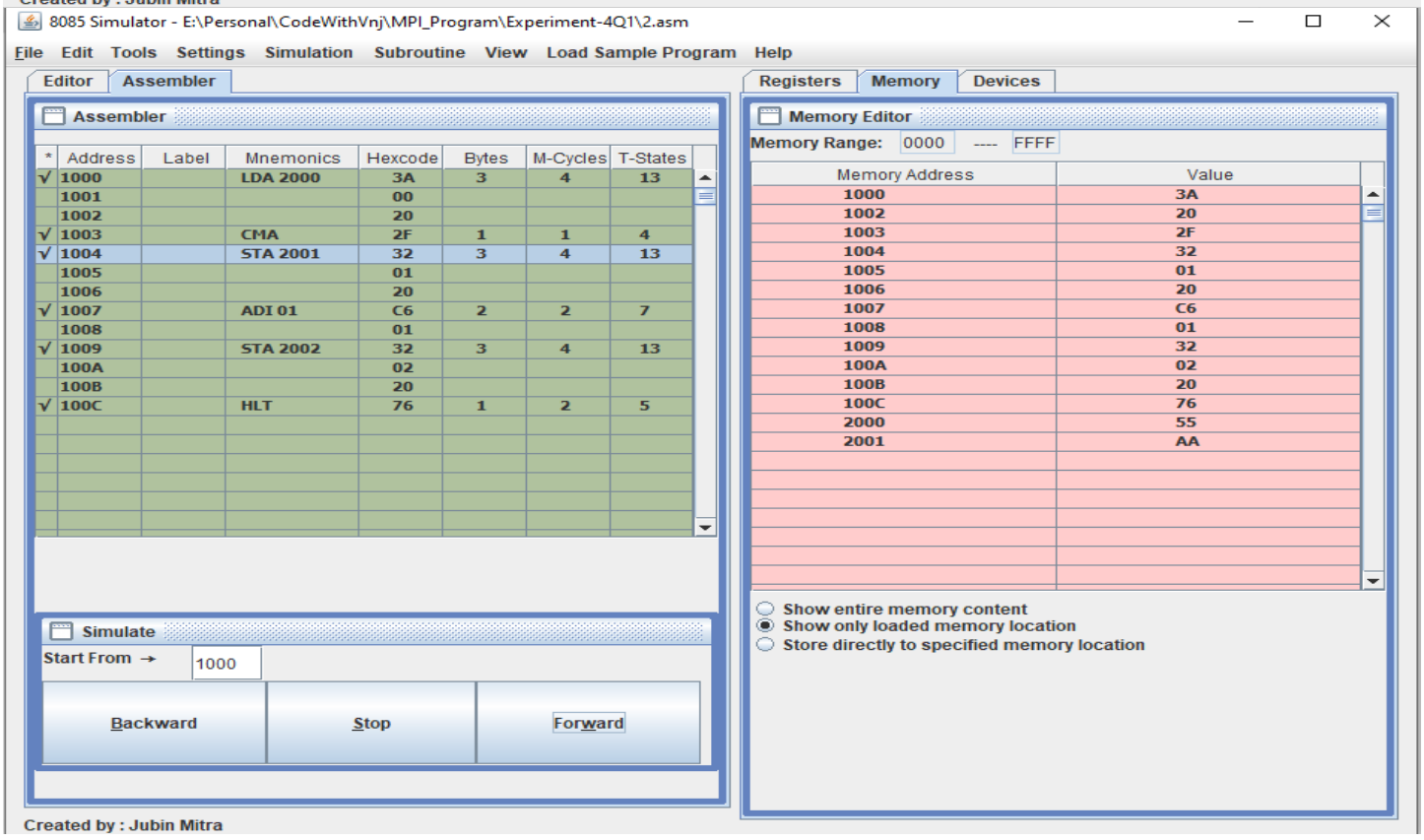
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LDA 2000	3A	3	4	13
	1001			00			
	1002			20			
√	1003		CMA	2F	1	1	4
√	1004		STA 2001	32	3	4	13
	1005			01			
	1006			20			
√	1007		ADI 01	C6	2	2	7
	1008			01			
√	1009		STA 2002	32	3	4	13
	100A			02			
	100B			20			
√	100C		HLT	76	1	2	5

Memory Address	Value
1000	3A
1002	20
1003	2F
1004	32
1005	01
1006	20
1007	C6
1008	01
1009	32
100A	02
100B	20
100C	76
2000	55
2001	AA

2's Complement:

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LDA 2000	3A	3	4	13
	1001			00			
	1002			20			
√	1003		CMA	2F	1	1	4
√	1004		STA 2001	32	3	4	13
	1005			01			
	1006			20			
√	1007		ADI 01	C6	2	2	7
	1008			01			
√	1009		STA 2002	32	3	4	13
	100A			02			
	100B			20			
√	100C		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	AB	1	0	1	0	1	0	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	80	1	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	AB80
Program Counter(PC)	1009
Clock Cycle Counter	37
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LDA 2000	3A	3	4	13
	1001			00			
	1002			20			
√	1003		CMA	2F	1	1	4
√	1004		STA 2001	32	3	4	13
	1005			01			
	1006			20			
√	1007		ADI 01	C6	2	2	7
	1008			01			
√	1009		STA 2002	32	3	4	13
	100A			02			
	100B			20			
√	100C		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	AB	1	0	1	0	1	0	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	80	1	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	AB80
Program Counter(PC)	100C
Clock Cycle Counter	50
Instruction Counter	5

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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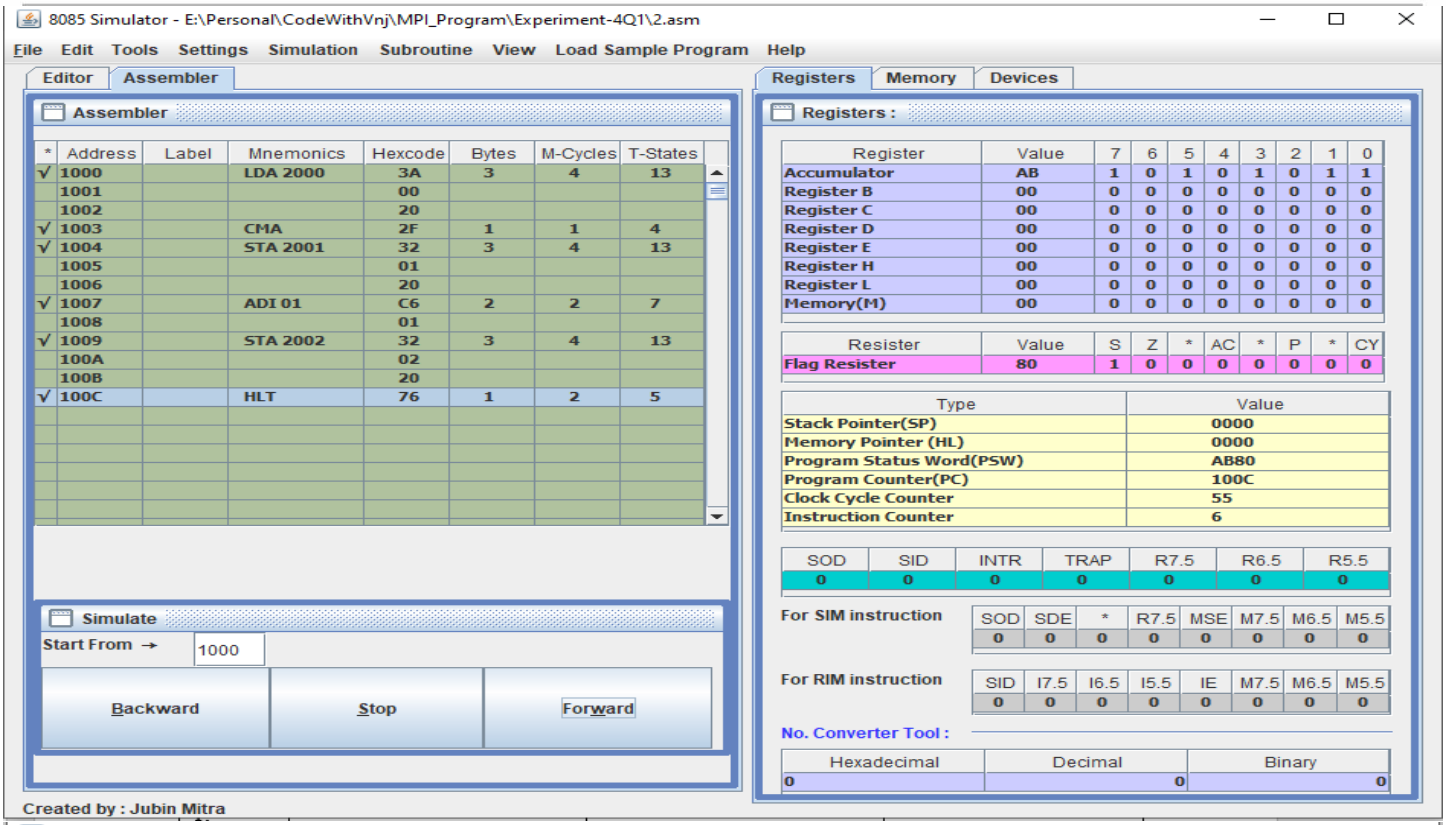
8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-4Q1\2.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LDA 2000 3A 3 4 13
1001 00
1002 20
√ 1003 CMA 2F 1 1 4
√ 1004 STA 2001 32 3 4 13
1005 01
1006 20
√ 1007 ADI 01 C6 2 2 7
1008 01
√ 1009 STA 2002 32 3 4 13
100A 02
100B 20
√ 100C HLT 76 1 2 5
Simulate
Start From → 1000
Backward Stop Forward
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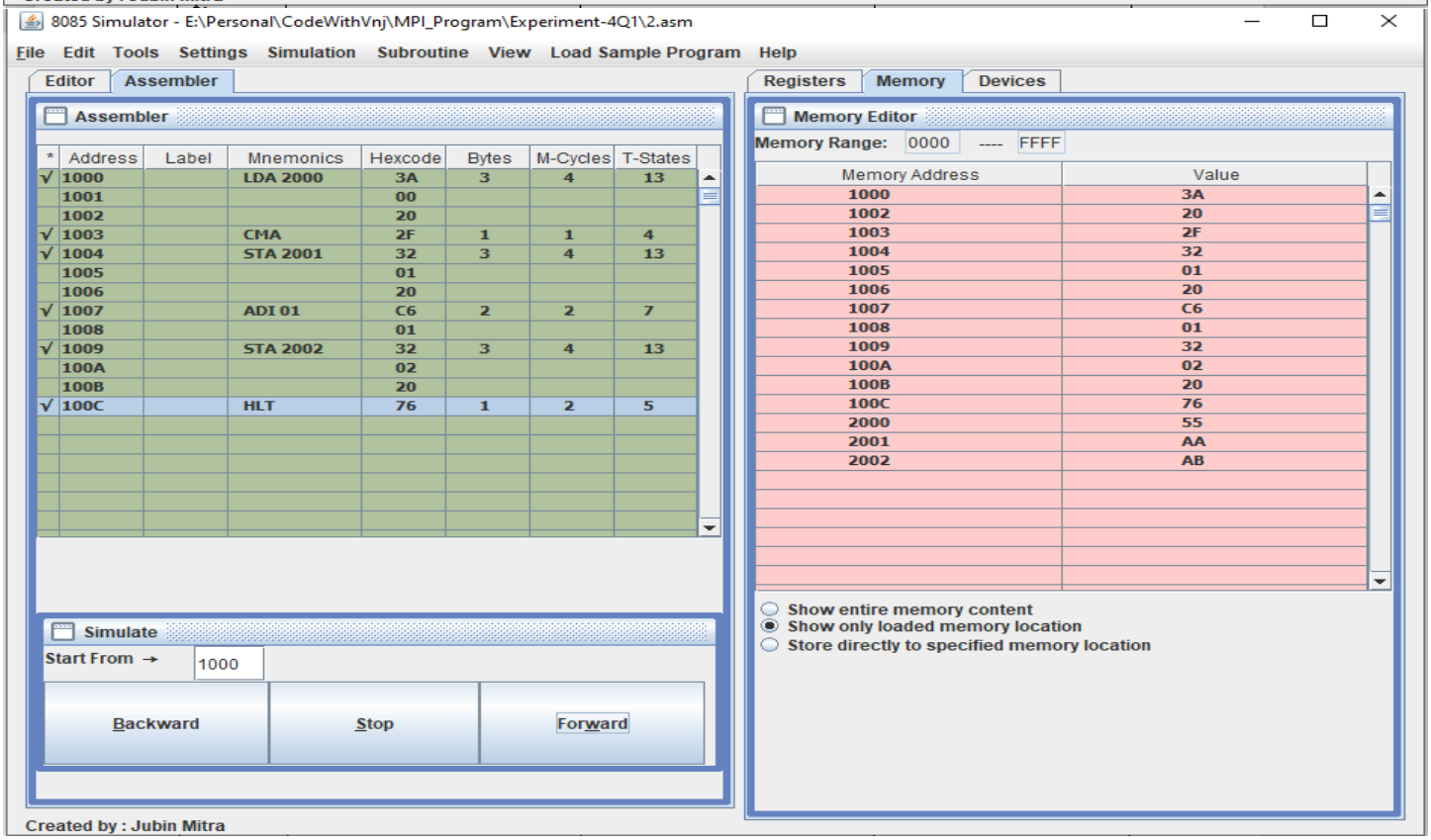
Registers Memory Devices
Registers :
Register Value 7 6 5 4 3 2 1 0
Accumulator AB 1 0 1 0 1 0 1 1
Register B 00 0 0 0 0 0 0 0 0
Register C 00 0 0 0 0 0 0 0 0
Register D 00 0 0 0 0 0 0 0 0
Register E 00 0 0 0 0 0 0 0 0
Register H 00 0 0 0 0 0 0 0 0
Register L 00 0 0 0 0 0 0 0 0
Memory(M) 00 0 0 0 0 0 0 0 0
Resister Value S Z * AC * P * CY
Flag Resister 80 1 0 0 0 0 0 0 0
Type Value
Stack Pointer(SP) 0000
Memory Pointer (HL) 0000
Program Status Word(PSW) AB80
Program Counter(PC) 100C
Clock Cycle Counter 55
Instruction Counter 6
SOD SID INTR TRAP R7.5 R6.5 R5.5
0 0 0 0 0 0 0
For SIM instruction
SOD SDE * R7.5 MSE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
For RIM instruction
SID I7.5 I6.5 I5.5 IE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
No. Converter Tool :
Hexadecimal Decimal Binary
0 0 0


8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-4Q1\2.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 1000 LDA 2000 3A 3 4 13
1001 00
1002 20
√ 1003 CMA 2F 1 1 4
√ 1004 STA 2001 32 3 4 13
1005 01
1006 20
√ 1007 ADI 01 C6 2 2 7
1008 01
√ 1009 STA 2002 32 3 4 13
100A 02
100B 20
√ 100C HLT 76 1 2 5
Simulate
Start From → 1000
Backward Stop Forward
Created by : Jubin Mitra
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
1000 3A
1002 20
1003 2F
1004 32
1005 01
1006 20
1007 C6
1008 01
1009 32
100A 02
100B 20
100C 76
2000 55
2001 AA
2002 AB
Show entire memory content
Show only loaded memory location
Store directly to specified memory location

Learning outcomes (What I have learnt):

1. Learnt to find the 1's complement of 8-bit number.
2. Learn to find the 2's complement if the number.

Evaluation Grid (To be created as per the SOP and Assessment guidelines by the faculty):

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			