Worksheet 3.1 or 8

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Section/Group: ON20BCS-809/A
Semester: 4th Sem
Date of Performance: 08/04/2022
Subject Name: MPI Lab
Subject Code: 22E-20CSP-253

1. Aim/Overview of the practical:

I. Mask the lower nibble of an 8-bit number.
II. Mask the higher nibble of an 8-bit number.

2. Task to be done:

Write a 8085 Microprocessor program to perform the lower nibble & higher nibble of 8-bit.

3. Apparatus/Simulator used (For applied/experimental sciences/materials-based labs):

I. 8085 Jubin simulator version 2 (Microprocessor Simulator)
II. Java (jdk/ jre1.8.0_321)

4. Algorithm/Flowchart (For programming-based labs):

Algorithm to mask the lower nibble of an 8-bit number:

I. Load the 1st data to the Accumulator ‘A’ from 1000 memory address.
II. Move the data from Accumulator ‘A’ to register B.
III. Load the 2nd data to Accumulator ‘A’ from 1001 memory address which is F0.
IV. Do ANDing operation between Accumulator ‘A’ and Register B by Using ANA B.
V. Store the ANDed value from Accumulator ‘A’ to 1002 memory location.
VI. End the execution using HLT.

OR,

I. Load the data to Memory from 1000 address using Immediate Instruction LXI H, 1000.
II. Move The data from Memory to Accumulator ‘A’.
III. Perform Immediate ANDing operation in Accumulator ‘A’ with ‘F0’ by Using ANI F0 instruction.
IV. Store the ANDed value from Accumulator ‘A’ to 1002 memory location.
V. End the execution using HLT.

Algorithm to mask the higher nibble of an 8-bit number:

I. Load the 1st data to the Accumulator 'A' from 1000 memory address.
II. Move the data from Accumulator 'A' to register B.
III. Load the 2nd data to Accumulator 'A' from 1001 memory address which is 0F.
IV. Do ANDing operation between Accumulator 'A' and Register B by Using ANA B.
V. Store the ANDed value from Accumulator 'A' to 1002 memory location.
VI. End the execution using HLT.

OR,

I. Load the data to Memory from 1000 address using Immediate Instruction LXI H, 1000.
II. Move The data from Memory to Accumulator 'A'.
III. Perform Immediate ANDing operation in Accumulator 'A' with '0F' by Using ANI 0F instruction.
IV. Store the ANDed value from Accumulator 'A' to 1002 memory location.
V. End the execution using HLT.

5. Description/ Code:

Program to mask the lower nibble of an 8-bit number:

```
# ORG 0900H
        LDA 1000
        MOV B, A
        LDA 1001
        ANA B
        STA 1002
        HLT
# ORG 1000
# DB D7H, F0H
```

OR

```
# ORG 0900H
        LXI H, 1000
        MOV A, M
        ANI F0H
        STA 1002
        HLT
# ORG 1000
# DB D7H
```

Program to mask the higher nibble of an 8-bit number:

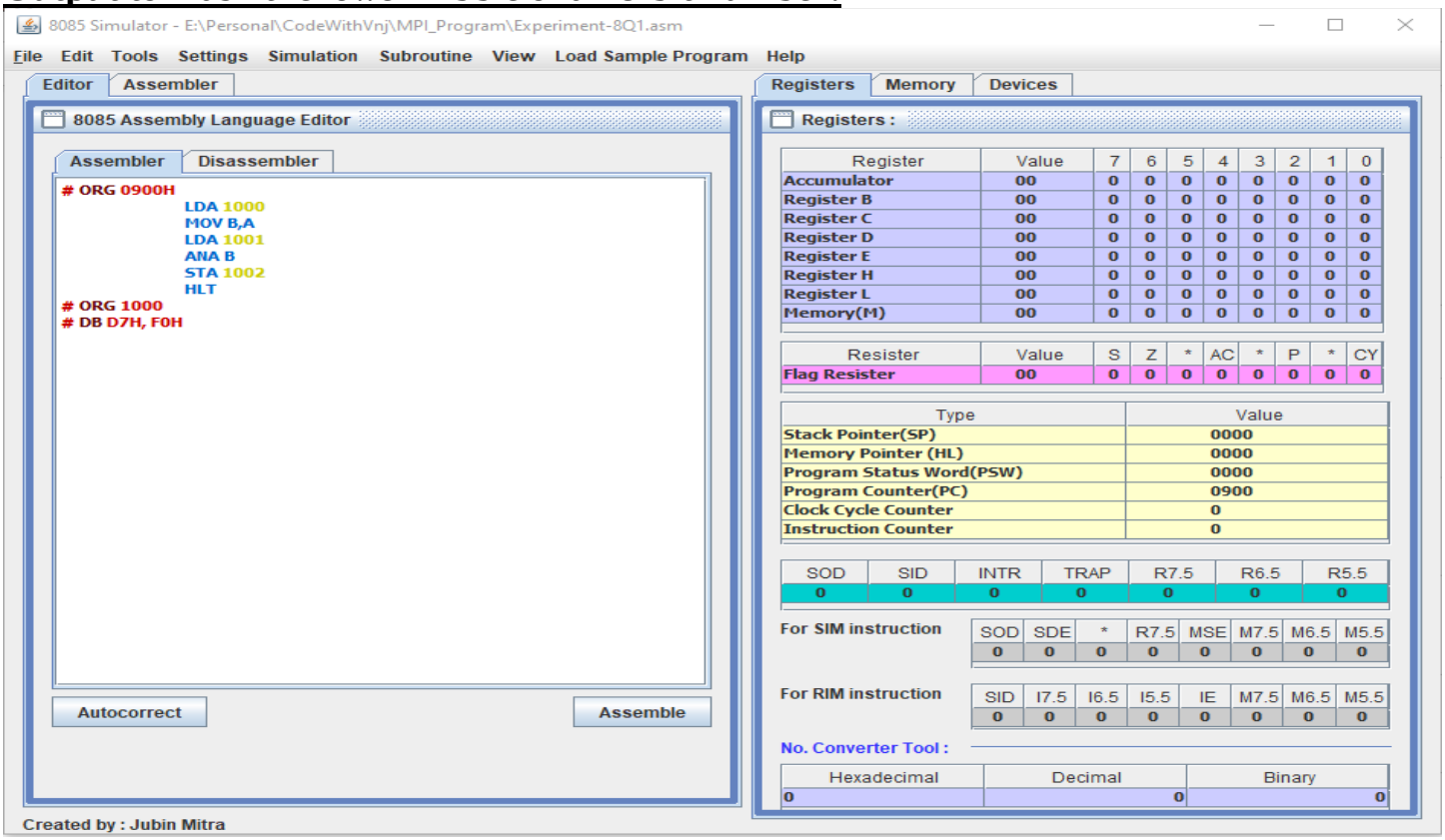
```
# ORG 0900H
        LDA 1000
        MOV B, A
        LDA 1001
        ANA B
        STA 1002
        HLT
# ORG 1000
# DB D7H, 0FH
```

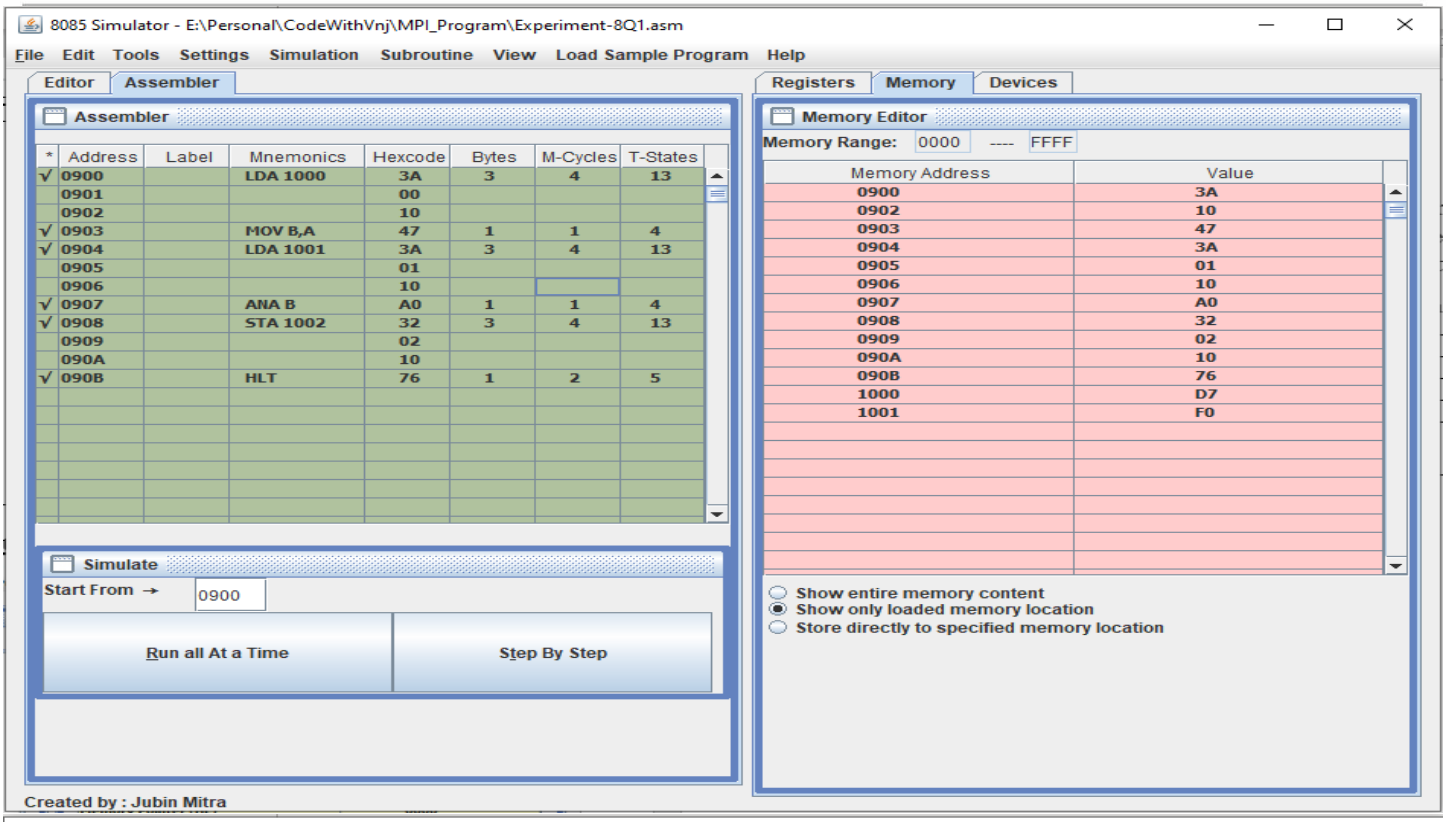
OR

```
# ORG 0900H
        LXI H, 1000
        MOV A, M
        ANI 0FH
        STA 1002
        HLT
# ORG 1000
# DB D7H
```

6. Result/Output/Writing Summary:

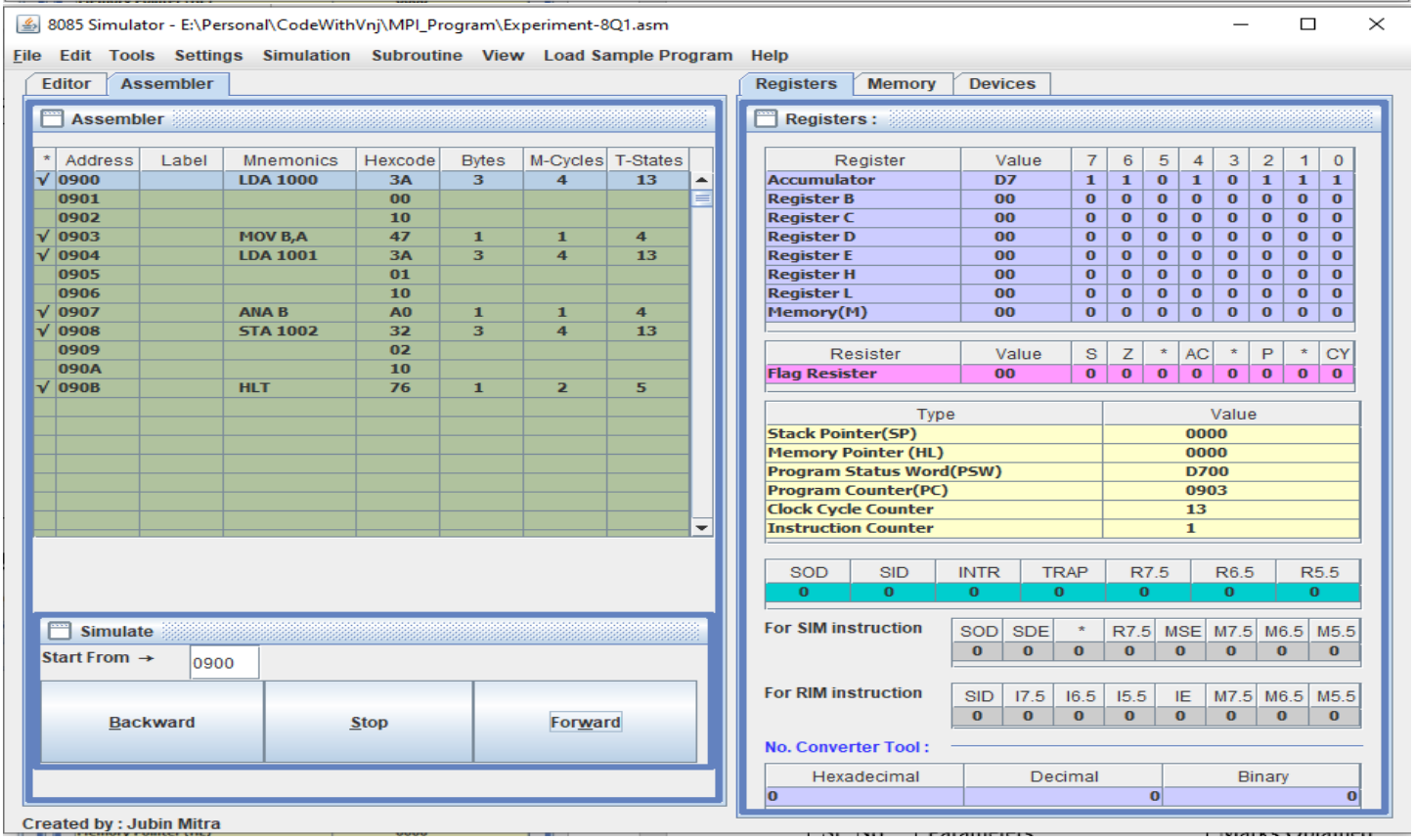
Output to mask the lower nibble of an 8-bit number:





*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Memory Address	Value
0900	3A
0902	10
0903	47
0904	3A
0905	01
0906	10
0907	A0
0908	32
0909	02
090A	10
090B	76
1000	D7
1001	F0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D7	1	1	0	1	0	1	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	D700
Program Counter(PC)	0903
Clock Cycle Counter	13
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

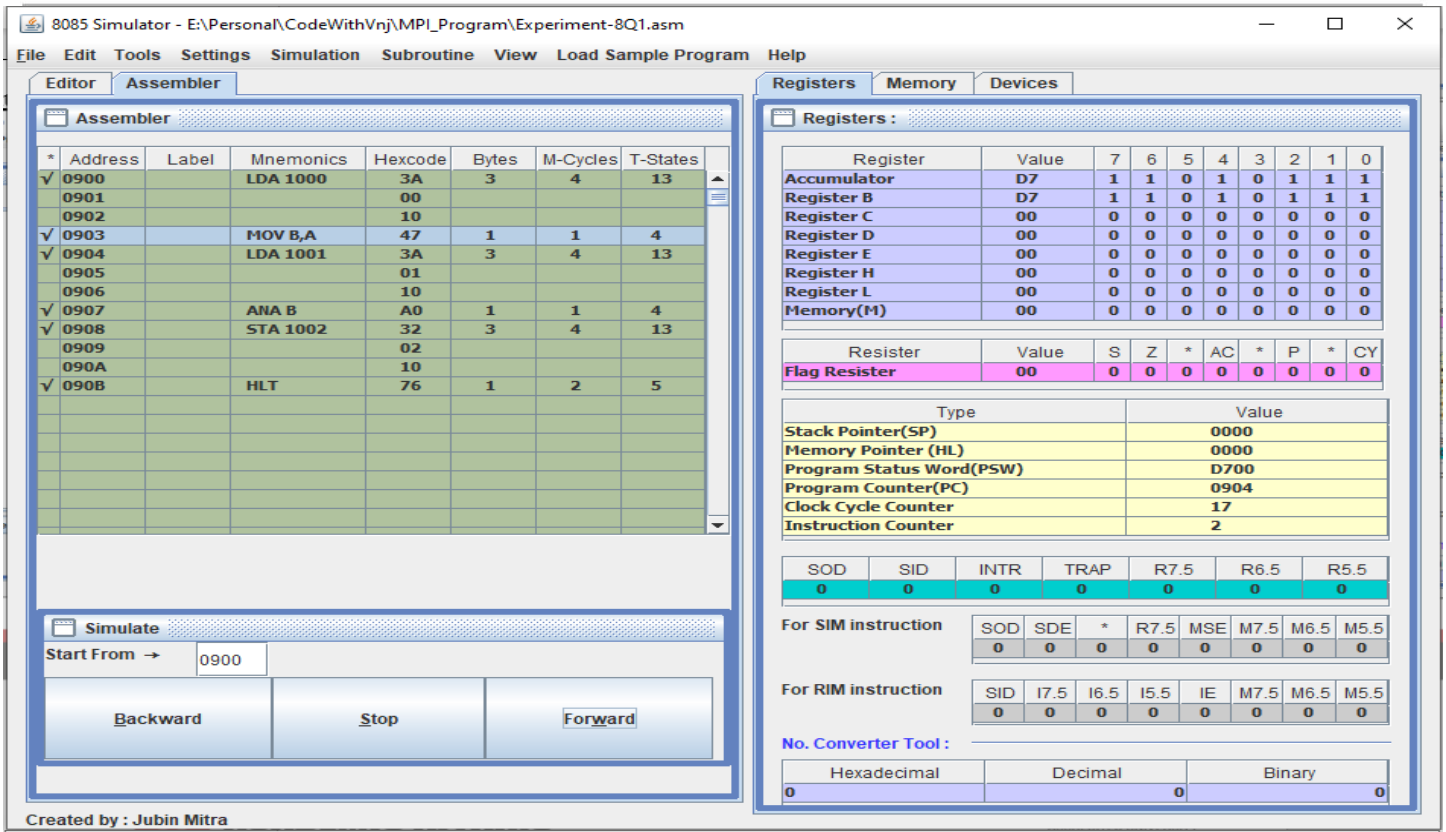
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D7	1	1	0	1	0	1	1	1
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	D700
Program Counter(PC)	0904
Clock Cycle Counter	17
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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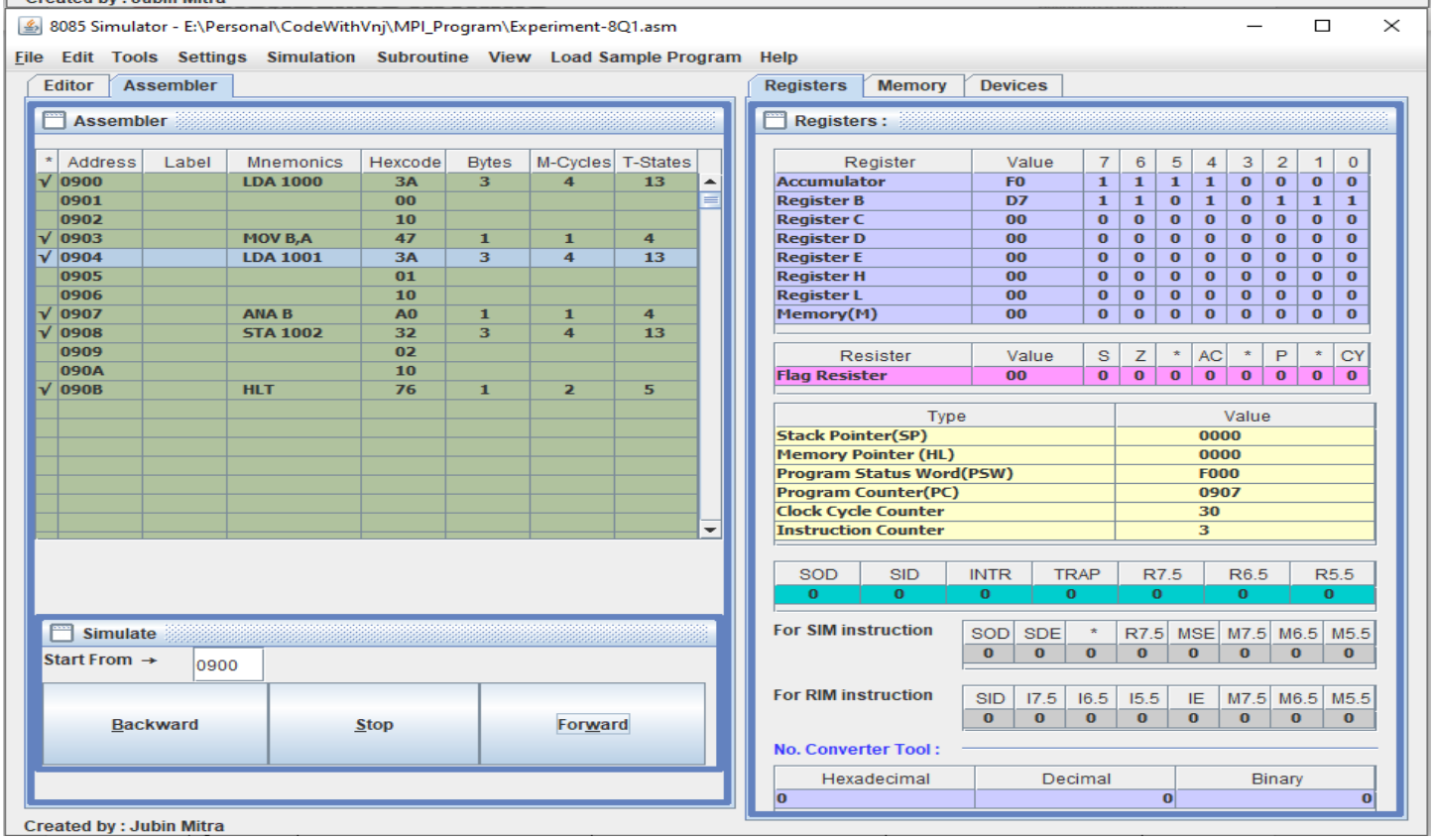

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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	F0	1	1	1	1	0	0	0	0
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	F000
Program Counter(PC)	0907
Clock Cycle Counter	30
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

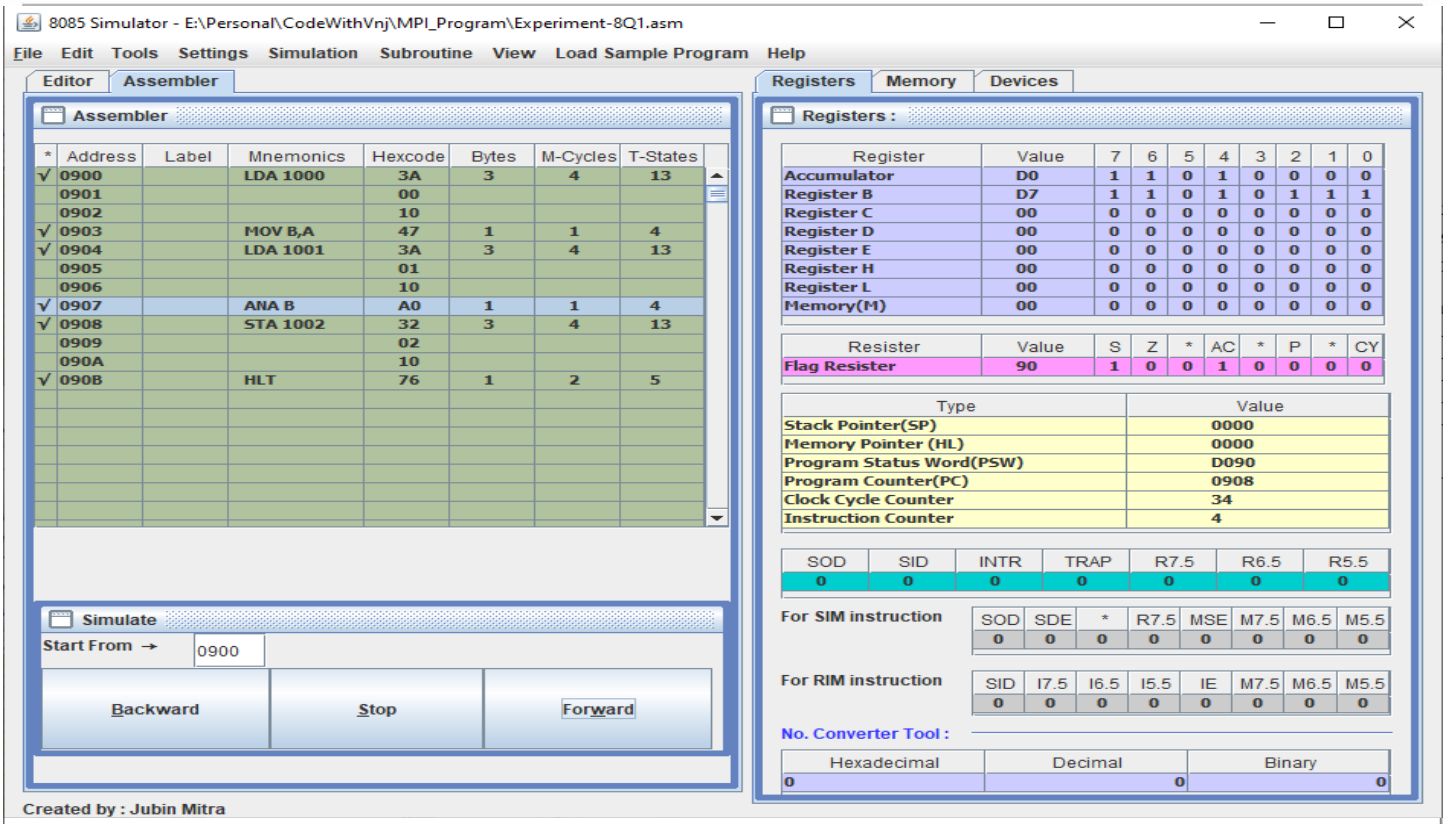
For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D0	1	1	0	1	0	0	0	0
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	90	1	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	D090
Program Counter(PC)	0908
Clock Cycle Counter	34
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

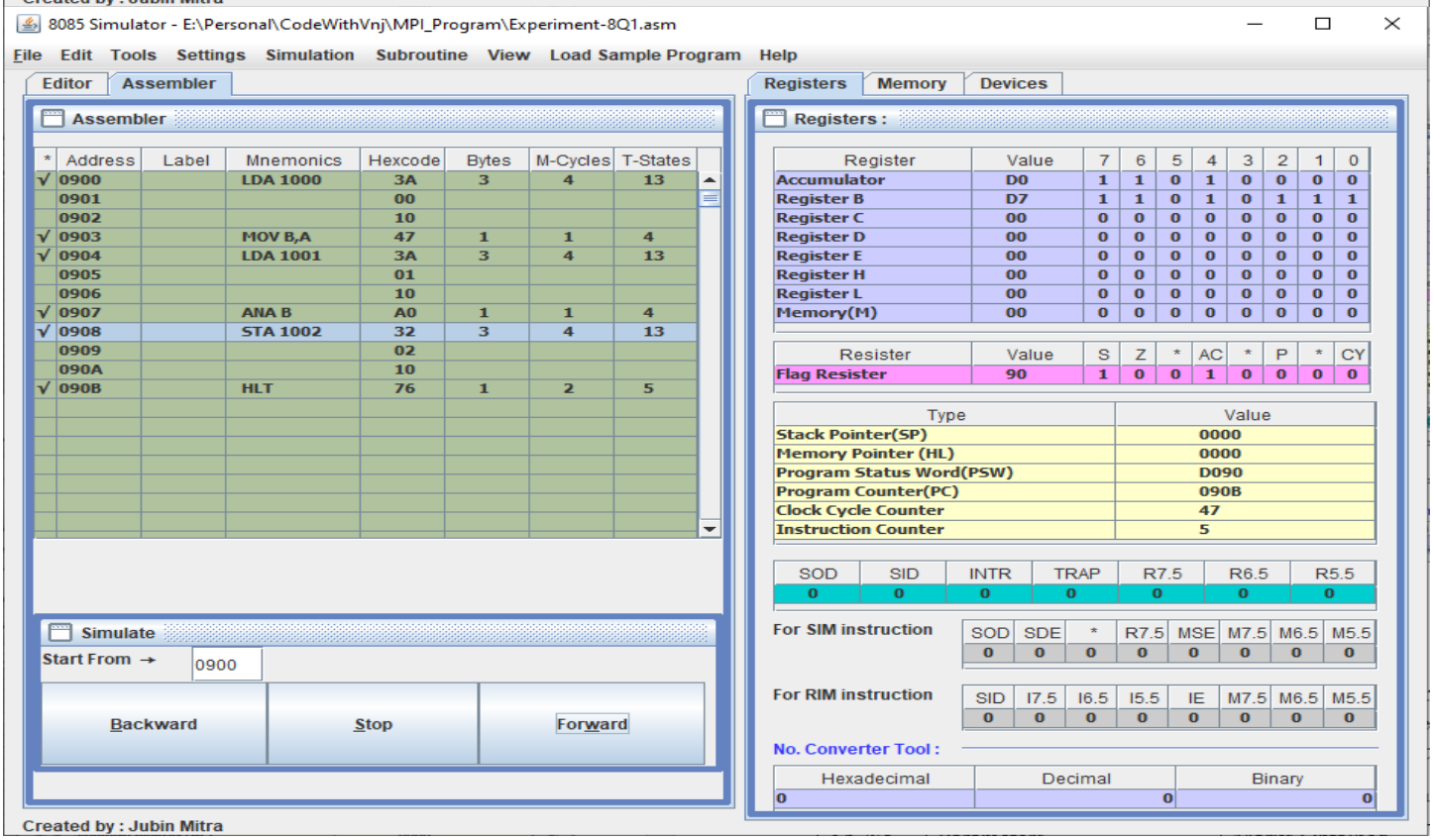
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D0	1	1	0	1	0	0	0	0
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	90	1	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	D090
Program Counter(PC)	090B
Clock Cycle Counter	47
Instruction Counter	5

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

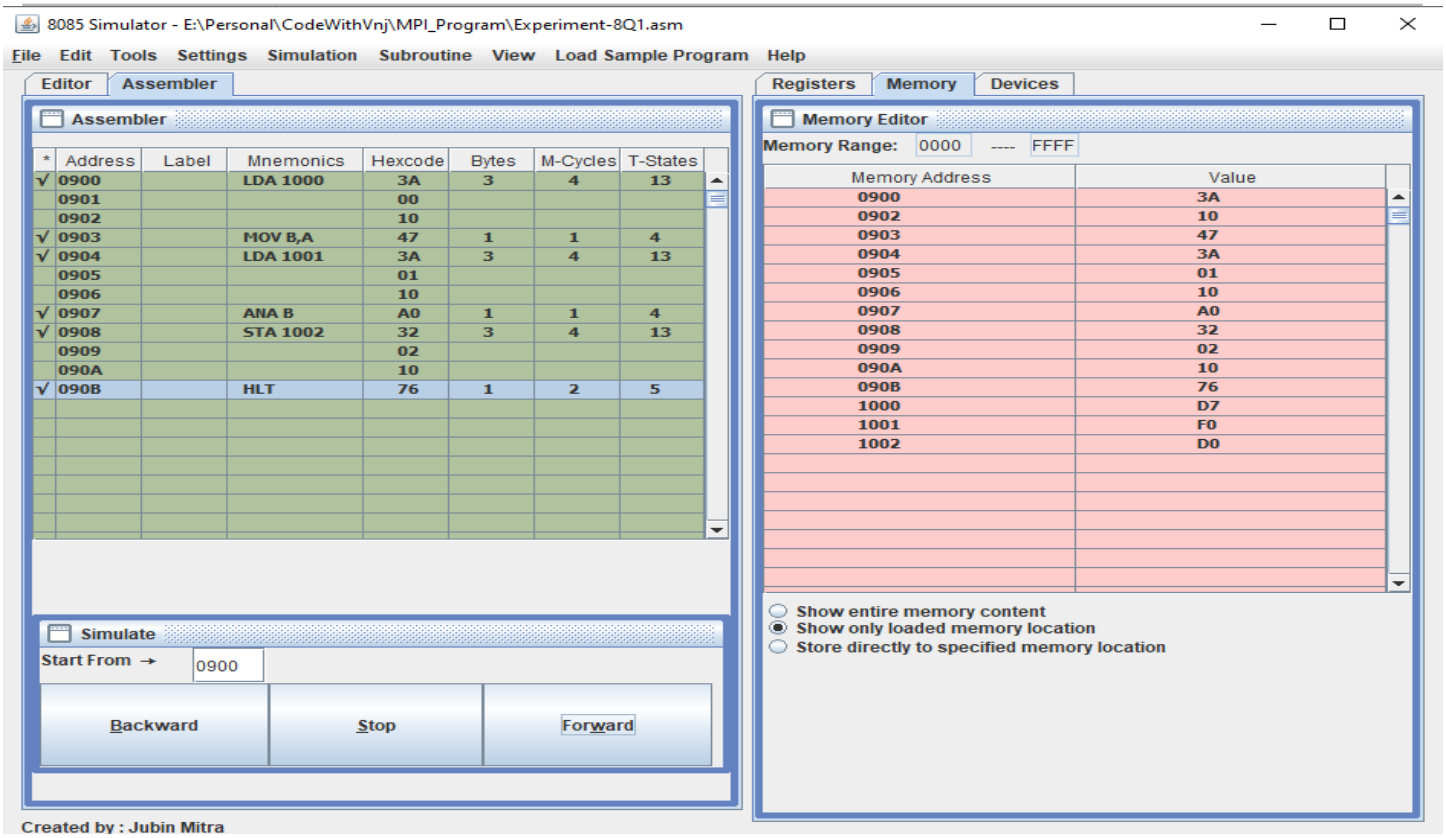
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0


8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q1.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 0900 LDA 1000 3A 3 4 13
0901 00
0902 10
√ 0903 MOV B,A 47 1 1 4
√ 0904 LDA 1001 3A 3 4 13
0905 01
0906 10
√ 0907 ANA B A0 1 1 4
√ 0908 STA 1002 32 3 4 13
0909 02
090A 10
√ 090B HLT 76 1 2 5
Simulate
Start From → 0900
Backward Stop Forward
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
0900 3A
0902 10
0903 47
0904 3A
0905 01
0906 10
0907 A0
0908 32
0909 02
090A 10
090B 76
1000 D7
1001 F0
1002 D0
Show entire memory content
Show only loaded memory location
Store directly to specified memory location
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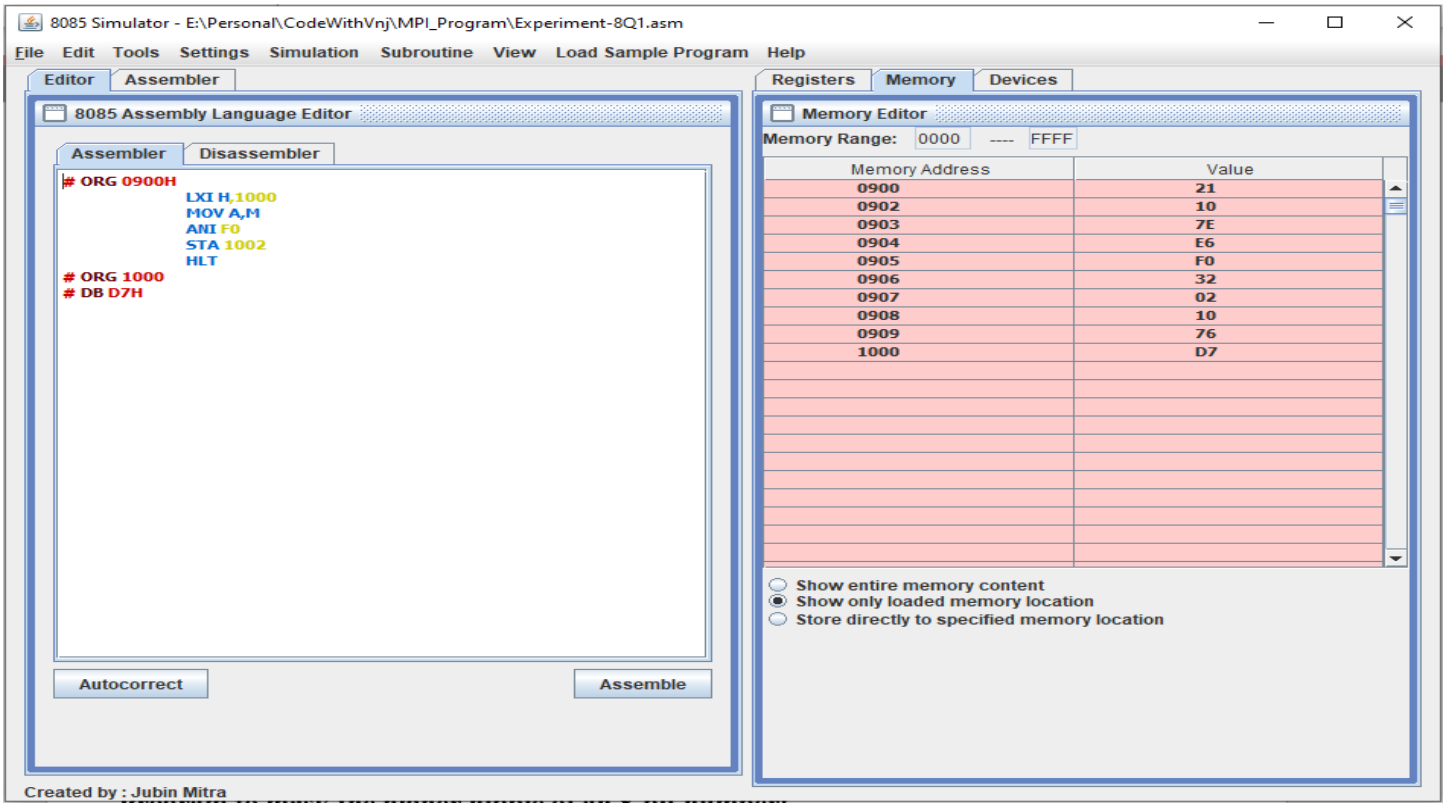
OR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File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
8085 Assembly Language Editor
Assembler Disassembler
ORG 0900H
LXI H,1000
MOV A,M
ANI F0
STA 1002
HLT
ORG 1000
DB D7H
Autocorrect Assemble
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
0900 21
0902 10
0903 7E
0904 E6
0905 F0
0906 32
0907 02
0908 10
0909 76
1000 D7
Show entire memory content
Show only loaded memory location
Store directly to specified memory location
Created by : Jubin Mitra

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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI F0	E6	2	2	7
	0905			F0			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Simulate

Start From → 0900

Run all At a Time | Step By Step

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	0900
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra

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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI F0	E6	2	2	7
	0905			F0			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	0000
Program Counter(PC)	0903
Clock Cycle Counter	10
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

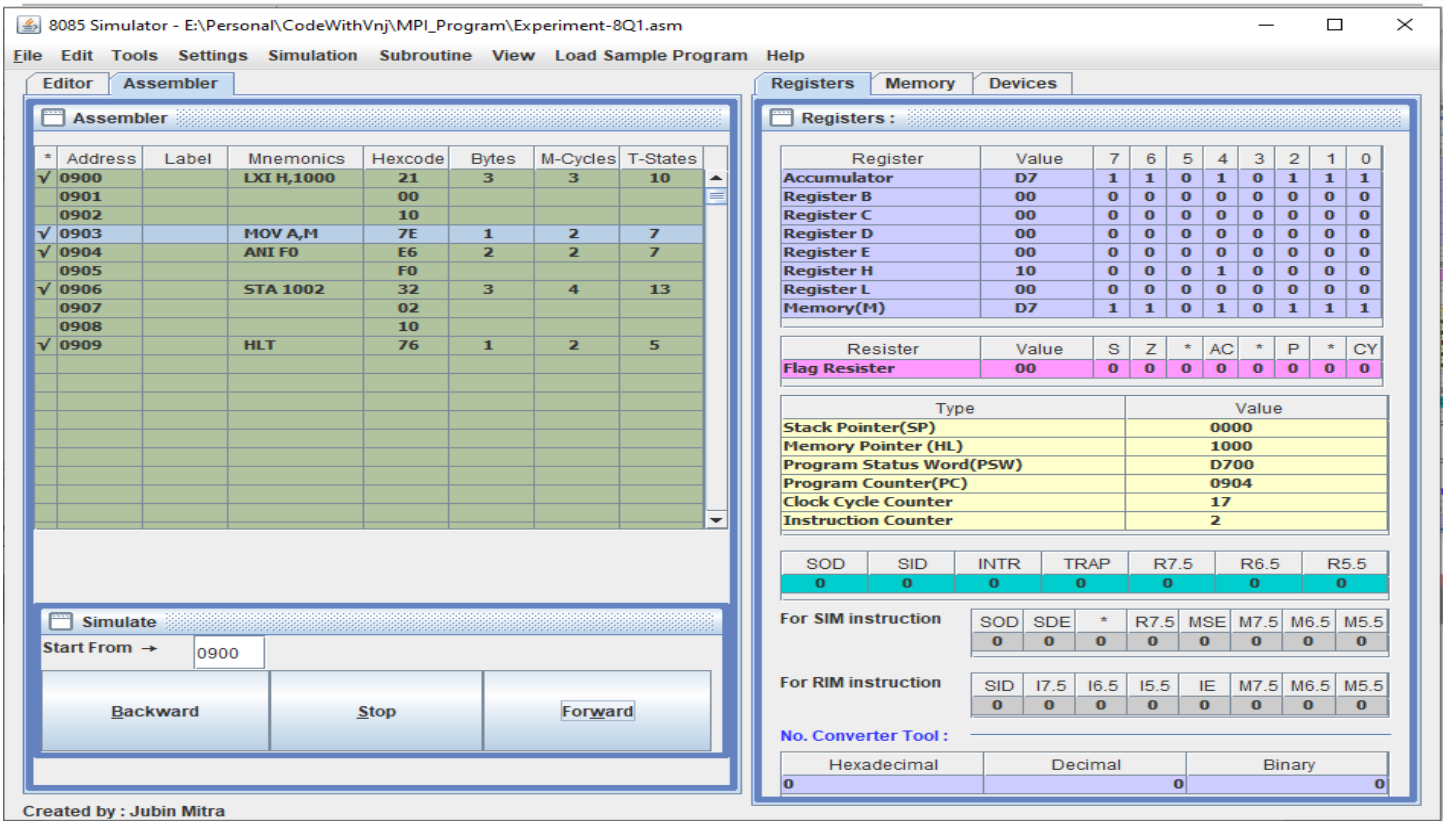
For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI F0	E6	2	2	7
	0905			F0			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D7	1	1	0	1	0	1	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	D700
Program Counter(PC)	0904
Clock Cycle Counter	17
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

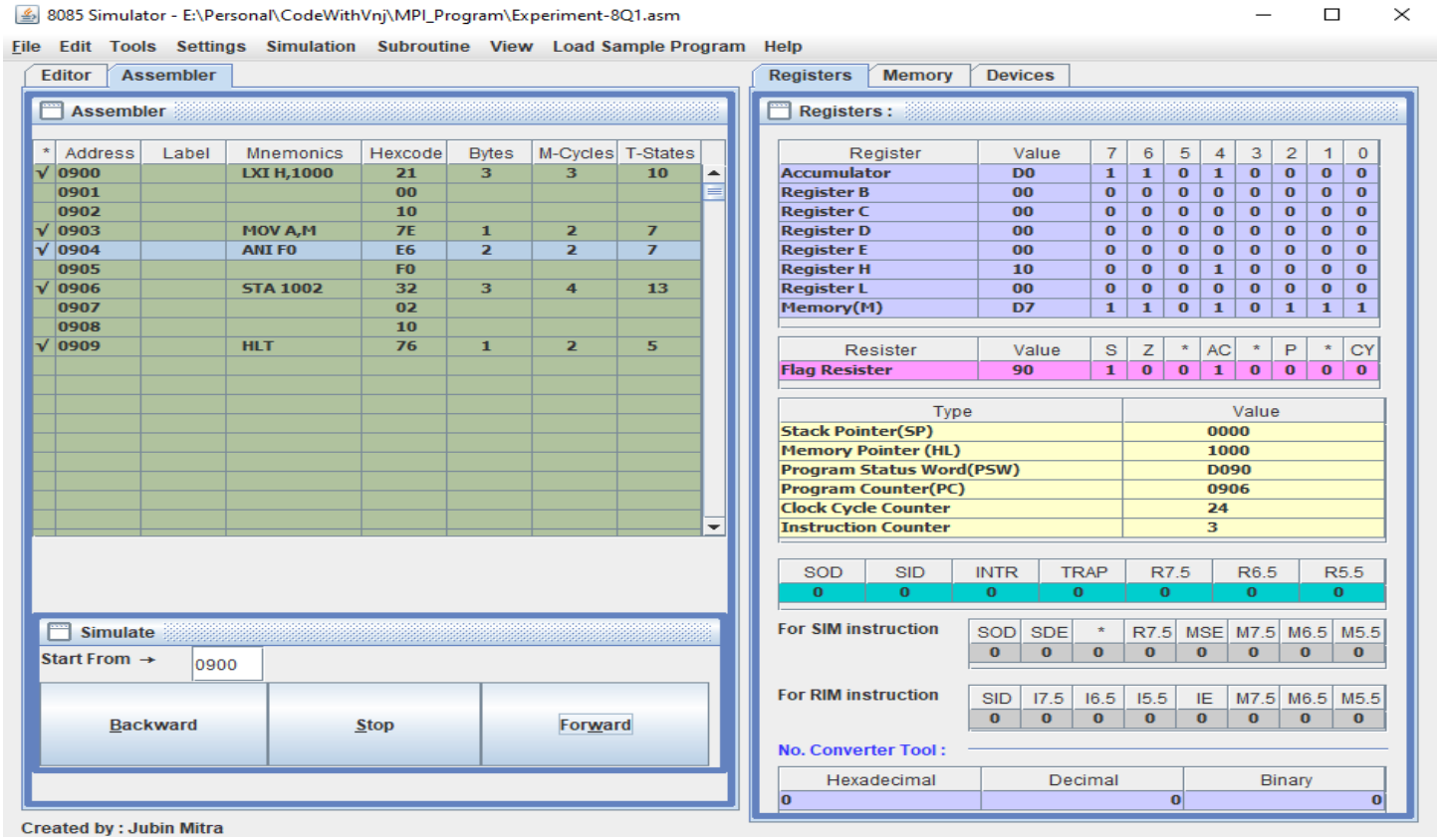
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI F0	E6	2	2	7
	0905			F0			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D0	1	1	0	1	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	90	1	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	D090
Program Counter(PC)	0906
Clock Cycle Counter	24
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

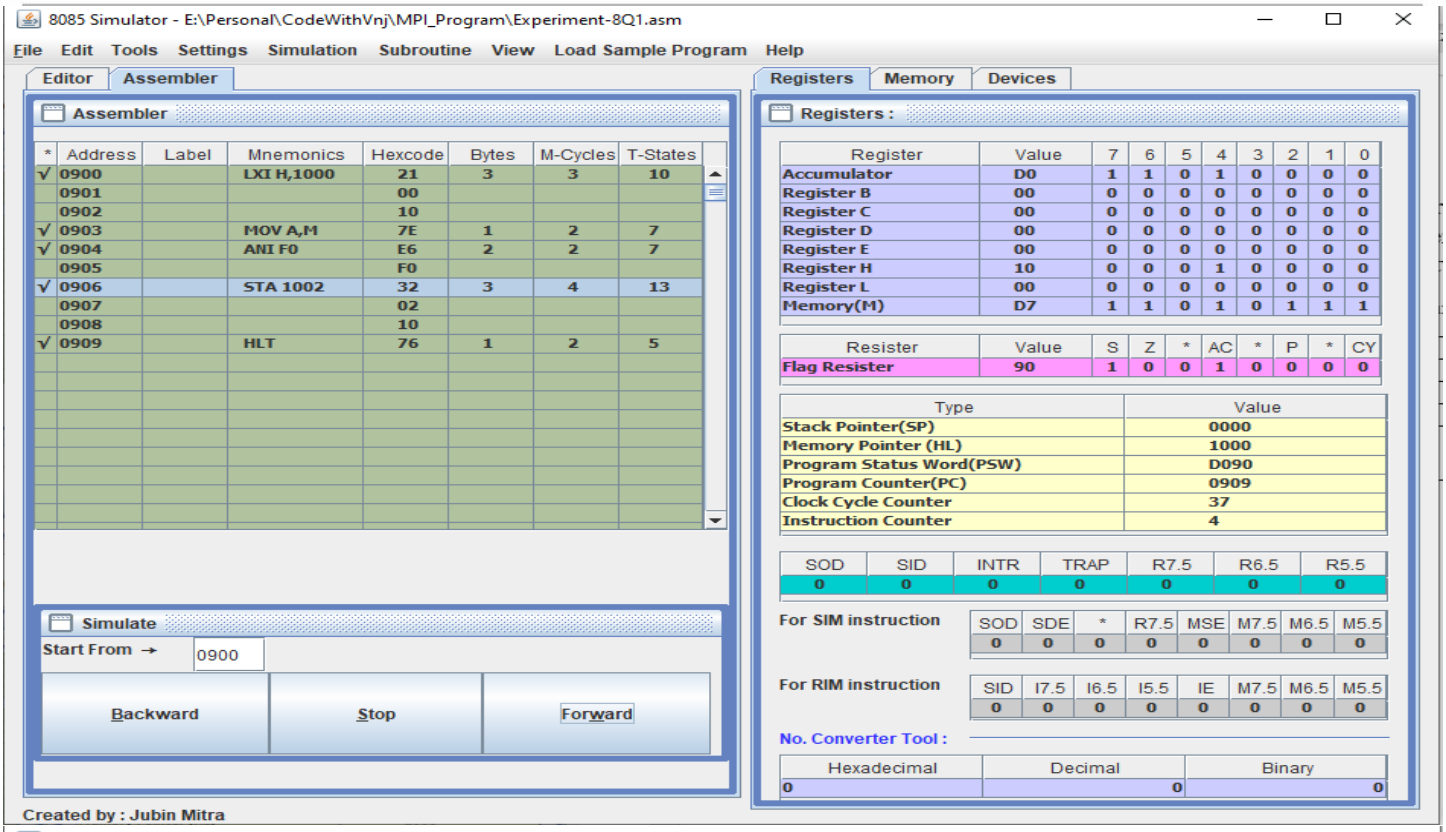
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI F0	E6	2	2	7
	0905			F0			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D0	1	1	0	1	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	90	1	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	D090
Program Counter(PC)	0909
Clock Cycle Counter	37
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

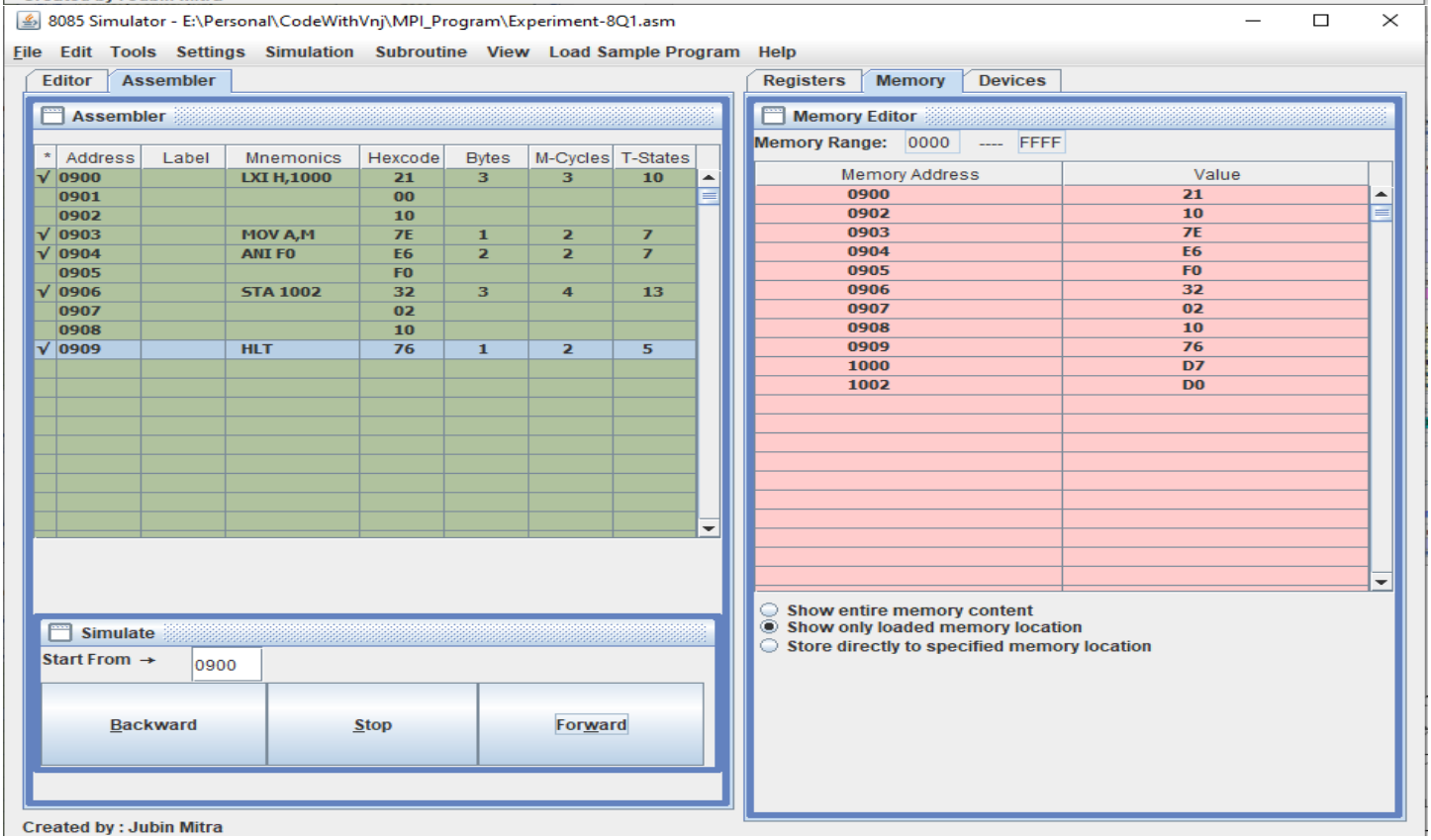
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI F0	E6	2	2	7
	0905			F0			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Memory Address	Value
0900	21
0902	10
0903	7E
0904	E6
0905	F0
0906	32
0907	02
0908	10
0909	76
1000	D7
1002	D0

Program to mask the higher nibble of an 8-bit number:

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

8085 Assembly Language Editor

Assembler | Disassembler

```
# ORG 0900H
        LDA 1000
        MOV B,A
        LDA 1001
        ANA B
        STA 1002
        HLT
# ORG 1000
# DB D7H,0FH
```

Autocorrect | Assemble

Registers | Memory | Devices

Memory Editor

Memory Range: 0000 ---- FFFF

Memory Address	Value
0900	3A
0902	10
0903	47
0904	3A
0905	01
0906	10
0907	A0
0908	32
0909	02
090A	10
090B	76
1000	D7
1001	0F

Show entire memory content
Show only loaded memory location
Store directly to specified memory location

Created by : Jubin Mitra

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Simulate

Start From → 0900

Run all At a Time | Step By Step

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	0900
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

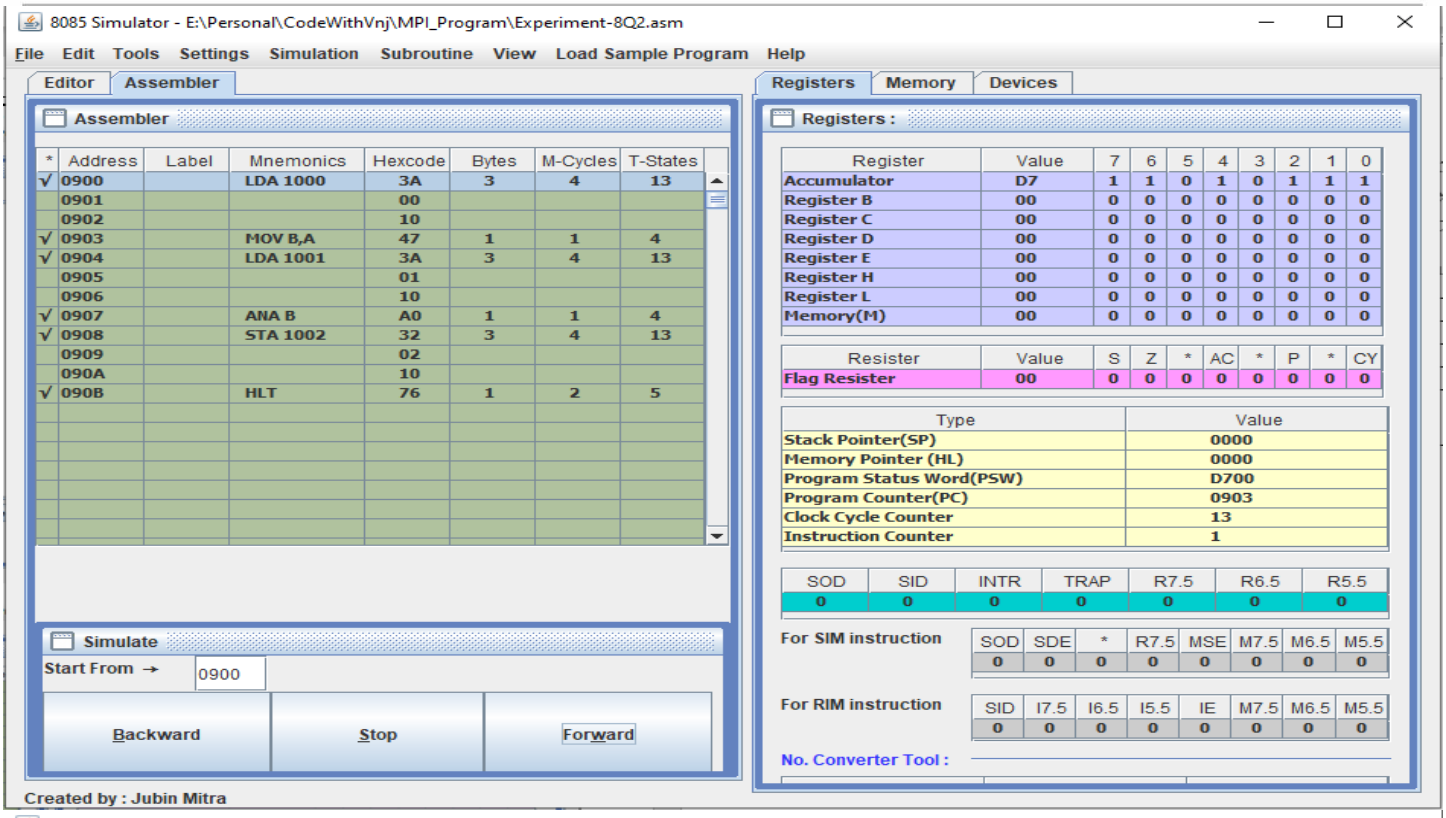
For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D7	1	1	0	1	0	1	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	D700
Program Counter(PC)	0903
Clock Cycle Counter	13
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

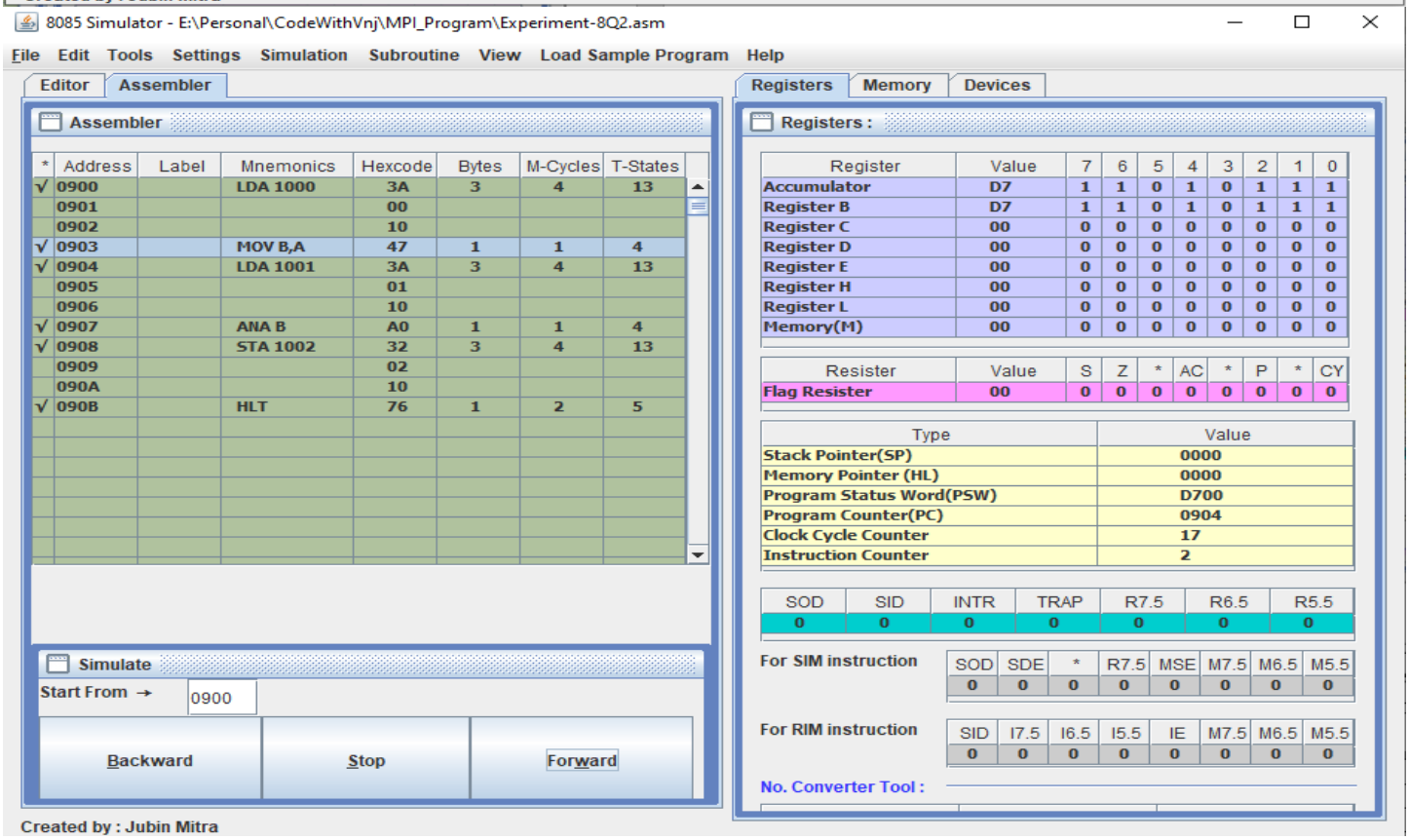
For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D7	1	1	0	1	0	1	1	1
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	D700
Program Counter(PC)	0904
Clock Cycle Counter	17
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

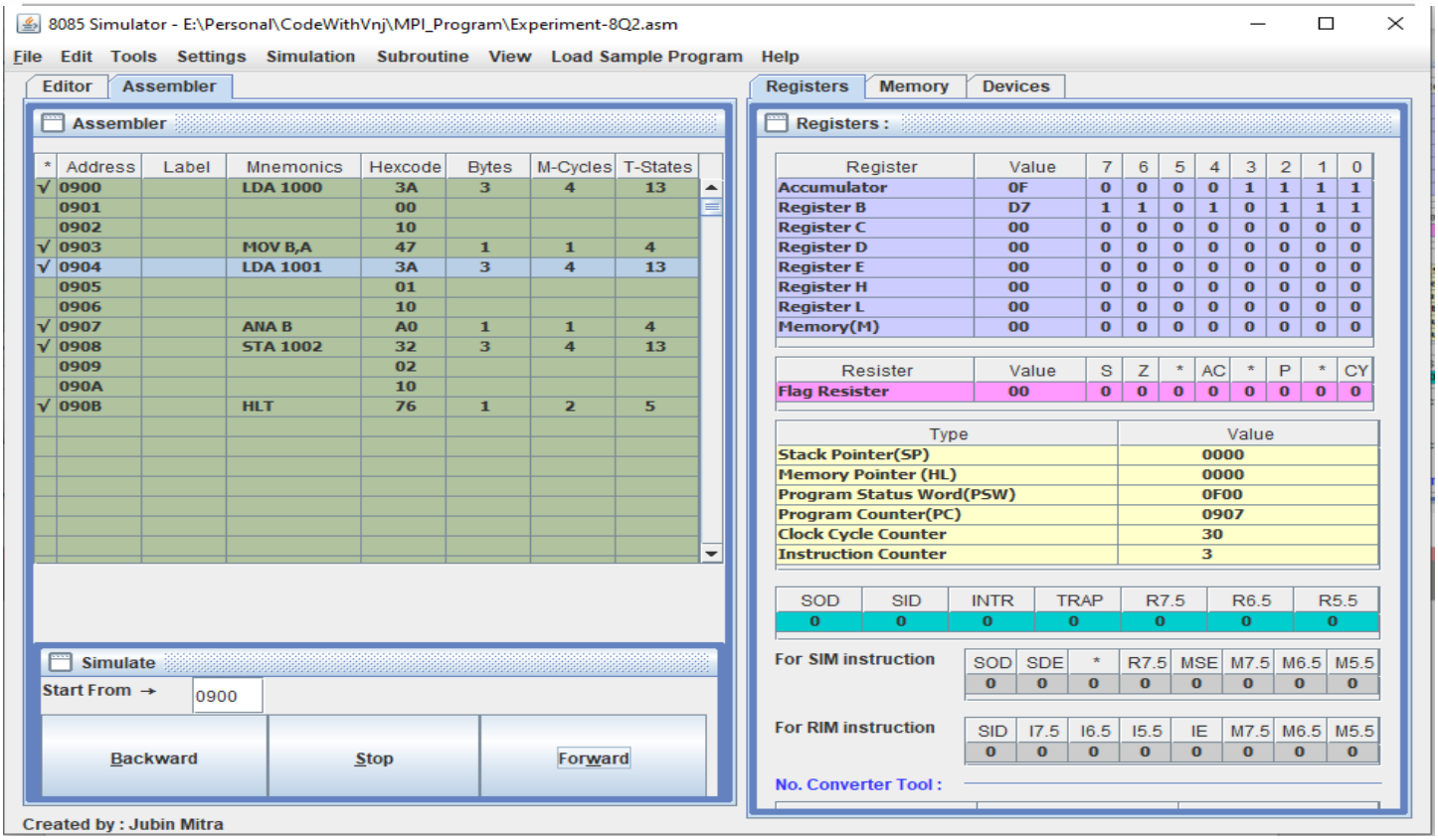
For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	0F	0	0	0	0	1	1	1	1
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0F00
Program Counter(PC)	0907
Clock Cycle Counter	30
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

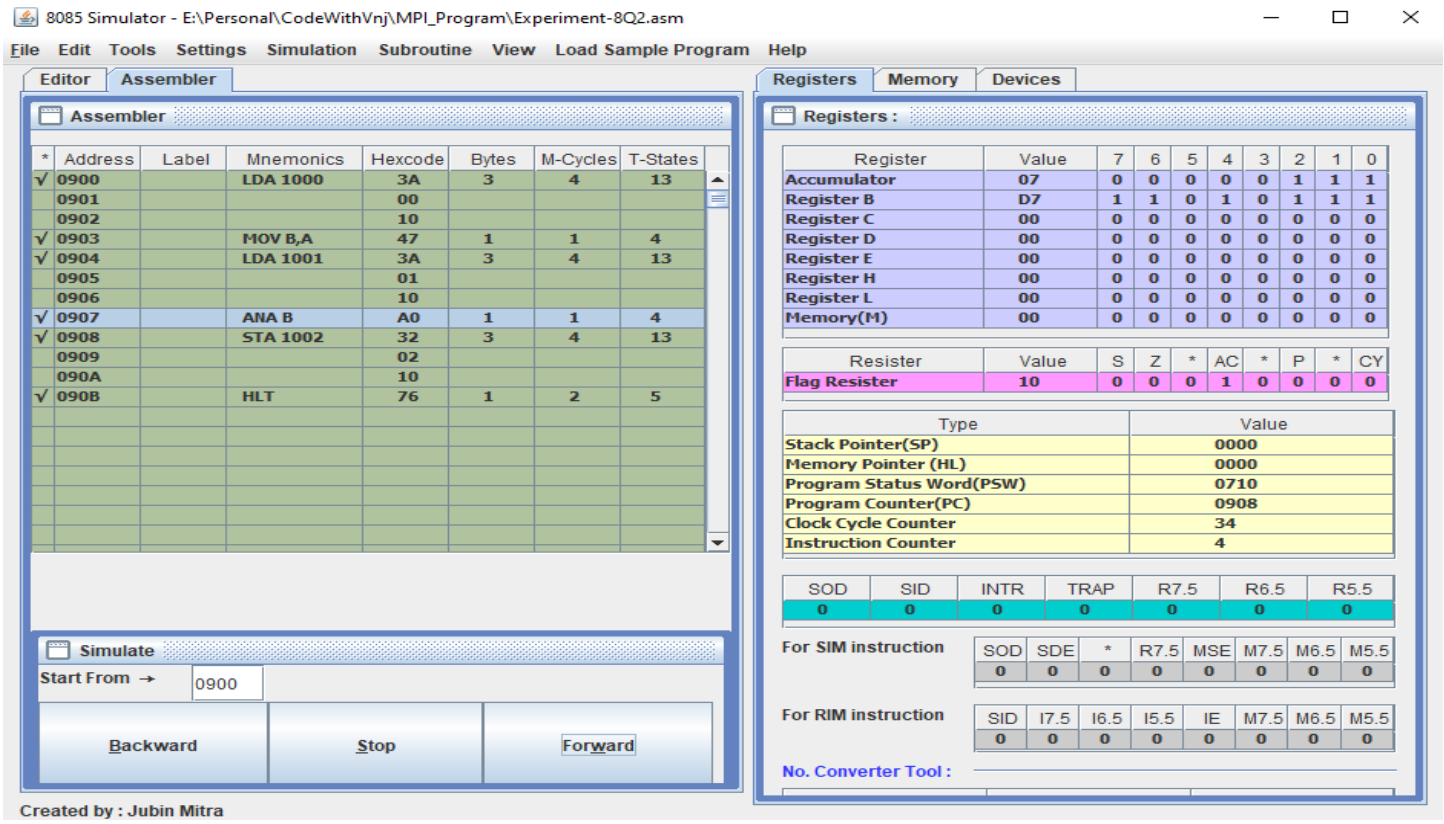
For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	07	0	0	0	0	0	1	1	1
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	10	0	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0710
Program Counter(PC)	0908
Clock Cycle Counter	34
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

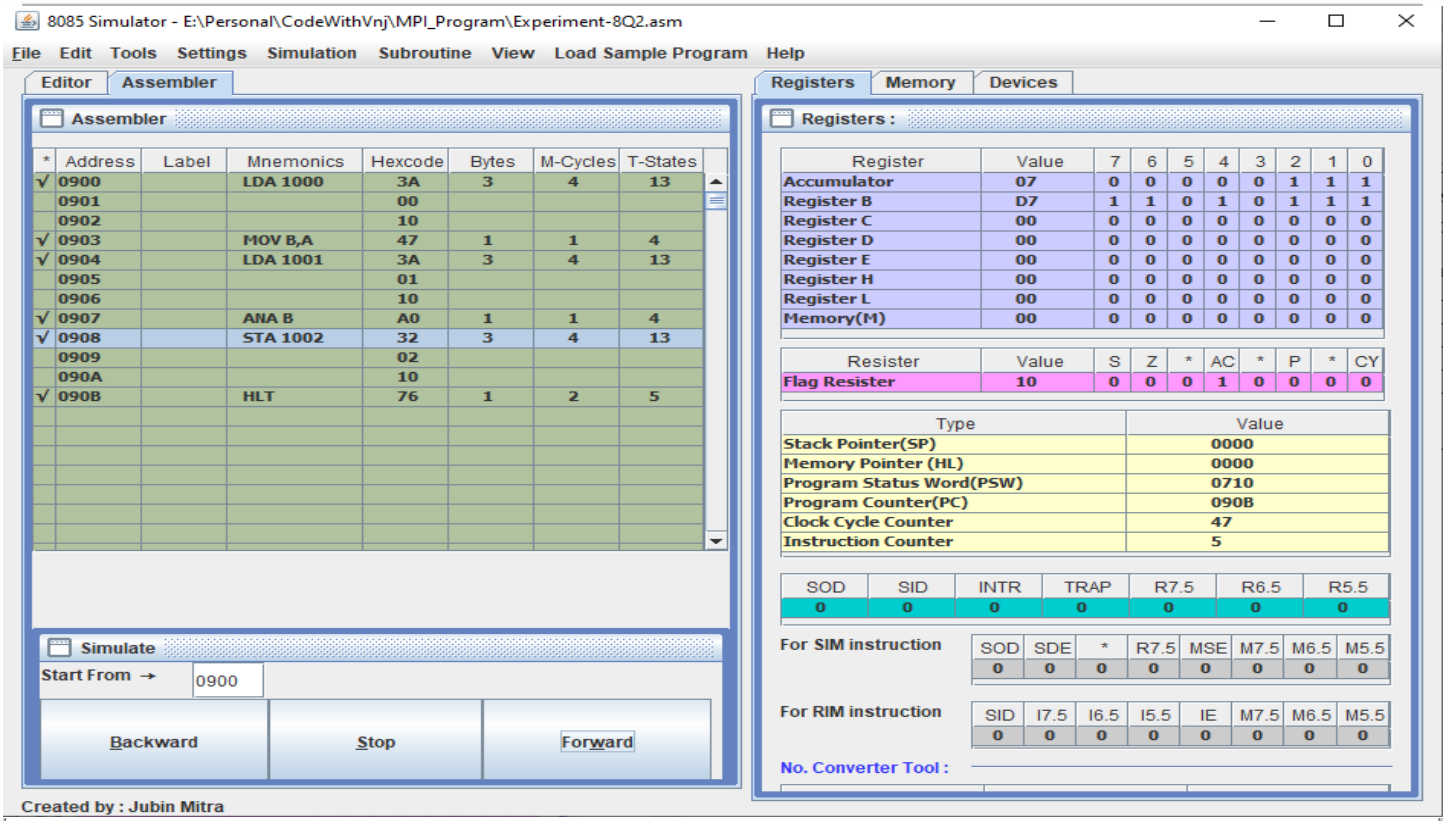
For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :



*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Register	Value	7	6	5	4	3	2	1	0
Accumulator	07	0	0	0	0	0	1	1	1
Register B	D7	1	1	0	1	0	1	1	1
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	10	0	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0710
Program Counter(PC)	090B
Clock Cycle Counter	47
Instruction Counter	5

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

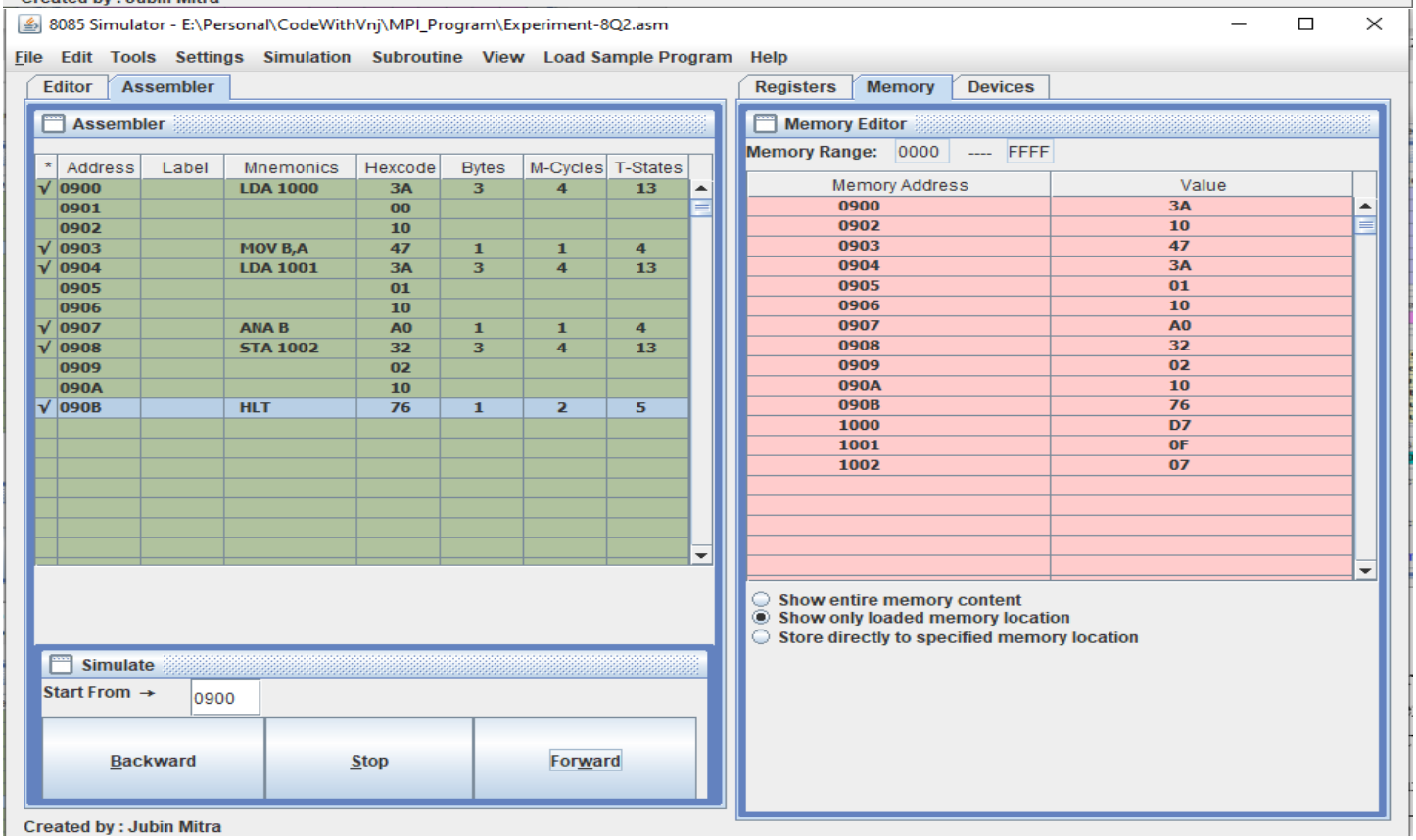
For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

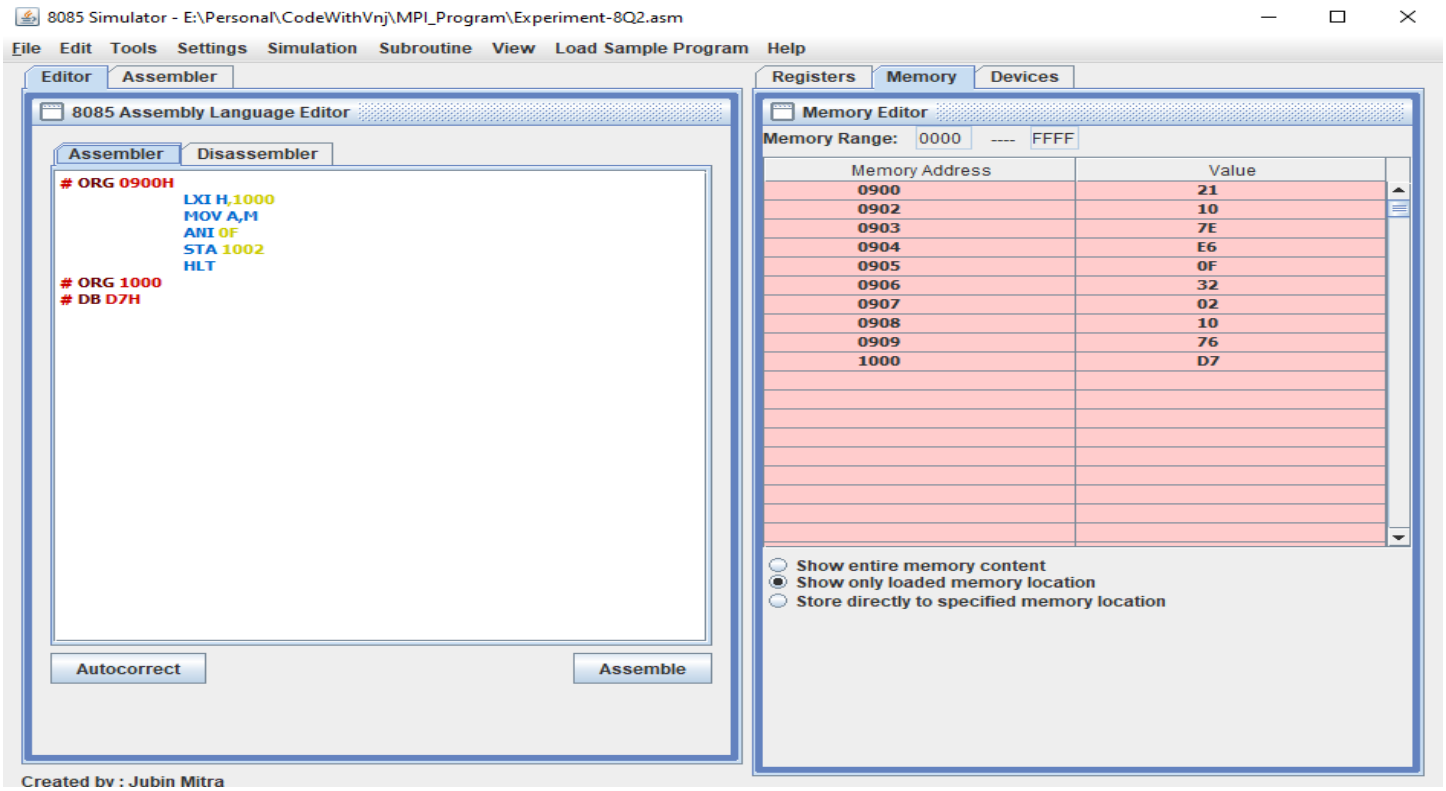
No. Converter Tool :

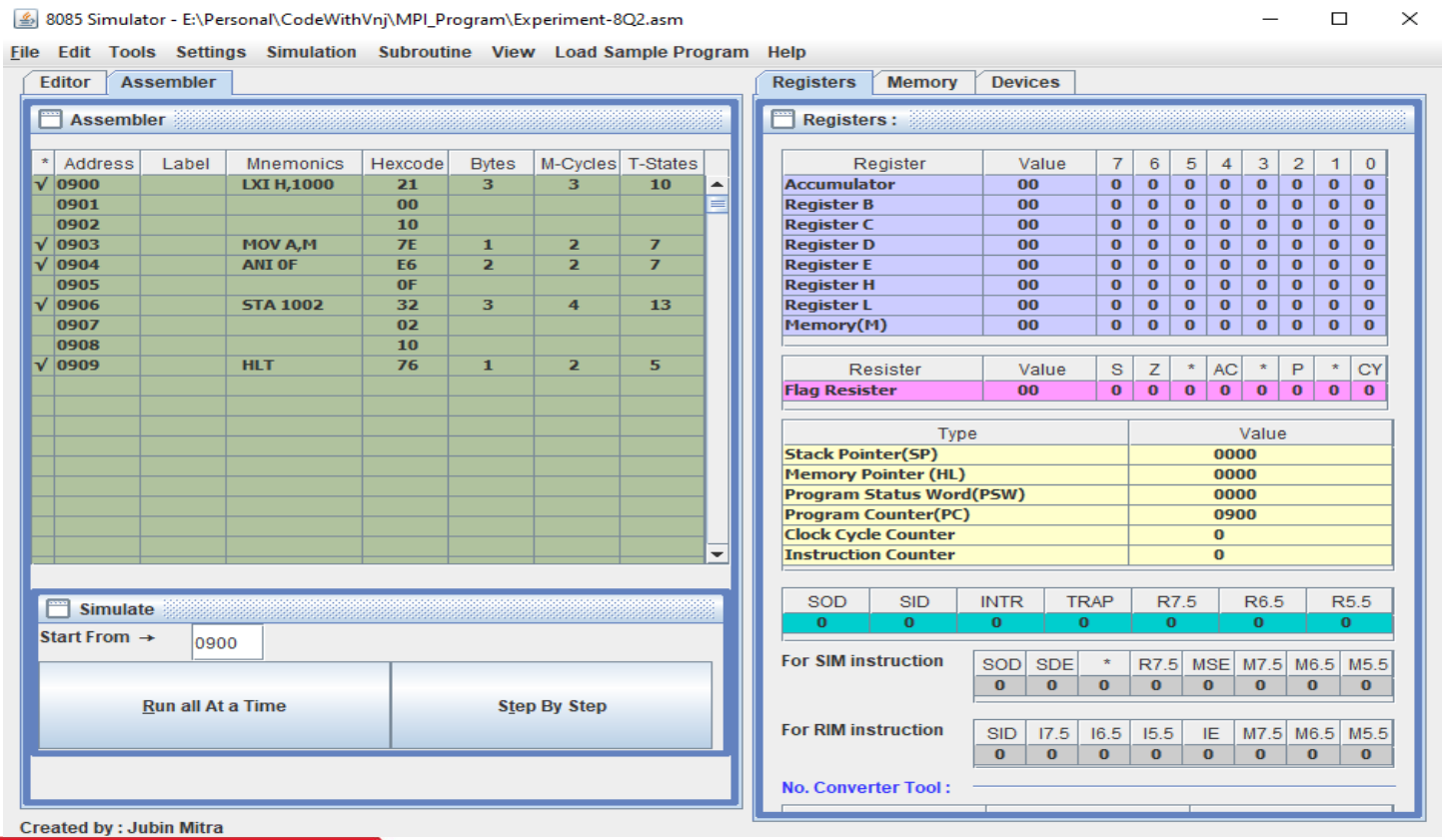


*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LDA 1000	3A	3	4	13
	0901			00			
	0902			10			
√	0903		MOV B,A	47	1	1	4
√	0904		LDA 1001	3A	3	4	13
	0905			01			
	0906			10			
√	0907		ANA B	A0	1	1	4
√	0908		STA 1002	32	3	4	13
	0909			02			
	090A			10			
√	090B		HLT	76	1	2	5

Memory Address	Value
0900	3A
0902	10
0903	47
0904	3A
0905	01
0906	10
0907	A0
0908	32
0909	02
090A	10
090B	76
1000	D7
1001	0F
1002	07

OR


8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
8085 Assembly Language Editor
Assembler Disassembler
ORG 0900H
LXI H,1000
MOV A,M
ANI 0F
STA 1002
HLT
ORG 1000
DB D7H
Autocorrect
Assemble
Registers Memory Devices
Memory Editor
Memory Range: 0000 ---- FFFF
Memory Address Value
0900 21
0902 10
0903 7E
0904 E6
0905 0F
0906 32
0907 02
0908 10
0909 76
1000 D7
Show entire memory content
Show only loaded memory location
Store directly to specified memory location
Created by : Jubin Mitra


8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm
File Edit Tools Settings Simulation Subroutine View Load Sample Program Help
Editor Assembler
Assembler
* Address Label Mnemonics Hexcode Bytes M-Cycles T-States
√ 0900 LXI H,1000 21 3 3 10
0901 00
0902 10
√ 0903 MOV A,M 7E 1 2 7
√ 0904 ANI 0F E6 2 2 7
0905 0F
√ 0906 STA 1002 32 3 4 13
0907 02
0908 10
√ 0909 HLT 76 1 2 5
Simulate
Start From → 0900
Run all At a Time
Step By Step
Registers Memory Devices
Registers :
Register Value 7 6 5 4 3 2 1 0
Accumulator 00 0 0 0 0 0 0 0 0
Register B 00 0 0 0 0 0 0 0 0
Register C 00 0 0 0 0 0 0 0 0
Register D 00 0 0 0 0 0 0 0 0
Register E 00 0 0 0 0 0 0 0 0
Register H 00 0 0 0 0 0 0 0 0
Register L 00 0 0 0 0 0 0 0 0
Memory(M) 00 0 0 0 0 0 0 0 0
Resister Value S Z * AC * P * CY
Flag Resister 00 0 0 0 0 0 0 0 0
Type Value
Stack Pointer(SP) 0000
Memory Pointer (HL) 0000
Program Status Word(PSW) 0000
Program Counter(PC) 0900
Clock Cycle Counter 0
Instruction Counter 0
SOD SID INTR TRAP R7.5 R6.5 R5.5
0 0 0 0 0 0 0
For SIM instruction
SOD SDE * R7.5 MSE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
For RIM instruction
SID I7.5 I6.5 I5.5 IE M7.5 M6.5 M5.5
0 0 0 0 0 0 0 0
No. Converter Tool :
Created by : Jubin Mitra

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI 0F	E6	2	2	7
	0905			0F			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	0000
Program Counter(PC)	0903
Clock Cycle Counter	10
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI 0F	E6	2	2	7
	0905			0F			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	D7	1	1	0	1	0	1	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	D700
Program Counter(PC)	0904
Clock Cycle Counter	17
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI 0F	E6	2	2	7
	0905			0F			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	07	0	0	0	0	0	1	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	10	0	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	0710
Program Counter(PC)	0906
Clock Cycle Counter	24
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

8085 Simulator - E:\Personal\CodeWithVnj\MPI_Program\Experiment-8Q2.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	0900		LXI H,1000	21	3	3	10
	0901			00			
	0902			10			
√	0903		MOV A,M	7E	1	2	7
√	0904		ANI 0F	E6	2	2	7
	0905			0F			
√	0906		STA 1002	32	3	4	13
	0907			02			
	0908			10			
√	0909		HLT	76	1	2	5

Simulate

Start From → 0900

Backward | Stop | Forward

Created by : Jubin Mitra

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	07	0	0	0	0	0	1	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	D7	1	1	0	1	0	1	1	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	10	0	0	0	1	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1000
Program Status Word(PSW)	0710
Program Counter(PC)	0909
Clock Cycle Counter	37
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

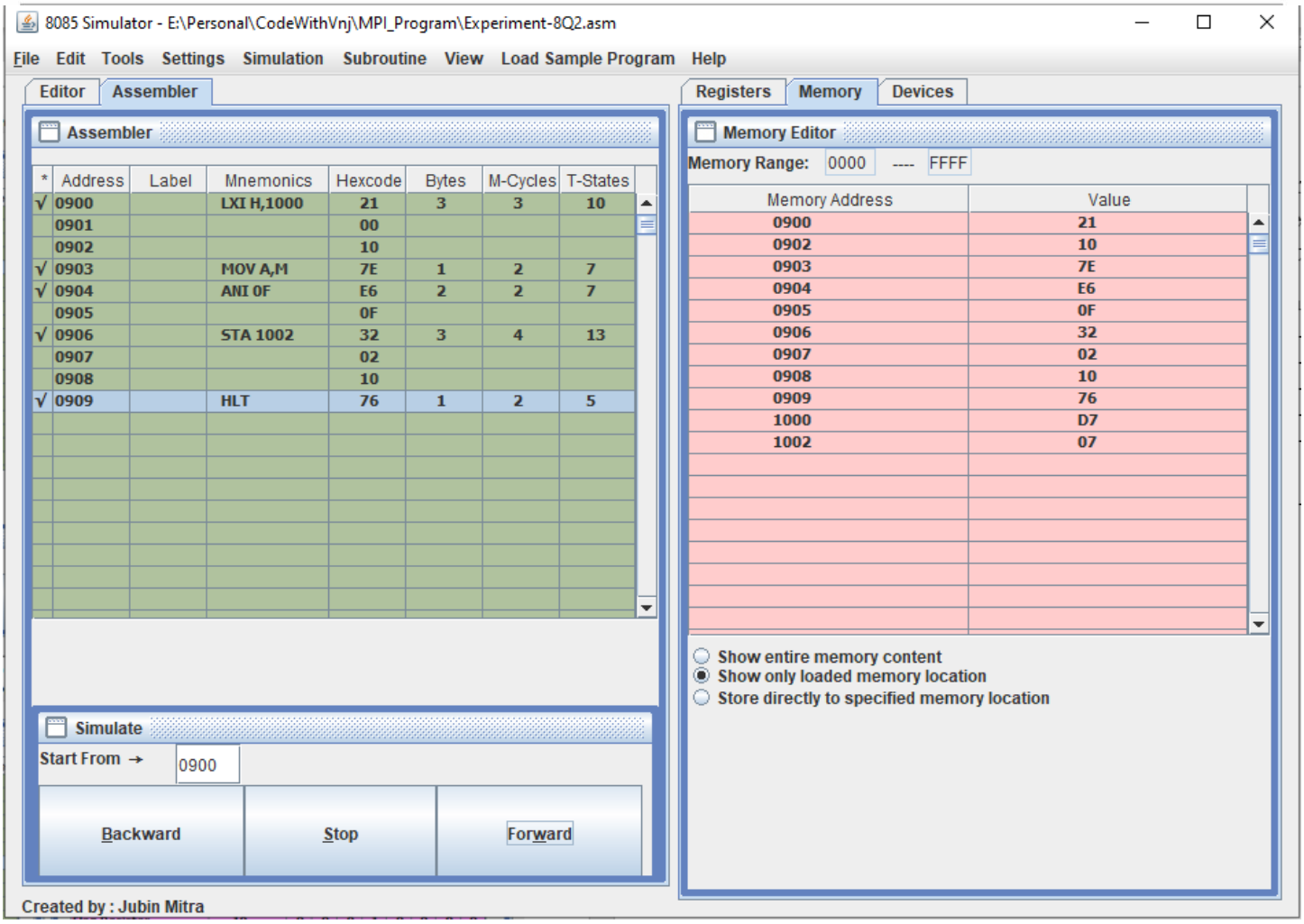
For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :



Learning outcomes (What I have learnt):

1. Learnt to mask the lower nibble of an 8-bit number.
2. Learnt to mask the higher nibble of an 8-bit number.
3. Learnt to perform the ANDing operation between two 8-bit number.

Evaluation Grid (To be created as per the SOP and Assessment guidelines by the faculty):

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			