Worksheet 1.1

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Branch: BE-CSE (LEET)

Section/Group: 20BCS-808/B

Semester: 4th Sem

Date of Performance: 20/02/2022

Subject Name: MPI Lab

Subject Code: 22E-20CSP-253

1. Aim/Overview of the practical:

Addition of two 8bit numbers, sum 8 bits.

2. Task to be done:

Write the 8085 Micro Processor program to calculate the addition of two 8bit numbers.

3. Apparatus/Simulator used (For applied/experimental sciences/materials-based labs):

I.   8085 Jubin simulator version 2 (Microprocessor Simulator)

II.   Java (jdk/ jre1.8.0_321)

4. Algorithm/Flowchart (For programming-based labs):

I.   Load the first number from memory location 1050 to Memory.

II. Move the content of memory to accumulator,

III. Move the content of accumulator to register H.

IV. Load the second number from memory location 1051 to Memory.

V.   Then add the content of register H and accumulator using "ADD" instruction and storing result at accumulator.

VI. Store the addition of both number in the register location at 1052.

5. Description/ Code:

According to the Given Instruction In Manual

```
# ORG 1000H
        LXI H,1000
        MOV A,M
        INX H
        MOV B,M
        MVI C,00
        ADD B
        JNC 000D
        INR C

000D:   INX H
        MOV M,C
        HLT
```

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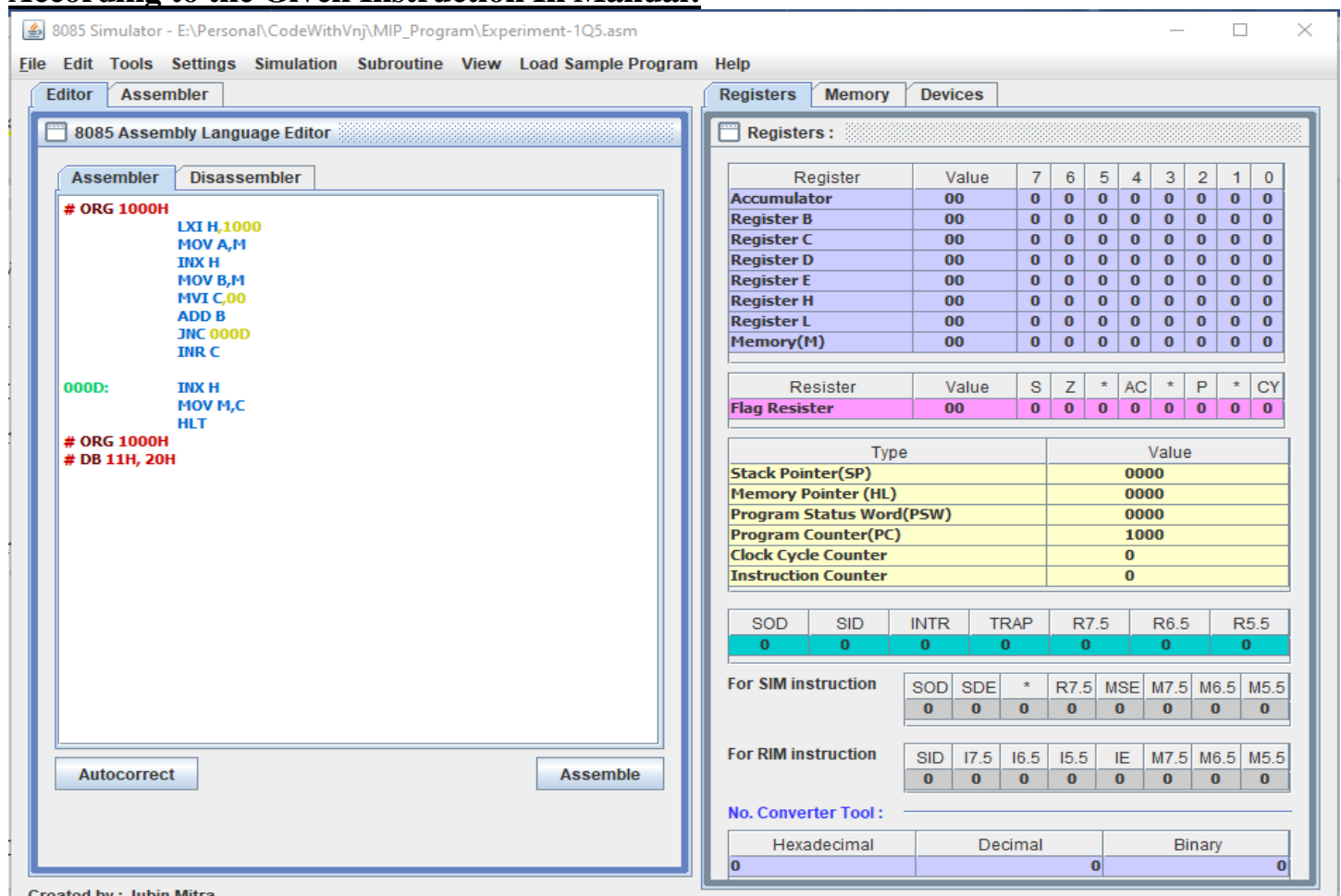
```
# ORG 1000H
# DB 11H, 20H
```

By Doing Experiment:

```
# ORG 1000H
        LXI H,1050
        MOV A,M
        INX H
        ADD M
        INX H
        MOV M,A
        HLT
# ORG 1050H
# DB 11H, 29H
```

6. Result/Output/Writing Summary:

According to the Given Instruction In Manual:

Screenshot 1

8085 Simulator - E:\Personal\CodeWithVnj\MIP_Program\Experiment-1Q5.asm

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1000	21	3	3	10
	1001			00			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		MOV B,M	46	1	2	7
√	1006		MVI C,00	0E	2	2	7
	1007			00			
√	1008		ADD B	80	1	1	4
√	1009		JNC 000D	D2	3	3	10
	100A			0D			
	100B			10			
√	100C		INR C	0C	1	1	4
√	100D	000D	INX H	23	1	1	6
√	100E		MOV M,C	71	1	2	7
√	100F		HLT	76	1	2	5

Simulate

Start From → 1000

Run all At a Time | Step By Step

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	1000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Screenshot 2

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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1000	21	3	3	10
	1001			00			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		MOV B,M	46	1	2	7
√	1006		MVI C,00	0E	2	2	7
	1007			00			
√	1008		ADD B	80	1	1	4
√	1009		JNC 000D	D2	3	3	10
	100A			0D			
	100B			10			
√	100C		INR C	0C	1	1	4
√	100D	000D	INX H	23	1	1	6
√	100E		MOV M,C	71	1	2	7
√	100F		HLT	76	1	2	5

Simulate

Start From → 1000

Run all At a Time | Step By Step

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	21	0	0	1	0	0	0	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	02	0	0	0	0	0	0	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1002
Program Status Word(PSW)	2104
Program Counter(PC)	100F
Clock Cycle Counter	69
Instruction Counter	10

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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By Doing Experiment Step By Step:

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8085 Assembly Language Editor

Assembler | Disassembler

```
# ORG 1000H
        LXI H,1050
        MOV A,M
        INX H
        ADD M
        INX H
        MOV M,A
        HLT
# ORG 1050H
# DB 11H, 29H
```

Autocorrect | Assemble

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Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	1000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Editor | **Assembler**

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Run all At a Time | Step By Step

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Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	0000
Program Counter(PC)	1000
Clock Cycle Counter	0
Instruction Counter	0

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

First Window

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Editor | Assembler

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

| Backward | Stop | Forward |

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	00	0	0	0	0	0	0	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	50	0	1	0	1	0	0	0	0
Memory(M)	11	0	0	0	1	0	0	0	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1050
Program Status Word(PSW)	0000
Program Counter(PC)	1003
Clock Cycle Counter	10
Instruction Counter	1

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

| Backward | Stop | Forward |

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	11	0	0	0	1	0	0	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	50	0	1	0	1	0	0	0	0
Memory(M)	11	0	0	0	1	0	0	0	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1050
Program Status Word(PSW)	1100
Program Counter(PC)	1004
Clock Cycle Counter	17
Instruction Counter	2

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Screenshot 1

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	11	0	0	0	1	0	0	0	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	51	0	1	0	1	0	0	0	1
Memory(M)	29	0	0	1	0	1	0	0	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1051
Program Status Word(PSW)	1100
Program Counter(PC)	1005
Clock Cycle Counter	23
Instruction Counter	3

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Screenshot 2

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

Backward | Stop | Forward

Registers | Memory | Devices

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	3A	0	0	1	1	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	51	0	1	0	1	0	0	0	1
Memory(M)	29	0	0	1	0	1	0	0	1

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1051
Program Status Word(PSW)	3A04
Program Counter(PC)	1006
Clock Cycle Counter	30
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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First Screenshot

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

| Backward | Stop | Forward |

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	3A	0	0	1	1	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	52	0	1	0	1	0	0	1	0
Memory(M)	00	0	0	0	0	0	0	0	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1052
Program Status Word(PSW)	3A04
Program Counter(PC)	1007
Clock Cycle Counter	36
Instruction Counter	5

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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Second Screenshot

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Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

| Backward | Stop | Forward |

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	3A	0	0	1	1	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	52	0	1	0	1	0	0	1	0
Memory(M)	3A	0	0	1	1	1	0	1	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1052
Program Status Word(PSW)	3A04
Program Counter(PC)	1008
Clock Cycle Counter	43
Instruction Counter	6

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra

Screenshot 1

8085 Simulator - E:\Personal\CodeWithVnj\MIP_Program\Experiment-1Q5.asm — □ ×

File   Edit   Tools   Settings   Simulation   Subroutine   View   Load Sample Program   Help

Editor | **Assembler**

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

[Backward]   [Stop]   [Forward]

Created by : Jubin Mitra

Registers | **Memory** | **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	3A	0	0	1	1	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	52	0	1	0	1	0	0	1	0
Memory(M)	3A	0	0	1	1	1	0	1	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1052
Program Status Word(PSW)	3A04
Program Counter(PC)	1008
Clock Cycle Counter	48
Instruction Counter	7

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Screenshot 2

8085 Simulator - E:\Personal\CodeWithVnj\MIP_Program\Experiment-1Q5.asm — □ ×

File   Edit   Tools   Settings   Simulation   Subroutine   View   Load Sample Program   Help

Editor | **Assembler**

Assembler

*	Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
√	1000		LXI H,1050	21	3	3	10
	1001			50			
	1002			10			
√	1003		MOV A,M	7E	1	2	7
√	1004		INX H	23	1	1	6
√	1005		ADD M	86	1	2	7
√	1006		INX H	23	1	1	6
√	1007		MOV M,A	77	1	2	7
√	1008		HLT	76	1	2	5

Simulate

Start From → 1000

[Run all At a Time]   [Step By Step]

Created by : Jubin Mitra

Registers | **Memory** | **Devices**

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	3A	0	0	1	1	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	10	0	0	0	1	0	0	0	0
Register L	52	0	1	0	1	0	0	1	0
Memory(M)	3A	0	0	1	1	1	0	1	0

Resister	Value	S	Z	*	AC	*	P	*	CY
Flag Resister	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	1052
Program Status Word(PSW)	3A04
Program Counter(PC)	1008
Clock Cycle Counter	53
Instruction Counter	8

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

Created by : Jubin Mitra

Learning outcomes (What I have learnt):

1. Learnt how to do the 8085-microprocessor programming.

2. Learnt how to add the two 8bit numbers with the carry.

3. Learnt how to add the two 8bits numbers without the carry.

Evaluation Grid (To be created as per the SOP and Assessment guidelines by the faculty):

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			