“FinFET Simulation in Cadence”

A Project Report Submitted
in Partial Fulfilment of the Requirements
for the Degree of

B.Tech.
in
ELECTRONICS AND COMMUNICATION ENGINEERING

By
Manish Jataw (2020BECE086)

ELECTRONICS AND COMMUNICATION ENGINEERING

MALVIYA NATIONAL INSTITUTE OF TECHNOLOGY
JAIPUR

2022-23

BONAFIDE CERTIFICATE

This is to certify that the project titled “FinFET Technolgy” is a bonafide record of the work done by

Manish Jataw (2020BECE086)

submitted to **MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY**, JAIPUR towards the partial requirement of Bachelor of Technology in **ELECTRONICS AND COMMUNICATION ENGINEERING**, during the year 2022-2023.

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Assistant Prof. (ECE)
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NO: NIT/T&P/INTP/2022-23/BECE/024
Date: 01-12-2022

Dr. Menka Yadav,
Assistant professor, MNIT Jaipur

Subject: **Permission of Internship online/offline for student of NIT Srinagar.**

In – Plant/on–the –project internship/Practical Training is an important part of our engineering curriculum. This internship/training is regarded as a vital component of engineering education and is an indicator of extent of field experience, which is very essential for attaining excellence in the technical education. In this context, **Mr. /Ms. Manish Jataw,** Enrolment No: **2020BECE086** pursuing B. Tech in ELECTRONICS & COMMUNICATIONS ENGINEERING DEPARTMENT (2020-2024) in this Institute has completed his/her 4th semester of the degree (pursuing in 5th semester) and is interested in 45 days internship in your esteemed organization.

It will be highly appreciated if your organization provides him/her a chance to get an exposure to some project related to him/her branch of engineering online/offline that is being carried out by your organization during winter vacation from 20th December 2022 to 15th February 2023.

We fervently hope that you will accede to our request and allow him/her to pursue him/her internship in your esteemed organization. The student has been advised to abide by the rules and regulation of your organization. Also, the student has to submit completion report and certificate in the training & placement department after completion of the internship, failing this his/her internship will be deemed incomplete.

Associate TPO (Internships)
Training and Placement
NIT Srinagar

Associate TPO (Internships)
Training & Placement Department
National Institute of Technology
Srinagar, J&K.

Deptt. of Training & Placement, NIT Srinagar, J&K

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Date: February **10**, 2023,

To Whom It May Concern

This is to certify that **Ms. Manish Jataw (2020BECE086),** Department of Electronics and Communication Engineering, National Institute of Technology Srinagar has carried out his internship on **Cadence Based Simulation of FinFET** during **December 20, 2022,** to **February 10, 2023,** under my supervision and guidance.

Menka 10/02/2023

Dr. Menka Yadav
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ASSISTANT PROFESSOR
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Acknowledgment

We took this opportunity to express our profound gratitude and deep regards to our guide Mr. Devendra Singh sir for his exemplary guidance, monitoring, and constant encouragement throughout the course of this training. The blessing, help, and guidance given by him from time to time shall carry us a long way in the journey of life on which we are about to embark.

We also take this opportunity to express a deep sense of gratitude to Mrs. Meneka Yadav mam for his cordial support, valuable information, and guidance, which helped us in completing this task through various stages.

Lastly, we thank Almighty, our parents, and our accompanying friends for their constant encouragement without whom this training would not have been possible.

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1 Introduction

Scaling of planar MOS increases the SCEs like hot carrier effects, gate-induced drain leakage (GIDL), leakage current such as subthreshold S/D leakage, gate direct tunneling leak-age, and drain-induced barrier lowering (DIBL). The impression of short channel effects (SCE) goes down the performance of planar MOS devices.

The limits most often cited are control of the density and location of dopants providing high I on /I off ratio and finite subthreshold slope and quantum-mechanical tunneling of carriers through the thin gate from drain to source and from drain to the body. The channel depletion width must scale with the channel length to contain the off-state leakage.

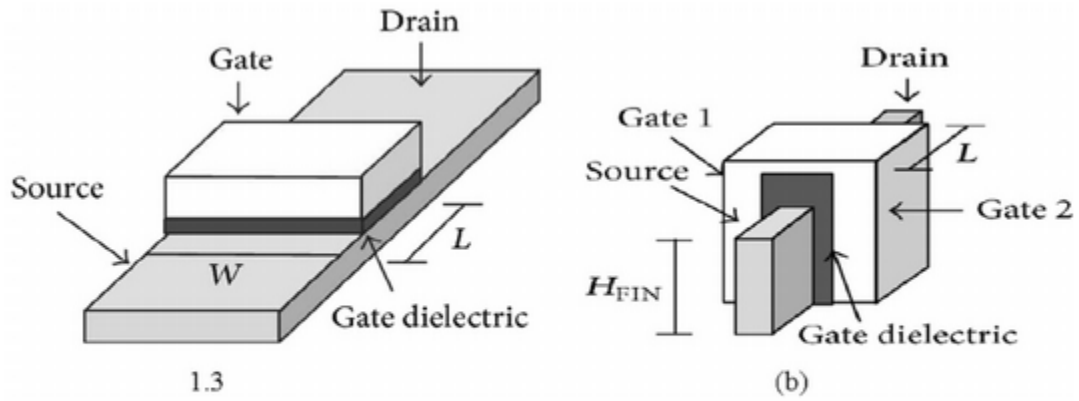
This **leads to high doping concentration, which degrades the carrier mobility and causes junction edge leakage due to tunneling. Furthermore, in terms of depth and steepness, the dopant profile control becomes much more difficult.**

The gate oxide thickness tox must also scale with the channel length to maintain gate control and proper threshold voltage VTand performance. The thinning of the gate dielectric results in gate tunneling leakage, degrading the circuit performance, power, and noise margin.

So the planar MOS technology moves towards the multi-gate MOSFETs for increased device performance.

Double gate MOSFET (DG-FET) is a MOSFET that has two gates to control the channel. Its schematic is shown in Fig. 1. Its main advantage is improved short-channel effects. Now a day FINFETS are very usually used because of short channel effects, are better at driving current, and are more compactable than other devices.

The structure of DG and Tri-gate FinFETs are almost the same except for the fact that in DG FinFET, the hard mask is used at the top portion of the fin so that only two gate remains effective for the channel control as shown in Fig.



The FinFETs are 3D-based emerging devices. It has low power consumption, smaller SCE effects, and a higher speed of operation.

The separate biasing in the DG devices quickly provides multiple threshold voltages. Its CMOS Logic Design with FINFETS Using 32nm TECHNOLOGY 33 can also be exploited to reduce the number of transistors for implementing logic functions. In this paper scale, down up to 32nm.

here power consumption of FINFETS will be less compared to bulk CMOS.

Effective channel length Leff = Lgate + 2×Lext (1)

Effective channel width W = Tfin + 2×Hfin

Where Hfin and Tfin are the fin height and thickness respectively, Lgate is the length of the gate, Lext is the extended source or drain region seen in the figure.

The main features offsets are – Ultra thin Si fin for suppression of short-channel effects, raised source/drain to reduce parasitic resistance, and improved current drive. FINFETs are designed to use multiple fins to achieve larger widths. FINFETS provides much lower sub-threshold leakage currents than bulk CMOS at the same gate length.

2 Fin Field-Effect Transistor

A FinFET is a transistor. Being a transistor, it is an amplifier and a switch. Its applications include home computers, laptops, tablets, smartphones, wearables, high-end networks, automotive, and more.

FinFET stands for a fin-shaped field-effect transistor. **Fin because it has a fin-shaped body – the silicon fin that forms the transistor's main body distinguishes** it. Field-effect because an electric field controls the conductivity of the material.

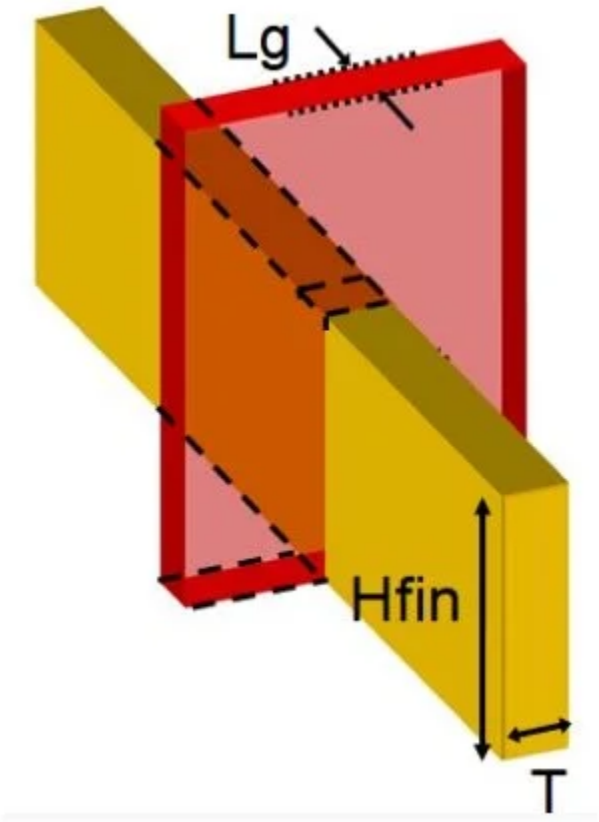
A FinFET is a non-planar device, i.e., not constrained to a single plane. It is also called 3D for having a third dimension.

To avoid confusion, it is essential to understand that different literature uses different labels when referring to FinFET devices.

- Choosing FinFET devices instead of traditional MOSFETs happens for a variety of reasons. Increasing computational power implies increasing computational density. More transistors are required to achieve this, which leads to larger chips. However, for practical reasons, it is crucial to keep the area about the same.
- **FinFET devices display superior short-channel behavior, have considerably lower switching times, and have higher current density than conventional MOSFET technology.**

The channel (fin) of the FinFET is vertical. This device requires keeping in mind specific dimensions. Evoking Max Planck's "quanta," the FinFET exhibits a property known as width quantization: its width is a multiple of its height. Random widths are not possible.

The fin thickness is a crucial parameter because it controls the short-channel behavior and the device's subthreshold swing. The subthreshold swing measures the efficiency of a transistor. It is the variation in gate voltage that increases the drain current one order of magnitude.



Lg = gate length

T = fin thickness

Hfin = fin height

W = transistor width (single fin)

Weff = effective transistor width (multiple fins)

For double-gate:

$$W = 2 \cdot Hfin$$

For tri-gate:

$$W = 2 \cdot Hfin + T$$

Multiple fins will increase the transistor width.

$$Weff = n \cdot W$$

Where n = number of fins

3 Prerequisite

1. Cadence Virtuoso:-

Key Benefits

- Supports custom analog, digital, and mixed-signal designs at the device, cell, block, and chip levels
- Accelerated performance and productivity from advanced full custom polygon editing through more flexible schematic and constraint-driven assisted full custom layout, to full custom layout automation
- Enables creation of differentiated custom silicon that is both fast and silicon accurate

Features

- New patented Virtuoso Layout Suite L graphics-rendering engine provides from 10X to 100X accelerated zoom, fit, pan, drag, and redraw performance on large layouts
- New Virtuoso Layout Suite XL connectivity extractor technology accelerates trace net, probe net, and mark net performance from 10X to 50X on large layouts
- Patented multi-user Express PCell capability continues to boost design opening performance from 10X to 20X whenever users require PCell evaluation
- New patented stream-in engine provides accelerated performance from 2X to 20X
- Virtuoso Layout Suite GXL Space-Based Routing technology automatically enforces process and design rules during interactive and assisted wire and bus editing

2. Verilog A:-

- Verilog-A is the analog-only subset of Verilog-AMS. It is intended to allow users of SPICE class simulators to create models for their simulations. Verilog-A models can be used in Verilog-AMS simulators, but in this case, you would be better served in most cases by using the full Verilog-AMS language. However, an initial step in learning the Verilog-AMS language is to learn Verilog-A.

- Verilog-A, like Verilog, is a hardware description language. As such, it is quite different from programming languages. There are similarities of course, and knowing a programming language will help you to understand Verilog-A, but hardware description imposes much different goals and constraints on a language than general programming and results in a much different language, one that might seem quite strange when unfamiliar. Unlike Verilog, which is a language intended to describe digital hardware, Verilog-A is intended to describe analog hardware. As such, Verilog-A is much different from Verilog and may seem quite strange to anyone comfortable with Verilog.

4 Candance-Based Simulations

Circuit NO. - 01

Title: - NMOS using FinFet.

Discussion:-

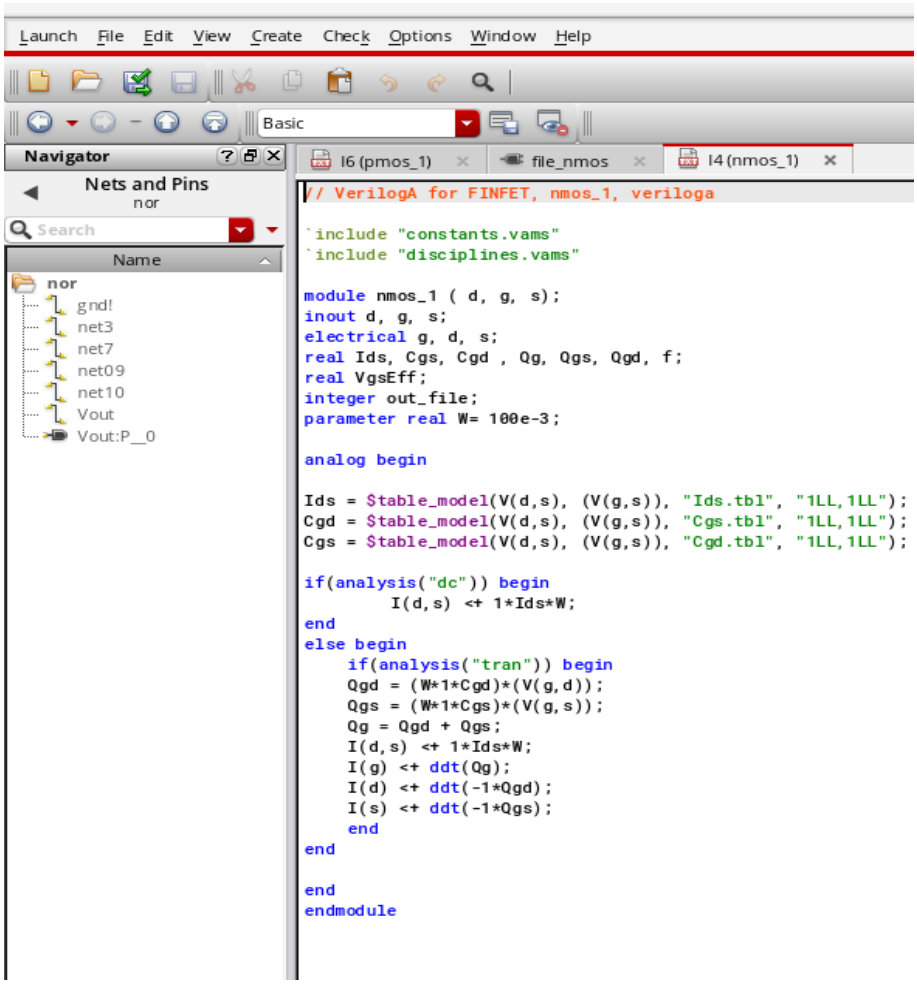
N-type metal–oxide–semiconductor logic uses n-type MOSFETs to implement logic gates and other digital circuits. These nMOS transistors operate by creating an inversion layer in a p-type transistor body. This inversion layer called the n-channel, can conduct electrons between n-type "source" and "drain" terminals.

We use Verilog-A code and cadence virtuoso to simulate our software.

- First, we make the NMOS model using Verilog - A and export their code.
- Then we make a new library in virtuoso and then a new cell and paste our NMOS code that gets from Verilog.
- While saving code in virtuoso set the type as VerilogA.

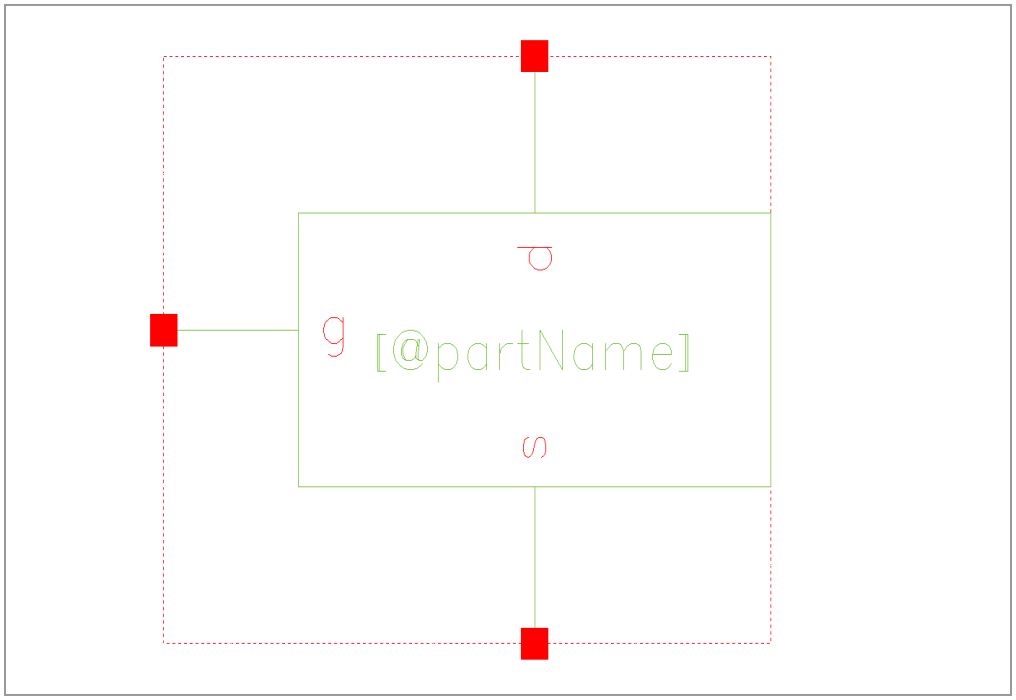
Making a Verilog-A Cell View

- And then save your code like this

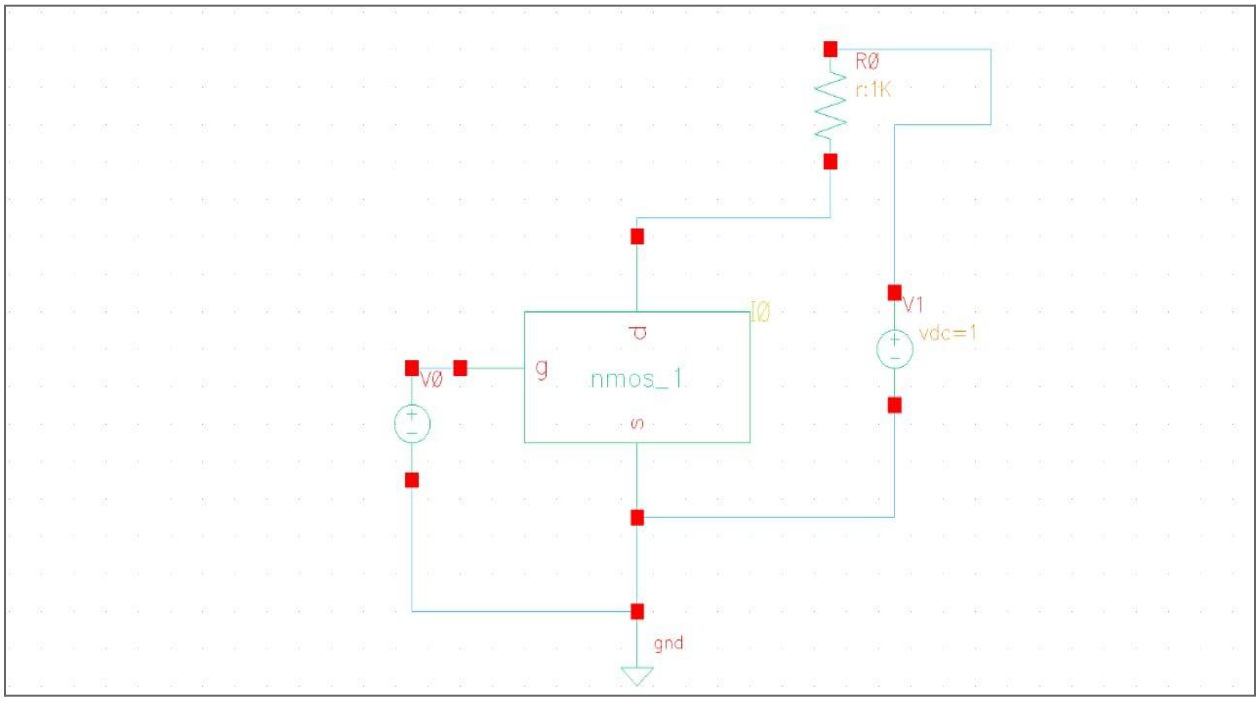


- After saving the code give them a good pin name with directions to create a good component
- Then open a cell and set the type as schematic and then make our NMOS circuit and simulate for different widths and heights of FinFET.

Component of NMOS using FinFET-



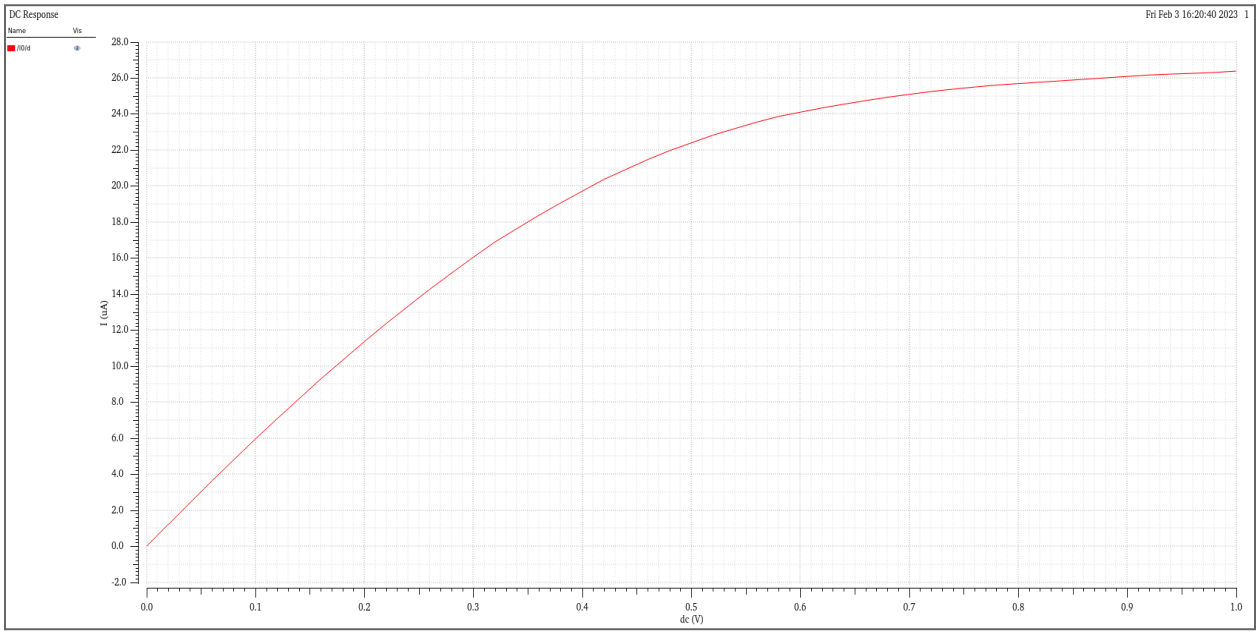
Schematic of NMOS-



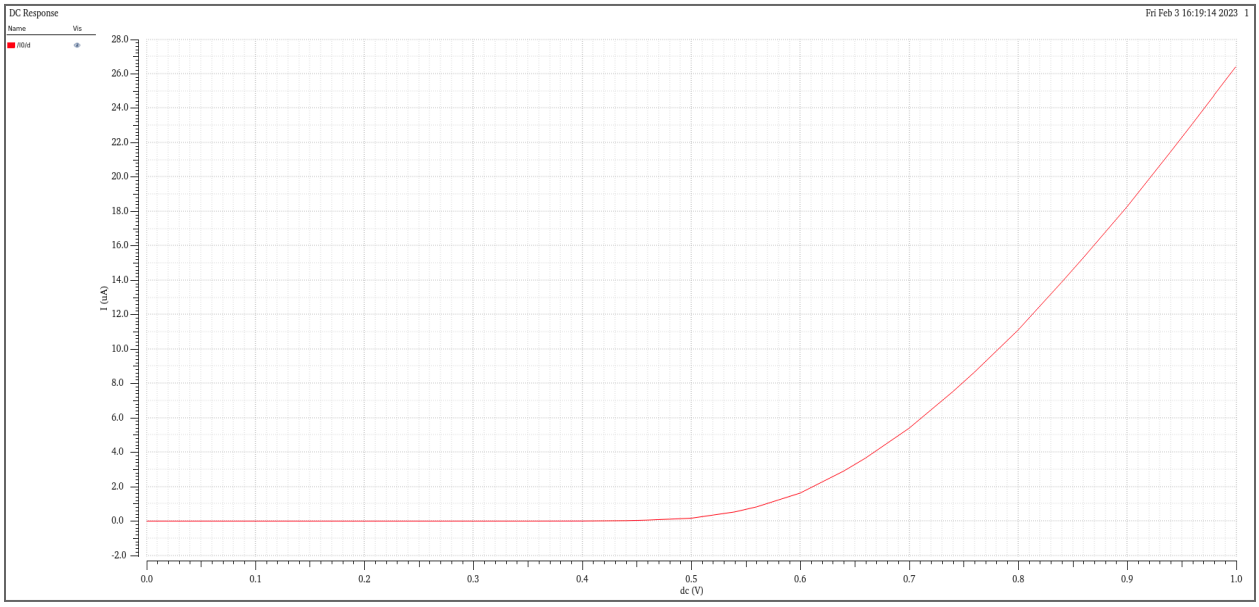
Results:-

Graphs-

- Ids v/s Vds



- Ids v/s Vgs



Title: - PMOS using FinFet.

Discussion:-

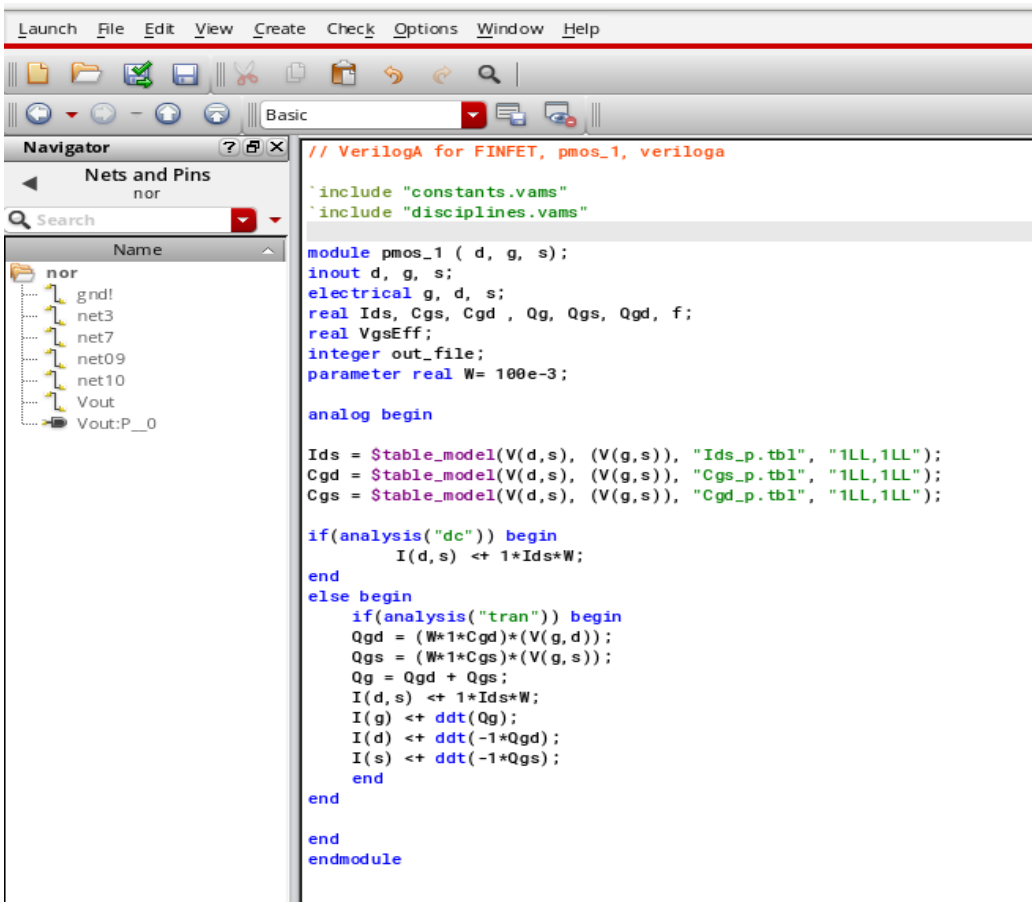
PMOS or pMOS logic is a family of digital circuits based on p-channel, enhancement mode metal–oxide–semiconductor field-effect transistors.

We use Verilog-A code and cadence virtuoso to simulate our software.

- First we make a PMOS model using Verilog - A and export their code.
- Then we make a new library in virtuoso and then a new cell and paste our NMOS code that gets from Verilog.
- While saving code in virtuoso set the type as Verilog

Making a Verilog-A Cell View

- And then save your code like this

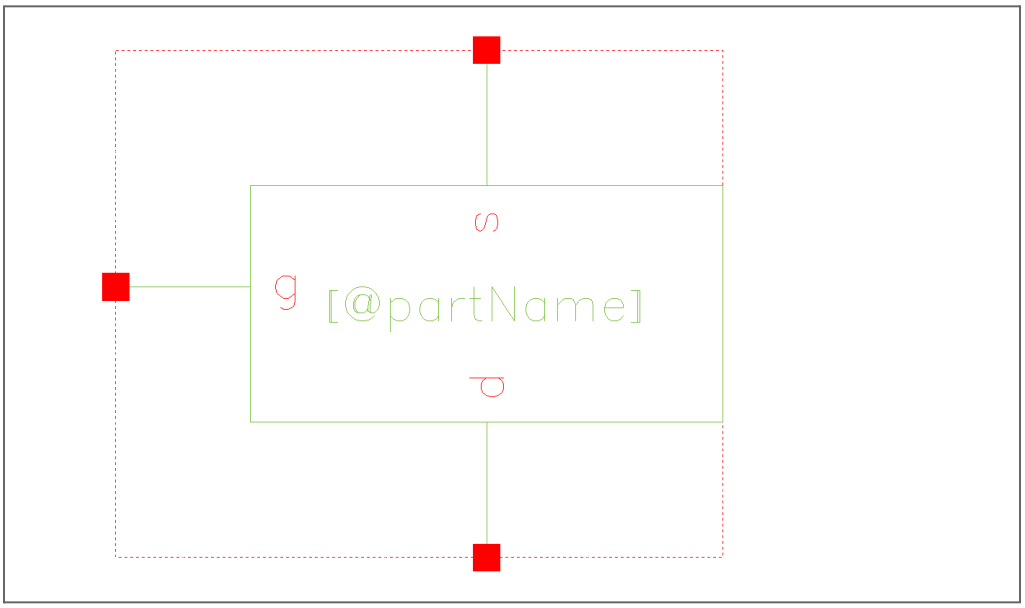


- After saving the code give them a good pin name with directions to create a good component

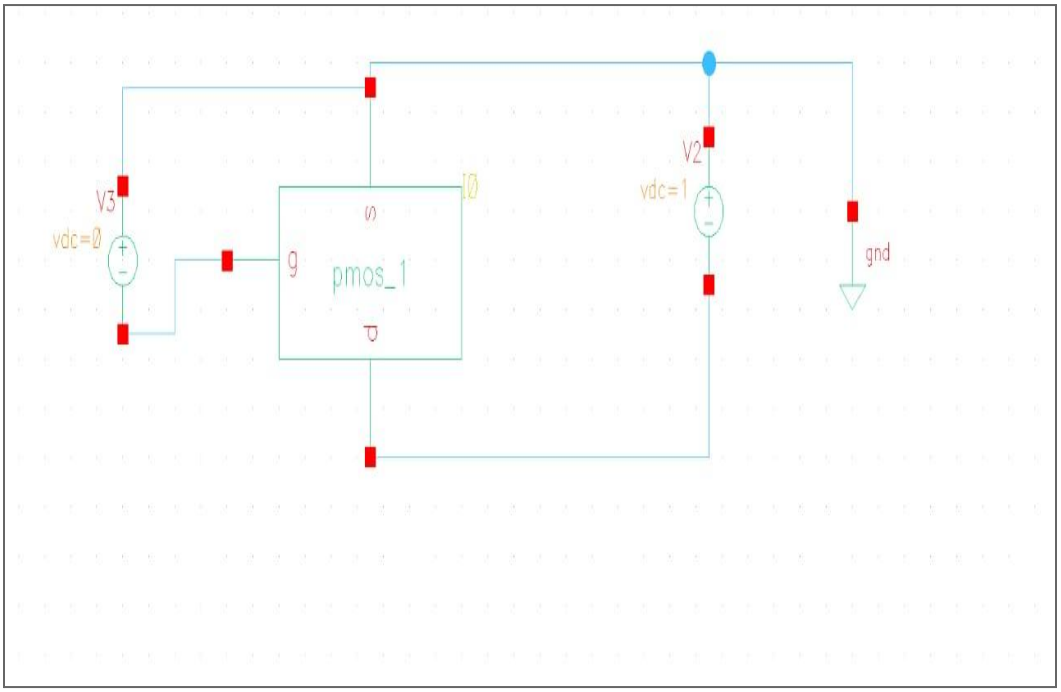
- Then open a cell and set the type as schematic and then make our NMOS circuit and simulate for different widths and heights of FinFet.

Schematic (In cadence):-

Component of PMOS-

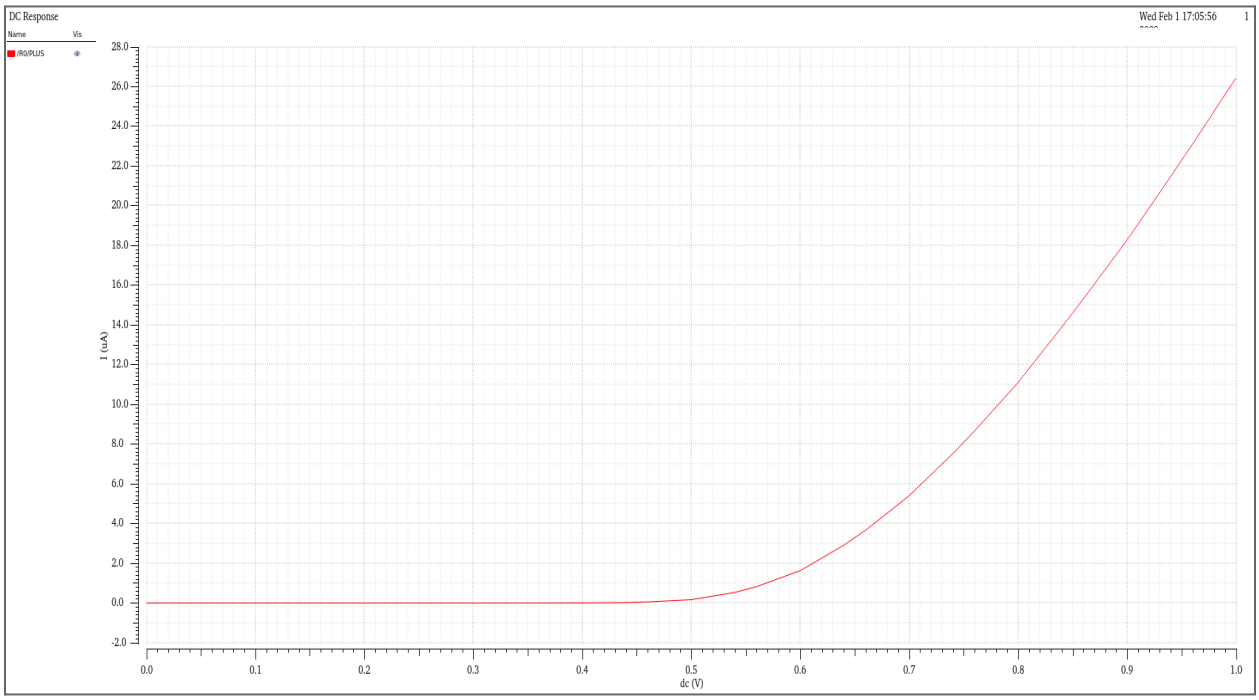


Schematic of PMOS-

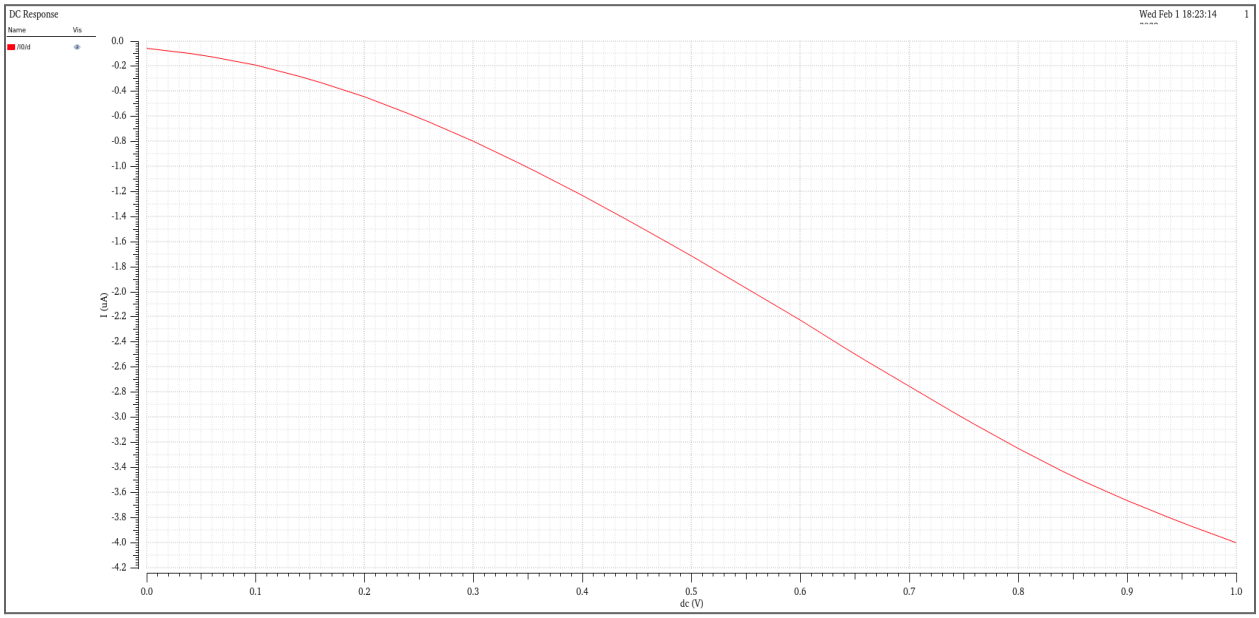


Results:-

- Ids vs Vgs



- Ids vs Vds



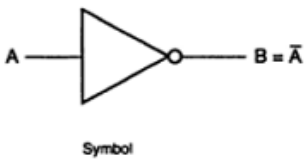
Title:- CMOS inverter using FinFet.

Discussion:-

A simple inverter inverts the logically high input to low output and vice versa. It is of immense significance in clock generation, generation of delays, memories to store the data, improving the circuit's noise immunity, and much more.

It is a simple two-transistor device. For input 0, PMOS turns ON, and NMOS stays OFF. This charges the output capacitance, thus making output logic HIGH. Whereas for input 1, PMOS is OFF, and NMOS is ON. The charged capacitance now discharges, making output logic LOW. On a periodic application of pulse, an inverted pulse is obtained at the output.

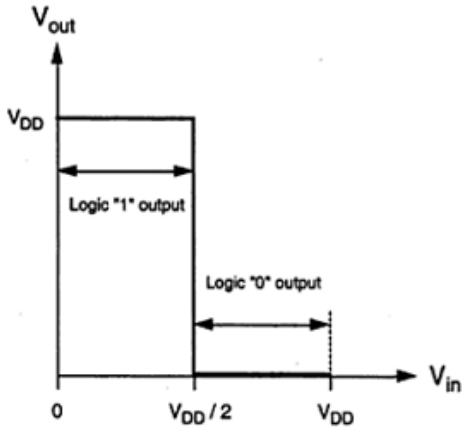
The in-depth analysis of the output on logic 0 to 1 at the input is summed up by its Voltage Transfer Characteristics (VTC).



Symbol

A	B
0	1
1	0

Truth Table

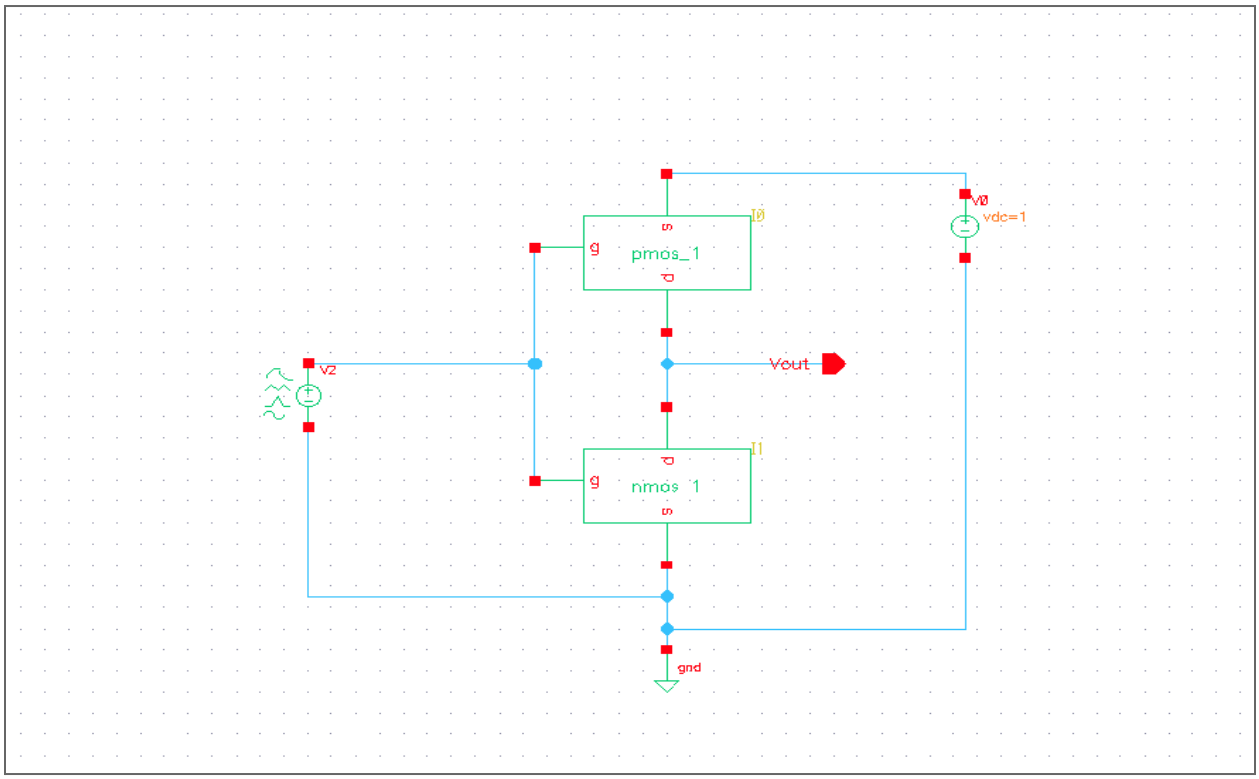


We use Verilog-A code and cadence virtuoso to simulate our software.

- First, we open our cadence virtuoso using the Linux terminal and create a new cell.
- Now we get FinFET PMOS and NMOS components, ground, and voltage.
- Then we make a circuit using wire and define our voltage sources.
- Now we make input and output labels and save the schematic.
- Then we run our schematic and analyze the output.

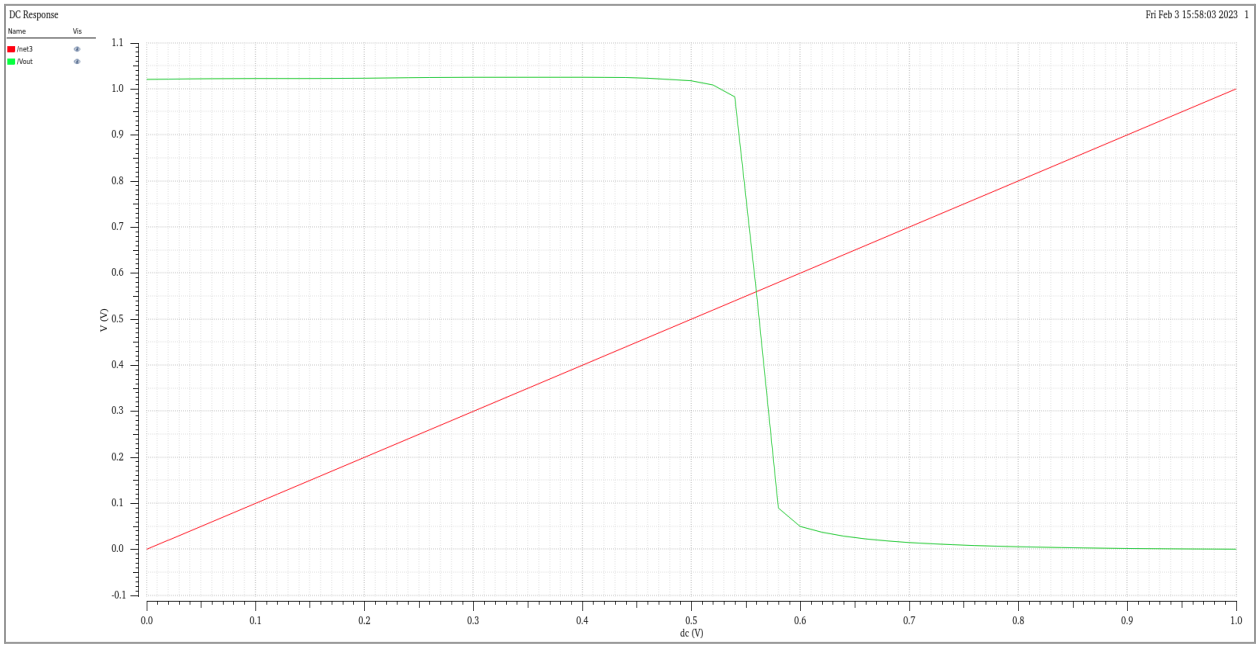
Schematic (In cadence):-

Schematic of CMOS Inverter-

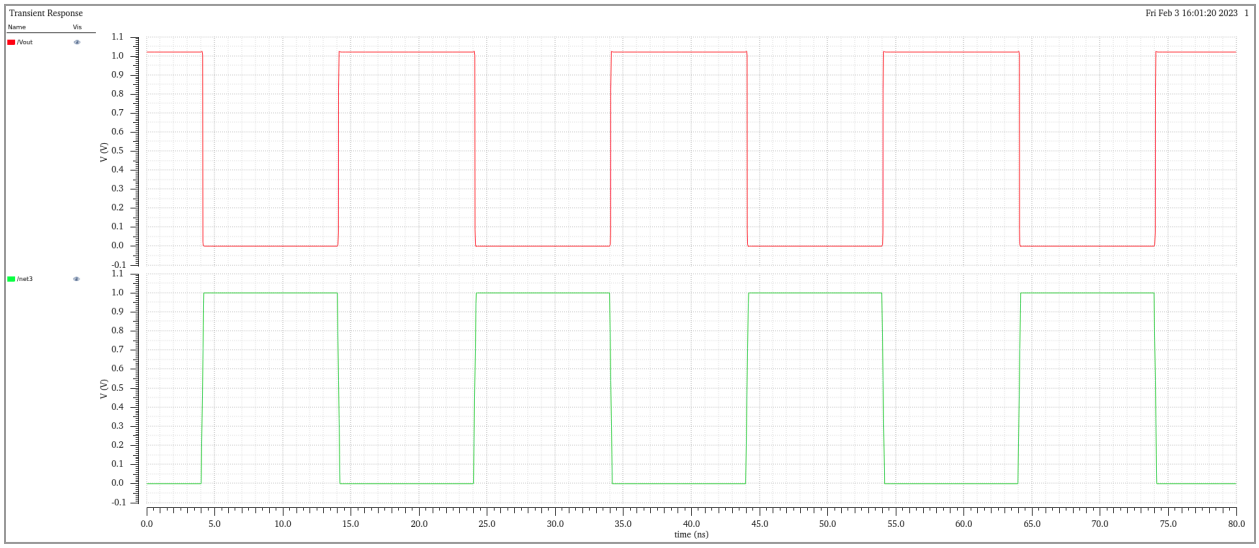


Results:-

- DC simulation:-



- Transient Analyse:-



Title: - NOR logic using FinFet.

Discussion:-.

The NOR gate is a digital logic gate that implements logical NOR - it behaves according to the truth table to the right. A HIGH output results if both the inputs to the gate are LOW; if one or both input is HIGH, a LOW output results. NOR is the result of the negation of the OR operator.

The logical expression for the output is

$$\overline{A} \; \overline{B} = \overline{A + B}$$

It is clear from the truth table that the output is '1' only if all the inputs are at logic '0'. It can also say that if the inputs A' = B' = 1, the output Y is 1. Thus, the NOR gate is equivalent to the AND gate with inverted inputs, and it can be realized by a bubbled AND gate, as shown above.

NOR Gate Truth Table

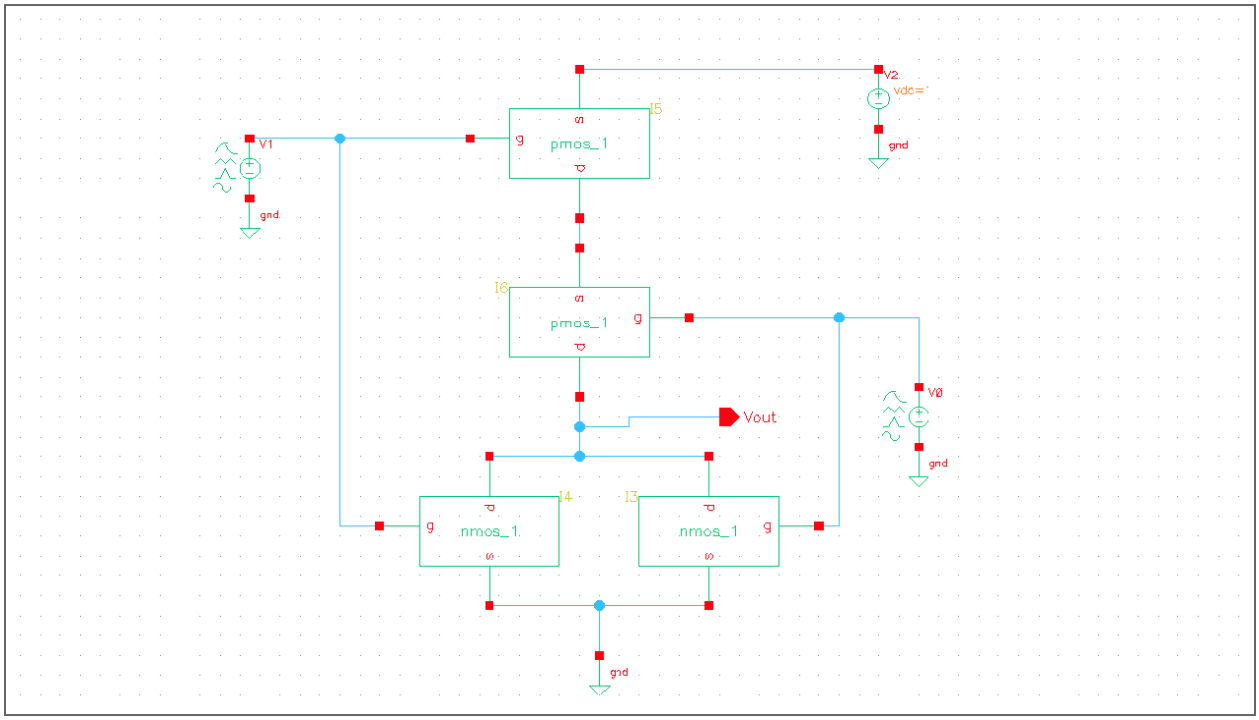
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

We use Verilog-A code and cadence virtuoso to simulate our software.

- First, we open our cadence virtuoso using the Linux terminal and create a new cell.
- Now we get FinFET PMOS and NMOS components, ground, and voltage.
- Then we make a circuit using wire and define our voltage sources.
- Now we make input and output labels and save the schematic.
- Then we run our schematic and analyze the output.

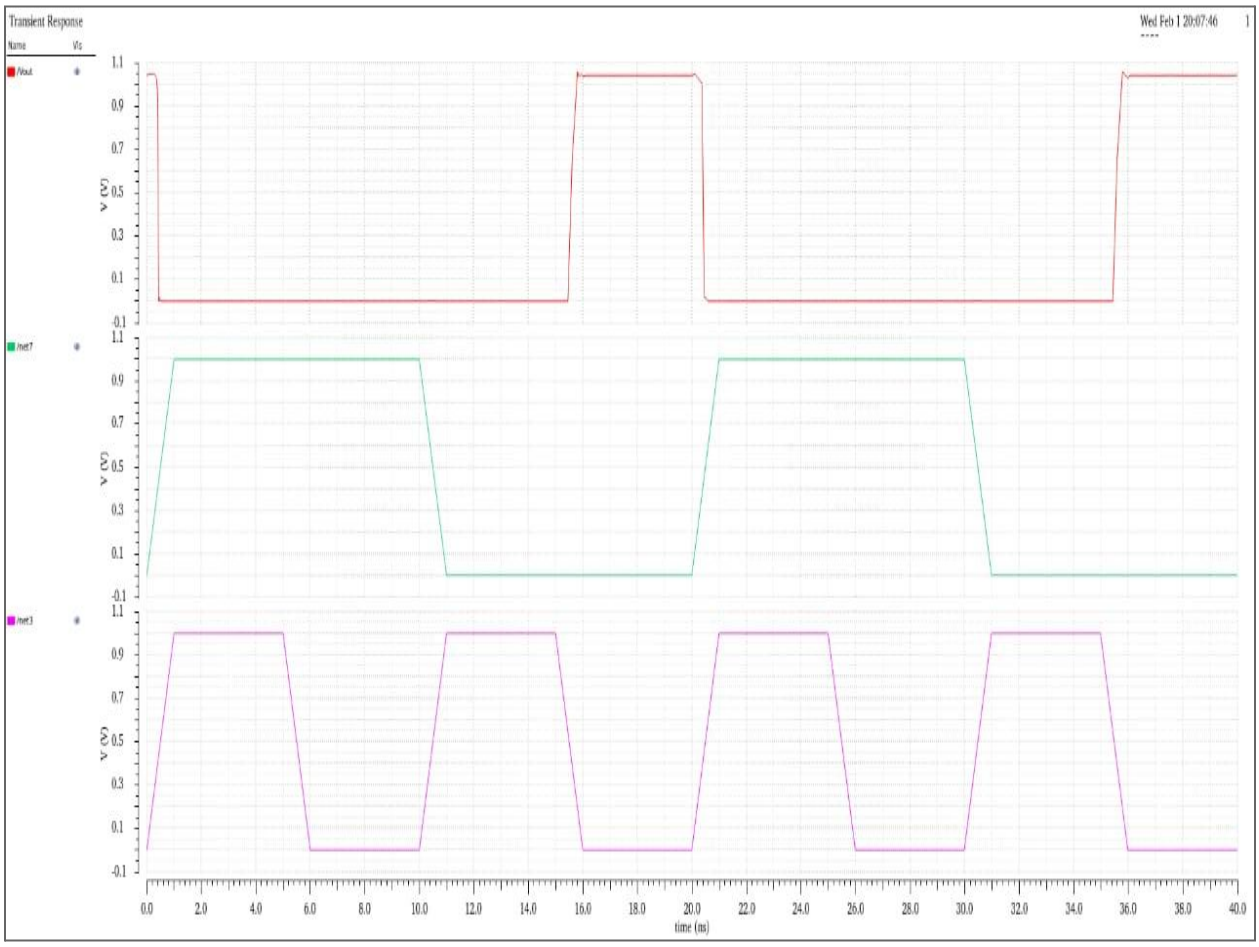
Schematic (In cadence):-

Schematic of NOR-



Results:-

Graph:-


Transient Response
Wed Feb 1 20:07:46
Name
Vout
net7
net3
v (V)
time (ns)
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
22.0
24.0
26.0
28.0
30.0
32.0
34.0
36.0
38.0
40.0

Title:- NAND logic using FinFet.

Discussion:-

NAND is an abbreviation for “NOT AND.” A two-input NAND gate is a digital combination logic circuit that performs the logical inverse of an AND gate.

While an AND gate outputs a logical “1” only if both inputs are logical “1,” a NAND gate outputs a logical “0” for this same combination of inputs. The symbol and truth table for a NAND gate is shown in Figure 1. The Boolean expression for a NAND gate with two inputs (A, B) and output X is:

$$X = \overline{A.B}$$

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

NAND gates help detect if a single input to a digital system has gone low. For example, a simple security system consisting only of NAND gates could be used to monitor the status of sensors connected to windows

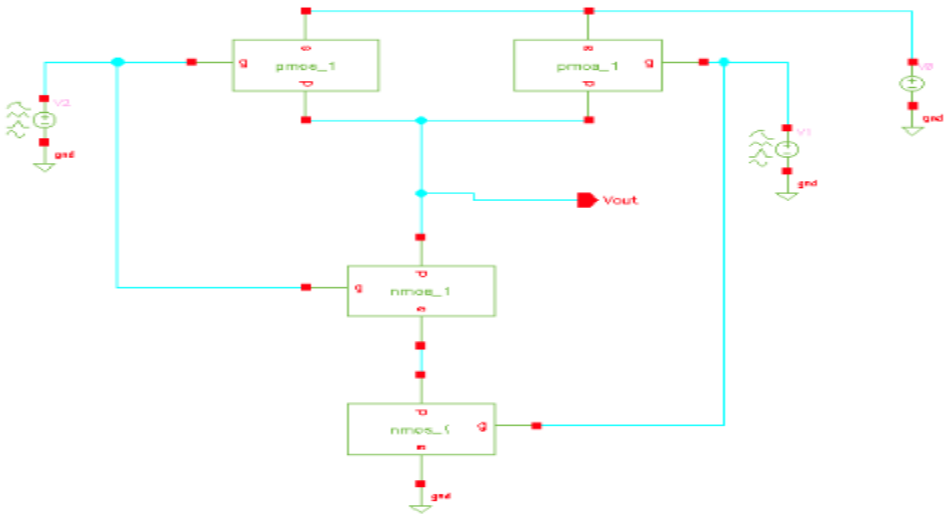
and/or doors. If a window/door is closed, the sensor sends a logical “1” signal to the security system. While all windows and doors are closed, the alarm output is “0.” If a single window or door is opened, the security system output changes state to become “1” and this can be used to trigger an alarm or take some other action.

We use Verilog-A code and cadence virtuoso to simulate our software.

- First, we open our cadence virtuoso using the Linux terminal and create a new cell.
- Now we get FinFET PMOS and NMOS components, ground, and voltage.
- Then we make a circuit using wire and define our voltage sources.
- Now we make input and output labels and save the schematic.
- Then we run our schematic and analyze the output.

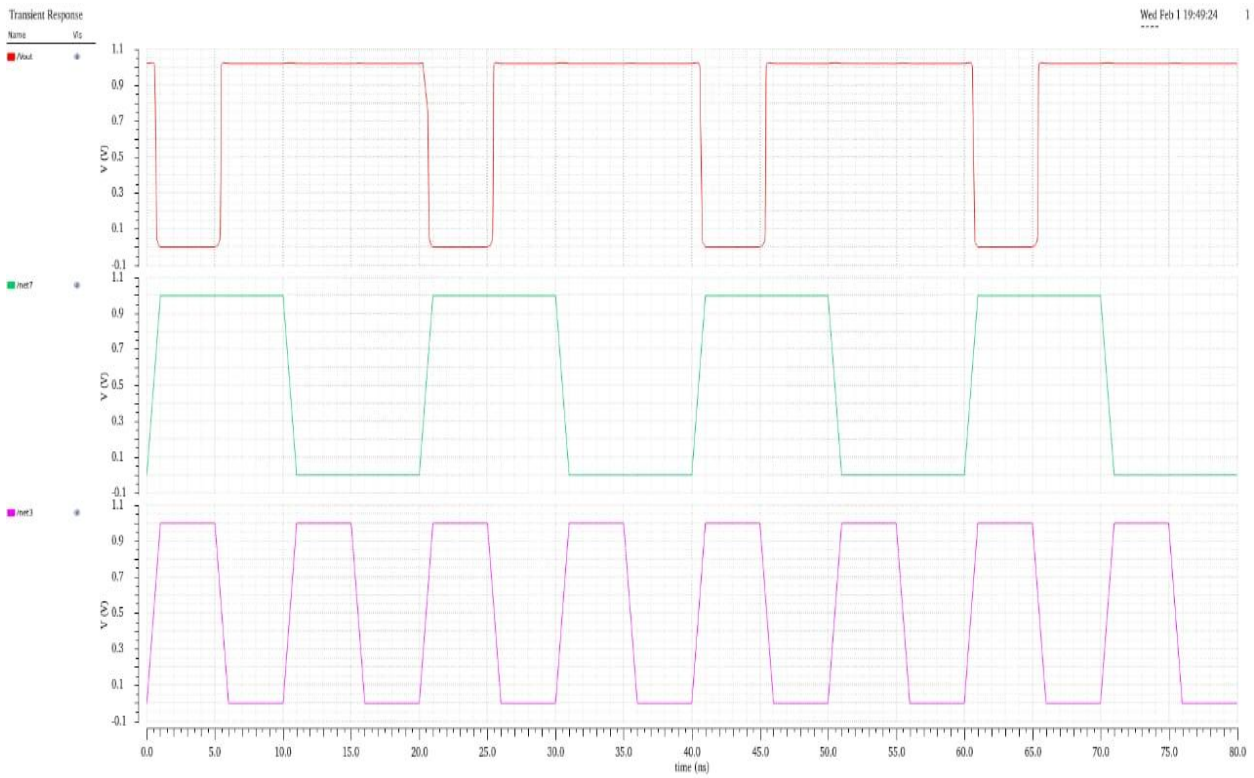
Schematic (In cadence):-

Schematic of NAND gate:-



Results:-

Graph:-



5 Summary

Future Holds for FinFET Usage

FinFET will not be useful beyond 5nm, as it will not have enough electrostatic control, requiring new architectures for the transistors. However, as technology nodes advance, some companies may decide, for economic reasons, to stay with the same node for longer. Other companies, due to the nature of their processes, will be forced to adopt new technologies.

A Review of FinFETs

The innovations in CMOS technology has been obtained through continuous downscaling for higher density, better performance, and low power consumption, leading to detrimental short-channel effects. Short-channel control is central since it allows shorter channel lengths and lower operating voltages.

Planar MOSFETs encountered tough challenges in the nanometer space, so FinFETs emerged as their replacements. FinFETs block short-channel effects better than planar MOSFETs, enabling transistor scaling.

FinFET Advantages

- Better control over the channel
- Suppressed short-channel effects
- Lower static leakage current
- Faster switching speed
- Higher drain current (More drive-current per footprint)
- Lower switching voltage
- Low power consumption

FinFET Disadvantages

- Difficult to control dynamic Vth
- Quantized device-width. It is impossible to make fractions of the fins, whereby designers can only specify the devices' dimensions in multiples of whole fins.
- Higher parasitics due to 3-D profile
- Very high capacitances
- Corner effect: electric field at the corner is always amplified compared to the electric field at the sidewall. This can be minimized using a nitrate layer in corners.
- High fabrication cost

6 Reference

- https://en.wikipedia.org/wiki/Fin_field-effect_transistor
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