A Continuous, Analytic Drain-Current Model for DG MOSFETs

Yuan Taur, *Fellow, IEEE*, Xiaoping Liang, *Student Member, IEEE*, Wei Wang, *Student Member, IEEE*, and Huaxin Lu, *Student Member, IEEE*

***Abstract*—This letter presents a continuous analytic current–voltage (*I–V*) model for double-gate (DG) MOSFETs. It is derived from closed-form solutions of Poisson's equation, and current continuity equation without the charge-sheet approximation. The entire $I_{ds}(V_g, V_{ds})$ characteristics for all regions of MOSFET operation: linear, saturation, and subthreshold, are covered under one continuous function, making it ideally suited for compact modeling. By preserving the proper physics, this model readily depicts "volume inversion" in symmetric DG MOSFETs—a distinctively noncharge-sheet phenomenon that cannot be reproduced by standard charge-sheet based *I–V* models. It is shown that the *I–V* curves generated by the analytic model are in complete agreement with two-dimensional numerical simulation results for all ranges of gate and drain voltages.**

***Index Terms*—Modeling, MOSFETs, transistors.**

ANALYTIC current–voltage (*I–V*) models are indispensable in compact modeling and for comprehension of the fundamentals of MOSFET characteristics, for example, in different regions of bias operation. In a bulk MOSFET, the starting point is the Pao–Sah integral based on Poisson and current continuity equations with gradual channel approximation [1]. While the Pao–Sah integral uses the channel quasi-Fermi potential and contains both the drift and diffusion current components hence is valid under all regions of MOSFET operation (subthreshold, linear, saturation), its mathematical form renders no general analytic solution. This would necessitate the charge sheet approximation [2] which would lead to further simplification into separate current expressions for different bias regions. The final piecewise current solutions, while physical, would cause severe numerical problems like convergence in compact modeling applications.

As CMOS scaling is approaching the limit imposed by gate oxide tunneling, double-gate (DG) MOSFET is becoming an intense subject of very large-scale integration (VLSI) research because in theory it can be scaled to the shortest channel length possible for a given gate oxide thickness [3]. In this letter, a continuous, analytic *I–V* model is derived for DG MOSFETs directly from the Pao–Sah integral without the charge sheet approximation. It is shown that this analytic solution covers all three regions of MOSFET operations: linear, saturation, and subthreshold, thus maintaining strong continuity between different regions, and yet is completely physics based without the need for ad-hoc fitting parameters. The model has been validated by two–dimensional (2-D) numerical simulations.

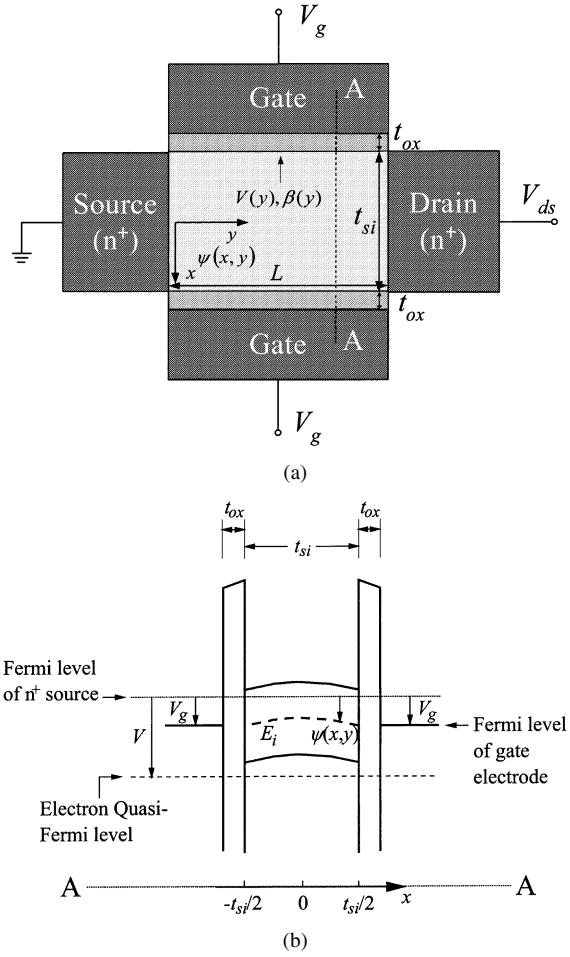

Fig. 1. (a) Schematic diagram of a DG MOSFET. $V(y)$ is the quasi-Fermi potential at a point in the channel. β is a function of V. (b) Band diagram along a vertical cut (AA) in (a). The potential $\psi(x, y)$ is defined as the intrinsic Si (midgap) level referenced to the Fermi level of the n^+ source as shown (so that $n = n_i$ where $\psi = 0$).

Consider an undoped (or lightly doped), symmetric DG MOSFET shown schematically in Fig. 1(a). Following Pao–Sah's gradual channel approach [1], Poisson's equation along a vertical cut perpendicular to the Si film [Fig. 1(b)] takes the following form with only the mobile charge (electrons) term:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{\rm si}} n_i e^{\frac{q(\psi - V)}{kT}} \tag{1}$$

Manuscript received October 17, 2003. This work was supported in part by the SRC Customization Project under Grant 2002-NJ-1001.002, co-sponsored by IBM and AMD. The review of this letter was arranged by Editor A. Wang.

The authors are with the Department of Electrical and Computer Engineering, University of California-San Diego, La Jolla, CA 92093 USA.

Digital Object Identifier 10.1109/LED.2003.822661

where q is the electronic charge, $\varepsilon_{\rm si}$ is the permittivity of silicon, n_i is the intrinsic carrier density, $\psi(x)$ is the electrostatic potential [reference shown in Fig. 1(b)] and V is the electron quasi-Fermi potential. Here we consider an nMOSFET with $q\psi/kT \gg 1$ so that the hole density is negligible.

Since the current flows predominantly from the source to the drain along the y-direction, the gradient of the electron quasi-Fermi potential is also in the y-direction. This justifies the gradual channel approximation that V is constant in the x-direction. Equation (1) can then be integrated twice to yield the solution [4]

$$\psi(x) = V - \frac{2kT}{q}\ln\left[\frac{t_{\rm si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{\rm si}kT}}\cos\left(\frac{2\beta x}{t_{\rm si}}\right)\right] \quad (2)$$

where β is a constant (of x) to be determined from the boundary condition

$$\varepsilon_{\rm ox}\frac{V_g - \Delta\phi - \psi\left(x = \pm\frac{t_{\rm si}}{2}\right)}{t_{\rm ox}} = \pm\varepsilon_{\rm si}\frac{d\psi}{dx}\Big|_{x=\pm\frac{t_{\rm si}}{2}}. \quad (3)$$

Here $\varepsilon_{\rm ox}$ is the permittivity of oxide, V_g is the voltage applied to both gates, $t_{\rm si}$ and $t_{\rm ox}$ are the silicon and oxide thicknesses, and $\Delta\phi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon. In other words, $\Delta\phi = 0$ for midgap work function gate, $-E_g/2q$ for $\rm n^+$ poly, and $+E_g/2q$ for $\rm p^+$ poly, etc. Substituting (2) into (3) leads to

$$\frac{q(V_g - \Delta\phi - V)}{2kT} - \ln\left[\frac{2}{t_{\rm si}}\sqrt{\frac{2\varepsilon_{\rm si}kT}{q^2 n_i}}\right] = \ln\beta - \ln[\cos\beta] + \frac{2\varepsilon_{\rm si}t_{\rm ox}}{\varepsilon_{\rm ox}t_{\rm si}}\beta\tan\beta. \quad (4)$$

For a given V_g, β can be solved from (4) as a function of V. Along the channel direction (y), V varies from the source to the drain. So does β. The functional dependence of $V(y)$ and $\beta(y)$ is determined by the current continuity condition which requires the current $I_{ds} = \mu W Q_i dV/dy = \text{constant}$, independent of V or y. Here μ is the effective mobility, W is the device width, and Q_i is the total mobile charge per unit gate area. Integrating $I_{ds}dy$ from the source to the drain and expressing dV/dy as $(dV/d\beta)(d\beta/dy)$, Pao–Sah's integral [1] can be written as

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_i(\beta)\frac{dV}{d\beta}d\beta \quad (5)$$

where β_s, β_d are solutions to (4) corresponding to $V = 0$ and $V = V_{ds}$ respectively. From Gauss's law, $Q_i = 2\varepsilon_{\rm si}(d\psi/dx)_{x=tsi/2}$ [5], which equals $2\varepsilon_{\rm si}(2kT/q)(2\beta/t_{\rm si})\tan\beta$ using (2). $dV/d\beta$ can also be expressed as a function of β by differentiating (4). Substitute these factors in (5) and carry out the integration analytically

$$I_{ds} = \mu\frac{W}{L}\frac{4\varepsilon_{\rm si}}{t_{\rm si}}\left(\frac{2kT}{q}\right)^2 \times \int_{\beta_d}^{\beta_s}\left[\tan\beta + \beta\tan^2\beta + \frac{2\varepsilon_{\rm si}t_{\rm ox}}{\varepsilon_{\rm ox}t_{\rm si}}\beta\tan\beta\frac{d}{d\beta}(\beta\tan\beta)\right]d\beta$$

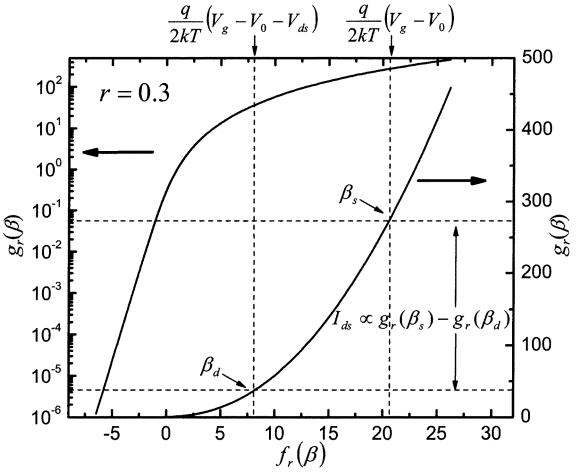

Fig. 2. Plot of g_r versus f_r with β as a hidden parameter. The same curve is plotted on both logarithmic (left) and linear (right) scales. f_r spans the entire $(-\infty, \infty)$ range as β varies from 0 to $\pi/2$. The algorithm of calculating the drain current for given V_g, V_{ds} is illustrated graphically using the linear curve.

$$= \mu\frac{W}{L}\frac{4\varepsilon_{\rm si}}{t_{\rm si}}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{\rm si}t_{\rm ox}}{\varepsilon_{\rm ox}t_{\rm si}}\beta^2\tan^2\beta\right]\Big|_{\beta_d}^{\beta_s}. \quad (6)$$

The procedure for drain current calculation is summarized as follows. The righthand side of (4) and (6) can be represented by two functions

$$f_r(\beta) = \ln\beta - \ln[\cos\beta] + 2r\beta\tan\beta \quad (7)$$

$$g_r(\beta) = \beta\tan\beta - \frac{\beta^2}{2} + r\beta^2\tan^2\beta \quad (8)$$

where $r = \varepsilon_{\rm si}t_{\rm ox}/\varepsilon_{\rm ox}t_{\rm si}$ is a structural parameter. The range of β is $0 < \beta < \pi/2$. For given V_g and V_{ds}, β_s and β_d are found from the conditions $f_r(\beta_s) = (q/2kT)(V_g - V_0)$ and $f_r(\beta_d) = (q/2kT)(V_g - V_0 - V_{ds})$, where

$$V_0 \equiv \Delta\phi + \frac{2kT}{q}\ln\left[\frac{2}{t_{\rm si}}\sqrt{\frac{2\varepsilon_{\rm si}kT}{q^2 n_i}}\right]. \quad (9)$$

Then $I_{ds} \propto [g_r(\beta_s) - g_r(\beta_d)]$ can be easily computed. Graphically, one can plot g_r versus f_r with β as an intermediary parameter and proceed as shown in Fig. 2.

MOSFET characteristics for all regions: linear, saturation, and subthreshold, can be generated from this continuous, analytic solution. For example, in the linear region above threshold, both $f_r(\beta_s), f_r(\beta_d) \gg 1$, so $\beta_s, \beta_d \sim \pi/2$. f_r and g_r are dominated by the last terms of (7) and (8), therefore

$$I_{ds} = \mu C_{\rm ox}\frac{W}{L}\left[(V_g - V_t)^2 - (V_g - V_t - V_{ds})^2\right] = 2\mu C_{\rm ox}\frac{W}{L}\left(V_g - V_t - \frac{V_{ds}}{2}\right)V_{ds}. \quad (10)$$

Here $V_t = V_0 + \delta$ where $\delta = (2kT/q)\ln[q(V_g - V_0)/4rkT]$ is a second-order effect (~ 0.05 V) [4] coming from the $\ln(\cos\beta)$ term in (7). Note that the factor of r in δ cancels the $t_{\rm si}$ factor in V_0 so that V_t is independent of $t_{\rm si}$.

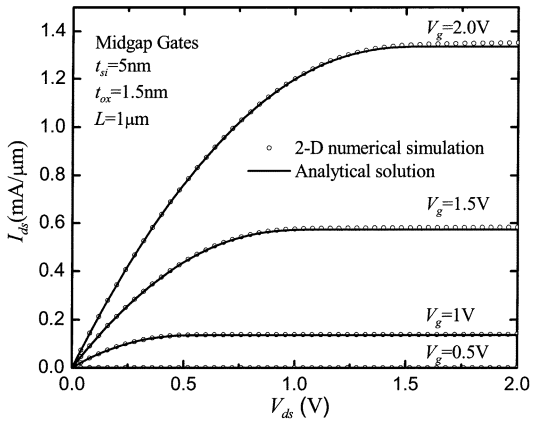

Fig. 3. I_{ds}–V_{ds} curves calculated from the analytic model (solid curves), compared with the 2-D numerical simulation results (open circles). A constant mobility of 300 $\mathrm{cm}^2/\mathrm{V\text{-}s}$ is used in both calculations.

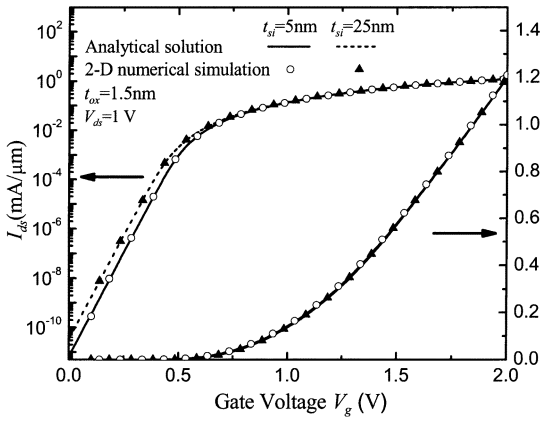

Fig. 4. I_{ds}–V_g characteristics obtained from the analytic model for two different values of t_{si} (solid and dashed curves), compared with the 2-D numerical simulation results (symbols). The same currents are plotted on both logarithmic (left) and linear (right) scales.

In the saturation region, where $\beta_s \sim \pi/2$, but $f_r(\beta_d) \ll -1$ so $\beta_d \ll 1$, one obtains

$$I_{ds} = \mu C_{\mathrm{ox}} \frac{W}{L} \left[(V_g - V_t)^2 - \frac{8rk^2T^2}{q^2} e^{\frac{q(V_g - V_0 - V_{ds})}{kT}} \right]. \quad (11)$$

Note that in this continuous model, the current approaches the saturation value with a difference term exponentially decreasing with V_{ds}, in contrast to common piecewise models in which the current is made to be constant in saturation.

In the subthreshold region, both β_s, $\beta_d \ll 1$, so $f_r \sim \ln\beta$, $g_r \sim \beta^2/2$, and

$$I_{ds} = \mu \frac{W}{L} kTn_i t_{\mathrm{si}} e^{\frac{q(V_g - \Delta\phi)}{kT}} \left(1 - e^{-\frac{qV_{ds}}{kT}}\right) \quad (12)$$

as would be expected from the basic diffusion current, $J_{\mathrm{diff}} = qDdn/dx$ [5]. Note that the subthreshold current is proportional to the silicon thickness, but independent of t_{ox}—a manifestation of "volume inversion" [4] that cannot be reproduced by standard charge sheet-based *I–V* models. In contrast, the above threshold currents, (10) and (11), are proportional to C_{ox}, but independent of silicon thickness. These observations show that all the essential physics are preserved in this continuous, analytic model.

Figs. 3 and 4 show that the analytic I_{ds}–V_{ds} and I_{ds}–V_g curves computed from this model are in complete agreement with 2-D numerical simulations of a long-channel DG MOSFET. No fitting parameters are needed. "Volume inversion," in which the subthreshold current is proportional to t_{si}, is self evident in Fig. 4.

Analytic solutions for asymmetric DG MOSFETs can be obtained in a similar fashion as in the symmetric case, although more tediously. Due to the mismatch of the gate work functions, there are two boundary conditions [6] and therefore two parameters: β_1, β_2, which satisfy a relationship $h(\beta_1, \beta_2) = 0$ in the $\beta_1 - \beta_2$ plane. The I_{ds}–V_{ds} and I_{ds}–V_g curves generated from the analytic model for asymmetric DG MOSFETs are also in complete agreement with 2-D numerical simulations.

In conclusion, a continuous *I–V* model is derived from analytic solutions of Poisson's and current continuity eqs. for long-channel DG MOSFETs. No charge sheet approximation is invoked—a key to the proper depiction of "volume inversion" in subthreshold. It is shown that the *I–V* curves constructed by the analytic model are in complete agreement with 2-D numerical simulation results without fitting terms or parameters. All regions of MOSFET operation, including the linear, saturation, and subthreshold regions, are covered by a pair of continuous functions that can be easily calculated. This avoids the pitfalls of the piecewise models, thus making this model ideally suited for compact model applications.[1]

ACKNOWLEDGMENT

The authors would like to thank M. Chan and J. He for helpful discussions.

REFERENCES

[1] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)—semiconductor transistors," *Solid-State Electron.*, vol. 9, p. 927, 1966.
[2] J. R. Brews, "A charge sheet model of the MOSFET," *Solid-State Electron.*, vol. 21, p. 345, 1978.
[3] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, pp. 259–288, Mar. 2001.
[4] Y. Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Lett.*, vol. 21, pp. 245–247, May 2000.
[5] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[6] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, p. 2861, Dec. 2001.

[1]For a complete compact model, this long-channel core would need to be augmented with additional physical effects, for example, short-channel effect, quantum mechanical effect, low and high field transport, etc.