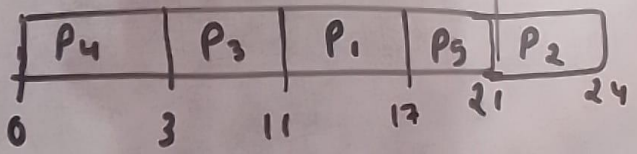
➢ OPERATING SYSTEM NOTES

PROCESS MANAGEMENT

F.C.F.S

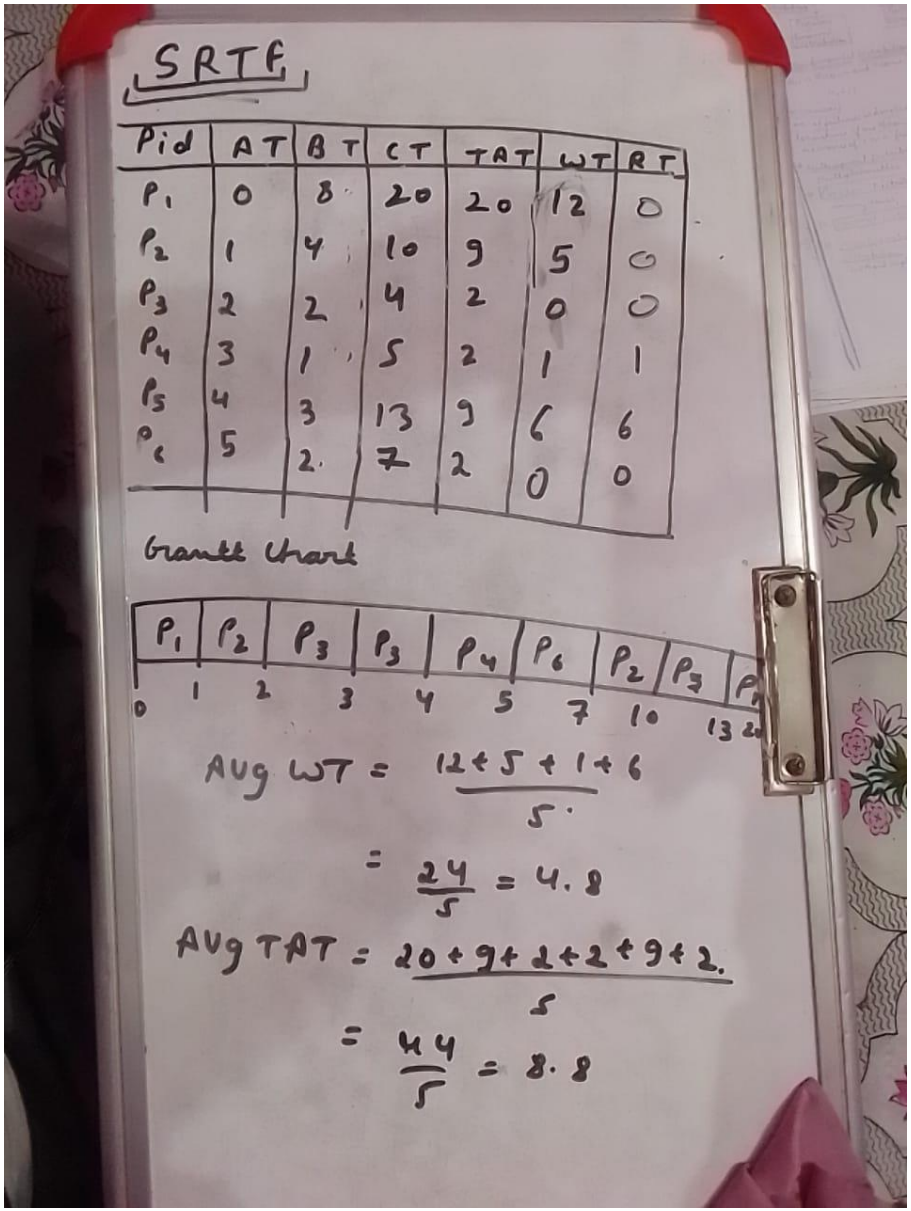
FCFS

Process	AT	BT	C.T	TAT	WT
P_1	2	6	17	15	9
P_2	5	3	24	19	16
P_3	1	8	11	10	2
P_4	0	3	3	3	0
P_5	4	4	21	17	13
					40



$$\text{avg wt} = \frac{40}{5} = 8$$

$$\text{avg TAT} = \frac{64}{5} = 12.8$$


SRTF
Pid AT BT CT TAT WT RT
P1 0 8 20 20 12 0
P2 1 4 10 9 5 0
P3 2 2 4 2 0 0
P4 3 1 5 2 1 1
P5 4 3 13 9 6 6
P6 5 2 7 2 0 0
Gantt Chart
P1 P2 P3 P3 P4 P6 P2 P3
0 1 2 3 4 5 7 10 13
Avg WT = 12+5+1+6 / 5
= 24/5 = 4.8
Avg TAT = 20+9+2+2+9+2 / 5
= 44/5 = 8.8

Round Robin

Pid	AT	BT	CT	TAT	WT	RT
P_1	0	5	13	13	8	0
P_2	1	3	12	11	8	1
P_3	2	1	5	3	2	1
P_4	3	2	9	6	4	4
P_5	4	3	14	10	7	5

Criteria : "Time Quantum"
Mode : "Preemptive".

(Ready queue) —ST→ (Running state) —MT→ (Terminate)
(Running state) → (Ready queue)

$Q = 2$

Ready Queue:

~~P1~~ ~~P2~~ ~~P3~~ ~~P1~~ ~~P4~~ ~~P5~~ ~~P2~~ P1 P5

Running Queue / Gantt chart

P_1	P_2	P_3	P_1	P_4	P_5	P_2	P_1	P_5

0 2 4 5 7 9 11 12 13 14

$$\text{Avg TAT} = \frac{13+11+3+6+10}{5} = \frac{43}{5} = 8.6 \text{ sec}$$

$$\text{Avg WT} = \frac{8+8+2+4+7}{5} = \frac{29}{5} = 5.8 \text{ sec}$$

O.S

P40

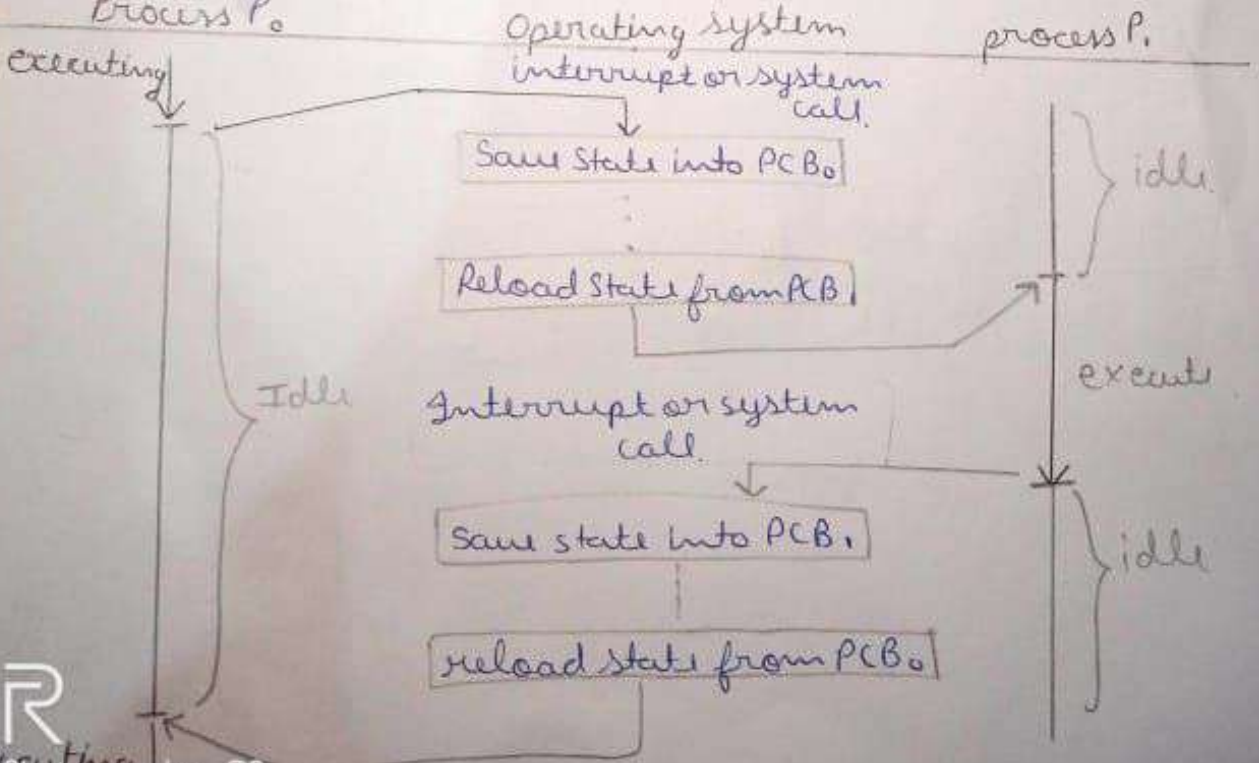
Q1

1 a) PCB - Process Control Block

Structure

Process ID
Program Counter
Process State
Priority
GPR (General Purpose Registers)
List of open files
List of open devices

Flowchart to show how PCB switch from process to process



Difference between

Symmetric multiprocessing	asymmetric multiprocessing
1) All processors are treated equally and have equal access to the system.	1) Processors are not treated equally. One processor is Master and the other is slave.
2) Task or processes can be dynamically assigned to any available processor in the system.	Task or processes Master processor typically handles system management such as scheduling, resource allocation and I/O operations while slave processor execute application specific task.
3) Highly scalable as adding more processors generally lead to improved system performance and through put.	limited scalability as the performance improvement achieved by adding more processors depends on the workload and efficiency of task distribution.
4) SMP's are generally more complex in terms of hardware design, system architecture and soft ware development.	Simpler in design and implementation compared to SMP systems

are stored in a structured format (e.g. JSON, XML)

Q3b)

Scheduler	Dispatcher
1. Scheduler is responsible for selecting the next process to run on the CPU.	1. Dispatcher is responsible for actually switching the CPU from one process to another.
2. Level of Operation Operates at higher level and makes decisions about process management	2. Level of Operation. Operates at lower level and is involved in actual switching of execution from process to process.
3. Frequency of Operations Operates less frequently.	Frequency of Operations Operates more frequently.
4. Responsibility. focuses on long term and medium term. scheduling	4. Focuses on short term scheduling.
5. Visibility Its actions are visible to users in form of process execution.	Its actions are not visible to users as it does underlying context switching.

2.

b) Handheld devices usually have virtual memory system because of. this feature is essential for handheld. run more applications and due to its handyness it don't has much memory.

→ Real Time Operating System (RTOS) uses Batch programming. not virtual memory because this can create latency.

a)

Process	Arrival Time	Execution Time	Priority
P1	0	12	5 (highest)
P2	2	25	1
P3	3	3	3
P4	5	9	4