B.Tech. *Computer Engineering*-SEMESTER III

Course Code	Type	Subject	L	T	P	Credits	CA	MS	ES	CA	ES	Pre-requisites
COCSC07	CC	Computer Architecture and Organization	3	1	0	4	25	25	50	-	-	COCSC02

COURSE OUTCOMES

1. To understand the architecture of modern processors and organization of its components, and relationship between hardware and software in digital machines.
2. To design instructions and corresponding logic circuits for a simple CPU with its essential components such as ALU, a register file, memory and input-output.
3. To understand the organization of computer systems
4. To understand the computation standards and using them in writing algorithms
5. To appreciate the evolving technology that governs the evolution of modern computers and continue to keep abreast of state-of-art in computing technology

COURSE CONTENT

UNIT-1

Overview of computer organization: Characteristics of a general purpose computer, The stored program concept, von Neumann architecture, Harvard architecture, Programmer's model - the Instruction set architecture (ISA), ISA design and performance criteria, Basic computer organization with CPU, memory and IO subsystems, Interconnect busses, Evolution of CISC and RISC based processors and their merging.

UNIT-2

Instruction Set Architectures: Machine instruction, Machine cycle and Instruction cycles, Instruction Set: memory and non-memory reference instructions, instruction categories: data movement, data manipulation, program control and machine control instructions, CISC types addressing modes and instruction formats, RISC type addressing modes and instruction formats.

UNIT-3

Central Processing Unit: Specification of a simple CPU using RTL, Design of the data path

for the simple CPU, Designing the hardwired control path for the simple CPU, Performance analysis of the simple CPU, Enhancement of the ISA for the simple CPU and design

extensions, Characteristics of RISC CPU design: ISA characteristics, pipelining, data and instruction caches, Practical case studies in CISC type and RISC type CPU designs.

UNIT-4

Microprogrammed Control Unit: Control memory system, Microinstruction-sequencing, conditional branch, mapping and subroutines, direct, horizontal and vertical microcoding, micro-instruction format and symbolic representation, design of micro-control unit for a simple CPU, applications of microprogramming

Memory organization: Memory hierarchy, Cache organization: Direct, associative and Set associative cache, Auxiliary memory organization, RAID organizations

Input output organization: IO interfacing, Asynchronous data transfer, Programmed IO, Interrupt driven IO, Priority schemes, Direct Memory Access, Serial communication techniques

UNIT-5

Computer arithmetic: Design of Binary addition and subtraction units, Algorithms for multiplication and division and their implementation, Floating point arithmetic, etc.

Pipelined architecture: Basic concepts of pipelining, Speedup and throughput, Minimum Average Latency, Instruction pipeline.

GPU architecture: Hardware Basics, Execution Model, GPU instruction set architecture, NVIDIA GPU instruction set architecture

Guidelines for Project work:

- Exercises using assembly-level programming and debugging to illustrate the working of instructions in the ISA of a CISC based /RISC based processor. These exercises should illustrate the status of various registers, flags, counters and pointers after data movement, data manipulation, program control, and stack operations.
- Semester-long group project on the design and simulation /hardware emulation ofa simple processor.