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Low Power VLSI Design

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PROJECT REPORT:

Design of Low Power TSPC CMOS D Flipflop

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Design of Low Power TSPC CMOS D Flipflop using Supply Voltage Level (SVL) Methods:

I. **Introduction:** This Project details about the design of D Flip Flop**.** This D Flip Flop circuit is analyzed by using the supply voltage level methods. These methods are used mainly to suppress the power consumption caused due to leakage currents. In addition, because of this implemented technique, the time taken for battery backup, and the supply voltage given at standby mode gets minimized. The projected circuit uses a smaller number of transistors, such that power consumption and leakage currents are in prior limit. CMOS D flip flops are first preference to implement different type of binary counters, shift registers and analog and digital circuit system. In CMOS technology leakage power is primary significance. To reduce power dissipation and to develop the time of battery backup, the supply voltage to the given circuit during standby mode should be reduced.

Also the proposed design uses less number of clocked transistors, thus reduces the dynamic power consumption as well as leakage current to accessible design. Each accessible design and proposed design is replicated utilizing Cadence device at at 180nm technology.

In this Report the performance comparision among different TSPC D Flip-flops with respect to transistor Density, Power and Energy is done for the following TSPC D Flip-flops.

a. Design of 5T-TSPC CMOS D Flip-flop:

Achieving high performance in any Very Large Scale Integration (VLSI) systems is the most important part and the demand had increased with the growth of the semiconductor technology. As technology advances, a Systems-On-a-Chip (SOC) design contains more number of components that lead to a higher transistor density and increased power consumption . As well as it needs a faster clock for its operation, that consumes more power. To improve the frequency of operation and integration of components of the Very Large Scale Integration (VLSI) Integrated Circuits (ICs) has been increased with the advance of Complementary Metal Oxide Semiconductor (CMOS) technology. The distribution of the global clock input and the inverse of it results in the clock skew problems in relation to each other, and also this consumes more power. Thus to overcome this problem Single Phase Clocking is very advantageous . The True Single Phase Clock (TSPC) is a broad dynamic flip-flop that operates at high speed and with low power consumption. It uses one phase clock for synchronization. Many researches has shown TSPC method has small area, no clock skew problem and even higher clock frequencies can be achieved thereby improving the performance of the digital systems. It is used in various applications like digital VLSI clocking system, microprocessors, buffers, wireless communication systems etc

Implementation:

Fig.1 and Table1 shows Circuit and Truth table of positive edge triggered 5 transistors TSPC D Flip-flop respectively. 5T TSPC D Flip-flop is constructed using 3 NMOS and 2 PMOS transistors. This flip-flop uses single clock phase signal for synchronization. It consumes less area since it uses only 5 transistors, which signify low transistor count and it also consumes less power. Thus the performance of this design is improved.

The working principle of this flip-flop is as follows: When clock and input signal is HIGH i.e. clk=1, D input=1 then the NMOS transistors m2 and m3 is ON while PMOS transistor m1 is OFF this in turn turns ON PMOS transistor m4 and turns OFF NMOS transistor m5 thus pulling the output to HIGH i.e. Q=1. Similarly when clk=1 and D input=0 then m1 and m2 transistors are ON while m3 is OFF this turns ON m5 producing the output LOW. That is during ON period of clock signal whatever the value of the input is, the output follows the input. On the other hand when clk=0, the output follows the previous value of the output.

Actually TSPC stands for true single phase clocked logic design uses one aspect of clock Pulse and avoid skew Problems while designing and performs well in digital structure. Because of this reason low power consumption is observed.

Fig1. Schematic of 5T TSPC DFlipFlop:

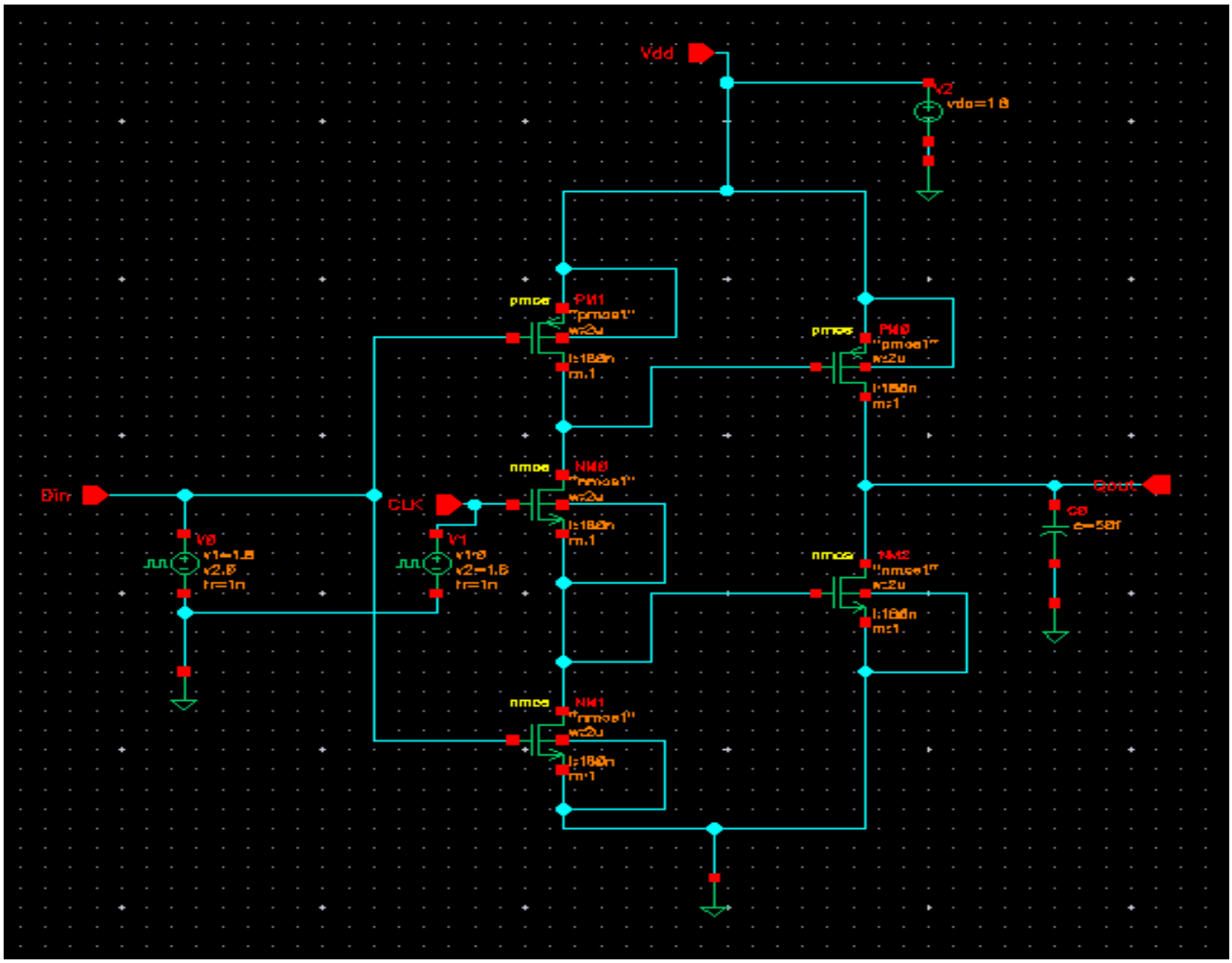

TABLE I

TRUTH TABLE OF 5T TSPC D FLIP-FLOP

Clk	D	M1	M2	M3	M4	M5	Q
1	0	ON	ON	OFF	OFF	ON	0
1	1	OFF	ON	ON	ON	OFF	1
0	0	ON	OFF	OFF	OFF	ON	0
0	1	OFF	OFF	ON	OFF	ON	0

b. SVL Method Enforced on CMOS DFLIPFLOP:

SVL stands for Self-Voltage Level. This is utilized to minimize power dissipation for clocked structure as Flipflops at the time if it is working at standby mode.

when Clock=0, SVL method utilize PMOS and NMOS transistor in equivalent as pull up network or pull down system. Pull up transistors gate is connected with complement of clock signal and pull down transistors gate terminal is connected with clock .This technique to reduce leakagepower uses a clock signal as the control signal to control supply voltage to D flip flop.Hence the name self voltage level is justified. When clock = 1, clock bar=0 and Psw1 will become ON, Nsw1 will be in off state. Clocked circuit will be connected to Vdd.

When clock =0, the circuit is in standbymode and do not require more power supply to maintain in standby mode. Hence even if we reduce the supply voltage during standby mode it will work perfectly fine and powerconsumption will be reduced, especially the leakage power that flows when transistors are in off state will be reduced.

Case1: clock = 1(active mode)

Psw1 is ON, Nsw2 is ON,Psw2 is OFF ,Nsw1 is OFF. D flip flop is connected to Vdd and ground for normalcircuit operation.

If D_in=0, P1,N1,N3 are ON and P2,N2 are OFF, connecting Q to ground i.e Q = 0

If D_in=1, P1, N3 are in OFF state and N1,N2,P2 are in ON state , connecting Q to Vdd i.e Q = 1

Case2: clock = 0(standby mode)

Psw1, Nsw2 are in OFF state i.e open circuits. Nsw1is ON but as it is used as pull up it provides Vdd-Vth as the supply voltage for D flip flop. The drop is due to resistive nature of NMOS when used as pull up. Similarly, Psw2 is ONbut as it is used as pull down it provides finite positive voltageinstead of ground (0 volts).This virtual ground positive voltage slightly reverse biases the NMOS transistors of D flip flop and reduces leakage power in standby mode. D flip flop's PMOS transistors leakage power is reduced, since they are connected to virtual supply in standby mode.

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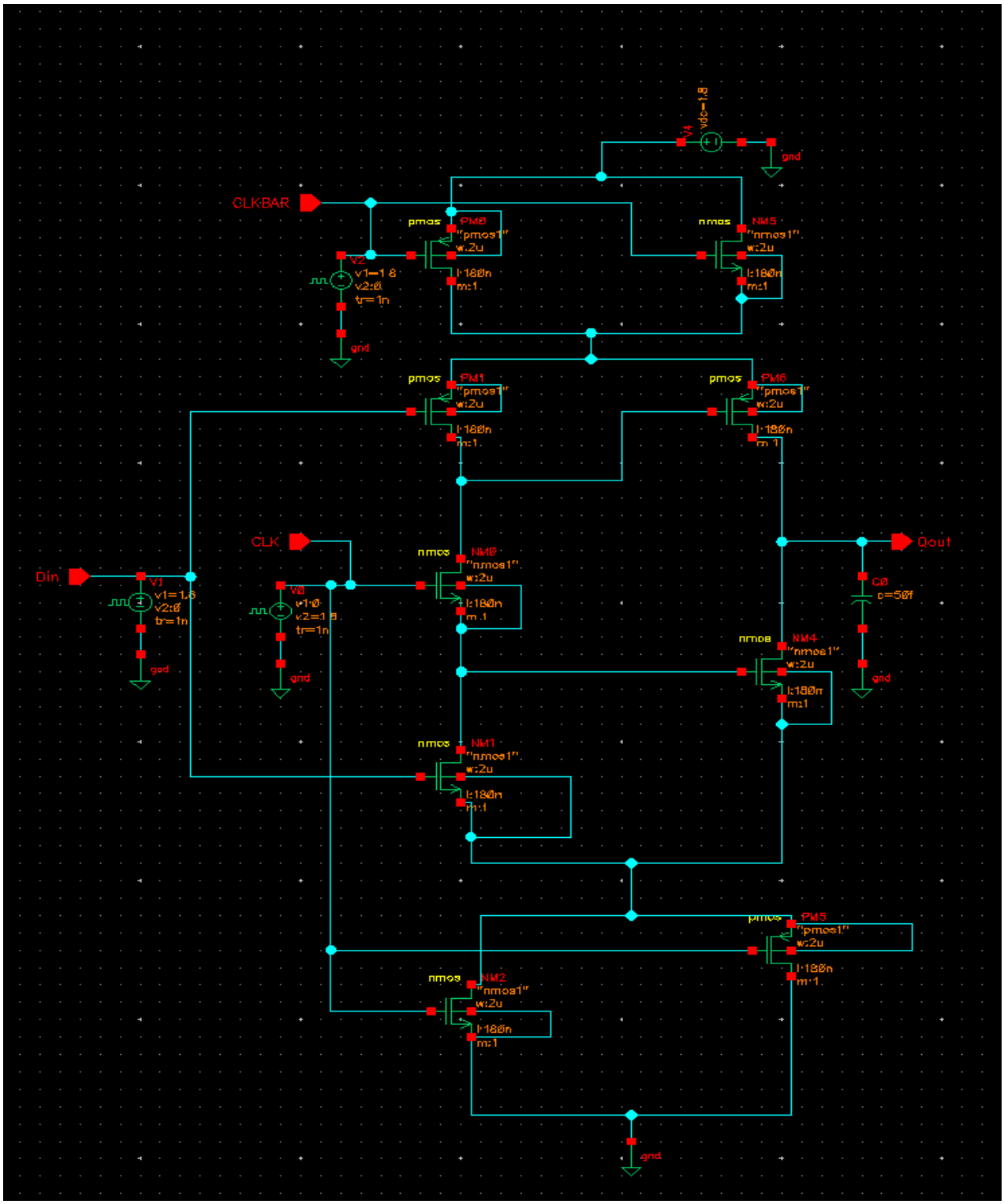
The virtual ground positive potentials will be moderately reverse biased the NMOS transistors of DFF such that minimizes Power dissipation of DFlipFlop in standby mode. And the PMOS transistors in DFlipflop, Power dissipation are optimized because the virtual supply is in standby mode. Figure 2 & 5 shows the schematic diagram and simulated outcomes of CMOS DFF utilizing supply voltage level methods.

Figure2: Schematic Implementation of CMOS D Flip Flop enforced using SVL method.



c. Modified SVL Technique applied on CMOS D-Flip Flop

The Figure 3 visualizes the D FlipFlop structure utilizing enhanced SVL method. The DFPFP is designed utilizing five transistors; those are two PMOS transistors(P1& P2) and three NMOS transistors (N1, N2 &N3).
This also contains two cases:

The first case is if the clock given is '1' which is in active mode:

P1 gets ON, N2 gets ON, and P2,P3 gets OFF and N1, N2 gets OFF. Then DFPFP gets joints to Vdd and ground for normal circuit operation.
And while Din is zero Pl, N1, N3 gets on and P2, N2 gets off, such that 'Q' connects to ground then a becomes Zero
And if Din is '1' ON then P1, N3 gets off and N1, N2 and P2 gets ON such that output Q joints to Vdd then Q becomes '1'

The second case is such that is clock given '0' which operates in standby mode:

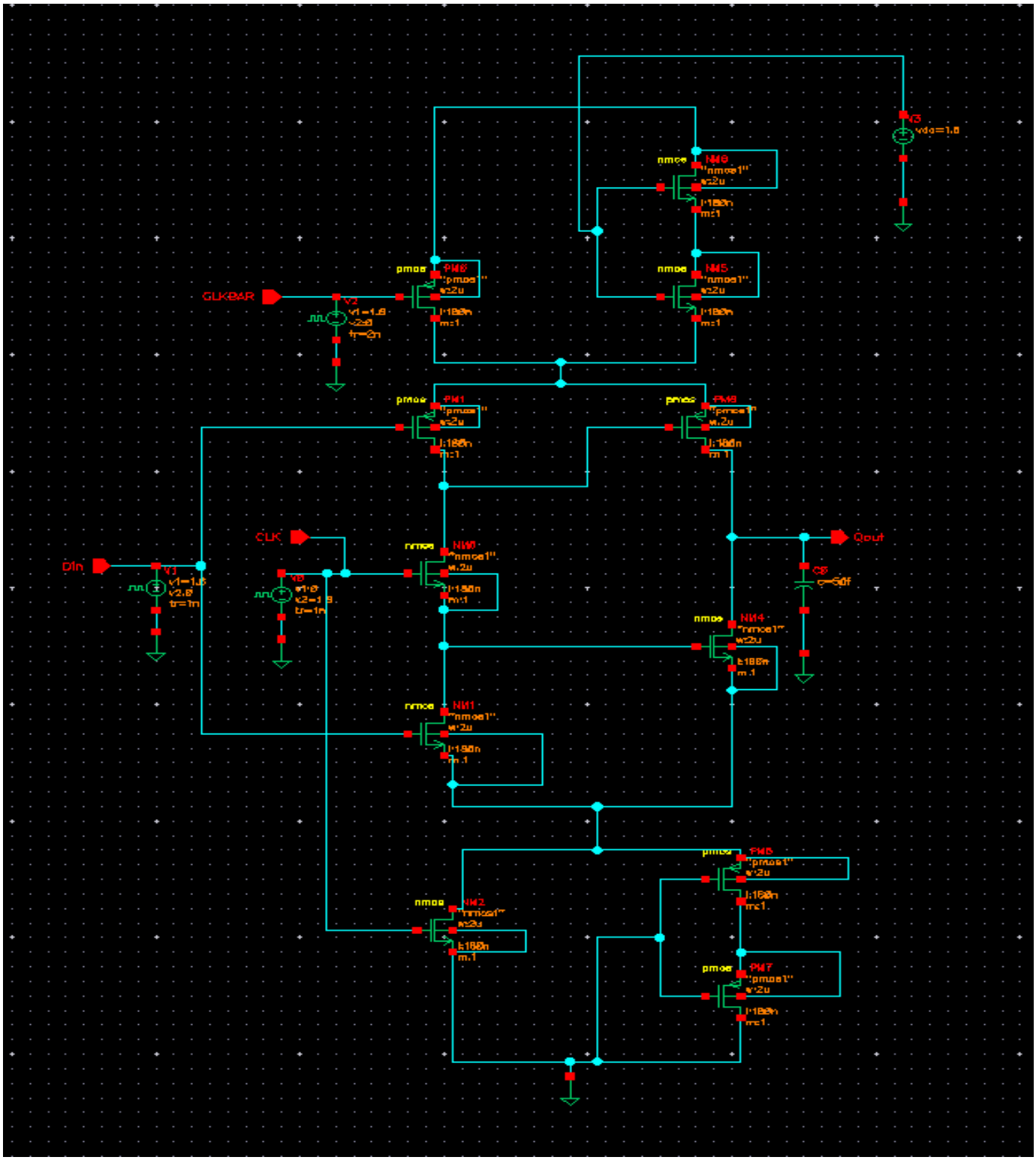
P1, N3 gets off operates open switch. NI, N2 gets ON because of transistors in pull up it shows VDD - Vth as supply potential to FlipFlop
At the time of extra two NMOS transistors internally related to threshold current gets shortened. In the same way P2, P3 gets ON which are in pull down gets limited positive Potential rather than ground which is at zero volts. If the virtual ground positive potential is moderately reverse bias to NMOS

transistors of DFF, such that optimizes power dissipation because of DFF, such that optimizes power dissipation because of DFF is in standby mode. The PMOS transistors of DFF leakage power gets optimized, because those are jointed to virtual supply which is in standby mode.

In enhanced SVL method, the power dissipation gets optimized in addition leakage current flow also gets minimized because of the connection of extra two transistors.

The basic is that supply potential for the flip-flop design is substantially optimized in static mode. The power dissipation at ideal condition is directly connected to supply potential and current, such that power dissipation is shortened for same value because of enhanced SVL method. Because of projected SVL technique the power dissipation gets optimized, in addition count of clocked transistors gets minimized. Hence working speed of design increases and also the dynamic power consumption gets optimized. So this method of DFF in standby mode is utilized to reduce power consumption.

Figure3: Schematic Implementation of CMOS D Flip Flop enforced using Modified SVL method.



SIMULATED OUTCOMES:

The simulated outcomes of CMOS DFF using Cadence Virtuoso tool using 180nm CMOS technology with supply potential of 1.8V. By using the projected techniques the power dissipation, propagation delay constraints get optimized. Specifically the enhanced SVL method for CMOS DFF design gives better results in terms of power dissipation, leakage current and propagation delay.

Fig4: Simulated Transient Outcome of CMOS D Flip Flop:

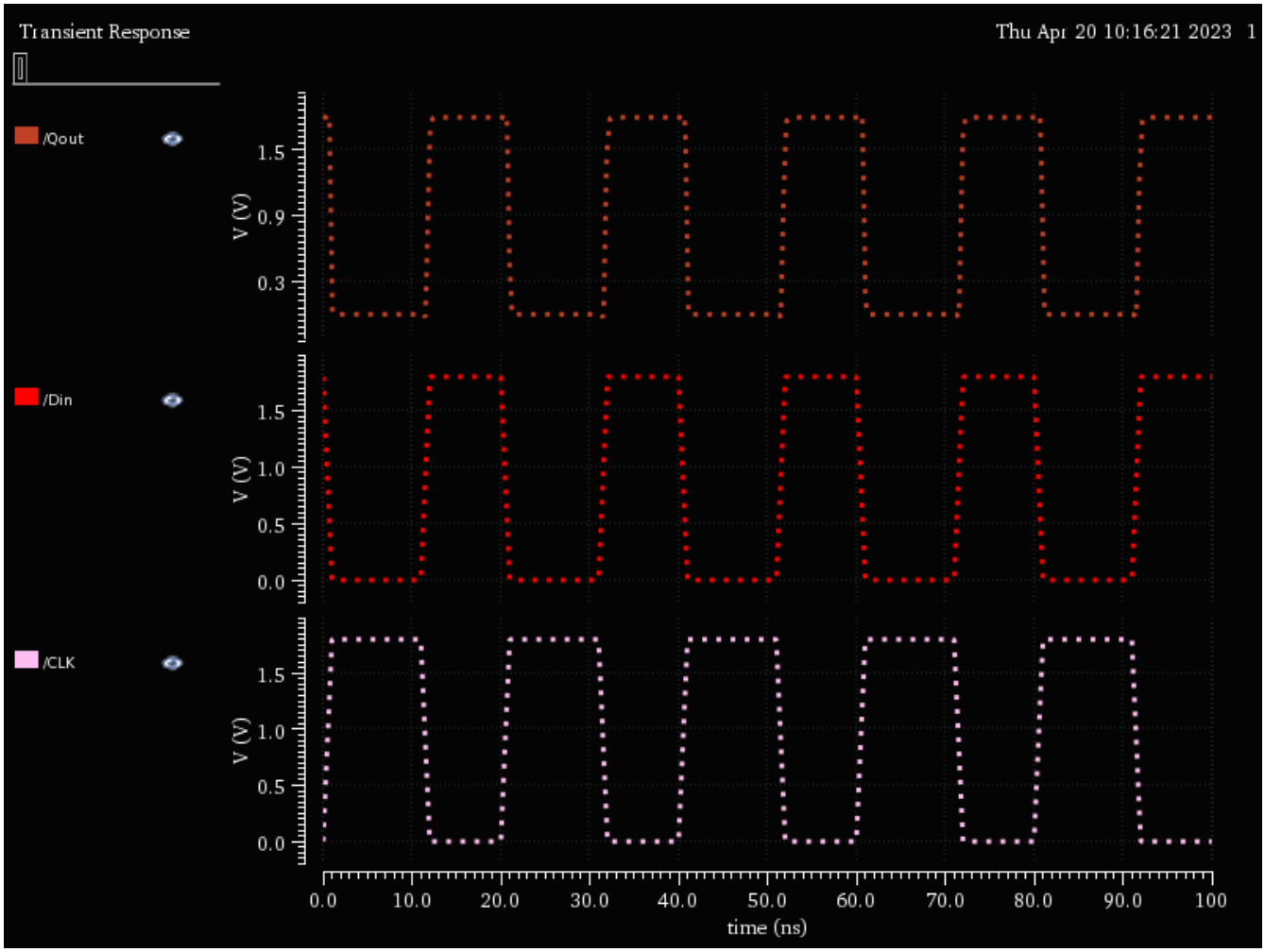


Figure5: Simulated Transient Outcome of CMOS D Flip Flop enforced using SVL method.

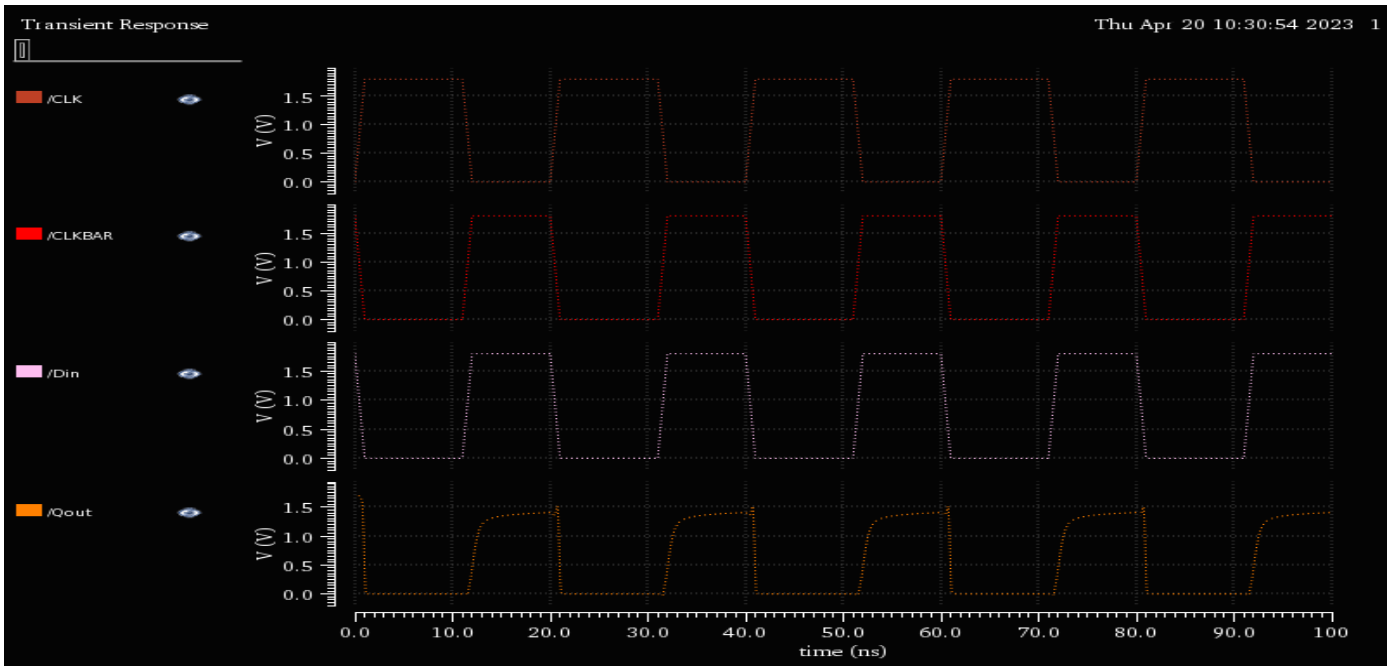
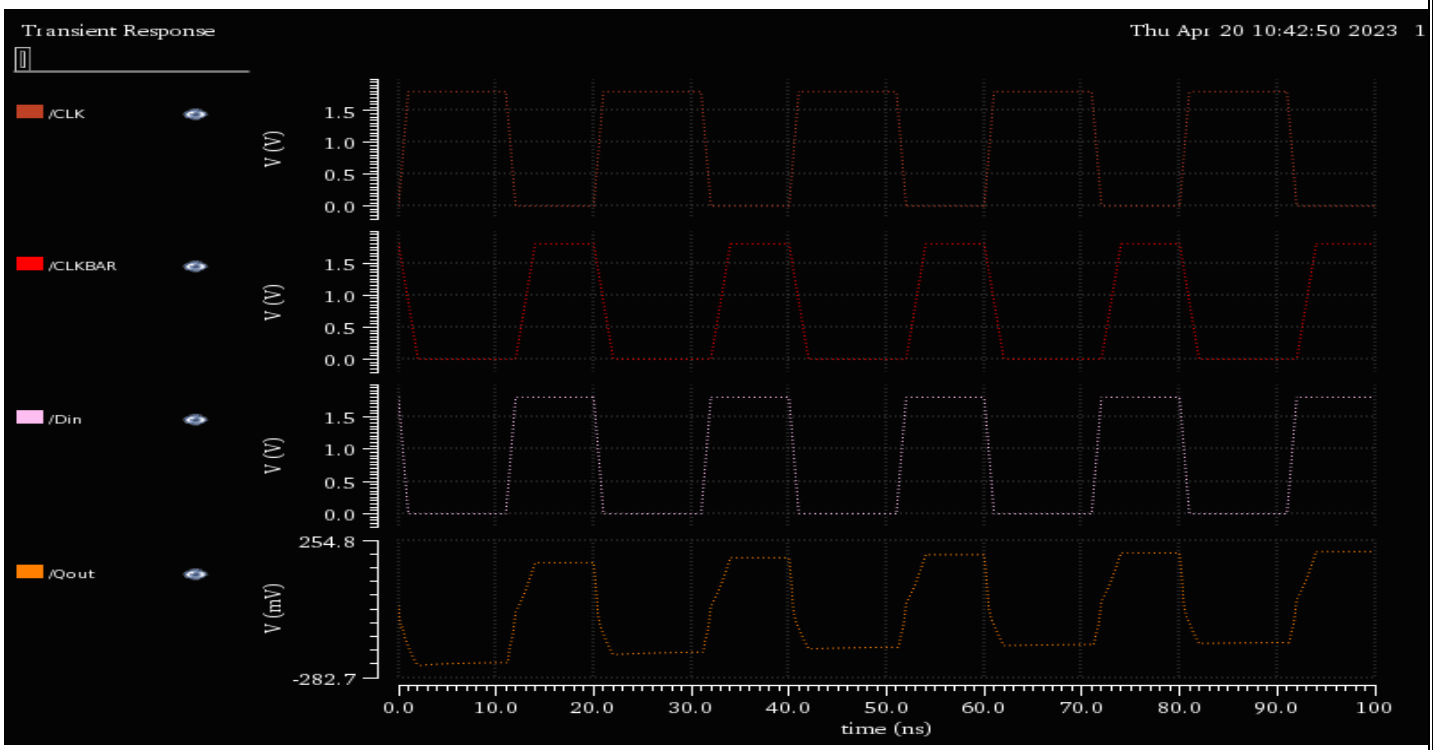


Figure6: Simulated Transient Outcome of CMOS D Flip Flop enforced using altered SVL method.



Power Analysis:

The total power dissipation of a circuit includes both a dynamic and a static component that can be challenging to isolate from each other in simulations. The dynamic power is due to switching currents required to charge/discharge output loads and short circuit (direct path) currents that flow between the pMOS and nMOS transistors as the input signal changes. The static power is due to leakage sources in the transistors, including subthreshold conduction between source and drain and reverse bias pn-junction leakage between the source/drain and substrate.

To measure the static power dissipation:

we simply apply a static (DC) input signal so that no switching occurs. For digital circuits, this amounts to a high (VDD) or low (ground) at the input, which typically turns one side of the circuit off and eliminates any static short circuit current through the transistors. For analog circuits, the input should be set to the appropriate DC operating point of the circuit, typically somewhere between ground and VDD. This is one of the reasons that analog circuits consume more power; in their static state many transistors are turned on and consume static power.

$$Pleak = Ileak\ Vdd$$

Where Pleak is leakage power of CMOS D-Flip Flop, Ileak abbreviated for leakage current, Vdd is power supply.

To measure dynamic power dissipation:

we can subtract the static power from the total power to estimate the contribution of dynamic sources.

Pdyn = CL * VDD2 * freq

To measure total power dissipation:

we have to apply an input signal that varies with time, causing the output node to charge/discharge. For digital circuits this simply requires applying a pulse input signal.

Observation:

If we remove the load capacitor the switching current is reduced to only that needed to charge/discharge the parasitic at the output, and as a result the measured power will be much closer to the value measured for static power.

TSPC DFF: Power Simulations

Fig: Leakage Current(Static Power dissipation) waveform for TSPC DFF

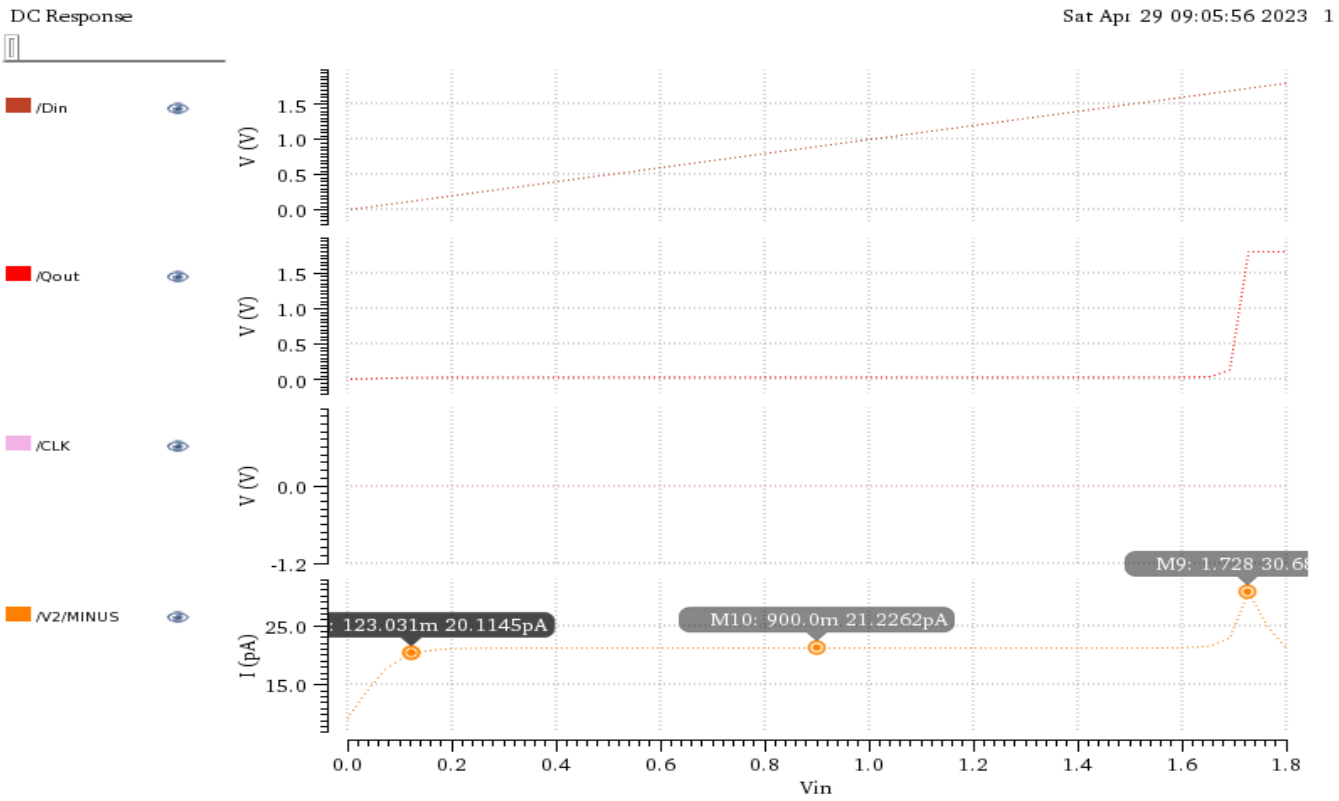


Fig: Propagation delay for TSPC CMOS DFF

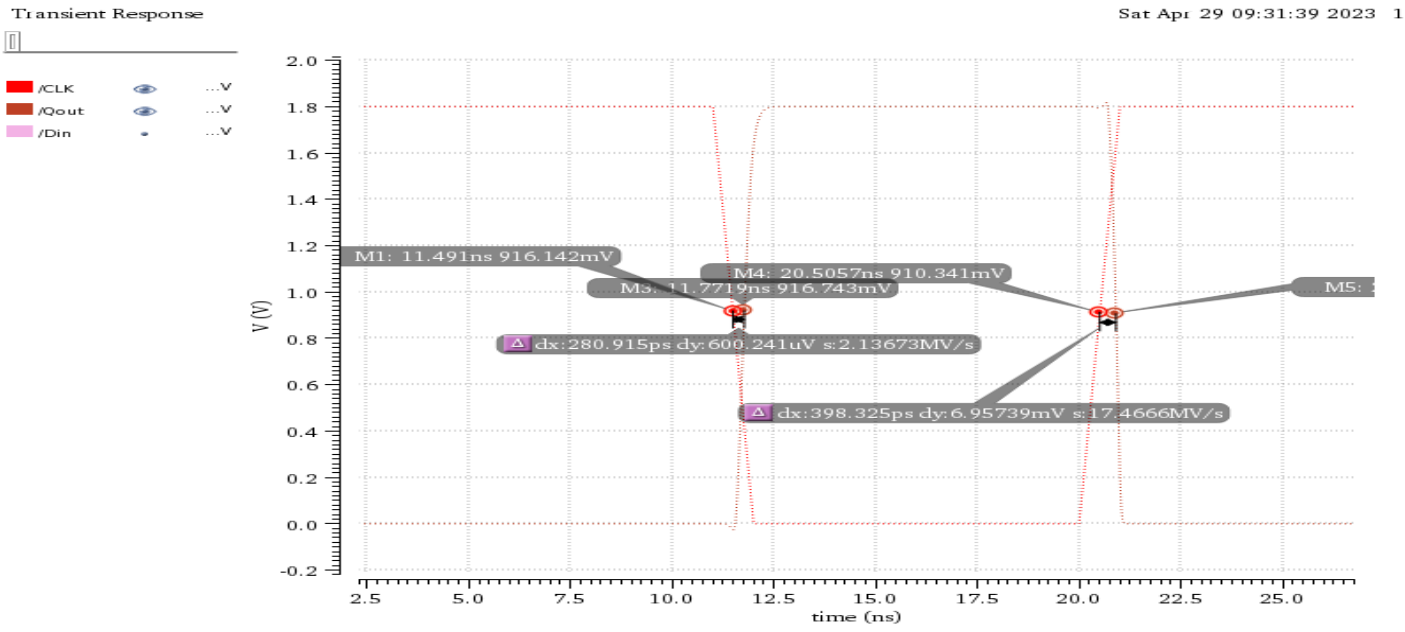


Fig: Dynamic Power Graph of TSPC CMOS DFF

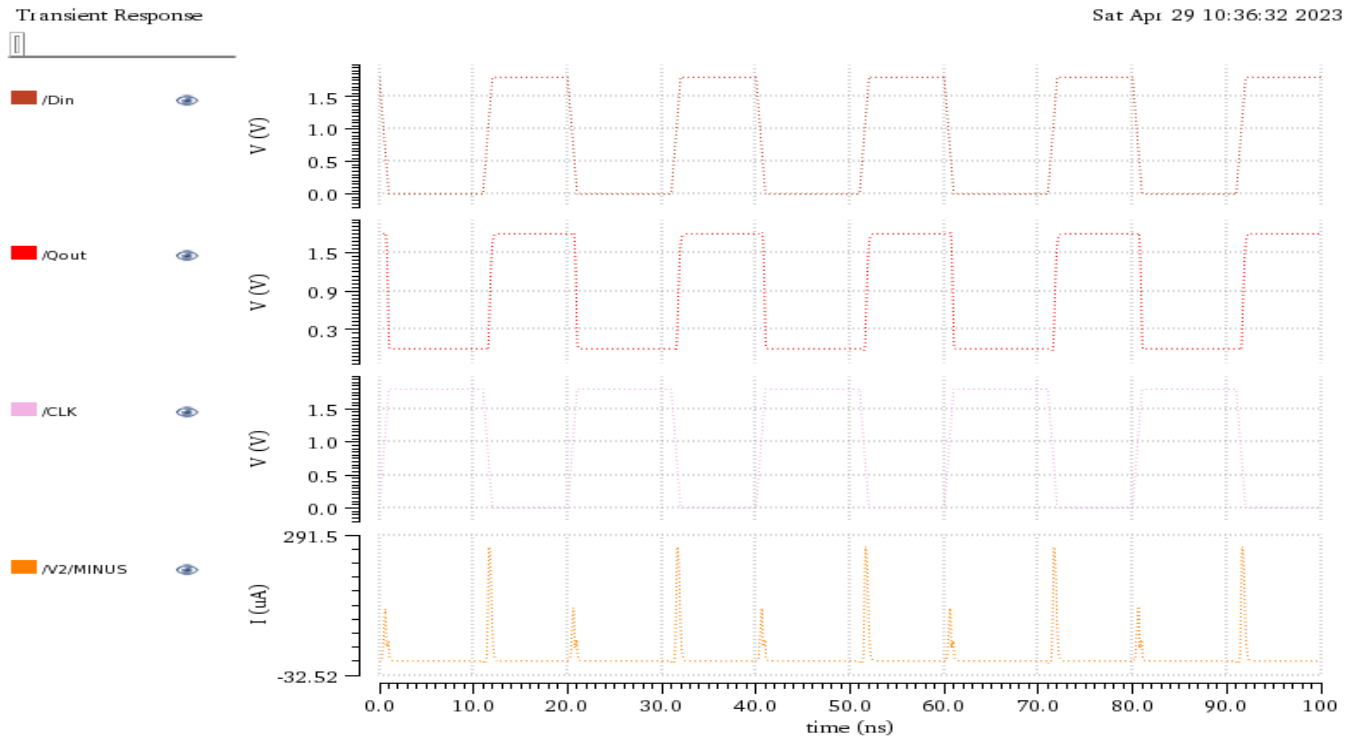
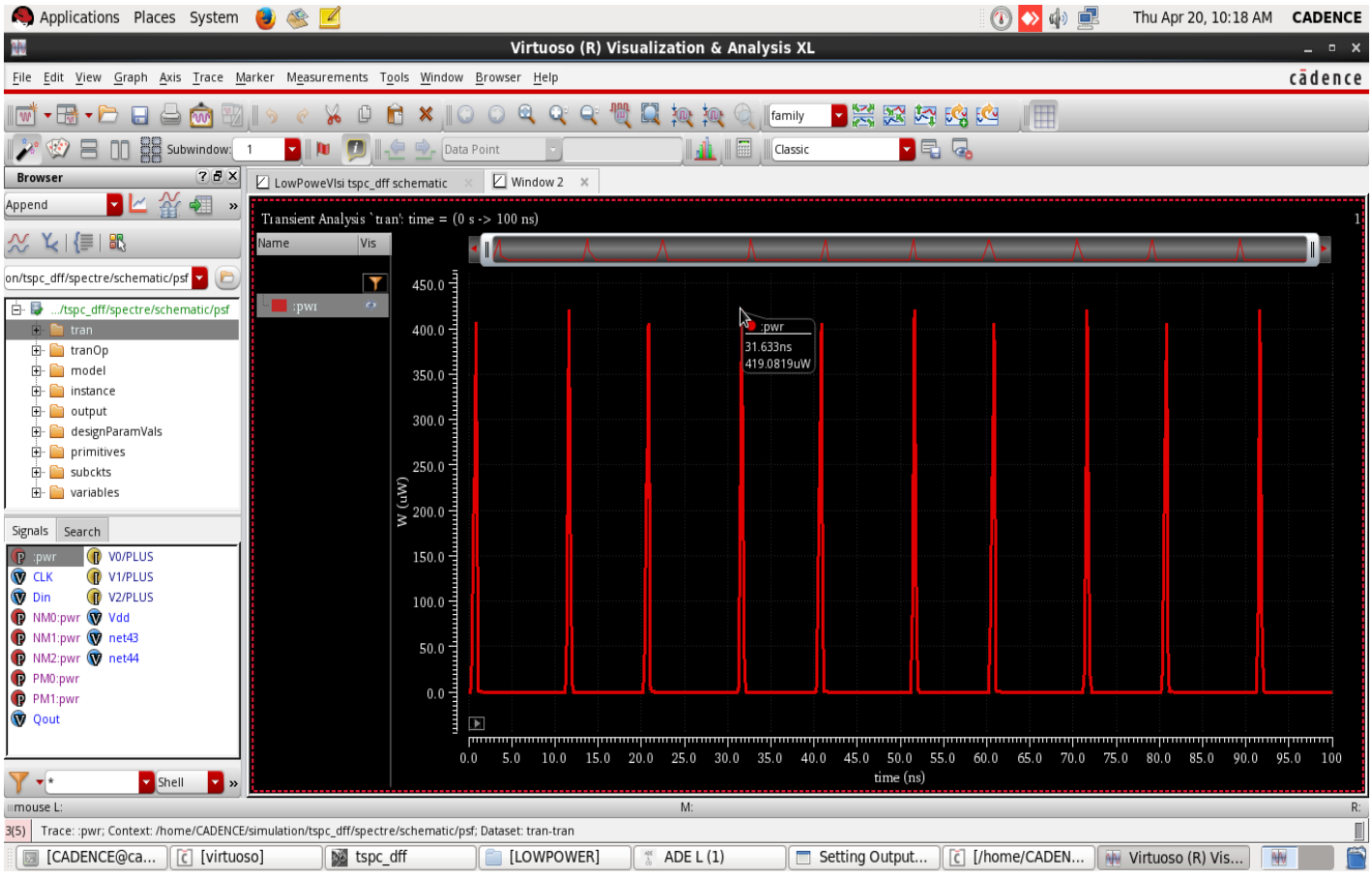


Fig: Total Power Graph for TSPC CMOS DFF



Power Simulations: SVL Enforced on TSPC CMOS DFF

Fig: Leakage Current (Static Power Dissipation) of SVL TSPC DFF

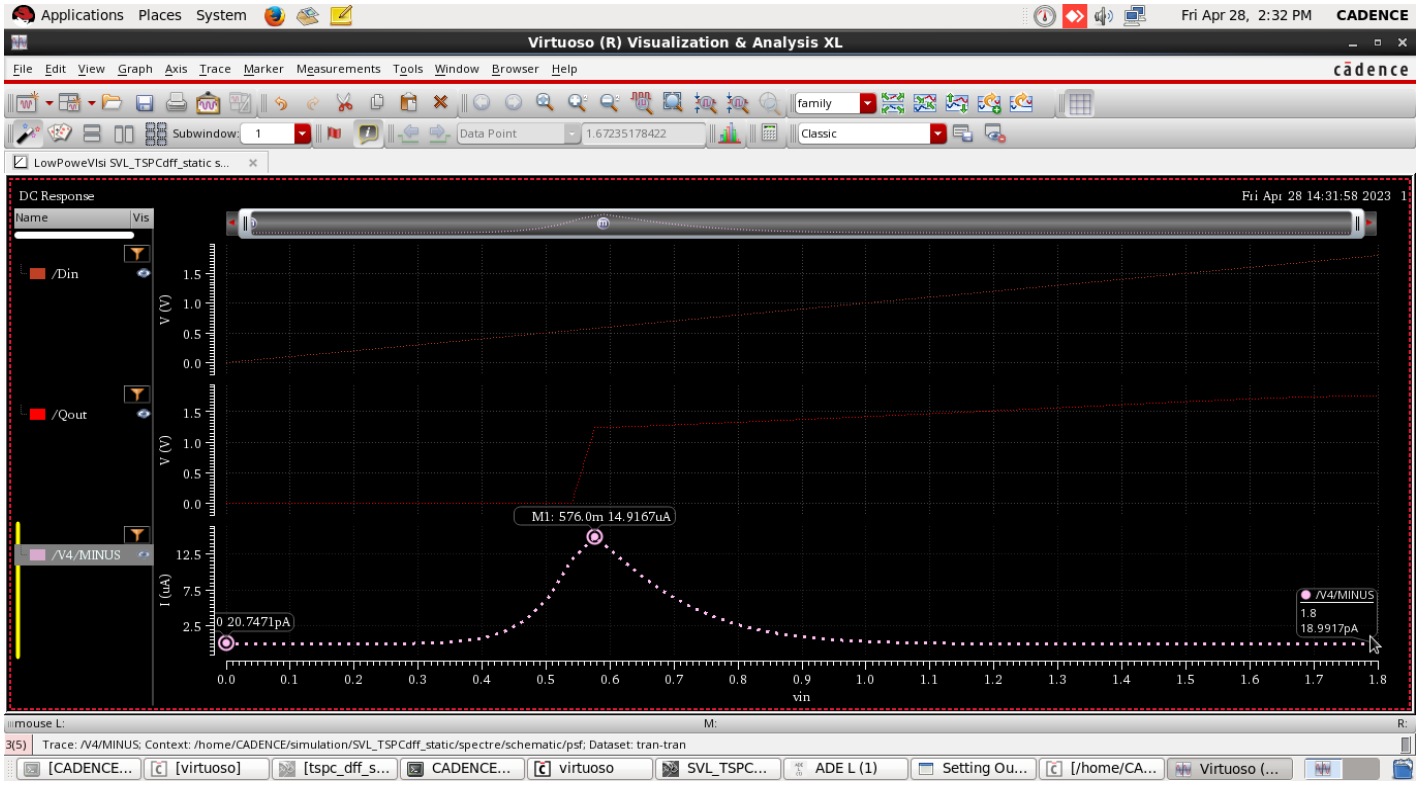
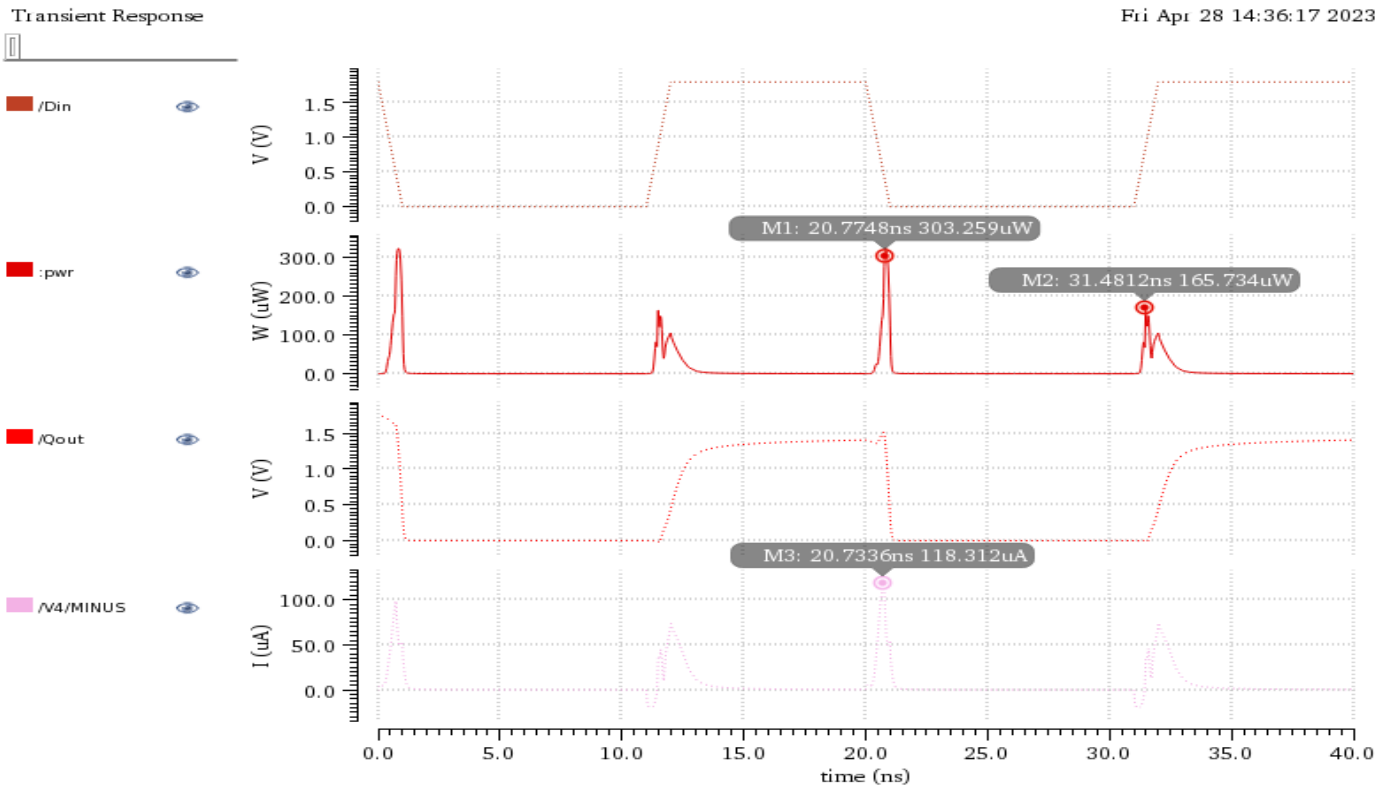
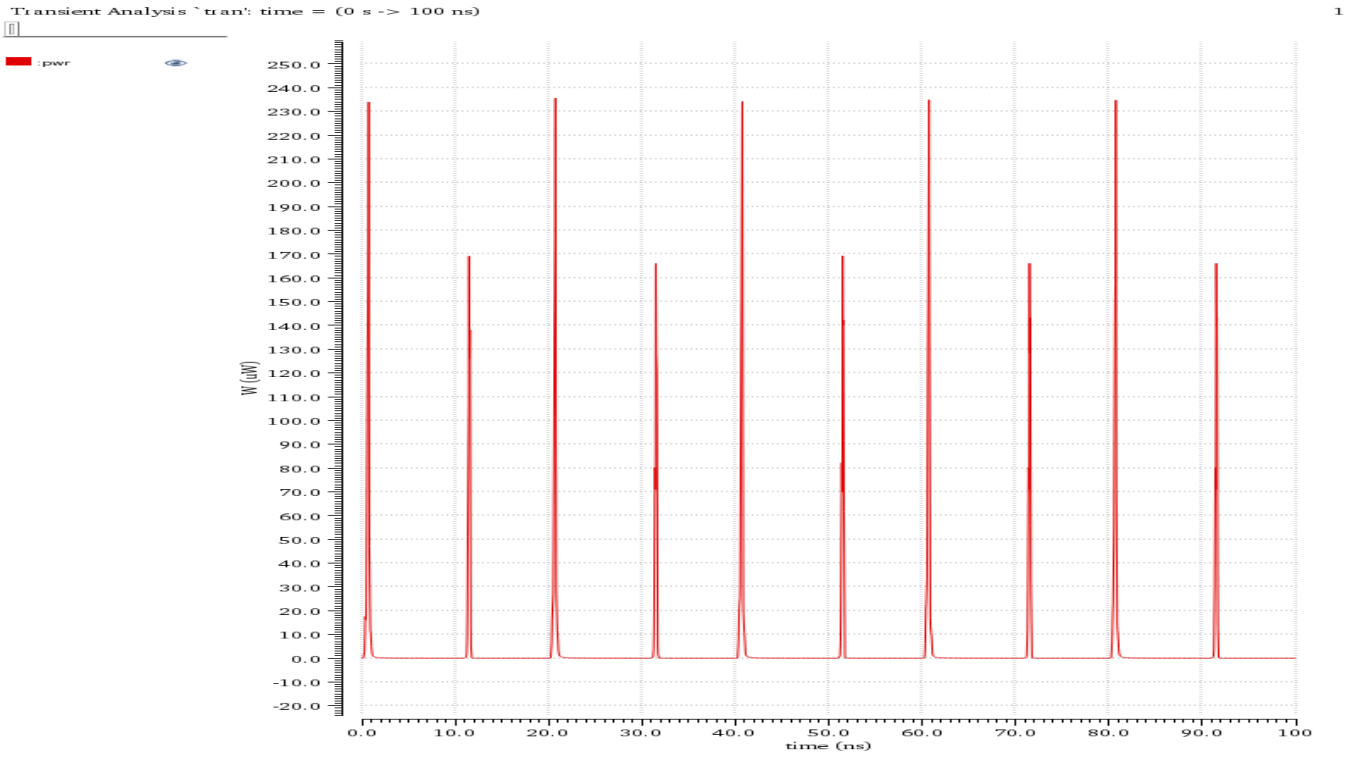


Fig: Dynamic Power Dissipation Graph of SVL TSPC DF

Fig: Total Power Dissipation of SVL TSPC DFF:





Power Simulations : Modified SVL on TSPC DFF

Fig: Leakage Current(Static Power Dissipation) waveform:

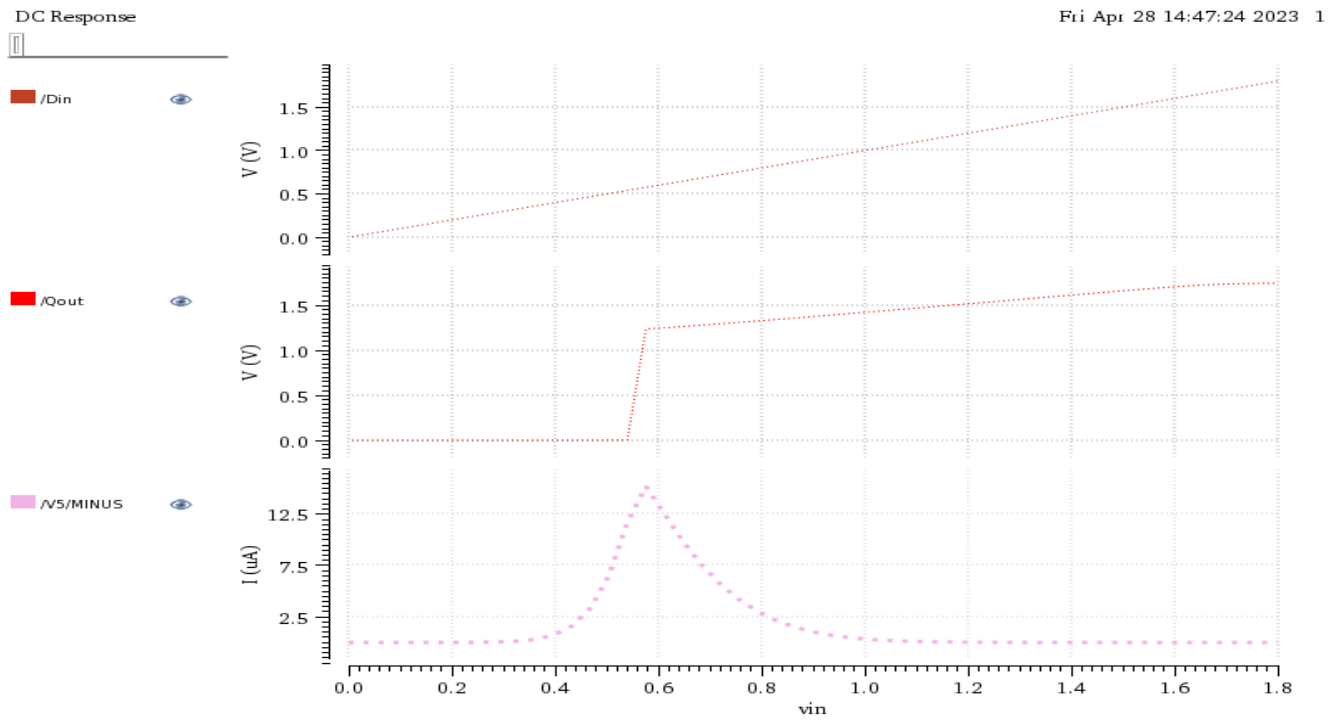
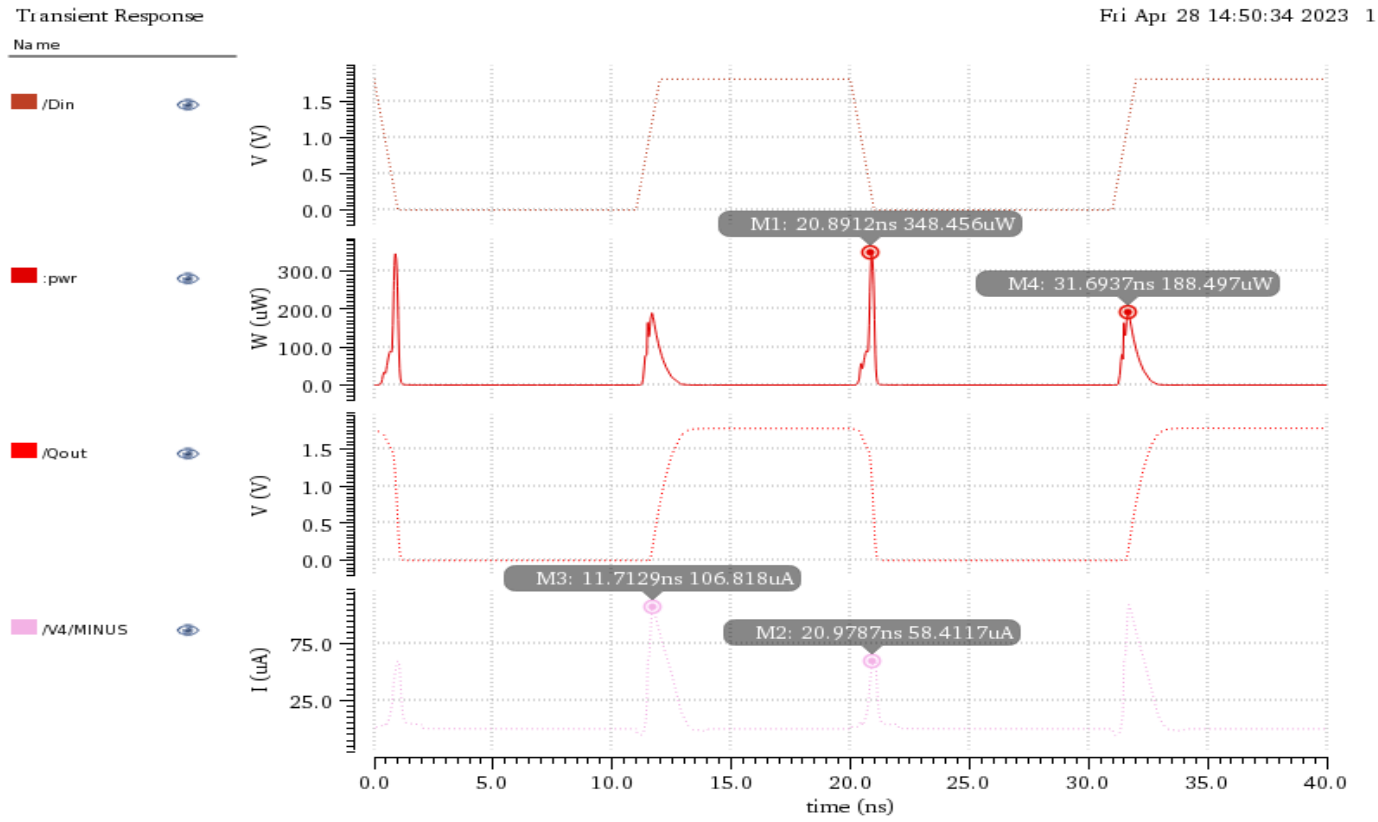


Fig: Total Power & Dynamic Power Dissipation waveform:



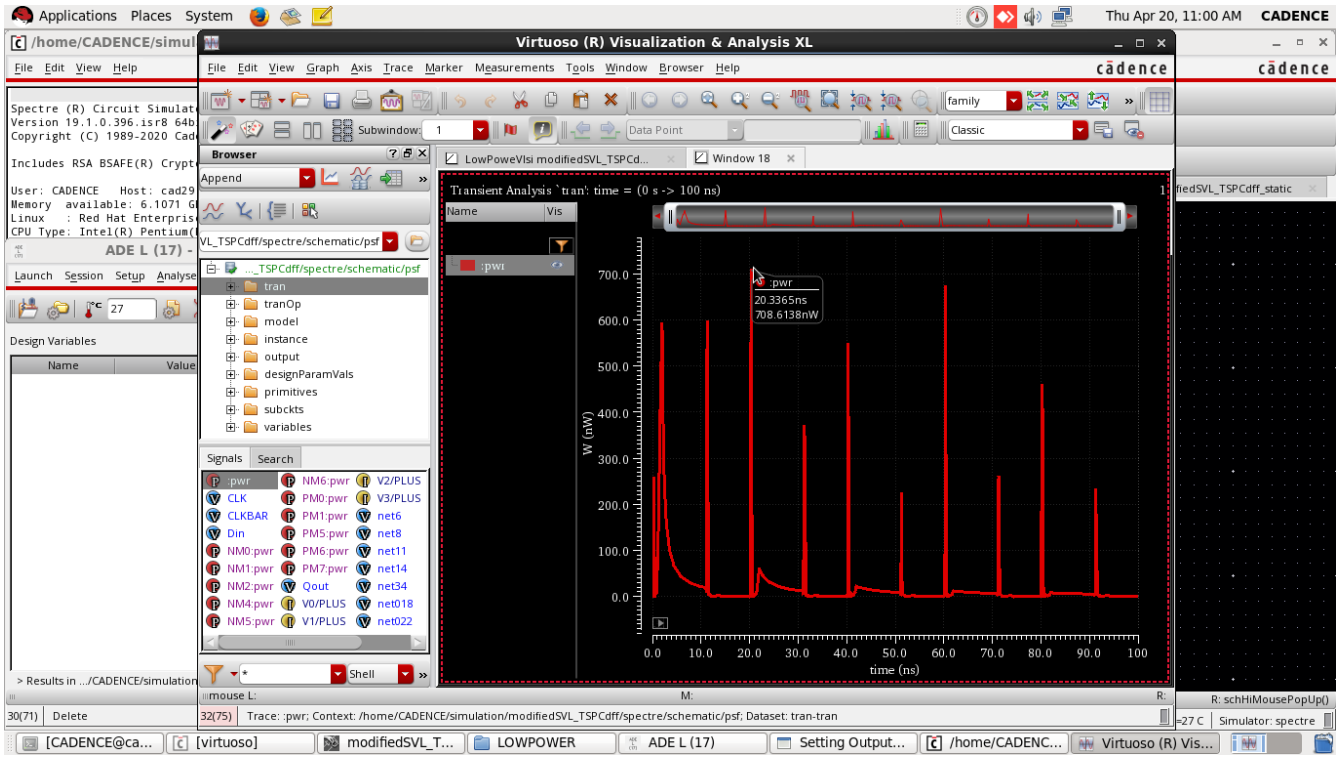


Table 1 visualizes the analogy of different CMOS DFPFPs by using variant supply voltage level (SVL) techniques.:

Performance Parameter	TSPC CMOS DFF	TSPC CMOS DFF with SVL	TSPC CMOS DFF with Modified SVL
Technology Used	180nm	180nm	180nm
Supply Voltage	1.8V	1.8V	1.8V
Leakage Power	38.06 pW	17.65 pW	16.09 pW
Power Dissipation	14.29 µW	10.99 µW	20.06 n W
Energy	363.3 fJ	289.3 fJ	5.605 fJ

CONCLUSION:

Mainly CMOS DFF requires less Power consumption in VLSI technology since for battery operated circuits power reduction isimportant key factor. So that we designed the low Power required CMOS DFF using SVL method, this circuit is improved by using this SVL method, so that Power dissipation, better backup, supply potential for the designed air is optimized. Altered SVL method enforced to CMOS DFF design optimizes Power consumption and also leakage currents in limited way. The projected schematic design consists of less number of clocked transistor count concurrently minimizes dynamic Power consumption, and also leakage current for required circuit. The implemented analogy discussion of SVL and Altered SVL methods. Explained mainly by using the constraints with data of reduced power dissipation at Voltage Potential of 1.8V . The simulated outcomes show CMOS DFPFP with Altered SVL methods gives better results than normal SVL methods. This type of CMOS DFF is used at low power consumption designs.

REFERENCES:

i)Implementation of Low power Flip Flop Design in Nanometer Regime" 2015 fifth International Conference on Advanced Computing and Communication Technologies.

ii) Design of Low Power and High-Speed Cmos D Flipflop using Supply Voltage Level (SVL) Methods C.Arunabala, A. Lohithakshi, D. Jyothsna, CH. Pranathi, A. Navaneetha