Advanced eXtensible Interface (AXI)

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AXI, the third generation of AMBA interface AMBA 3 specification, is targeted at high performance, high clock frequency system designs and suitable for high speed sub-micrometer interconnect:

- separate address/control and data phases
- support for unaligned data transfers using byte strobes
- burst based transactions with only start address issued & issuing of multiple outstanding addresses
- easy addition of register stages to provide timing closure.

AXI features

- AMBA AXI 3.0/4.0 Verification IP provides an smart way to verify the AMBA AXI 3.0/4.0 component of a SOC or a ASIC.
- AMBA AXI 3.0/4.0 VIP is supported natively in **SystemVerilog, VMM, RVM, AVM, OVM, UVM, Verilog, SystemC, VERA, Specman E** and **non-standard verification environment.**
- **Burst types**

  The AXI protocol supports three different burst types that are suitable for:

  • normal memory accesses

  • wrapping cache line bursts

  • streaming data to peripheral FIFO locations.

AXI features (cont..)

- System cache support

  The cache-support signal of the AXI protocol enables a master to provide to a system-level cache the bufferable, cacheable, and allocate attributes of a transaction.

- Protection unit support

  To enable both privileged and secure accesses, the AXI protocol provides three levels of protection unit support.

- Atomic operations

  The AXI protocol defines mechanisms for both exclusive and locked accesses.

AXI features (cont..)

- Error support

  The AXI protocol provides error support for both address decode errors and slave-generated errors.

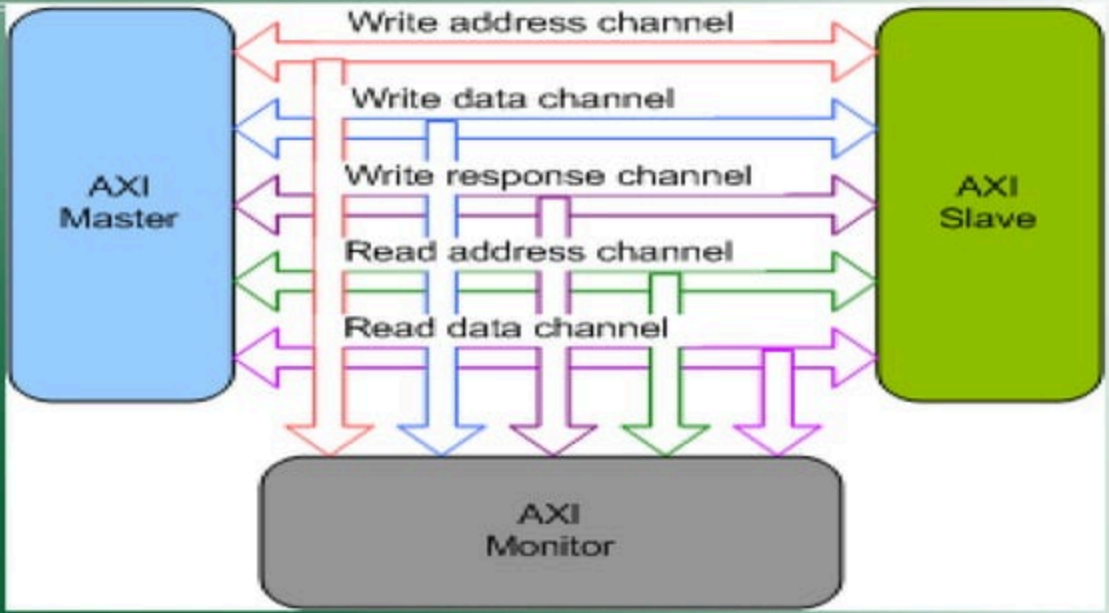
- Unaligned address

  To enhance the performance of the initial accesses within a burst, the AXI protocol supports unaligned burst start addresses

How AXI work?

- AXI consist of five different channels:
  - Write Address Channel
  - Write Data Channel
  - Write Response Channel
  - Read Address Channel
  - Read Data Channel

AXI bus - model



AXI -WRITE operation archietecture

Channel archietecture of WRITE

AXI -READ operation archietecture

Channel archietecture of READ

Transaction channel handshake pairs

Transaction channel	Handshake pair
• Write address channel	AWVALID, AWREADY
• Write data channel	WVALID, WREADY
• Write response channel	BVALID, BREADY
• Read address channel	ARVALID, ARREADY
• Read data channel	RVALID, RREADY

Basic transactions

- Read burst example

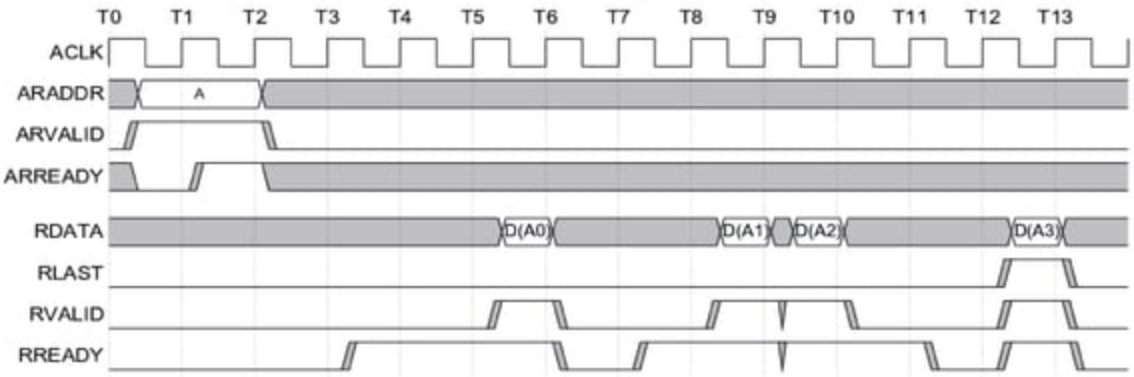


Figure 1-4 Read burst

Read burst example

- In this example, the master drives the address, and the slave accepts it one cycle later.
- The master also drives a set of control signals showing the length and type of the burst,but these signals are omitted from the figure for clarity.
- After the address appears on the address bus, the data transfer occurs on the read data channel. The slave keeps the VA L I D signal LOW until the read data is available. For the final data transfer of the burst, the slave asserts the RLAST signal to show that the last data item is being transferred.

Overlapping read burst example

Figure shows how a master can drive another burst address after the slave accepts the first address. This enables a slave to begin processing data for the second burst in parallel with the completion of the first burst.

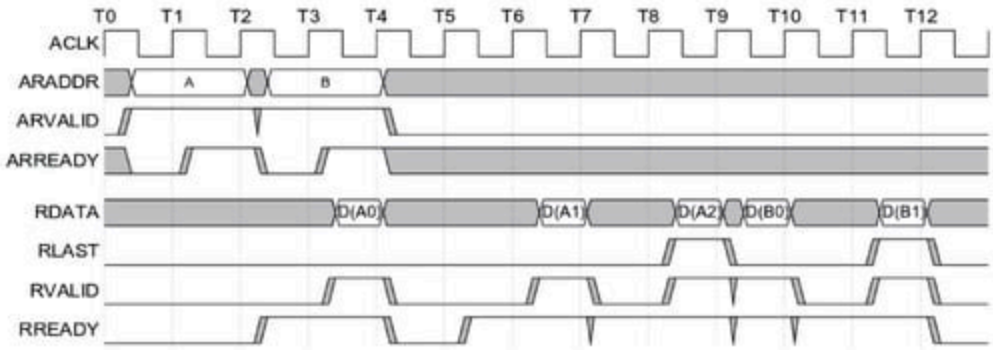


Figure 1-5 Overlapping read bursts

Write burst example

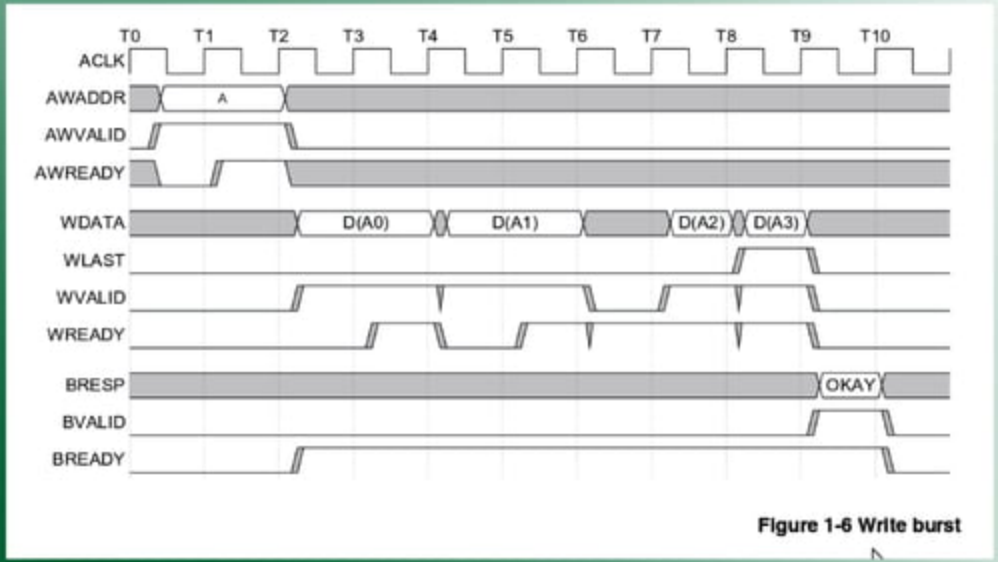


Figure 1-6 Write burst

Write burst

- Figure shows a write transaction. The process starts when the master sends an address and control information on the write address channel. The master then sends each item of write data over the write data channel. When the master sends the last data item, the WLAST signal goes HIGH. When the slave has accepted all the data items, it drives a write response back to the master to indicate that the write transaction is complete

Comparing AMBA AHB to AXI Bus- System Modeling

- AMBA AHB
- single-channel, shared bus.
- A 128 bit bus running at 400 MHz.
- The AHB bus speed was assumed to be double the AXI Bus, and two times the width.

- AMBA AXI
- Multi-channel, read/write optimized bus.
- A 64 bit bus running at 200 Mhz
- The primary throughput channels- R/W data channels, while the address, response channels are to improve pipelining of multiple requests.

The simulation study between AMBA AHB and AMBA AXI-Results

The AHB Bus performed best for the given traffic rates and sizes. The AXI Bus was rated higher for throughput.

Bus Type	Latency	Throughput	Power
AHB Bus	Excellent	Good	Excellent
AXI Bus	Good	Excellent	Good

Throughput

- Throughput or network throughput is the average rate of successful message delivery over a communication channel.
- It is closely related to the channel capacity of the system, and is the maximum possible quantity of data that can be transmitted under ideal circumstances.
- The throughput is usually measured in bits per second (bit/s or bps), data packets per second or data packets per time slot.

AXI benefits

- Faster testbench development and more complete verification of AMBA AXI 3.0/4.0 designs.
- Easy to use command interface simplifies testbench control and configuration of master and slave.
- Simplifies results analysis.
- Runs in every major simulation environment.

Drawback of AXI

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- The AMBA AXI4 has limitations with respect to the burst data and beats of information to be transferred.
- The burst must not cross the 4k boundary. Bursts longer than 16 beats are only supported for the INCR burst type.
- Both WRAP and FIXED burst types remain constrained to a maximum burst length of 16 beats. These are the drawbacks of AMBA AXI system which need to be overcome.

Summary of AXI

- Productivity—By standardizing on the AXI interface, developers need to learn only single protocol for IP.
- Flexibility- AXI4 memory mapped interfaces and allows burst of up to 256 data transfer cycles with just a single address phase.
- AXI4-Stream removes the requirement for an address phase altogether and allows unlimited data burst size.

Summary of AXI cont...

- Availability—By moving to an industry-standard, access to a worldwide community of ARM Partners.
- Many IP providers support the AXI protocol.
- A robust collection of third-party AXI tool vendors is available that provide a variety of verification, system development, and performance characterization tools.


Thank
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